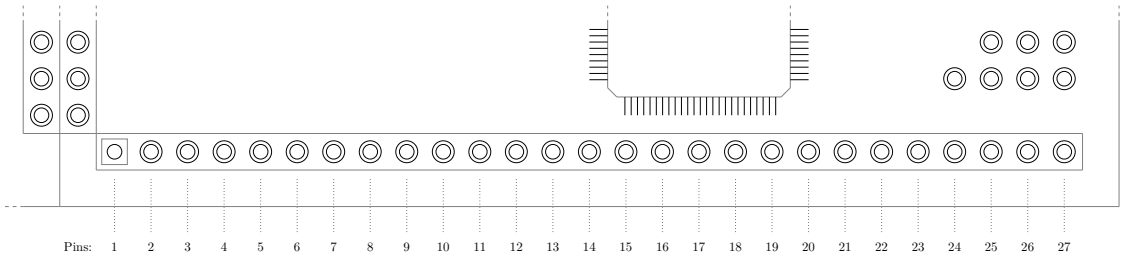
LPC1769 - LPCXpresso Board Consolidated Pinout Diagram

Rohit Ramesh

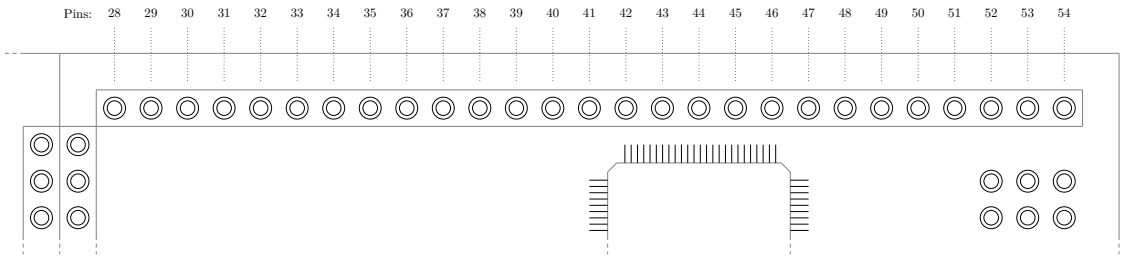
1 Header Pins 1 - 27



Pin Name	Pin Location	Pin Select Register	Pin Select Bits	Function 00	Function 01	Function 10	Function 11
GND	H[1]			NA	NA	NA	NA
VIN	H[2]			NA	NA	NA	NA
VB	H[3]			NA	NA	NA	NA
RESET_N	H[4]			NA	NA	NA	NA
P0[9]	H[5]	PINSEL0	18:19	GPIO 0.9	I2STX_SDA	MOSI1	MAT2.2
P0[8]	H[6]	PINSEL0	16:17	GPIO 0.8	I2STX_WS	MISO1	MAT2.2
P0[7]	H[7]	PINSEL0	14:15	GPIO 0.7	I2STX_CLK	SCK1	MAT2.1
P0[6]	H[8]	PINSEL0	12:13	GPIO 0.6	I2SRX_SDA	SSEL1	MAT2.0
P0[0]	H[9]	PINSEL0	0:1	GPIO 0.0	RD1	TXD3	SDA1
P0[1]	H[10]	PINSEL0	2:3	GPIO 0.1	TD1	RXD3	SCL1
P0[18]	H[11]	PINSEL1	4:5	GPIO 0.18	DCD1	MOSI0	MOSI
P0[17]	H[12]	PINSEL1	2:3	GPIO 0.17	CTS1	MISO0	MISO
P0[15]	H[13]	PINSEL0	30:31	GPIO 0.15	TXD1	SCK0	SCK
P0[16]	H[14]	PINSEL1	0:1	GPIO 0.16	RXD1	SSEL0	SSEL
P0[23]	H[15]	PINSEL1	14:15	GPIO 0.23	AD0.0	I2SRX_CLK	CAP3.0
P0[24]	H[16]	PINSEL1	16:17	GPIO 0.24	AD0.0	I2SRX_CLK	CAP3.0
P0[25]	H[17]	PINSEL1	18:19	GPIO 0.25	AD0.2	I2SRX_SDA	TXD3
P0[26]	H[18]	PINSEL1	20:21	GPIO 0.26	AD0.3	AOUT	RXD3
P1[30]	H[19]	PINSEL3	28:29	GPIO 1.30	Reserved	Vbus	AD0.4
P1[31]	H[20]	PINSEL3	30:31	GPIO 1.31	Reserved	SCK1	AD0.5
P0[2]	H[21]	PINSEL0	4:5	GPIO 0.2	TXD0	AD 0.7	Reserved

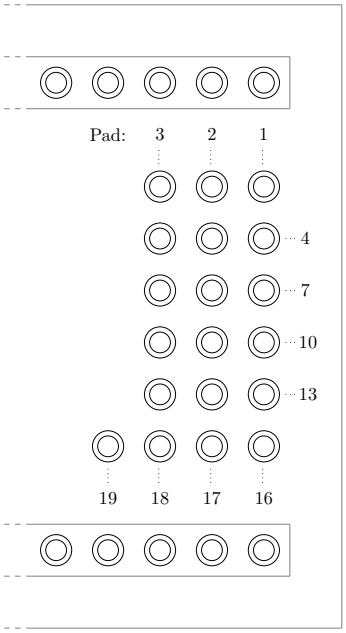
Pin Name	Pin Location	Pin Select Register	Pin Select Bits	Function 00	Function 01	Function 10	Function 11
P0[3]	H[22]	PINSEL0	6:7	GPIO 0.3	RXD0	AD 0.6	Reserved
P0[21]	H[23]	PINSEL1	10:11	GPIO 0.21	RI1	Reserved	RD1
P0[22]	H[24]	PINSEL1	12:13	GPIO 0.22	RTS1	Reserved	TD1
P0[27]	H[25]	PINSEL1	22:23	GPIO 0.27	SDA0	USB_SDA	Reserved
P0[28]	H[26]	PINSEL1	24:25	GPIO 0.28	SCL0	USB_SCL	Reserved
P2[13]	H[27]	PINSEL4	26:27	GPIO 2.13		Reserved	I2STX_SDA

2 Header Pins 28 - 54



Pin Name	Pin Location	Pin Select Register	Pin Select Bits	Function 00	Function 01	Function 10	Function 11
VIO	H[28]			NA	NA	NA	NA
–	H[29]			NA	NA	NA	NA
–	H[30]			NA	NA	NA	NA
–	H[31]			NA	NA	NA	NA
RD-	H[32]			NA	NA	NA	NA
RD+	H[33]			NA	NA	NA	NA
TD-	H[34]			NA	NA	NA	NA
TD+	H[35]			NA	NA	NA	NA
USB-D-	H[36]			NA	NA	NA	NA
USB-D+	H[37]			NA	NA	NA	NA
P0[4]	H[38]	PINSEL0	8:9	GPIO 0.4	I2SRX_CLK	RD2	CAP2.0
P0[5]	H[39]	PINSEL0	10:11	GPIO 0.5	I2SRX_WS	TD2	CAP2.1
P0[10]	H[40]	PINSEL0	20:21	GPIO 0.10	TXD2	SDA2	MAT3.0
P0[11]	H[41]	PINSEL0	22:23	GPIO 0.11	RXD2	SCL2	MAT3.1
P2[0]	H[42]	PINSEL4	0:1	GPIO 2.0	PWM1.1	TXD1	Reserved
P2[1]	H[43]	PINSEL4	2:3	GPIO 2.1	PWM1.2	RXD1	Reserved
P2[2]	H[44]	PINSEL4	4:5	GPIO 2.2	PWM1.3	CTS1	Reserved
P2[3]	H[45]	PINSEL4	6:7	GPIO 2.3	PWM1.4	DCD1	Reserved
P2[4]	H[46]	PINSEL4	8:9	GPIO 2.4	PWM1.5	DSR1	Reserved
P2[5]	H[47]	PINSEL4	10:11	GPIO 2.5	PWM1.6	DTR1	Reserved
P2[6]	H[48]	PINSEL4	12:13	GPIO 2.6	PCAP1.0	RI1	Reserved
P2[7]	H[49]	PINSEL4	14:15	GPIO 2.7	RD2	RTS1	Reserved
P2[8]	H[50]	PINSEL4	16:17	GPIO 2.8	TD2	TXD2	ENET_MDC
P2[10]	H[51]	PINSEL4	20:21	GPIO 2.10		NMI	Reserved
P2[11]	H[52]	PINSEL4	22:23	GPIO 2.11		Reserved	I2STX_CLK
P2[12]	H[53]	PINSEL4	24:25	GPIO 2.12		Reserved	I2STX_WS

3 Pad Pins 1 - 19



Pin Name	Pin Location	Pin Select Register	Pin Select Bits	Function 00	Function 01	Function 10	Function 11
P1[18]	PAD[1]	PINSEL3	4:5	GPIO 1.18	USB_UP_LED	PWM1.1	CAP1.0
P1[19]	PAD[2]	PINSEL3	6:7	GPIO 1.19	MCOA0		CAP1.1
P1[20]	PAD[3]	PINSEL3	8:9	GPIO 1.20	MCIO	PWM1.2	SCK0
P1[21]	PAD[4]	PINSEL3	10:11	GPIO 1.21		PWM1.3	SSEL0
P1[22]	PAD[5]	PINSEL3	12:13	GPIO 1.22	MCOB0	USB_PWRD	MAT1.0
P1[23]	PAD[6]	PINSEL3	14:15	GPIO 1.23	MCI1	PWM1.4	MISO0
P1[24]	PAD[7]	PINSEL3	16:17	GPIO 1.24	MCI2	PWM1.4	MISO0
P1[25]	PAD[8]	PINSEL3	18:19	GPIO 1.25	MCOA1	Reserved	MAT1.1
P1[26]	PAD[9]	PINSEL3	20:21	GPIO 1.26	MCOB1	PWM1.6	CAP0.0
P1[27]	PAD[10]	PINSEL3	22:23	GPIO 1.18	CLKOUT		CAP0.1
P1[28]	PAD[11]	PINSEL3	24:25	GPIO 1.28	MCOA2	PCAP1.0	MAT0.0
P1[29]	PAD[12]	PINSEL3	26:27	GPIO 1.29	MCOB	PCAL1.1	MAT0.1
P4[29]	PAD[16]	PINSEL9	26:27	GPIO 4.29	TX_MCLK	MAT2.1	RXD3
P0[19]	PAD[17]	PINSEL1	6:7	GPIO 0.19	DSR1	Reserved	SDA1
P0[20]	PAD[18]	PINSEL1	8:9	GPIO 0.20	DTR1	Reserved	SCL1
P2[9]	PAD[19]	PINSEL4	18:19	GPIO 2.9	USB_CONN	RXD2	ENET_MDIO