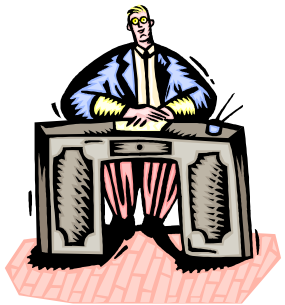
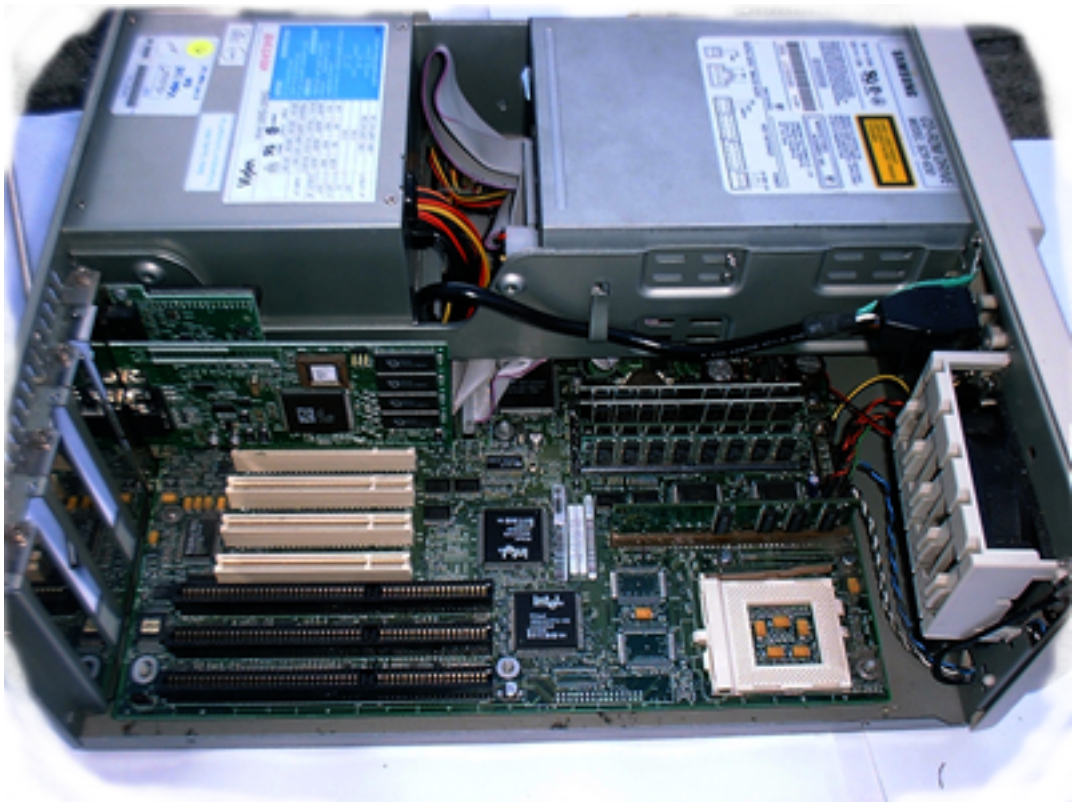
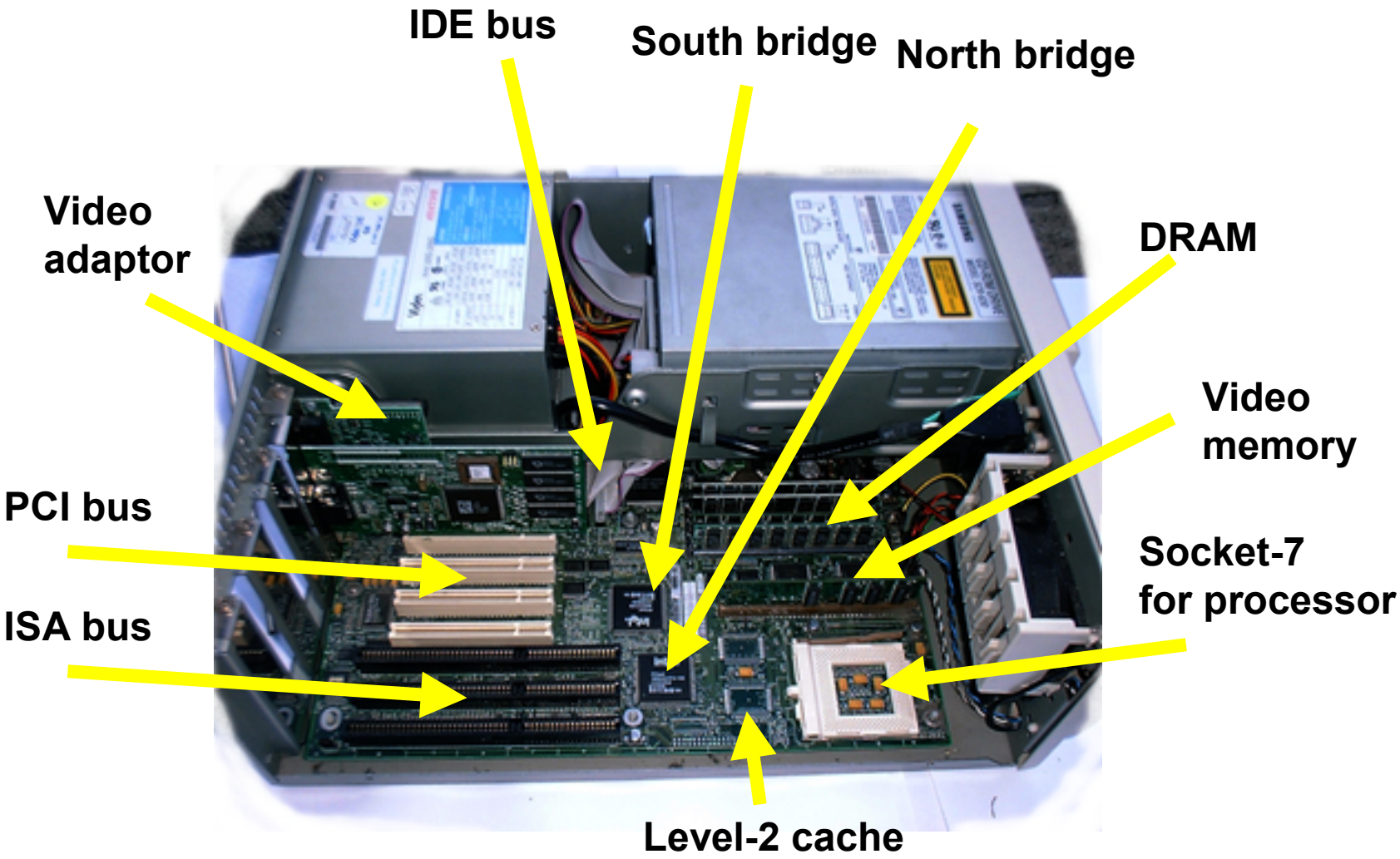
PC Architecture



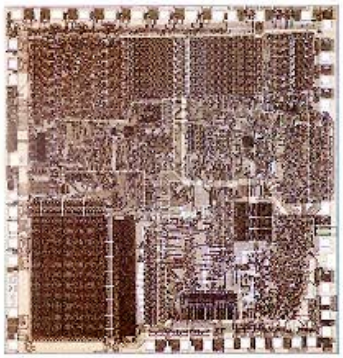
W.J. BUCHANAN, *Napier University, Edinburgh, UK.*



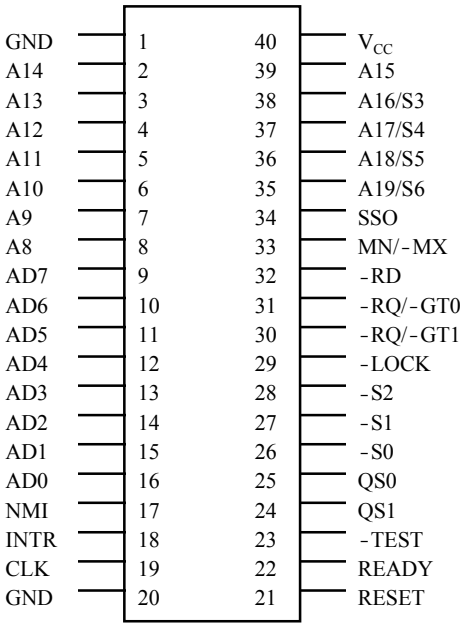

IDE bus
South bridge
North bridge
Video adaptor
DRAM
Video memory
PCI bus
Socket-7 for processor
ISA bus
Level-2 cache

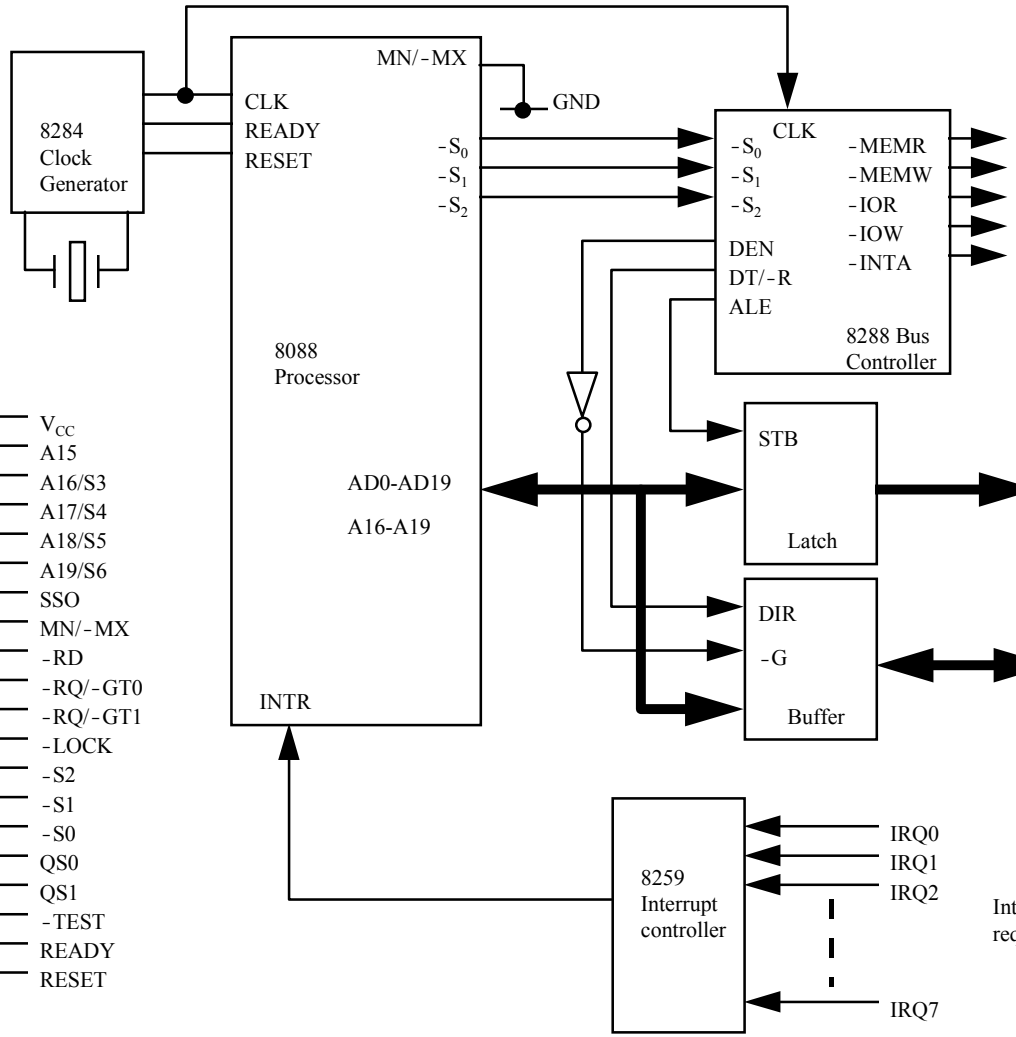
Aims

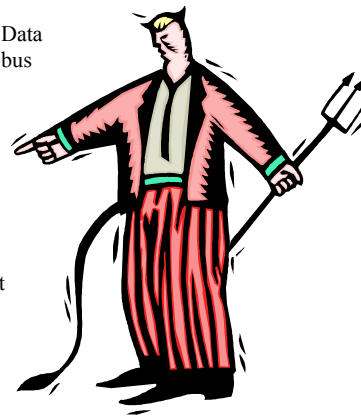
- To outline the **basic architecture** of the IBM PC.
- To show the **evolution** of the architecture, and the **enhancements** that have improved the performance of the modern PC.
- To show how **bridges** have enhanced the performance of the PC.
- To illustrate the usage of modern **chipsets**.
- To outline **hub-based** systems.
- To present a future **legacy-free system**.



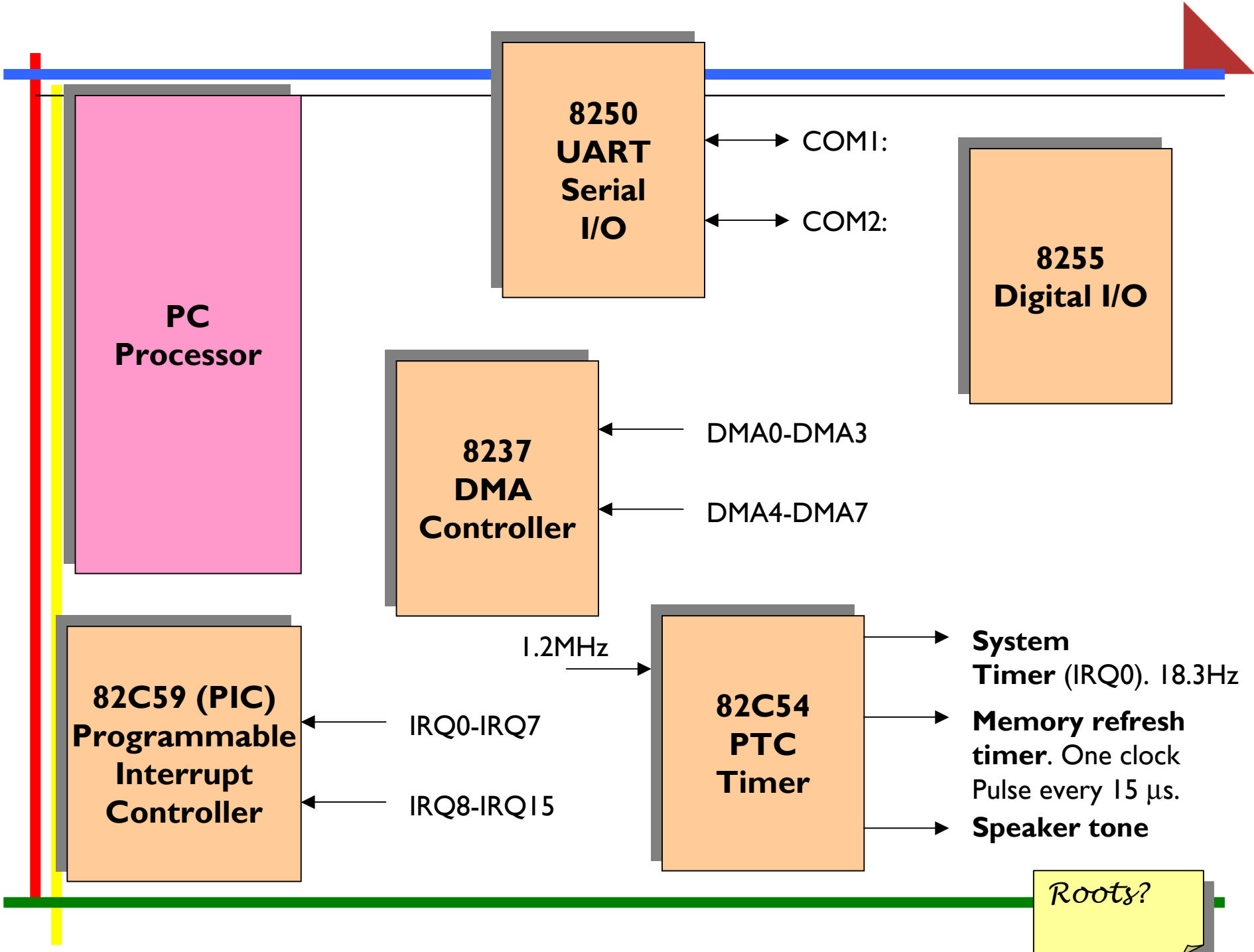
8088
Processor

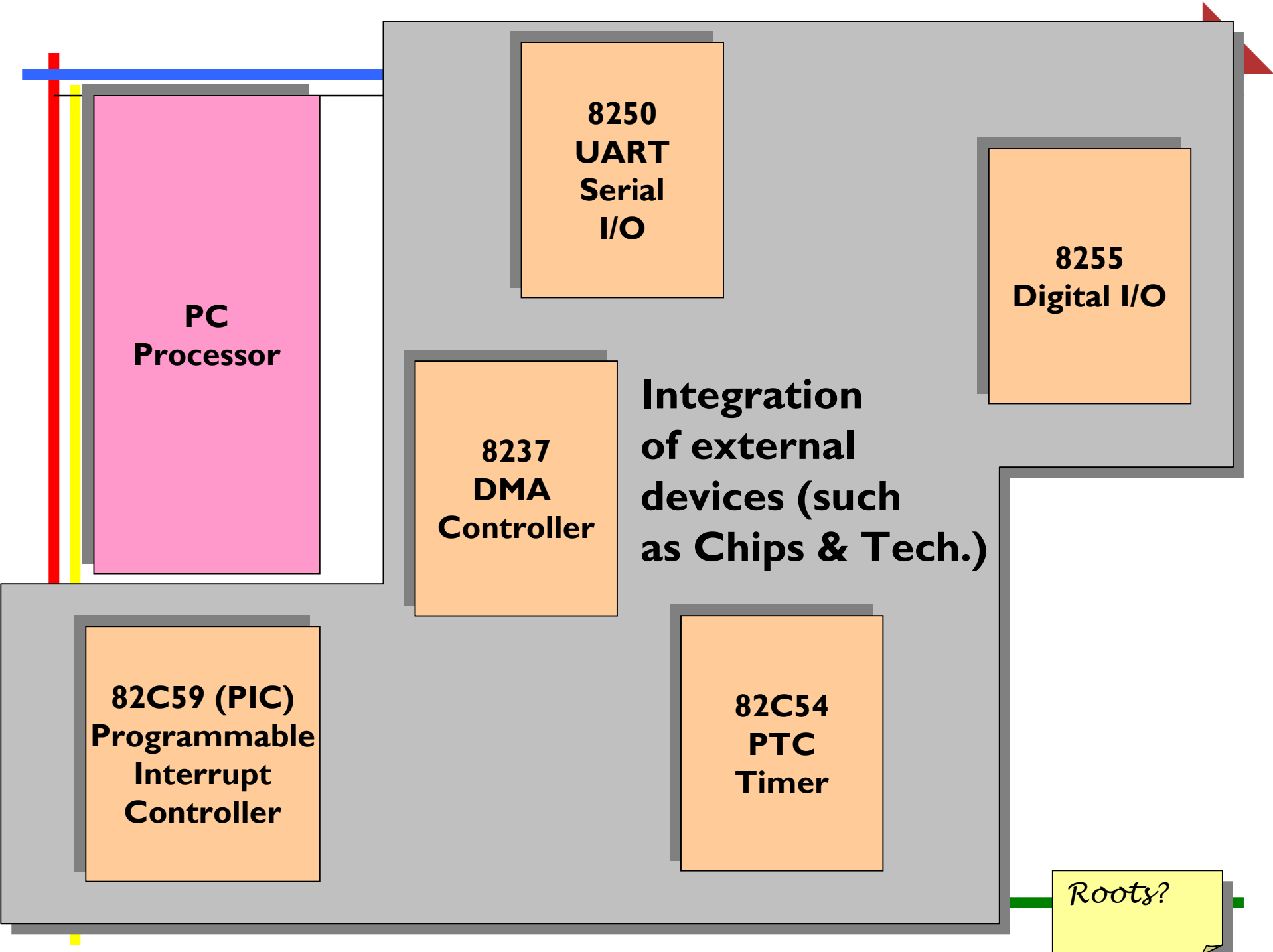


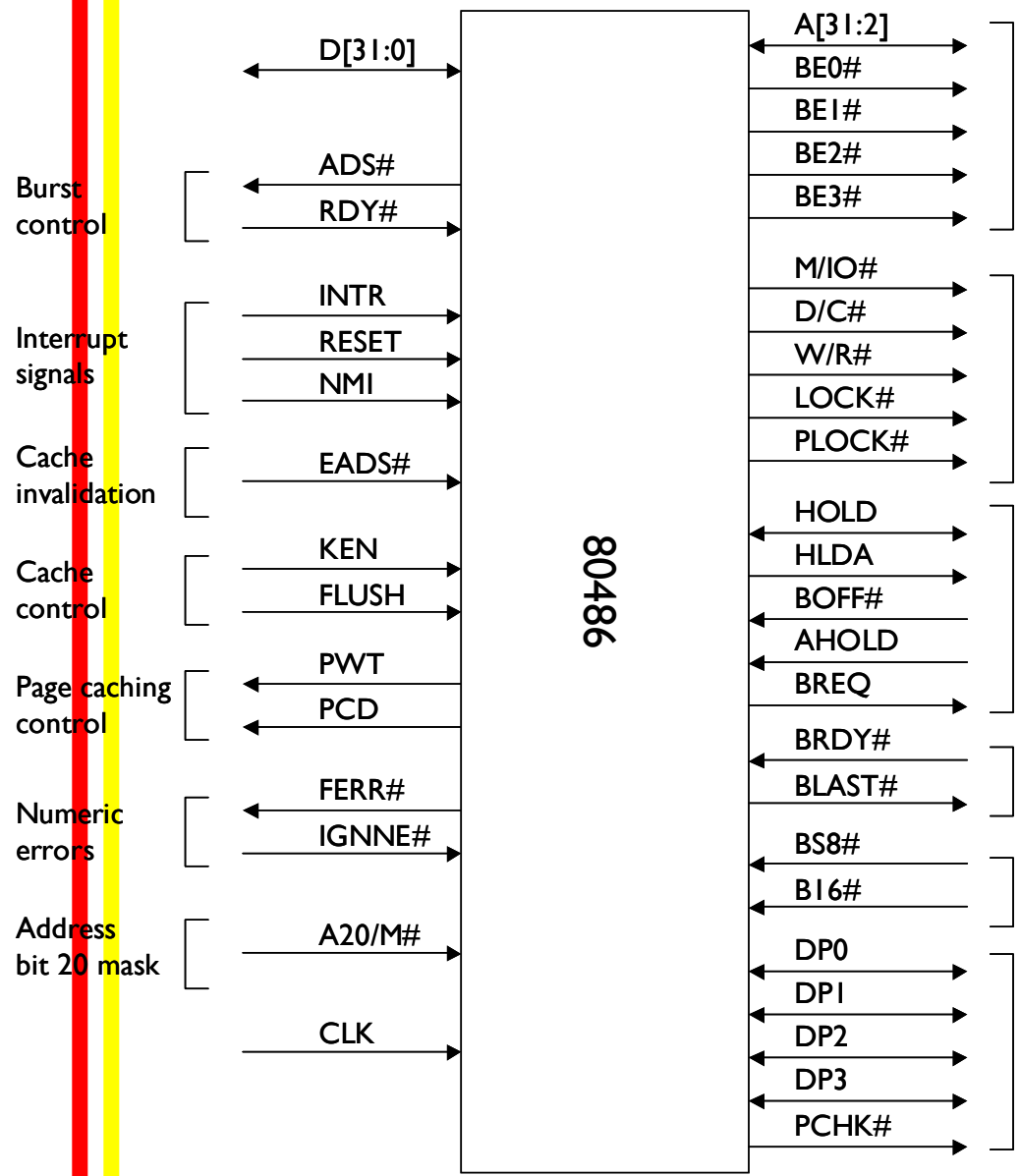




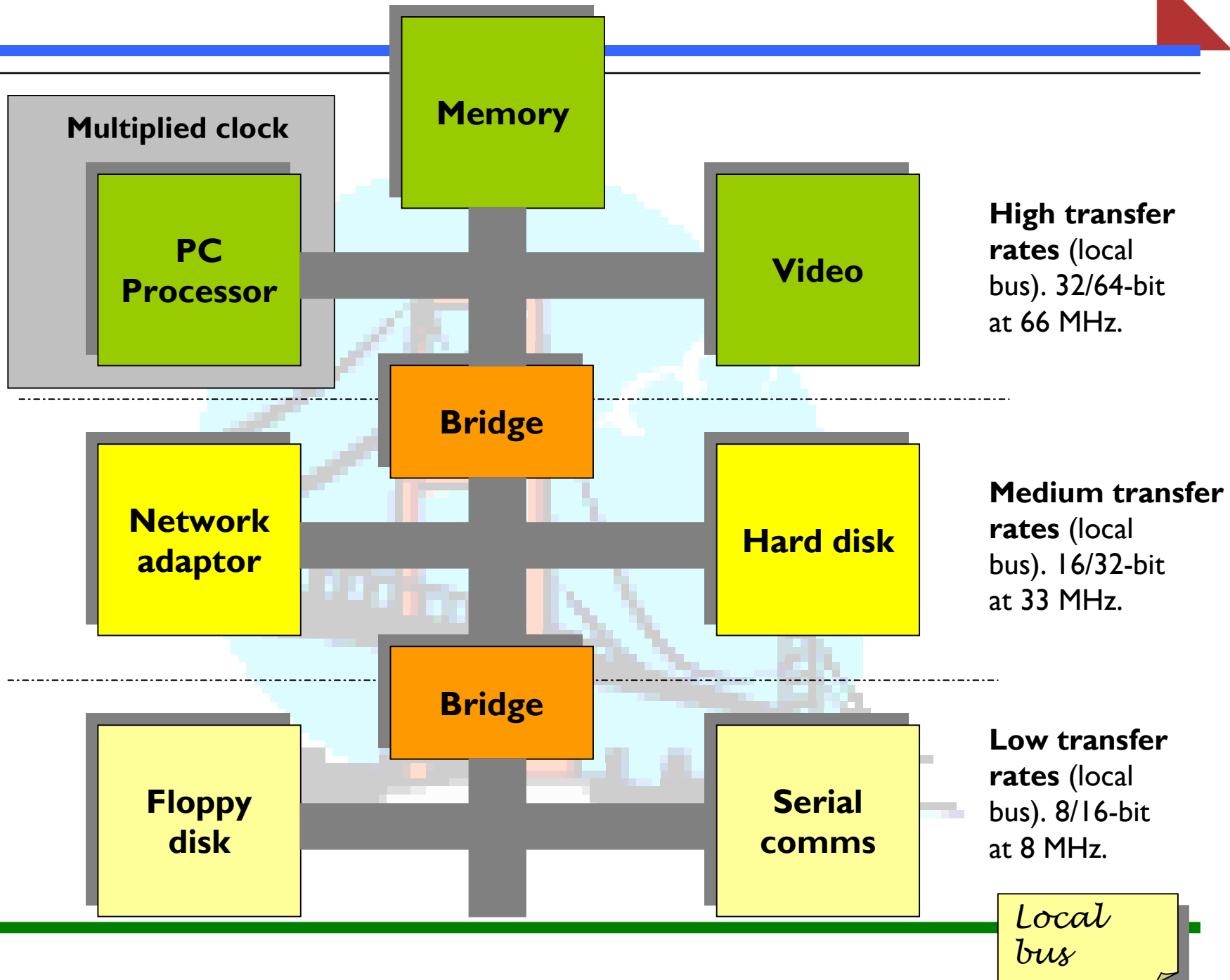
Roots?

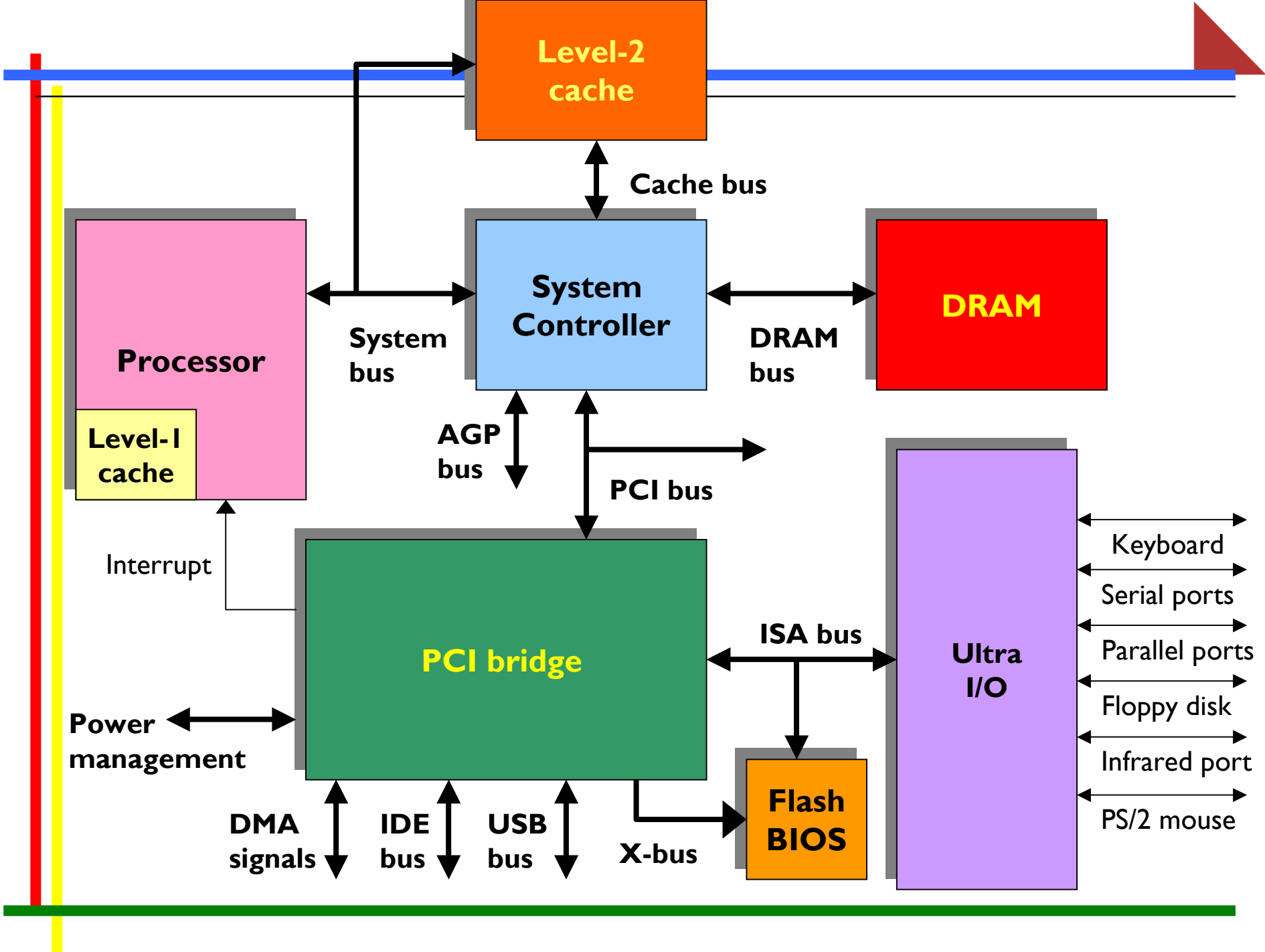

PC
Processor
8250
UART
Serial
I/O
COM1:
COM2:
8255
Digital I/O
8237
DMA
Controller
DMA0-DMA3
DMA4-DMA7
82C59 (PIC)
Programmable
Interrupt
Controller
IRQ0-IRQ7
IRQ8-IRQ15
1.2MHz
82C54
PTC
Timer
System
Timer (IRQ0). 18.3Hz
Memory refresh
timer. One clock
Pulse every 15 µs.
Speaker tone
Roots?

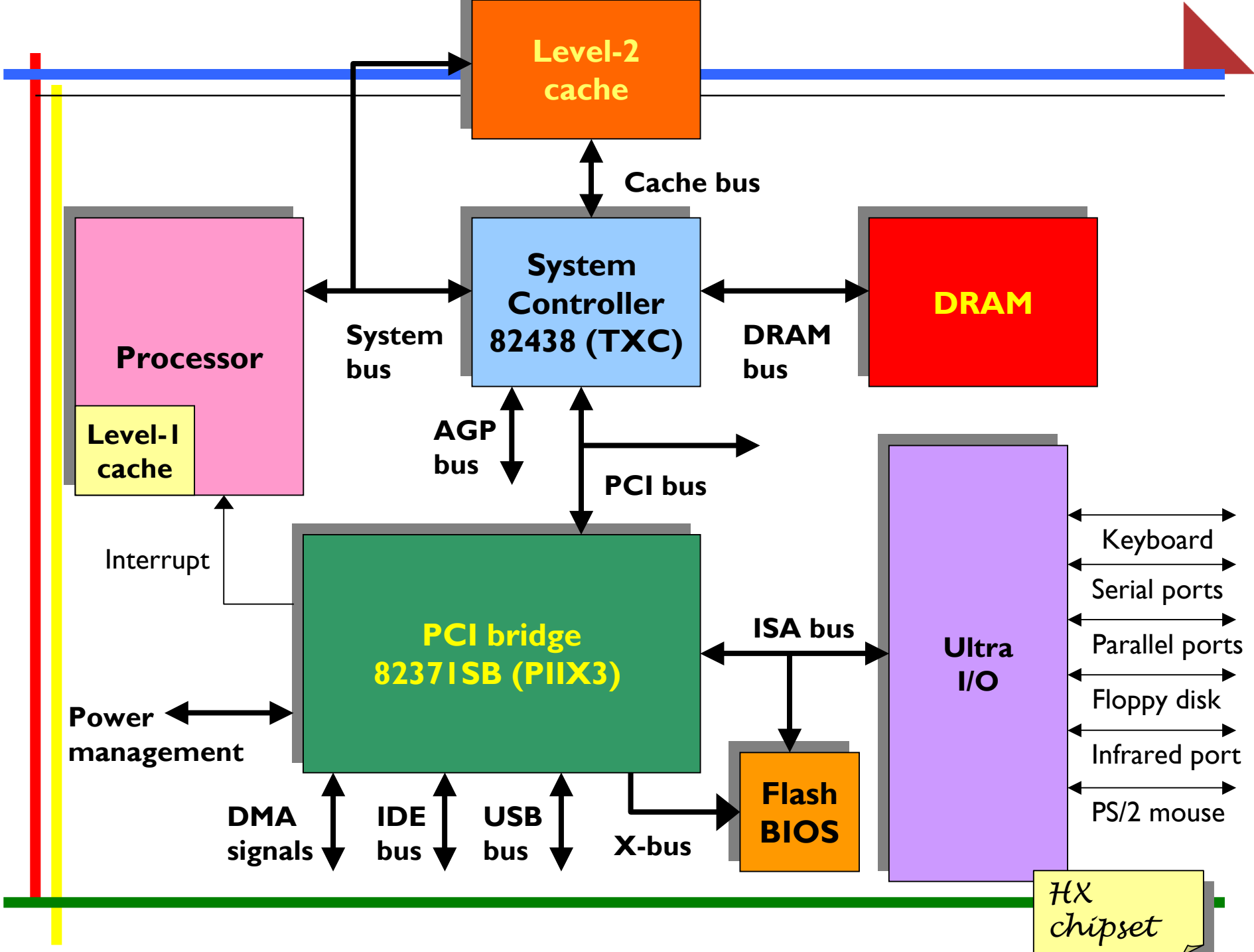

PC
Processor
8250
UART
Serial
I/O
8255
Digital I/O
8237
DMA
Controller
Integration
of external
devices (such
as Chips & Tech.)
82C59 (PIC)
Programmable
Interrupt
Controller
82C54
PTC
Timer
Roots?

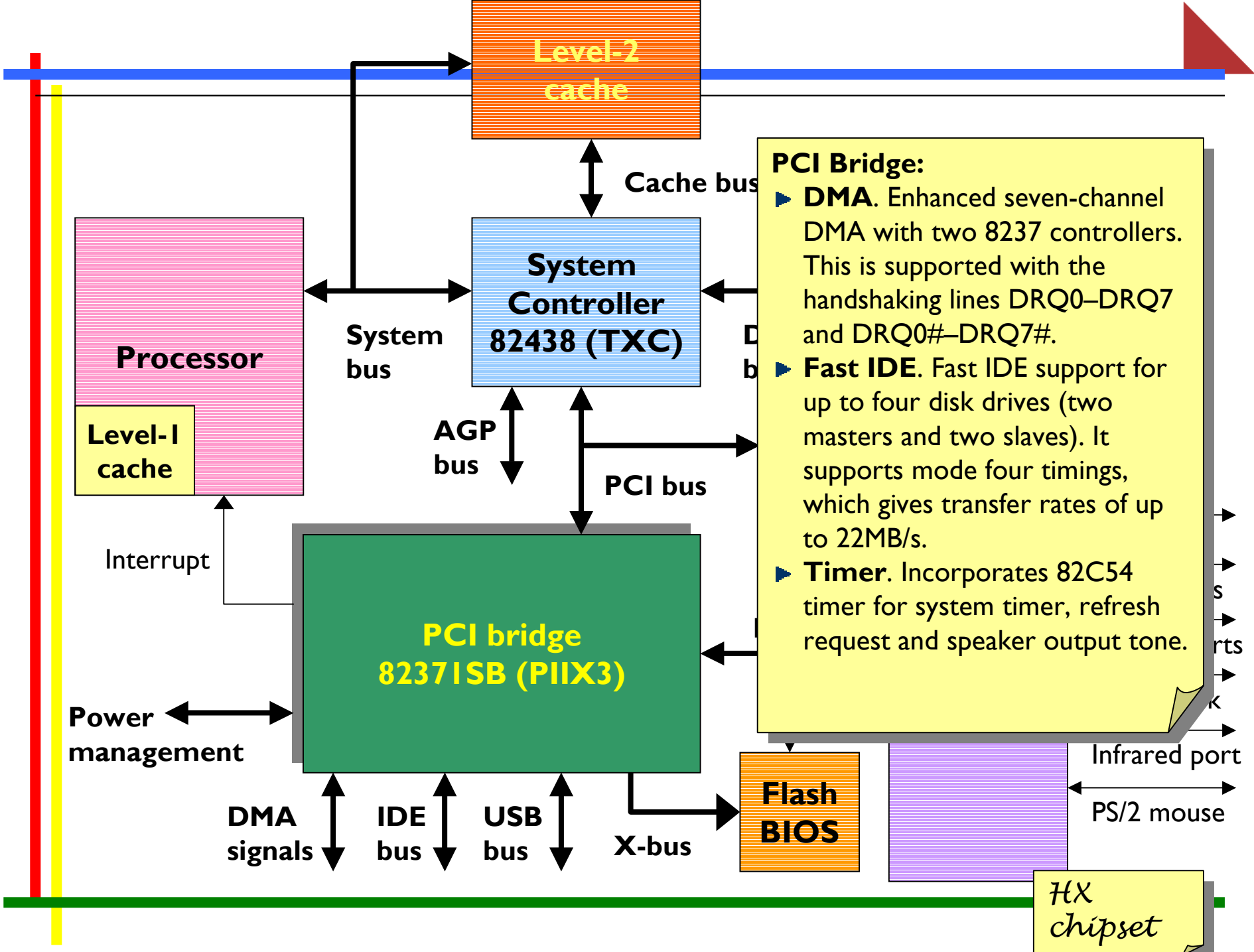


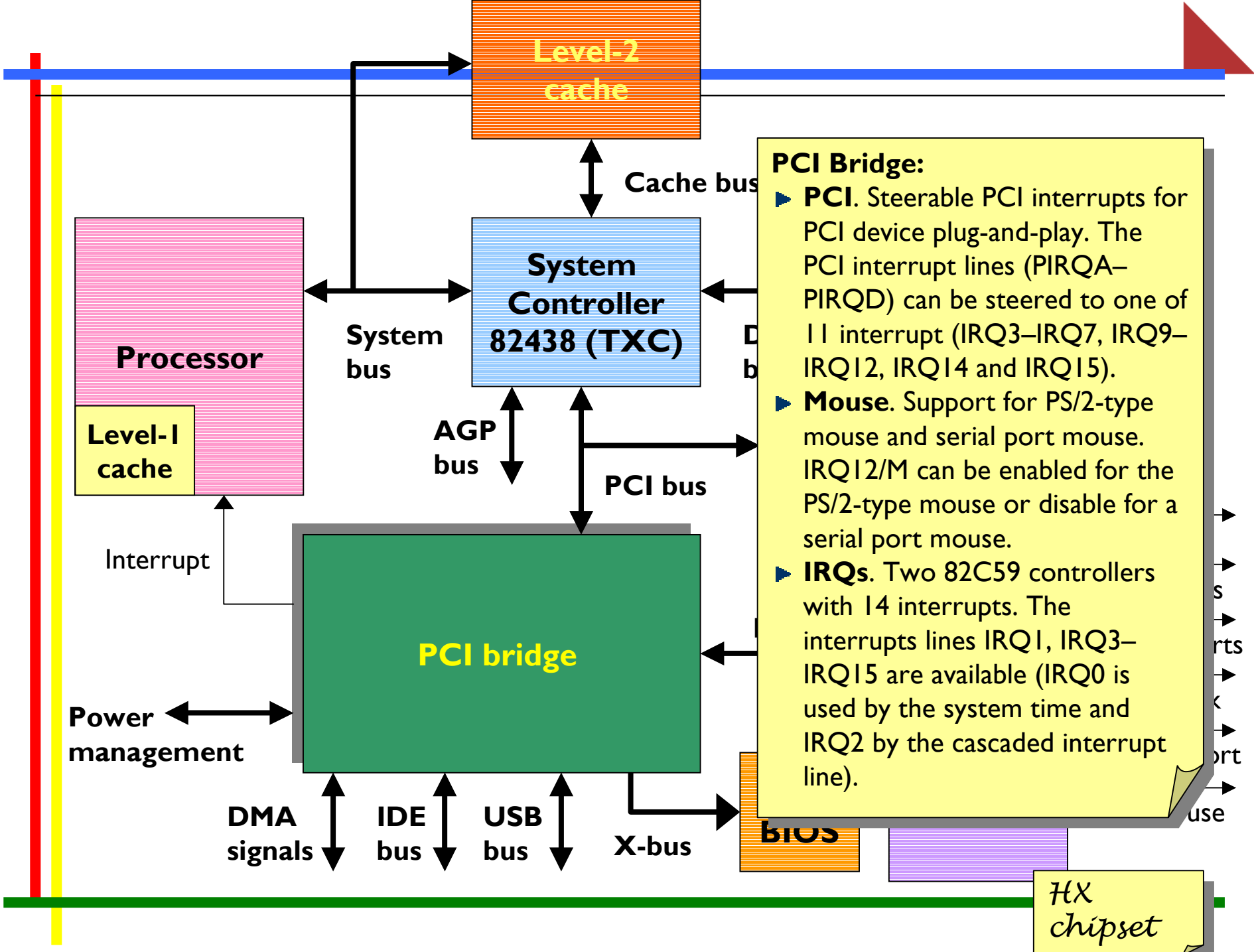
M/IO#	*D/C#*	*W/R#*	*Bus cycle type*
0	0	0	Interrupt acknowle
0	0	1	Special (see next)
0	1	0	I/O read
0	1	1	I/O write
1	0	0	Instruction fetch
1	1	0	Memory data read
1	1	1	Memory write

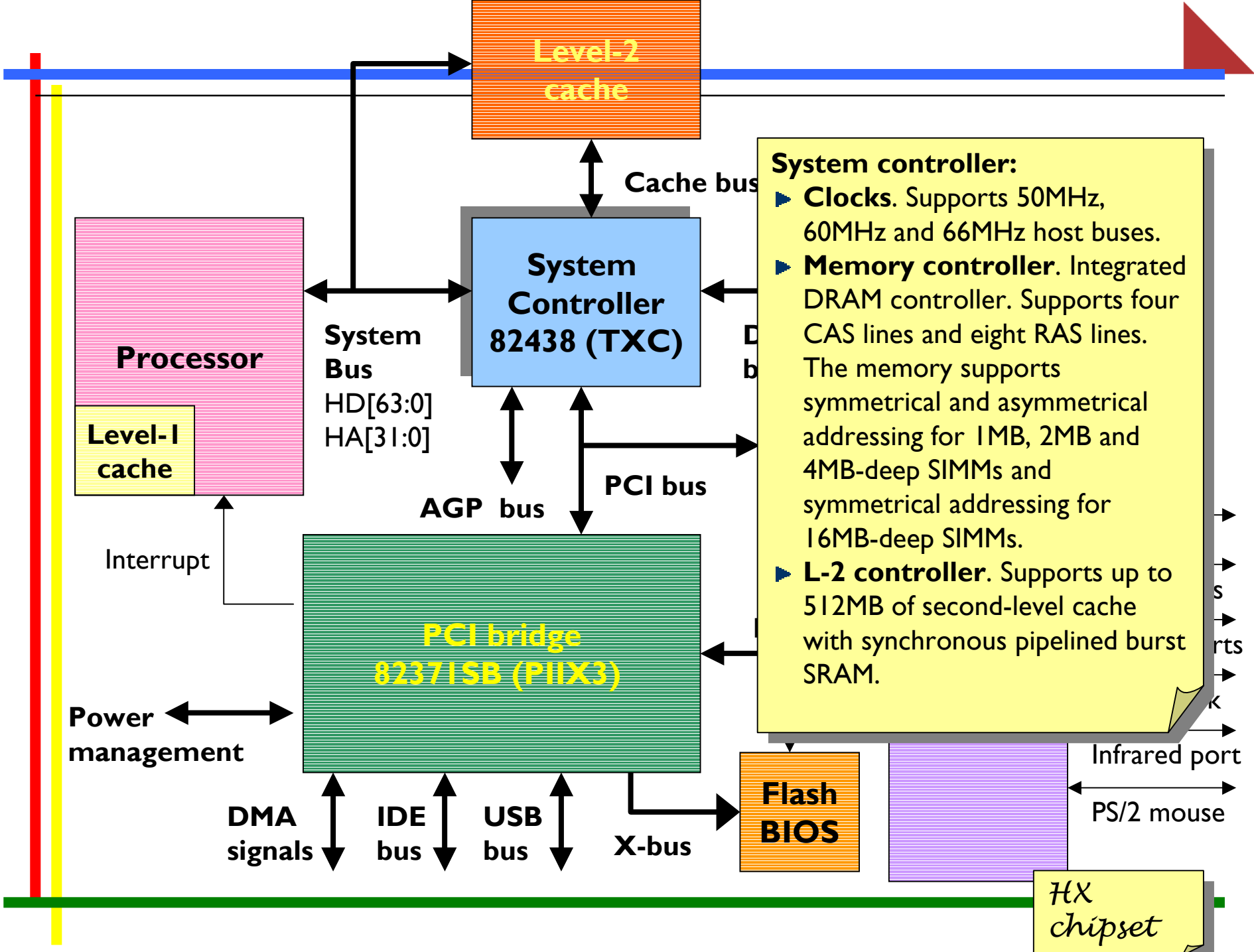

Memory
Multiplied clock
PC Processor
Video
Bridge
Network adaptor
Hard disk
Bridge
Floppy disk
Serial comms
High transfer rates (local bus). 32/64-bit at 66 MHz.
Medium transfer rates (local bus). 16/32-bit at 33 MHz.
Low transfer rates (local bus). 8/16-bit at 8 MHz.
Local bus

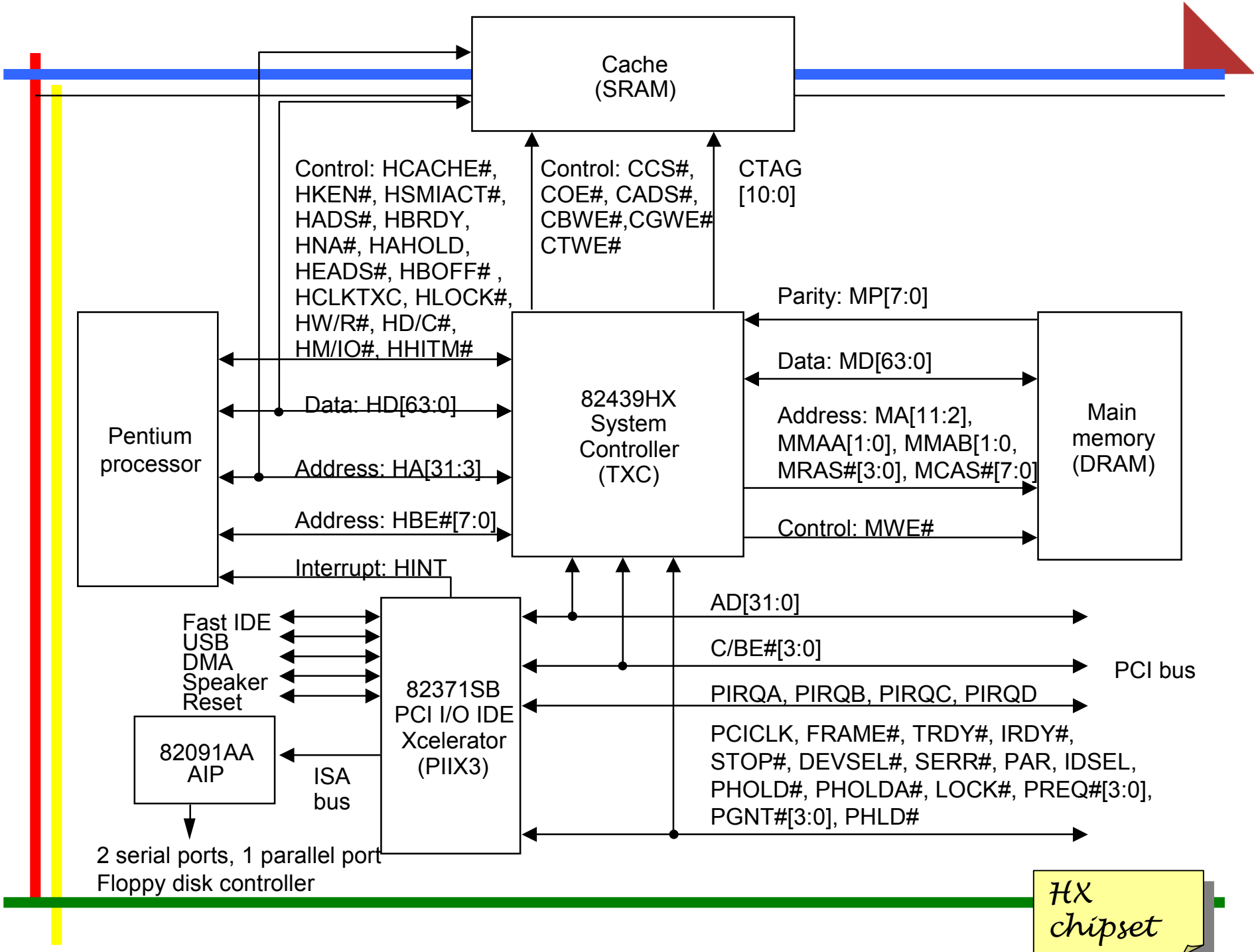

Level-2 cache
Cache bus
Processor
Level-1 cache
System bus
System Controller
DRAM bus
DRAM
AGP bus
PCI bus
Interrupt
PCI bridge
ISA bus
Ultra I/O
Keyboard
Serial ports
Parallel ports
Floppy disk
Infrared port
PS/2 mouse
Power management
DMA signals
IDE bus
USB bus
X-bus
Flash BIOS

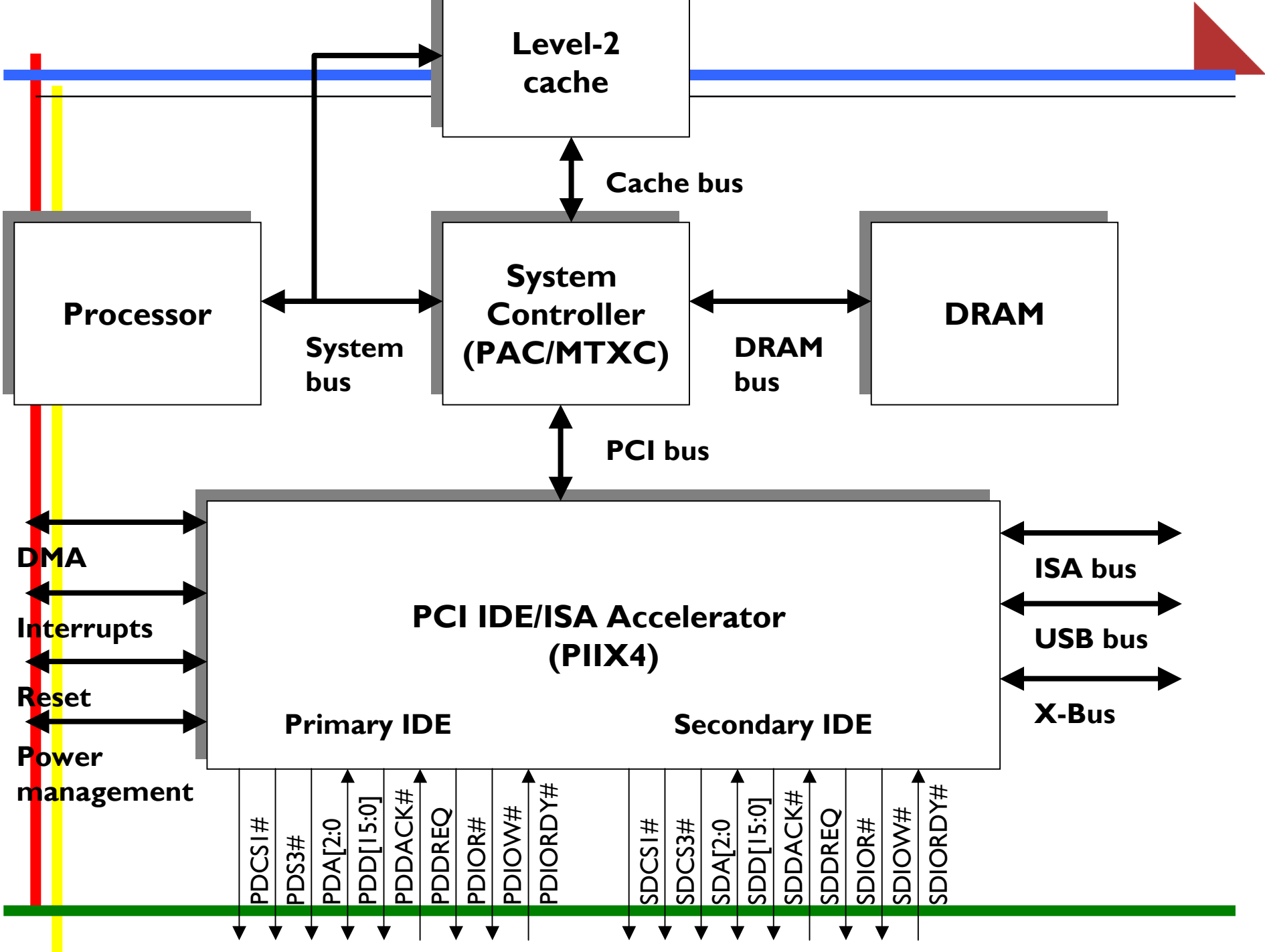

Level-2 cache
Cache bus
Processor
Level-1 cache
System bus
System Controller 82438 (TXC)
DRAM bus
DRAM
AGP bus
PCI bus
Interrupt
PCI bridge 82371SB (PIIX3)
ISA bus
Ultra I/O
Keyboard
Serial ports
Parallel ports
Floppy disk
Infrared port
PS/2 mouse
Power management
DMA signals
IDE bus
USB bus
X-bus
Flash BIOS
HX chipset

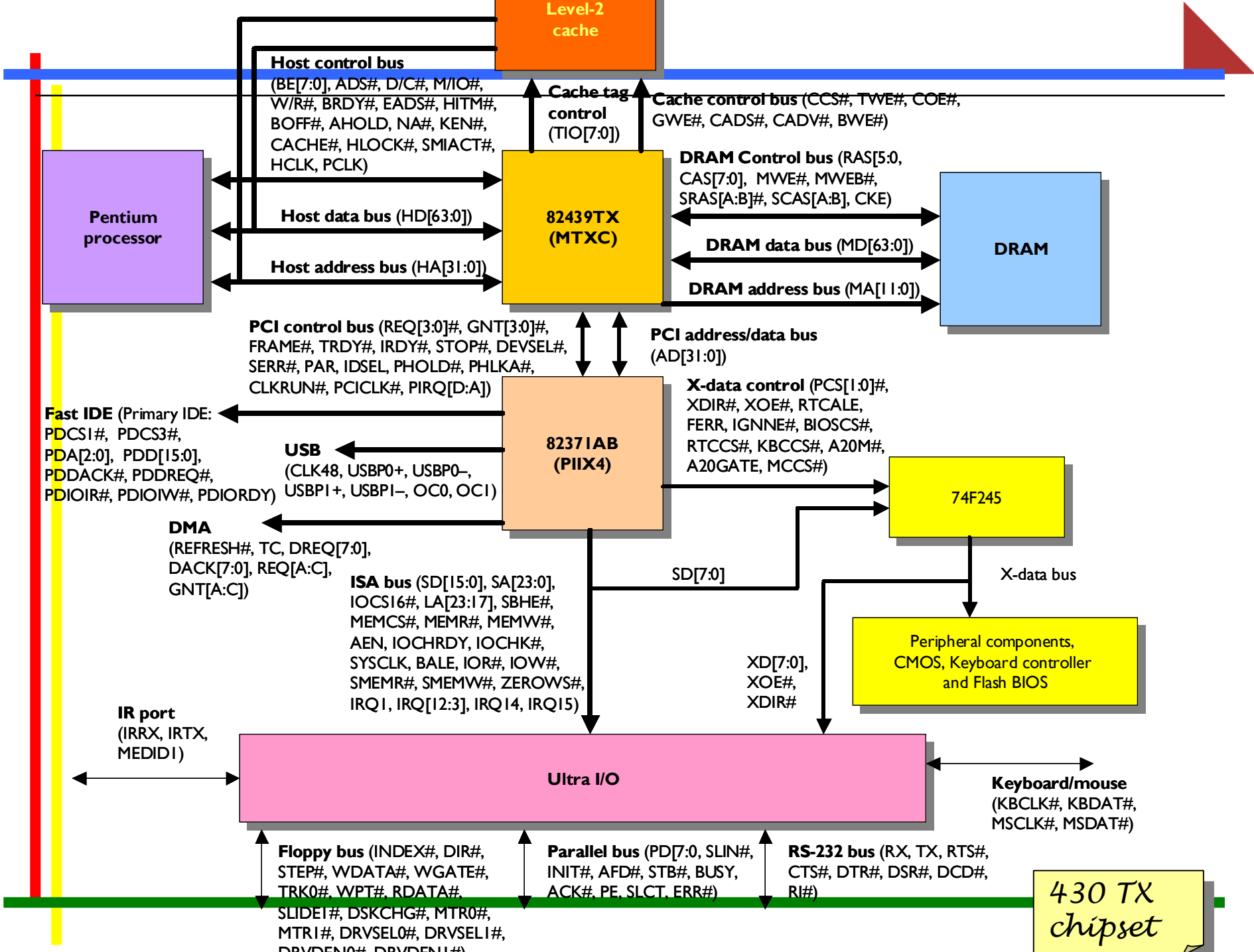

Level-2 cache
Cache bus
Processor
Level-1 cache
System bus
System Controller 82438 (TXC)
AGP bus
PCI bus
Interrupt
PCI bridge 82371SB (PIIX3)
Power management
DMA signals
IDE bus
USB bus
X-bus
Flash BIOS
Infrared port
PS/2 mouse
PCI Bridge:
DMA. Enhanced seven-channel DMA with two 8237 controllers. This is supported with the handshaking lines DRQ0–DRQ7 and DRQ0#–DRQ7#.
Fast IDE. Fast IDE support for up to four disk drives (two masters and two slaves). It supports mode four timings, which gives transfer rates of up to 22MB/s.
Timer. Incorporates 82C54 timer for system timer, refresh request and speaker output tone.
HX chipset

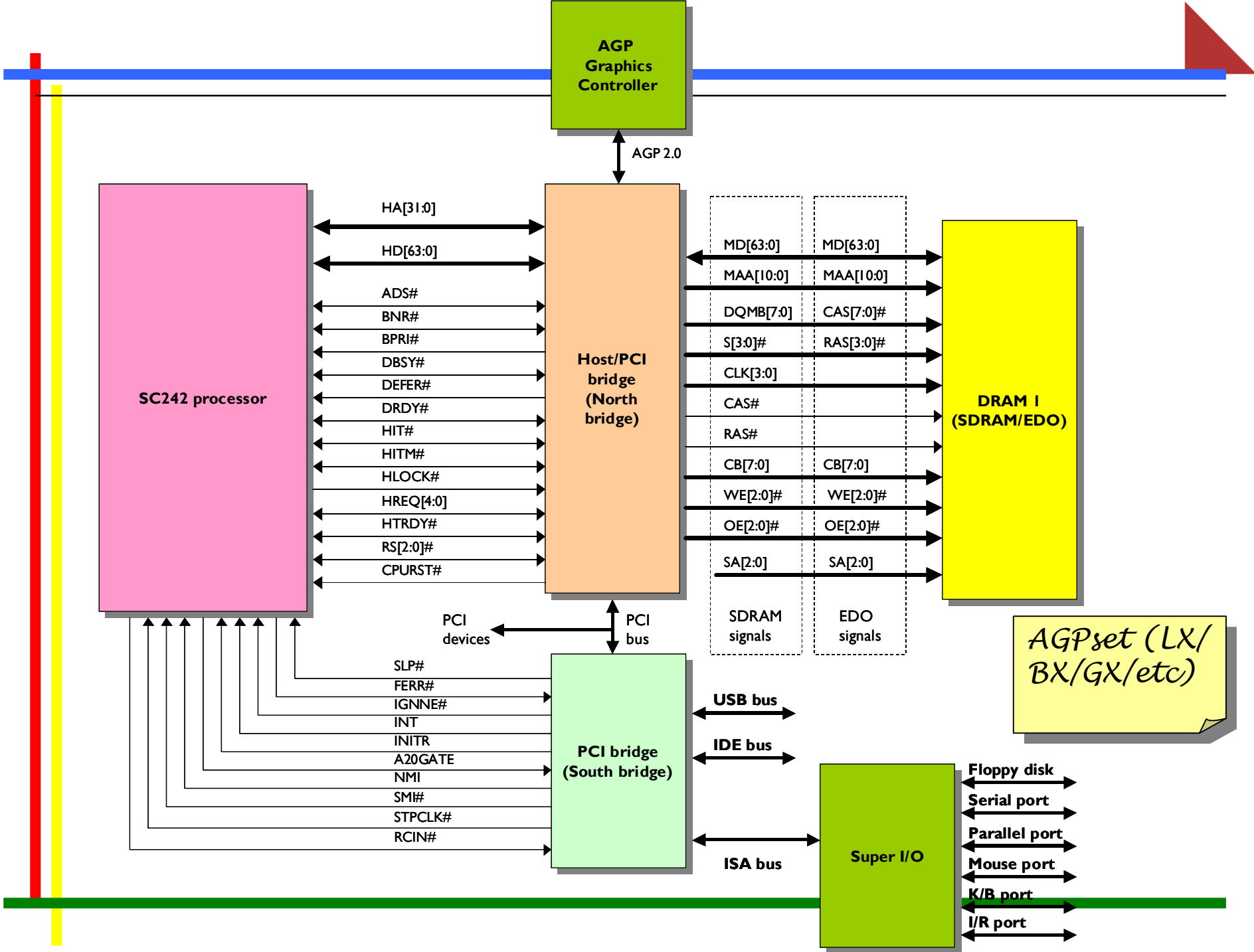

Level-2 cache
Cache bus
System Controller 82438 (TXC)
Processor
Level-1 cache
System bus
AGP bus
PCI bus
Interrupt
PCI bridge
Power management
DMA signals
IDE bus
USB bus
X-bus
BIOS
PCI Bridge:
PCI. Steerable PCI interrupts for PCI device plug-and-play. The PCI interrupt lines (PIRQA–PIRQD) can be steered to one of 11 interrupt (IRQ3–IRQ7, IRQ9–IRQ12, IRQ14 and IRQ15).
Mouse. Support for PS/2-type mouse and serial port mouse. IRQ12/M can be enabled for the PS/2-type mouse or disable for a serial port mouse.
IRQs. Two 82C59 controllers with 14 interrupts. The interrupts lines IRQ1, IRQ3–IRQ15 are available (IRQ0 is used by the system time and IRQ2 by the cascaded interrupt line).
HX chipset


Level-2 cache
Cache bus
System Controller 82438 (TXC)
Processor
Level-1 cache
System Bus
HD[63:0]
HA[31:0]
AGP bus
PCI bus
Interrupt
PCI bridge 82371SB (PIIX3)
Power management
DMA signals
IDE bus
USB bus
X-bus
Flash BIOS
Infrared port
PS/2 mouse
System controller:
Clocks. Supports 50MHz, 60MHz and 66MHz host buses.
Memory controller. Integrated DRAM controller. Supports four CAS lines and eight RAS lines. The memory supports symmetrical and asymmetrical addressing for 1MB, 2MB and 4MB-deep SIMMs and symmetrical addressing for 16MB-deep SIMMs.
L-2 controller. Supports up to 512MB of second-level cache with synchronous pipelined burst SRAM.
HX chipset


Cache
(SRAM)
Control: HCACHE#,
HKEN#, HSMIACT#,
HADS#, HBRDY,
HNA#, HAHOLD,
HEADS#, HBOFF# ,
HCLKTXC, HLOCK#,
HW/R#, HD/C#,
HM/IO#, HHITM#
Control: CCS#,
COE#, CADS#,
CBWE#,CGWE#
CTWE#
CTAG
[10:0]
Parity: MP[7:0]
Data: MD[63:0]
Address: MA[11:2],
MMAA[1:0], MMAB[1:0,
MRAS#[3:0], MCAS#[7:0]
Control: MWE#
Pentium
processor
Data: HD[63:0]
Address: HA[31:3]
Address: HBE#[7:0]
Interrupt: HINT
82439HX
System
Controller
(TXC)
Main
memory
(DRAM)
Fast IDE
USB
DMA
Speaker
Reset
82371SB
PCI I/O IDE
Xcelerator
(PIIX3)
AD[31:0]
C/BE#[3:0]
PIRQA, PIRQB, PIRQC, PIRQD
PCI bus
PCICLK, FRAME#, TRDY#, IRDY#,
STOP#, DEVSEL#, SERR#, PAR, IDSEL,
PHOLD#, PHOLDA#, LOCK#, PREQ#[3:0],
PGNT#[3:0], PHLD#
82091AA
AIP
ISA
bus
2 serial ports, 1 parallel port
Floppy disk controller
HX
chipset


Level-2
cache
Cache bus
Processor
System
bus
System
Controller
(PAC/MTXC)
DRAM
bus
DRAM
PCI bus
DMA
Interrupts
Reset
Power
management
PCI IDE/ISA Accelerator
(PIIX4)
Primary IDE
Secondary IDE
ISA bus
USB bus
X-Bus
PDCS1#
PDS3#
PDA[2:0
PDD[15:0]
PDDACK#
PDDREQ
PDIOR#
PDIOW#
PDIORDY#
SDCS1#
SDCS3#
SDA[2:0
SDD[15:0]
SDDACK#
SDDREQ
SDIOR#
SDIOW#
SDIORDY#


Level-2 cache
Host control bus (BE[7:0], ADS#, D/C#, M/IO#, W/R#, BRDY#, EADS#, HITM#, BOFF#, AHOLD, NA#, KEN#, CACHE#, HLOCK#, SMIACT#, HCLK, PCLK)
Cache tag control (TIO[7:0])
Cache control bus (CCS#, TWE#, COE#, GWE#, CADS#, CADV#, BWE#)
Pentium processor
Host data bus (HD[63:0])
Host address bus (HA[31:0])
82439TX (MTXC)
DRAM Control bus (RAS[5:0, CAS[7:0], MWE#, MWEB#, SRAS[A:B]#, SCAS[A:B], CKE)
DRAM data bus (MD[63:0])
DRAM address bus (MA[11:0])
DRAM
PCI control bus (REQ[3:0]#, GNT[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, DEVSEL#, SERR#, PAR, IDSEL, PHOLD#, PHLKA#, CLKRUN#, PCICLK#, PIRQ[D:A])
PCI address/data bus (AD[31:0])
Fast IDE (Primary IDE: PDCS1#, PDCS3#, PDA[2:0], PDD[15:0], PDDACK#, PDDREQ#, PDIOIR#, PDIOIW#, PDIORDY)
USB (CLK48, USBP0+, USBP0–, USBP1+, USBP1–, OC0, OC1)
DMA (REFRESH#, TC, DREQ[7:0], DACK[7:0], REQ[A:C], GNT[A:C])
82371AB (PIIX4)
X-data control (PCS[1:0]#, XDIR#, XOE#, RTCALE, FERR, IGNNE#, BIOSCS#, RTCCS#, KBCCS#, A20M#, A20GATE, MCCS#)
74F245
SD[7:0]
X-data bus
ISA bus (SD[15:0], SA[23:0], IOCS16#, LA[23:17], SBHE#, MEMCS#, MEMR#, MEMW#, AEN, IOCHRDY, IOCHK#, SYSCLK, BALE, IOR#, IOW#, SMEMR#, SMEMW#, ZEROWS#, IRQ1, IRQ[12:3], IRQ14, IRQ15)
Peripheral components, CMOS, Keyboard controller and Flash BIOS
XD[7:0], XOE#, XDIR#
IR port (IRRX, IRTX, MEDID1)
Ultra I/O
Keyboard/mouse (KBCLK#, KBDAT#, MSCLK#, MSDAT#)
Floppy bus (INDEX#, DIR#, STEP#, WDATA#, WGATE#, TRK0#, WPT#, RDATA#, SLIDE1#, DSKCHG#, MTR0#, MTR1#, DRVSEL0#, DRVSEL1#,
Parallel bus (PD[7:0, SLIN#, INIT#, AFD#, STB#, BUSY, ACK#, PE, SLCT, ERR#)
RS-232 bus (RX, TX, RTS#, CTS#, DTR#, DSR#, DCD#, RI#)
430 TX chipset


AGP Graphics Controller
AGP 2.0
SC242 processor
HA[31:0]
HD[63:0]
ADS#
BNR#
BPRI#
DBSY#
DEFER#
DRDY#
HIT#
HITM#
HLOCK#
HREQ[4:0]
HTRDY#
RS[2:0]#
CPURST#
Host/PCI bridge (North bridge)
MD[63:0]
MAA[10:0]
DQMB[7:0]
S[3:0]#
CLK[3:0]
CAS#
RAS#
CB[7:0]
WE[2:0]#
OE[2:0]#
SA[2:0]
MD[63:0]
MAA[10:0]
CAS[7:0]#
RAS[3:0]#
CB[7:0]
WE[2:0]#
OE[2:0]#
SA[2:0]
SDRAM signals
EDO signals
DRAM I (SDRAM/EDO)
PCI devices
PCI bus
SLP#
FERR#
IGNNE#
INT
INITR
A20GATE
NMI
SMI#
STPCLK#
RCIN#
PCI bridge (South bridge)
USB bus
IDE bus
ISA bus
Super I/O
Floppy disk
Serial port
Parallel port
Mouse port
K/B port
I/R port
AGPset (LX/BX/GX/etc)

PC Evolution

- ISA architecture.
- Addition of the PCI bus, for improved automated configuration.
- Addition of an on-chip level-1 cache.
- Addition of a level-2 cache onto the motherboards.
- Usage of the North/South bridge approach, for faster interfaces to memory.
- Enhancements of DRAM from EDO to SDRAM.
- Addition of the AGP interface, for faster interfaces to graphics.
- Movement of level-2 cache from motherboard to an on-package memory.
- Faster DRAM memory transfers with 100MHz and 133MHz SDRAM.
- **Hub-based architecture**, for faster transfers between the processor, graphics and memory.
- Fast **RDRAM**, for ultra-high data transfers between the processor and memory, and the AGP interface and memory.

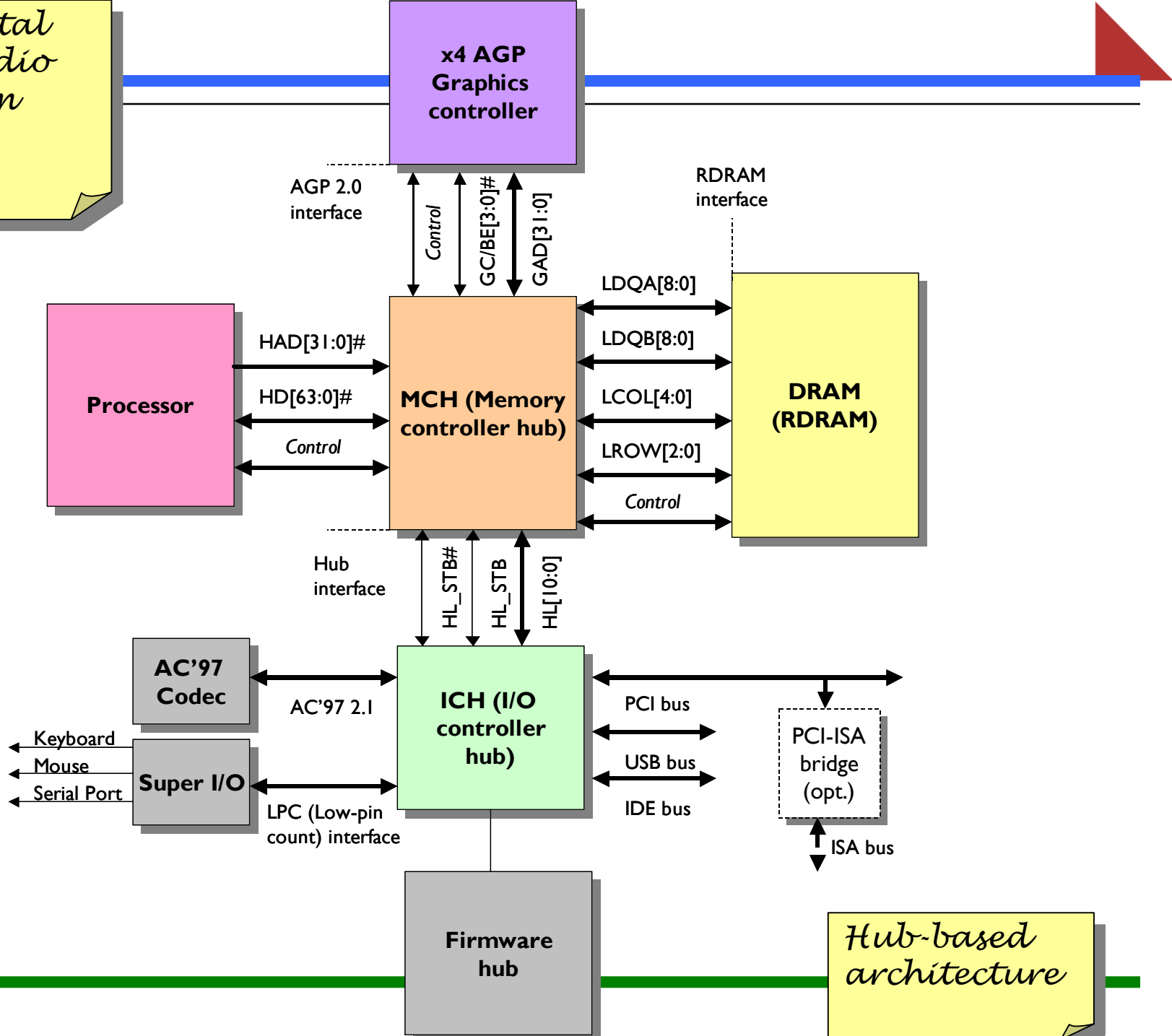
Hub-based architecture

- **810 series:** 82801 I/O controller hub (ICH), 82802 firmware hub (FWH) and 82810 graphics memory controller hub (GMCH). This GMCH has an integrated graphics controller that uses direct AGP (integrated AGP) for ultrafast 2D and 3D effects and images. The 82810 also has an integrated hardware motion compensation to improve soft DVD video quality and a digital TV out port.
- **820 series:** 82820 memory controller hub (MCH), 82801 ICH, 82802 FWH.
- **840 series:** 82840 MCH 82801 I/O ICH 82802 FWH 82806 64-bit PCI controller hub and 82803 RDRAM-based memory repeater hub (MRH-R) or 82804 SDRAM-based memory repeater hub.

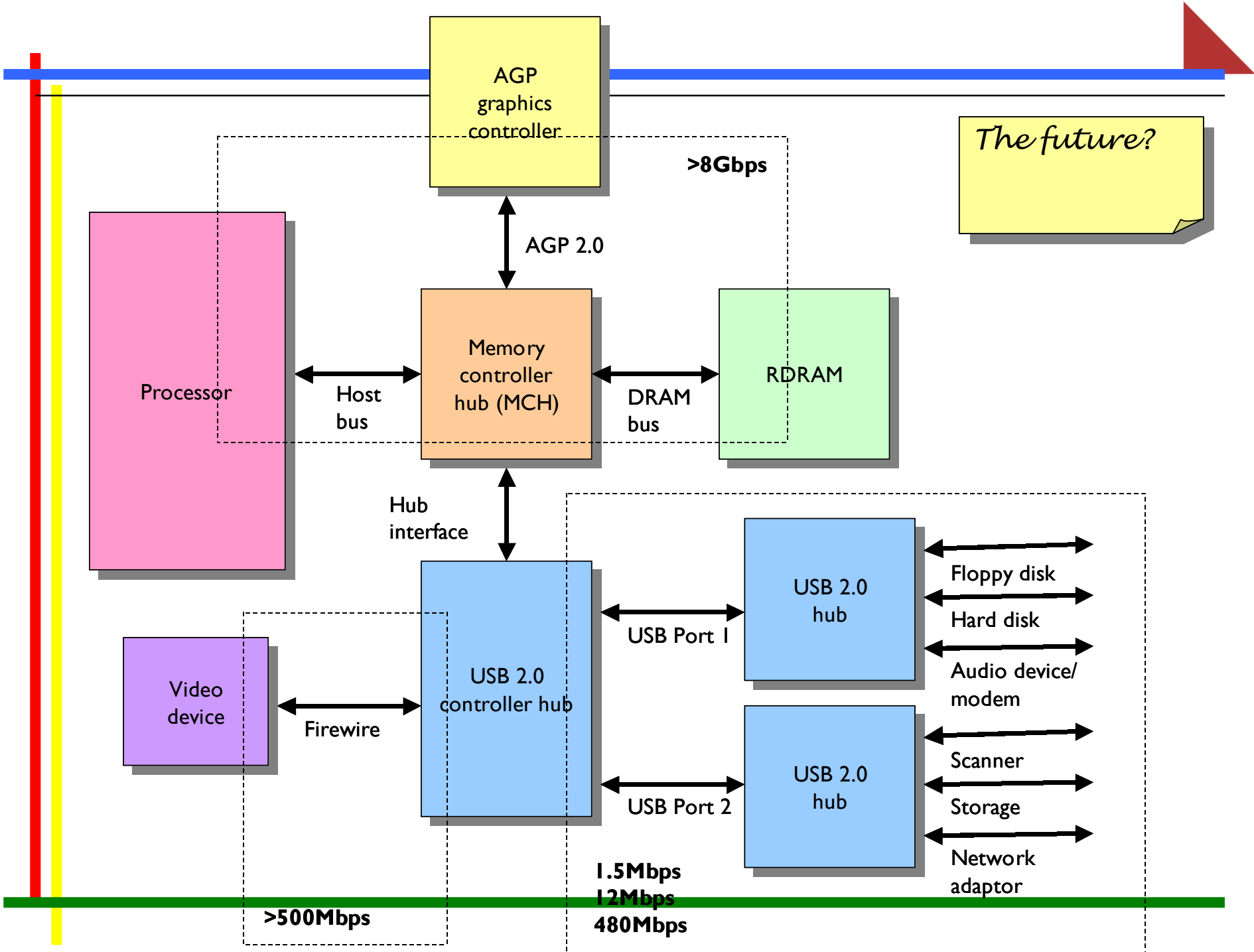
	Servers/workstation			Performance desktop			
	450NX	840	440GX	820	810E	440BX AGP	440ZX AGP
Processors	Pentium II/III Xeon	Pentium II/III Xeon	Pentium II/III Xeon	Pentium II/III	Pentium II/III	Pentium II/III	Pentium II/III
Bus signals	AGTL+	AGTL+	GTL+	AGTL+	AGTL+	GTL+	GTL+
Maximum number of processors	4	2	2	2	1	2	2
DRAM refresh	CAS-before-RAS	RDRAM Active Refresh	CAS-before-RAS	N/A	CAS-before-RAS	CAS-before-RAS	CAS-before-RAS
Memory support	8 rows	32 RDRAM devices per channel	8 rows	32 RDRAM	4 rows	8 rows	4 rows
DRAM chips supported	Yes	64/128/256 Mbit	64/128 Mbit	64/128/256 Mbit	Yes	Yes	Yes
Maximum memory	8 GB	8 GB	2 GB	1 GB	512 MB	1 GB	256 MB
Memory types	SDRAM / EDO	PC800/PC600 RDRAM PC100 SDRAM	SDRAM	RDRAM	PC100 SDRAM	SDRAM	SDRAM
PCI type	PCI 2.1	PCI 2.2	PCI 2.1	PCI 2.2	PCI 2.2	PCI 2.1	PCI 2.1
Integrated graphics	No	No	No	No	Yes	No	No
AGP type	No	AGP 1×/2×/4×	AGP 1×/2×	AGP	AGP	AGP	AGP
AGP pipe	No	PIPE	PIPE	PIPE	Integrated	PIPE	PIPE
AGP SBA	No	SBA	SBA	SBA	Integrated	SBA	SBA
South bridge	PIIX4E	ICH	PIIX4E	ICH	ICH	PIIX4E	PIIX4E
IDE type	ATA/33	ATA/66	ATA/33	ATA/66	ATA/66	ATA/33	ATA/33

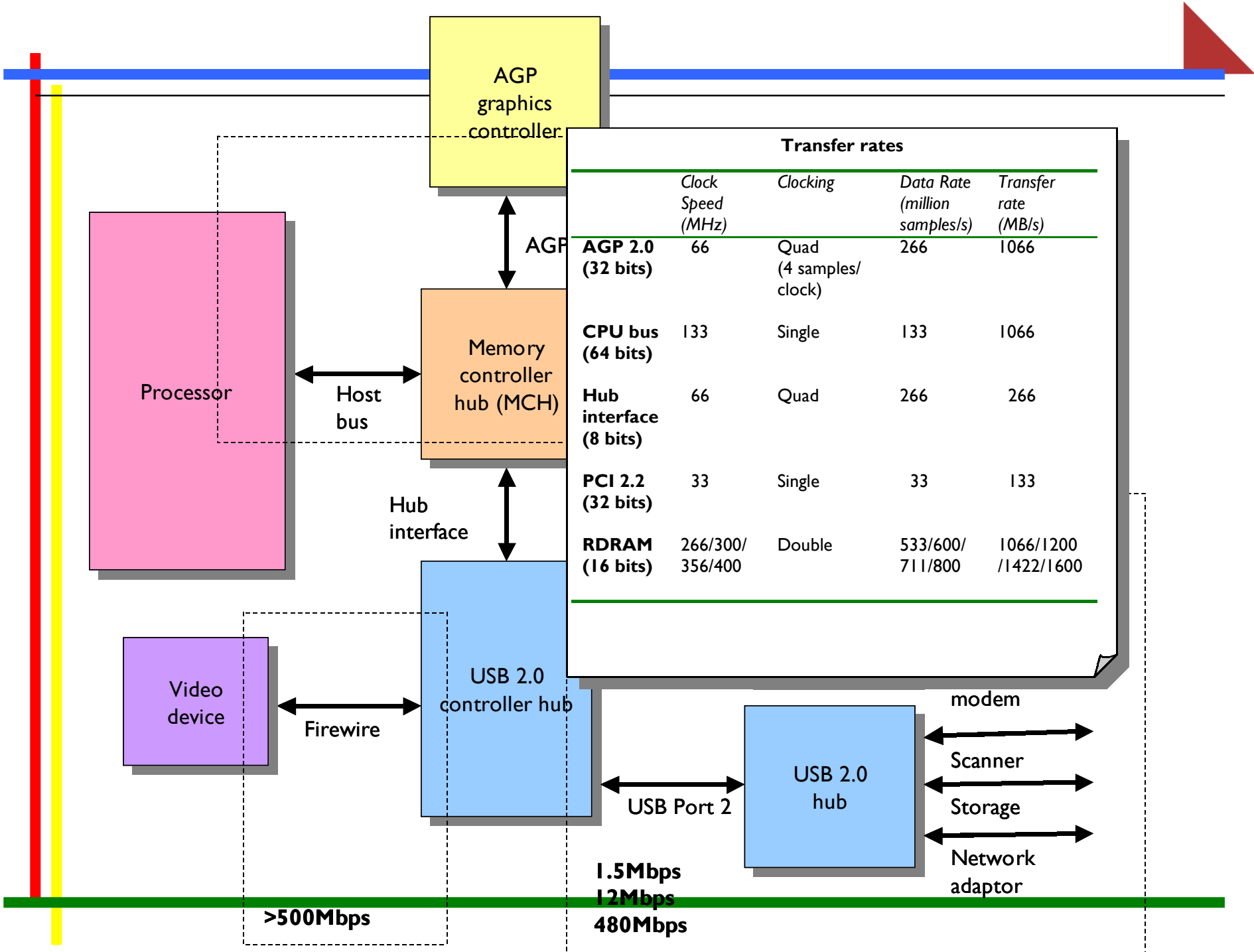
	810	440LX	440EX AGP	440ZX AGP
Processors	Pentium II/III	Pentium Celeron	Pentium Celeron	Pentium Celeron
Bus signals	AGTL+	GTL+	GTL+	AGTL+
Maximum number of processors	1	2	1	1
DRAM refresh	CAS-before-RAS	CAS-before-RAS	CAS-before-RAS	CAS-before-RAS
Memory support	4 rows	8 rows	4 rows	4 rows
DRAM chips supported	16/ 64/128 Mbit	Yes	Yes	Yes
Maximum memory	512MB	1 GB	256 MB	256 MB
Memory types	PC100 SDRAM	EDO SDRAM	SDRAM	EDO SDRAM
PCI type	PCI 2.2	PCI 2.1	PCI 2.1	PCI 2.1
Integrated graphics	Yes	No	No	No
AGP type	Integrated	AGP 1×/ 2×	AGP 1×/ 2×	AGP 1×/ 2×
AGP pipe	Integrated	PIPE	PIPE	PIPE
AGP SBA	Integrated	SBA	SBA	SBA
South bridge	ICH	PIIX4E	PIIX4E	PIIX4E
IDE type	ATA/66	ATA/33	ATA/33	ATA/33

AC'97: Digital link for audio and modem codec.



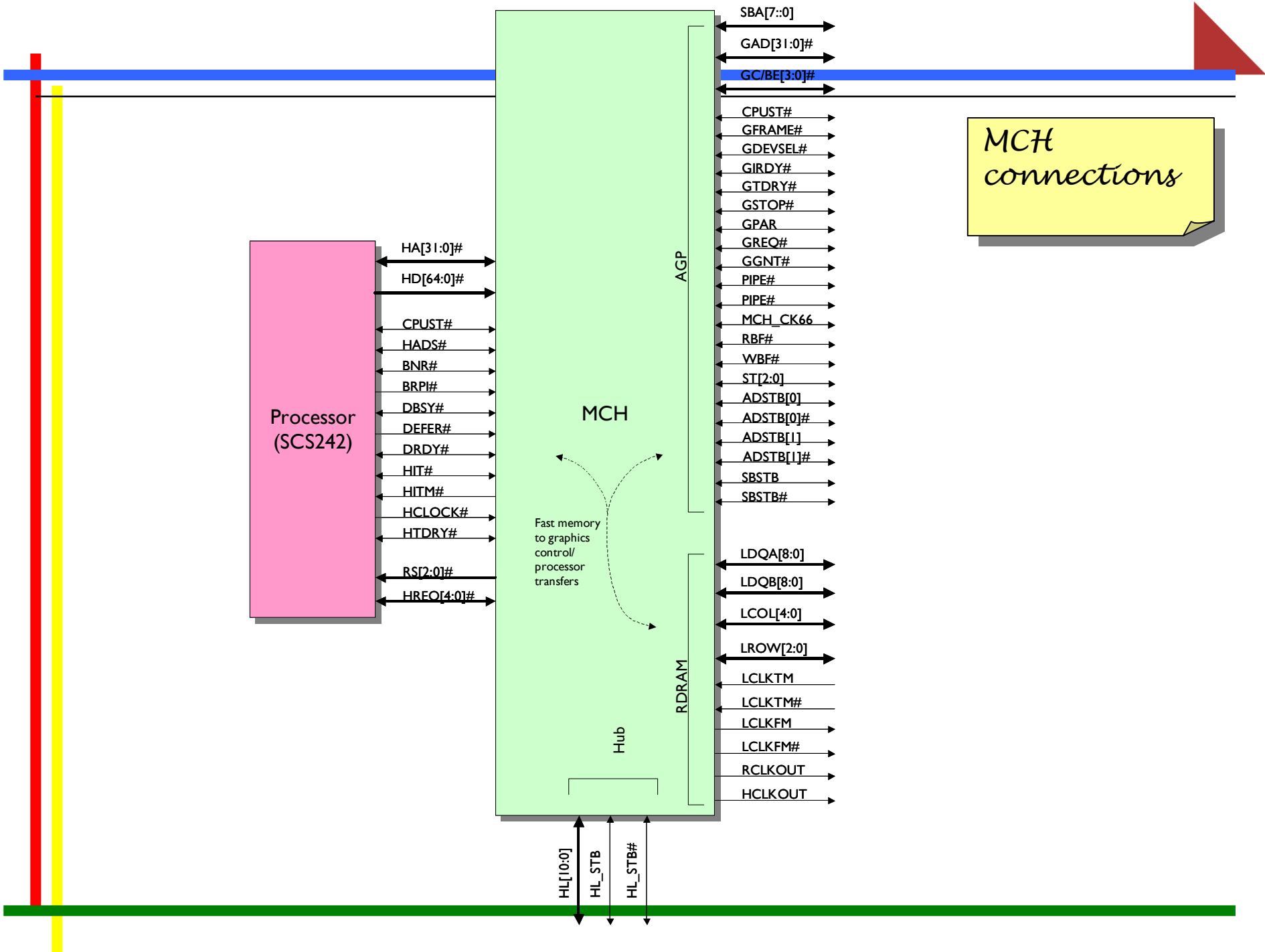
Hub-based architecture

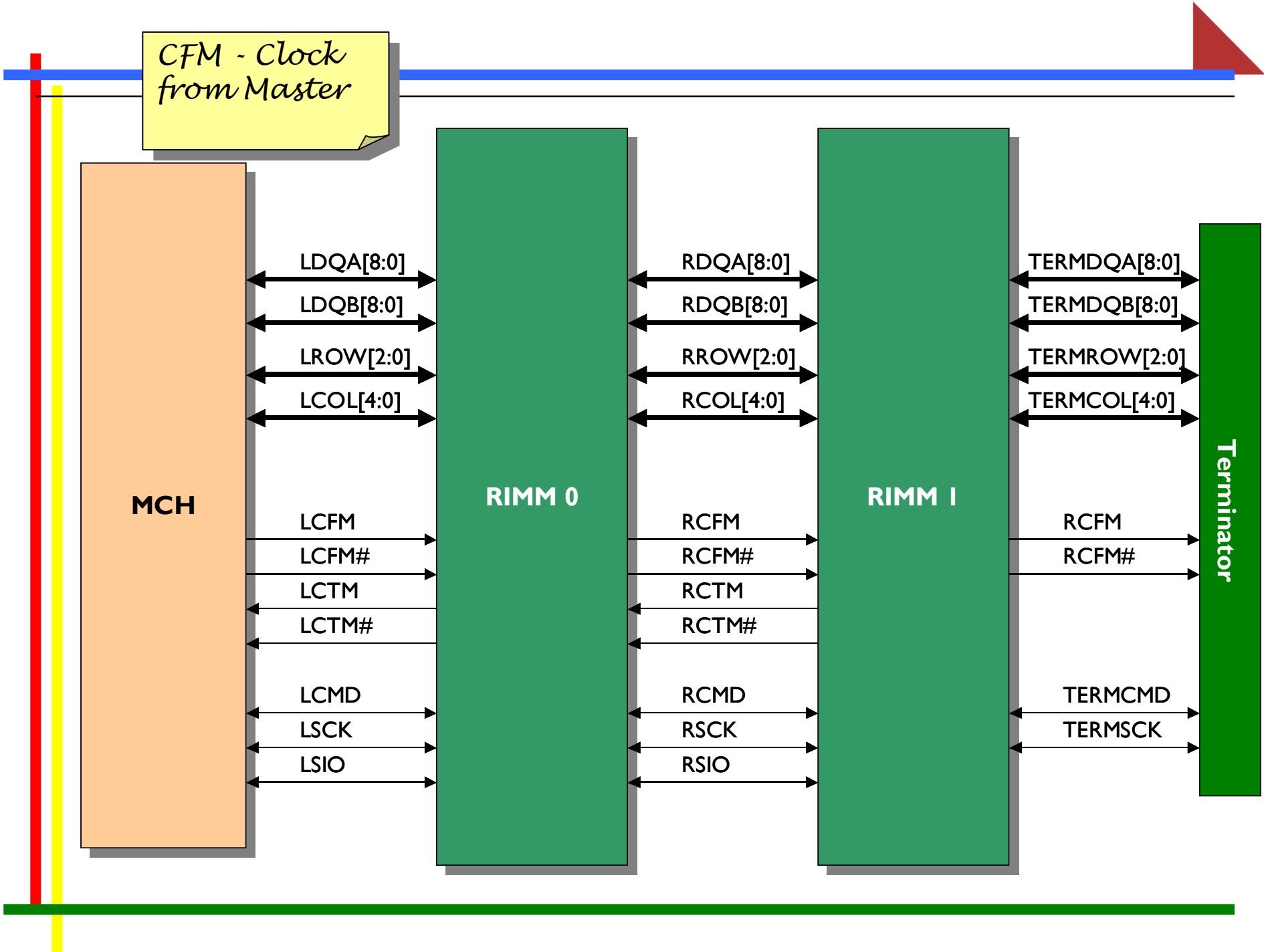

AGP graphics controller
>8Gbps
The future?
AGP 2.0
Processor
Host bus
Memory controller hub (MCH)
DRAM bus
RDRAM
Hub interface
USB 2.0 hub
Floppy disk
Hard disk
Audio device/ modem
USB Port 1
Video device
Firewire
USB 2.0 controller hub
USB 2.0 hub
Scanner
Storage
Network adaptor
USB Port 2
1.5Mbps
12Mbps
480Mbps
>500Mbps

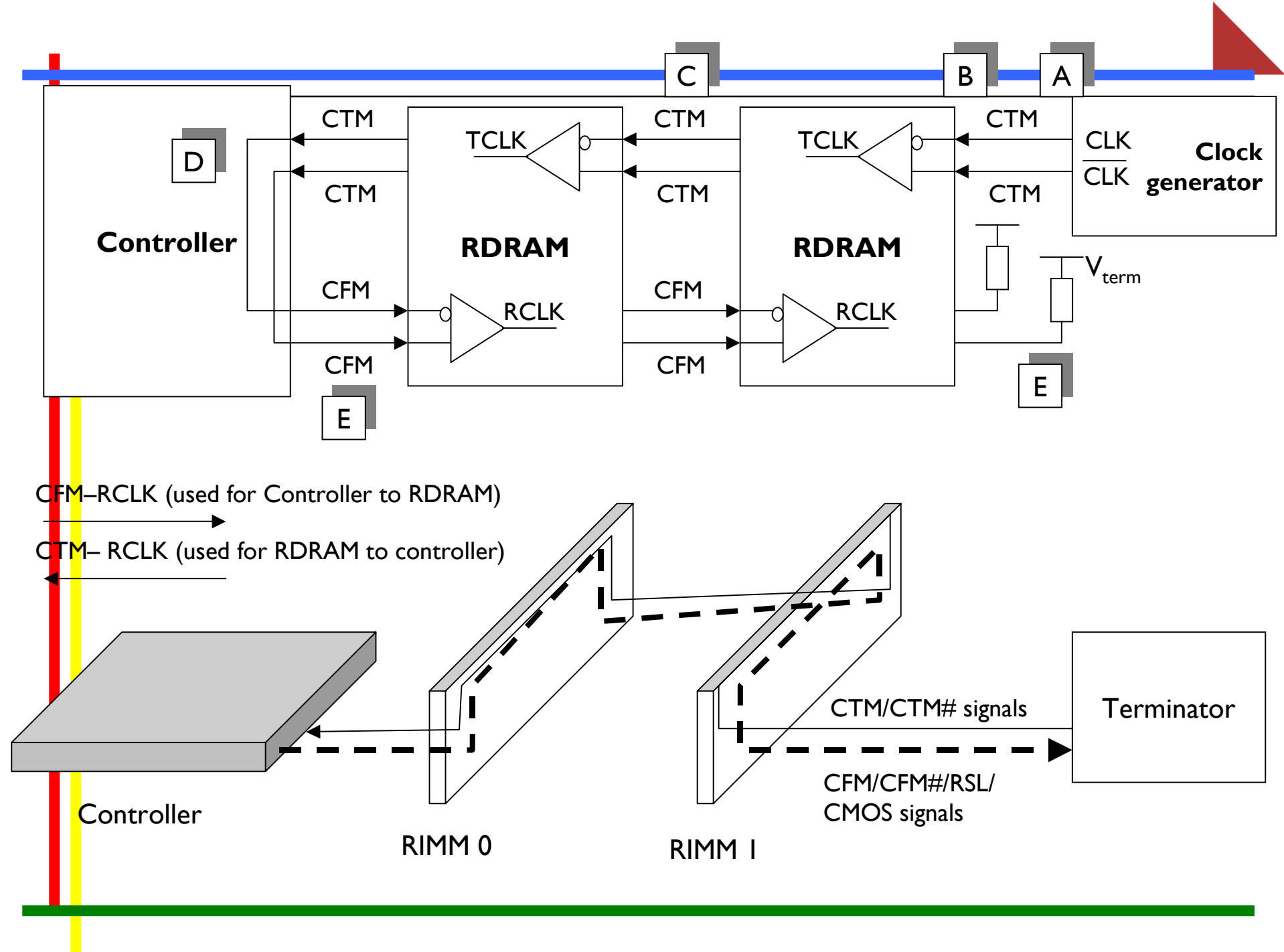


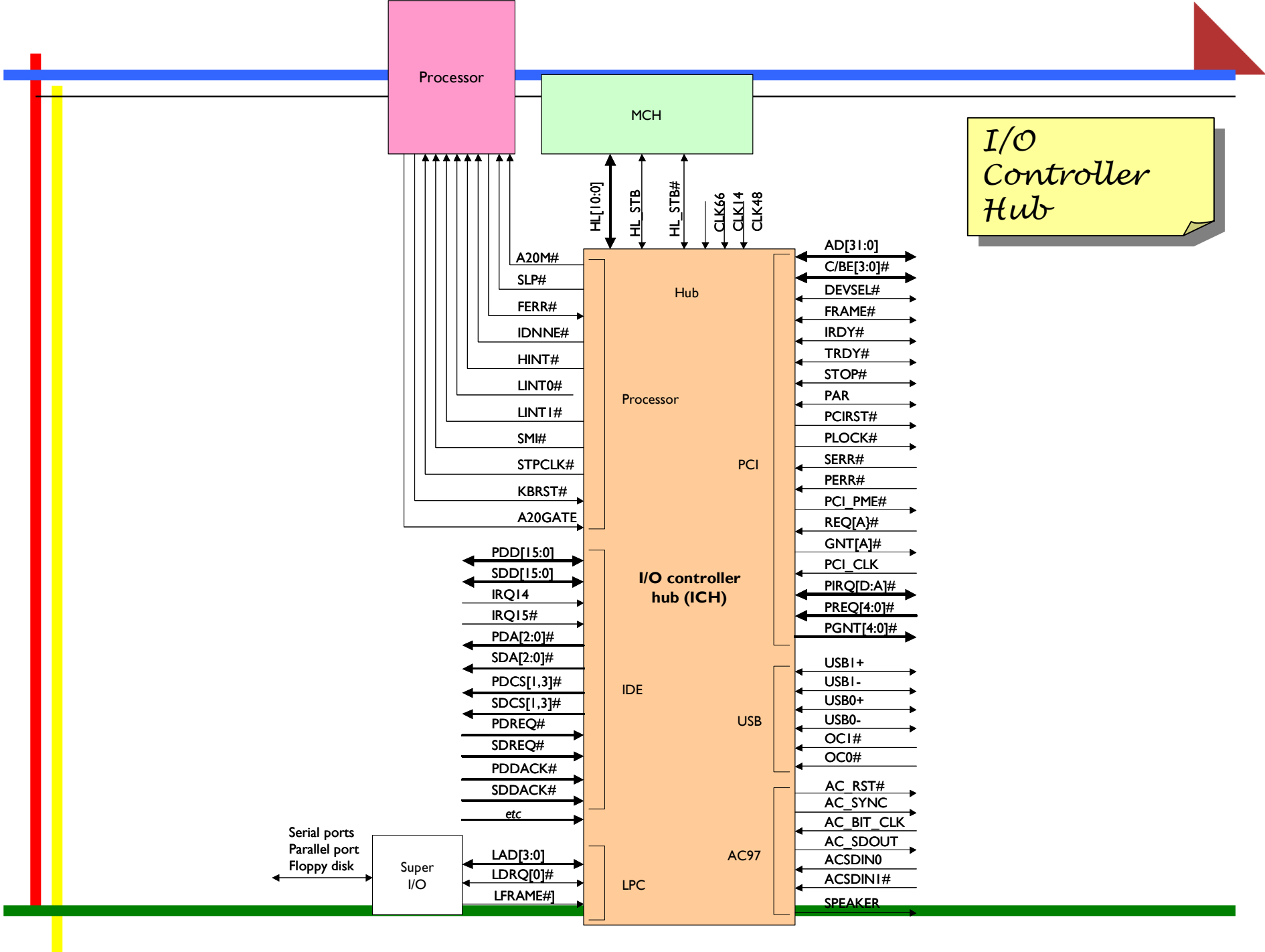
Transfer rates

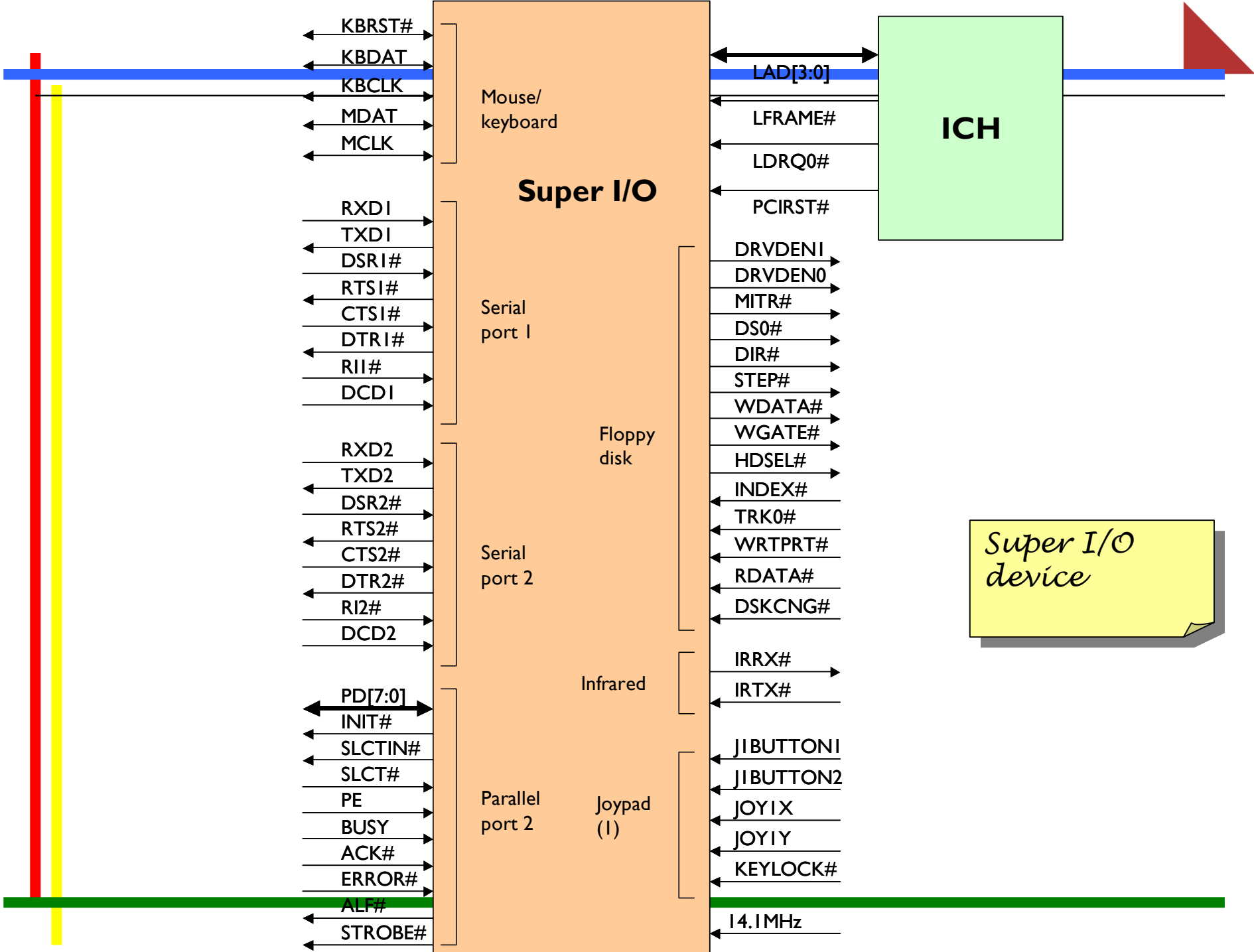
	Clock Speed (MHz)	*Clocking*	*Data Rate (million samples/s)*	*Transfer rate (MB/s)*
AGP 2.0 (32 bits)	66	Quad (4 samples/ clock)	266	1066
CPU bus (64 bits)	133	Single	133	1066
Hub interface (8 bits)	66	Quad	266	266
PCI 2.2 (32 bits)	33	Single	33	133
RDRAM (16 bits)	266/300/ 356/400	Double	533/600/ 711/800	1066/1200 /1422/1600

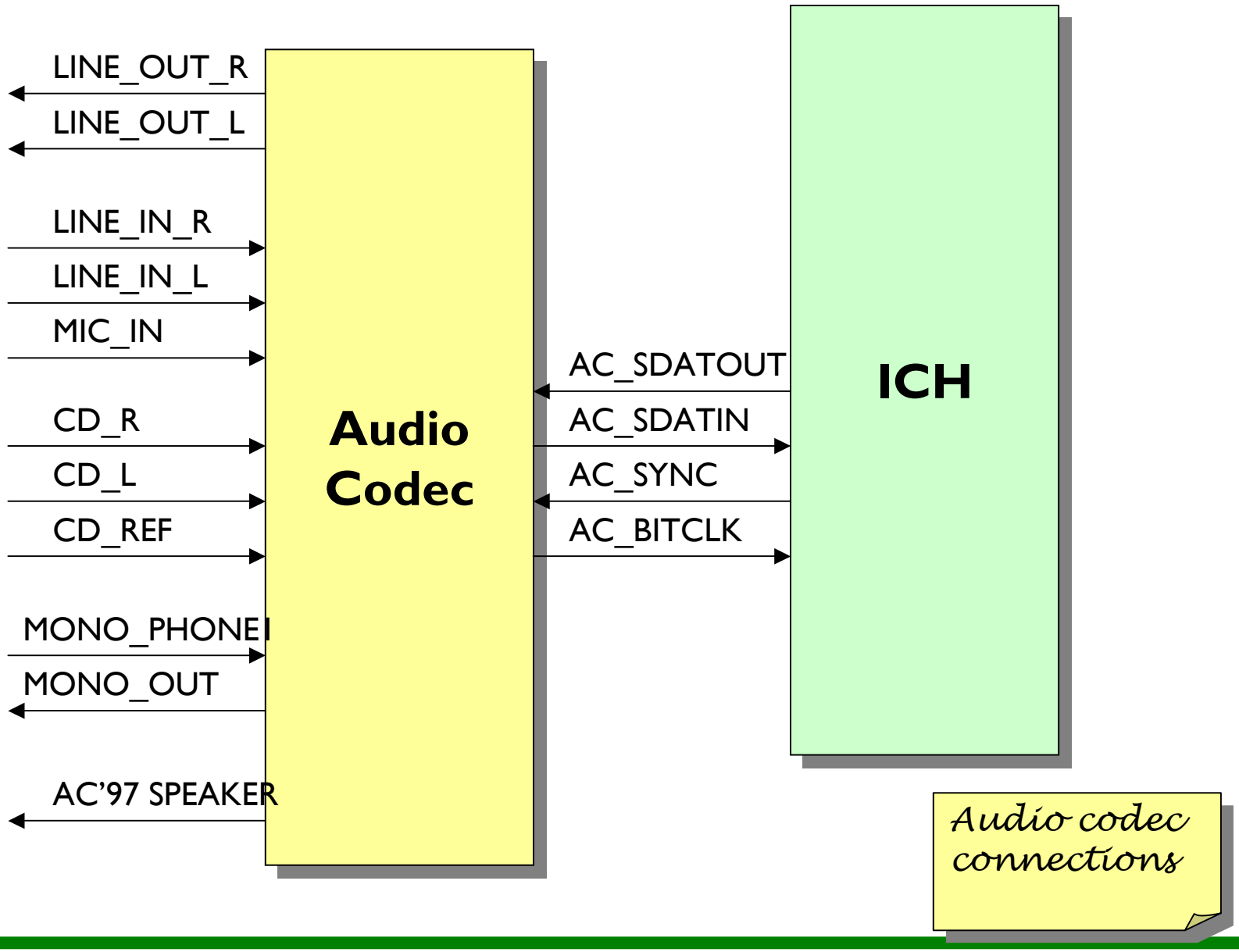

MCH connections
Processor (SCS242)
HA[31:0]#
HD[64:0]#
CPUST#
HADS#
BNR#
BRPI#
DBSY#
DEFER#
DRDY#
HIT#
HITM#
HCLOCK#
HTDRY#
RS[2:0]#
HREQ[4:0]#
MCH
Fast memory to graphics control/ processor transfers
Hub
AGP
RDRAM
SBA[7::0]
GAD[31:0]#
GC/BE[3:0]#
CPUST#
GFRAME#
GDEVSEL#
GIRDY#
GTDRY#
GSTOP#
GPAR
GREQ#
GGNT#
PIPE#
PIPE#
MCH_CK66
RBF#
WBF#
ST[2:0]
ADSTB[0]
ADSTB[0]#
ADSTB[1]
ADSTB[1]#
SBSTB
SBSTB#
LDQA[8:0]
LDQB[8:0]
LCOL[4:0]
LROW[2:0]
LCLKTM
LCLKTM#
LCLKFM
LCLKFM#
RCLKOUT
HCLKOUT
HL[10:0]
HL_STB
HL_STB#

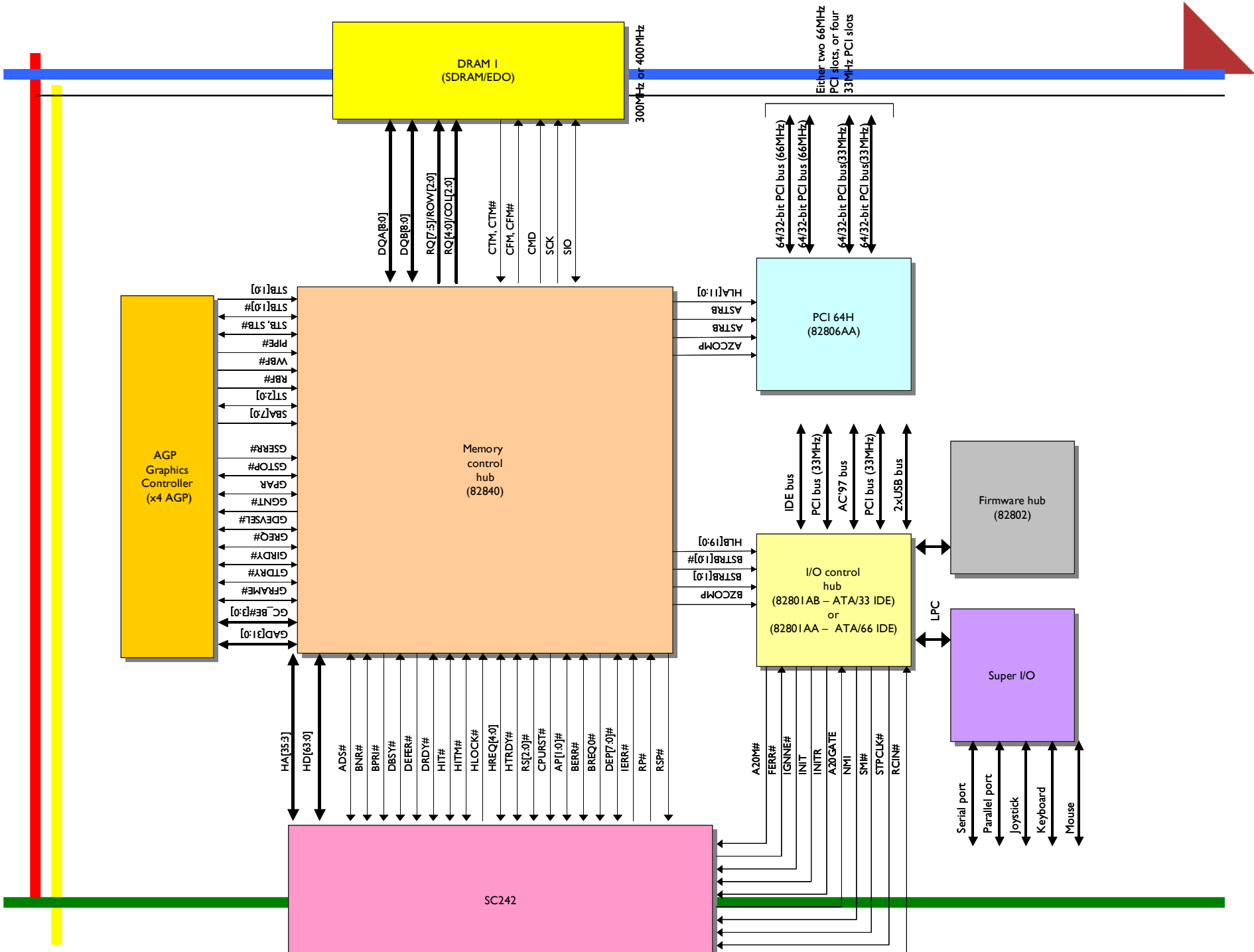

CFM - Clock from Master
MCH
RIMM 0
RIMM 1
Terminator
LDQA[8:0]
LDQB[8:0]
LROW[2:0]
LCOL[4:0]
RDQA[8:0]
RDQB[8:0]
RROW[2:0]
RCOL[4:0]
TERMDQA[8:0]
TERMDQB[8:0]
TERMROW[2:0]
TERMCOL[4:0]
LCFM
LCFM#
LCTM
LCTM#
RCFM
RCFM#
RCTM
RCTM#
RCFM
RCFM#
LCMD
LSCK
LSIO
RCMD
RSCK
RSIO
TERMCMD
TERMSCK

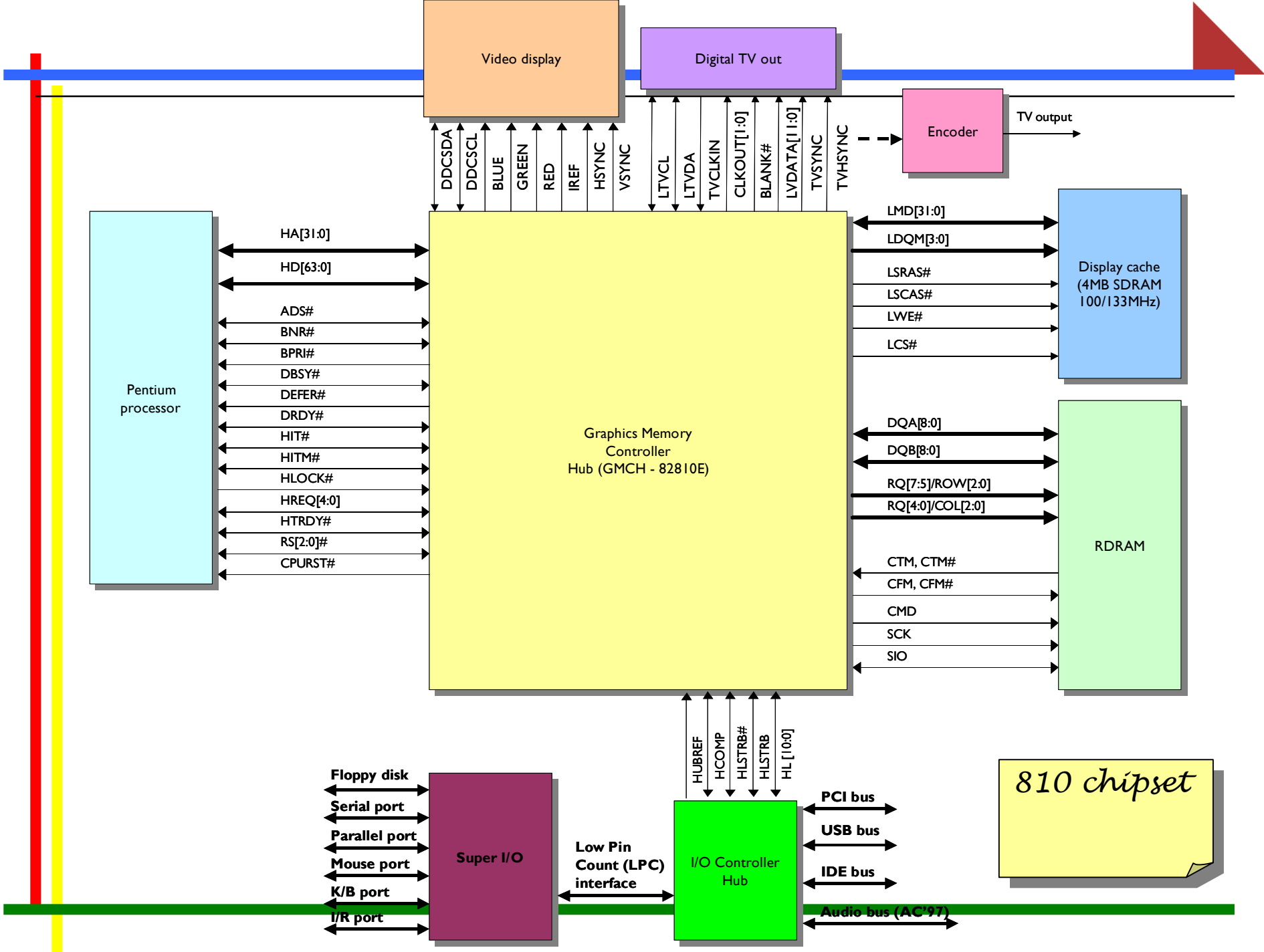

C
B
A
D
CTM
CTM
TCLK
CTM
CTM
TCLK
CTM
CLK
CLK
Clock generator
Controller
RDRAM
RDRAM
CTM
V_{term}
CFM
RCLK
CFM
RCLK
CFM
CFM
E
E
CFM–RCLK (used for Controller to RDRAM)
CTM– RCLK (used for RDRAM to controller)
CTM/CTM# signals
Terminator
CFM/CFM#/RSL/
CMOS signals
Controller
RIMM 0
RIMM 1


Processor
MCH
I/O Controller Hub
HL[10:0]
HL_STB
HL_STB#
CLK66
CLK14
CLK48
A20M#
SLP#
FERR#
IDNNE#
HINT#
LINT0#
LINT1#
SMI#
STPCLK#
KBRST#
A20GATE
Hub
Processor
PCI
I/O controller hub (ICH)
IDE
USB
AC97
LPC
AD[31:0]
C/BE[3:0]#
DEVSEL#
FRAME#
IRDY#
TRDY#
STOP#
PAR
PCIRST#
PLOCK#
SERR#
PERR#
PCI_PME#
REQ[A]#
GNT[A]#
PCI_CLK
PIRQ[D:A]#
PREQ[4:0]#
PGNT[4:0]#
PDD[15:0]
SDD[15:0]
IRQ14
IRQ15#
PDA[2:0]#
SDA[2:0]#
PDCS[1,3]#
SDCS[1,3]#
PDREQ#
SDREQ#
PDDACK#
SDDACK#
etc
USB1+
USB1-
USB0+
USB0-
OC1#
OC0#
AC_RST#
AC_SYNC
AC_BIT_CLK
AC_SDOUT
ACSDIN0
ACSDIN1#
SPEAKER
Serial ports
Parallel port
Floppy disk
Super I/O
LAD[3:0]
LDRQ[0]#
LFRAME#]


KBRST#
KBDAT
KBCLK
MDAT
MCLK
Mouse/
keyboard
Super I/O
RXD1
TXD1
DSR1#
RTS1#
CTS1#
DTR1#
RI1#
DCD1
Serial
port 1
RXD2
TXD2
DSR2#
RTS2#
CTS2#
DTR2#
RI2#
DCD2
Serial
port 2
PD[7:0]
INIT#
SLCTIN#
SLCT#
PE
BUSY
ACK#
ERROR#
ALF#
STROBE#
Parallel
port 2
LAD[3:0]
LFRAME#
LDRQ0#
PCIRST#
ICH
DRVDEN1
DRVDEN0
MITR#
DS0#
DIR#
STEP#
WDATA#
WGATE#
HDSEL#
INDEX#
TRK0#
WRTPRT#
RDATA#
DSKCNG#
Floppy
disk
IRRX#
IRTX#
Infrared
J1BUTTON1
J1BUTTON2
JOY1X
JOY1Y
KEYLOCK#
Joypad
(1)
14.1MHz
Super I/O
device


LINE_OUT_R
LINE_OUT_L
LINE_IN_R
LINE_IN_L
MIC_IN
CD_R
CD_L
CD_REF
MONO_PHONE1
MONO_OUT
AC'97 SPEAKER
Audio Codec
AC_SDATOUT
AC_SDATIN
AC_SYNC
AC_BITCLK
ICH
Audio codec connections


DRAM I
(SDRAM/EDO)
300MHz or 400MHz
Either two 66MHz
PCI slots, or four
33MHz PCI slots
64/32-bit PCI bus (66MHz)
64/32-bit PCI bus (66MHz)
64/32-bit PCI bus(33MHz)
64/32-bit PCI bus(33MHz)
DQA[8:0]
DQB[8:0]
RQ[7:5]/ROW[2:0]
RQ[4:0]/COL[2:0]
CTM, CTM#
CFM, CFM#
CMD
SCK
SIO
AGP
Graphics
Controller
(x4 AGP)
Memory
control
hub
(82840)
PCI 64H
(82806AA)
HLA[11:0]
ASTRB
ASTRB
AZCOMP
STB[1:0]
STB[1:0]#
STB, STB#
PIPE#
WBF#
RBF#
ST[2:0]
SBA[7:0]
GSERR#
GSTOP#
GPAR
GGNT#
GDEVSEL#
GREQ#
GIRDY#
GTDRY#
GFRAME#
GC_BE#[3:0]
GAD[31:0]
IDE bus
PCI bus (33MHz)
AC'97 bus
PCI bus (33MHz)
2xUSB bus
Firmware hub
(82802)
HLB[10:0]
BSTRB[1:0]#
BSTRB[1:0]
BZCOMP
I/O control
hub
(82801AB – ATA/33 IDE)
or
(82801AA – ATA/66 IDE)
LPC
Super I/O
HA[35:3]
HD[63:0]
ADS#
BNR#
BPRI#
DBSY#
DEFER#
DRDY#
HIT#
HITM#
HLOCK#
HREQ[4:0]
HTRDY#
RS[2:0]#
CPURST#
AP[1:0]#
BERR#
BREQ0#
DEP[7:0]#
IERR#
RP#
RSP#
A20M#
FERR#
IGNNE#
INIT
INITR
A20GATE
NMI
SMI#
STPCLK#
RCIN#
Serial port
Parallel port
Joystick
Keyboard
Mouse
SC242


Video display
Digital TV out
Encoder
TV output
DDCSDA
DDCSCL
BLUE
GREEN
RED
IREF
HSYNC
VSYNC
LTVCL
LTVDA
TVCLKIN
CLKOUT[1:0]
BLANK#
LVDATA[11:0]
TVSYNC
TVHSYNC
Pentium processor
HA[31:0]
HD[63:0]
ADS#
BNR#
BPRI#
DBSY#
DEFER#
DRDY#
HIT#
HITM#
HLOCK#
HREQ[4:0]
HTRDY#
RS[2:0]#
CPURST#
Graphics Memory Controller Hub (GMCH - 82810E)
LMD[31:0]
LDQM[3:0]
LSRAS#
LSCAS#
LWE#
LCS#
Display cache (4MB SDRAM 100/133MHz)
DQA[8:0]
DQB[8:0]
RQ[7:5]/ROW[2:0]
RQ[4:0]/COL[2:0]
CTM, CTM#
CFM, CFM#
CMD
SCK
SIO
RDRAM
HUBREF
HCOMP
HLSTRB#
HLSTRB
HL[10:0]
Floppy disk
Serial port
Parallel port
Mouse port
K/B port
I/R port
Super I/O
Low Pin Count (LPC) interface
I/O Controller Hub
PCI bus
USB bus
IDE bus
Audio bus (AC'97)
810 chipset

Conclusions

- Move towards hub-based systems.
- Move to systems based around hot plug-and-play systems such as Firewire and USB.
- Modern hub-based systems optimise the flow of data.
- PCI and ISA will be phased-out as they are legacy based.
- Enhanced memory devices, such as RDRAMs increase the maximum transfer rate.