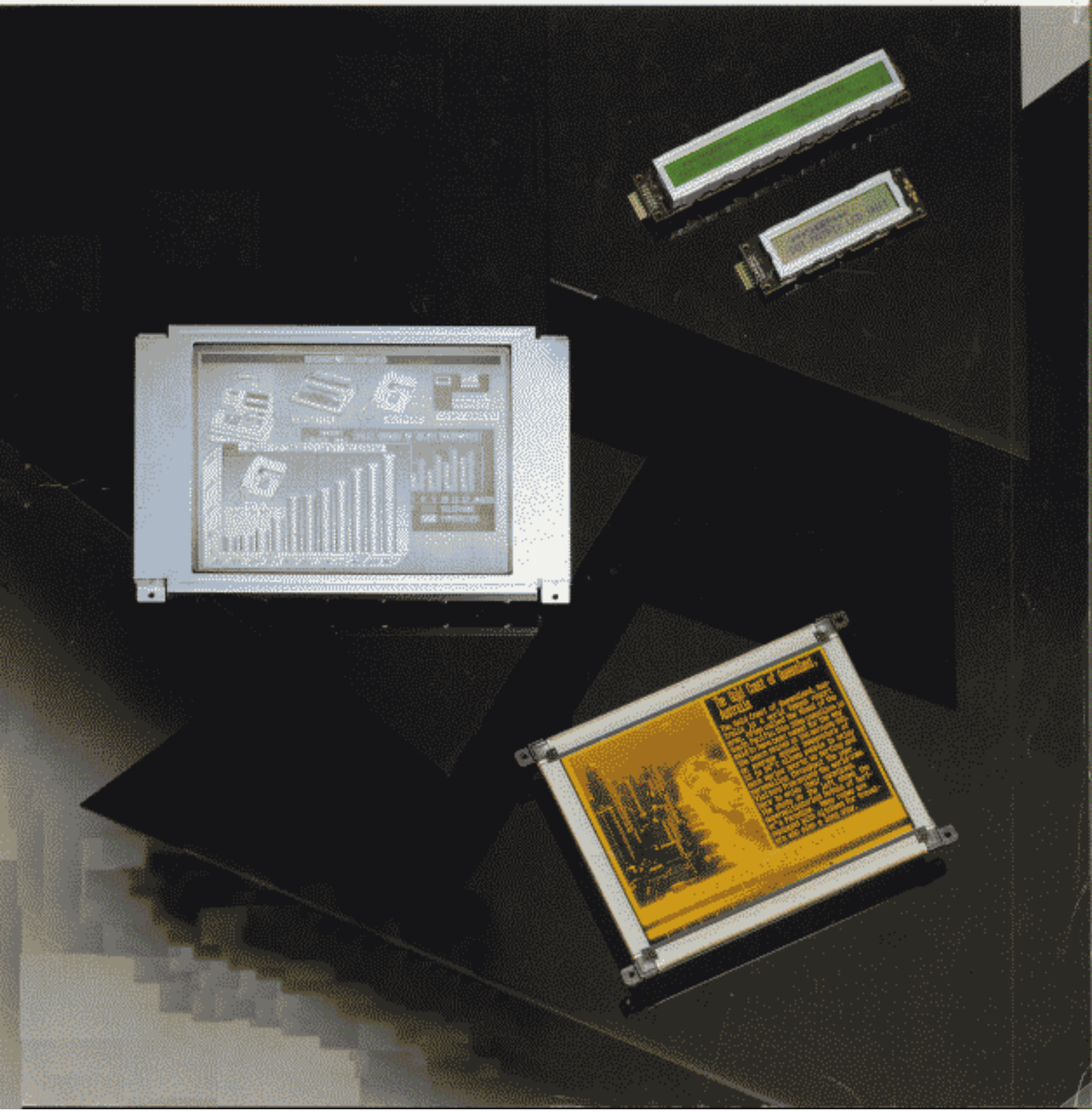
SHARP

Flat Panel Displays

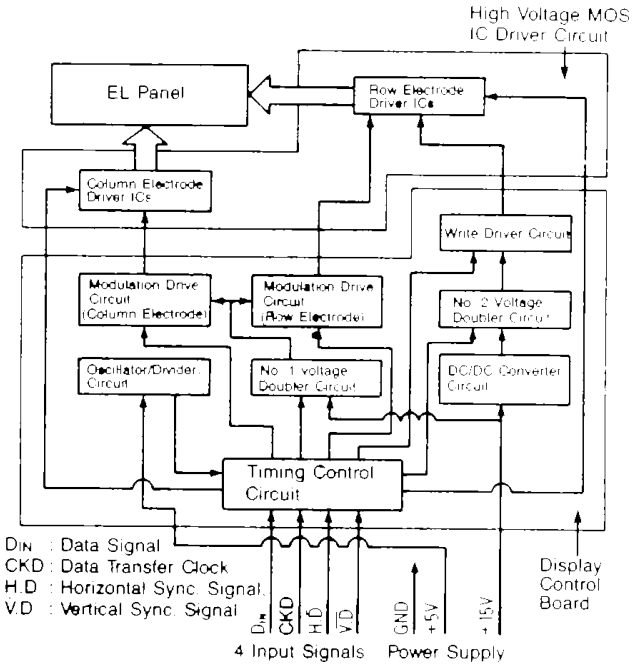
LCD Units/EL Display Units



■ Block Diagram

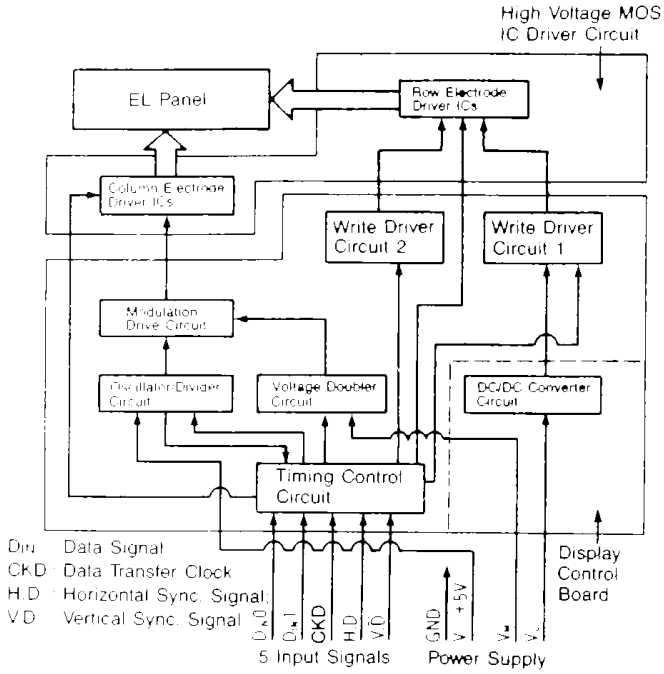
EL display units block diagram I

LJ320U21, LJ320U26, LJ512U21, LJ640U23, LJ640U24, LJ640U30



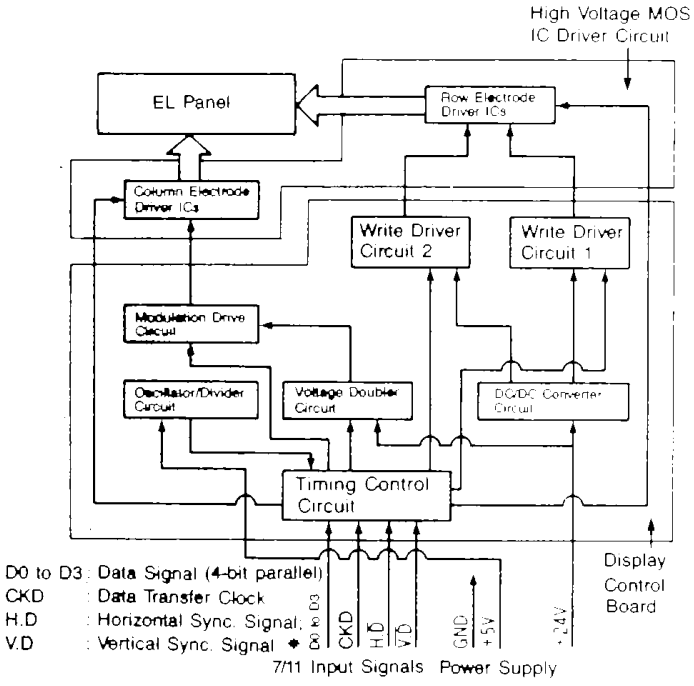
EL display units block diagram II

LJ640U48, LJ512U32*, LJ640U32, LJ640U25*, LJ024U33*



EL display units block diagram III

LJ64ZU31, LJ64ZU49



*Data Signal for LJ64ZU49: D0 to D7 (8-bit parallel)
*LJ64ZU31 is 7-input signal type; LJ64ZU49 is 11-input signal type.

1 *Models with a detachable DC/DC converter (marked with broken lines).
The maximum length of the flexible cable between the unit and the converter is 5 to 6 cm. (Refer to the specifications for details.)

2 *Model with a separated DC/DC converter (marked with broken lines).
V_M: Two types of EL display units are available, of which one type requires V_M while the other uses V_D in place of V_M (not requiring V_M).
Depending on the type of EL display unit, the values of V_D and V_M are +12V or +24V.
(Refer to the specifications for details.)

Since data signal input differs by each model, please refer to each specifications.

- Power supplies --- V_L : For logic circuit
  V_D : For panel drive
  V_M : For modulation drive circuit

■ Explanation of the Interface Signal

Signal Name	Input/Output	External Connection	Function
CKD or XSCL*1	Input	Controller	Data transfer clock This signal controls sampling and transfer of data signal.
D_{IN}*2	Input	Controller	Data signal This signal is sampled at the rising edge of each data transfer clock pulse. Data is shifted in from right to left.
UD0 to 7*1 LD0 to 7	Input	Controller	Data signal 8 bits from UD0 to UD7 are data for the upper part of the display panel and 8 bits from LD0 to LD7 are data for the lower part of the display panel. Sampled at the falling edge of the data transfer clock, this data is transferred in sequence row from right to left as 8-bit data. The data is displayed when the logic is "H" and is blanked when the logic is "L".
LP*1	Input	Controller	Latch pulse This signal controls the timing of line-at-a-time scanning and the latch timing of the data side shift register. When the logic is "H", the output of the latch circuit is directly sent to the output buffer. When the logic is "L", the preceding data is latched.
H.D	Input	Controller	Horizontal sync. signal This signal controls the timing of line-at-a-time scanning. The display data remain in effect while the logic is "H" and blanked when the logic is "L".
V.D or D_{IN}*1	Input	Controller	Vertical sync. signal This signal controls frame frequency. Frame starts when the logic rises to "H" from "L".
V_D V_L	Input	Power Supply	Power supply

*1 LJ024U33

*2 In case of 5-input type: $D_{IN}0$, $D_{IN}1$
7-input type: D0 to D3
11-input type: D00 to D03, D10 to D13

LJ320U21

Features

- **Display format:** 320 (W) × 240 (H) dots
- **Dot pitch ratio:** 1:1
- **Input signal level:** LS TTL level
- **Drive method:** P-N symmetric drive
- **Structure:** Al frame
- **Net weight:** Approx. 600g

■ Absolute maximum ratings

(Ta=25°C)

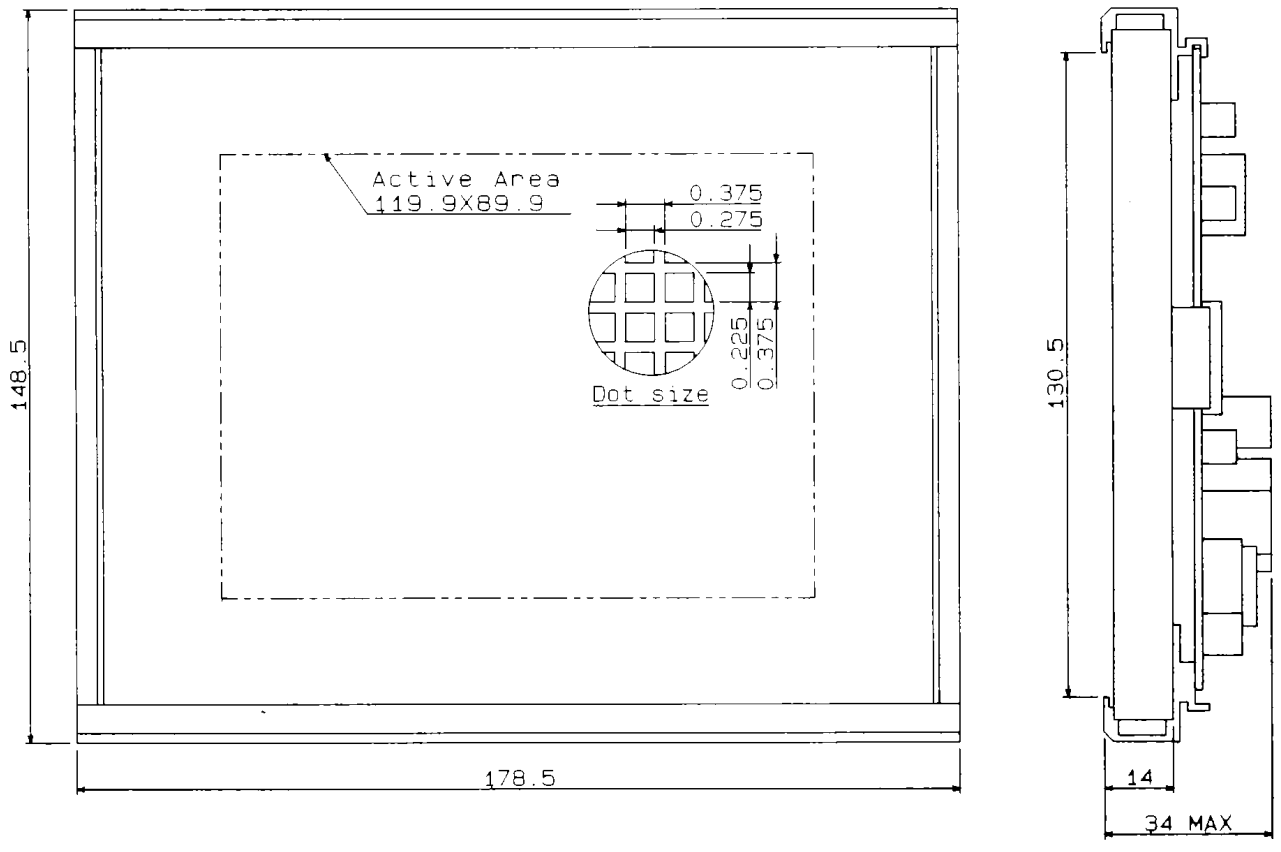
Parameter	Symbol	Rating	Unit
Interface signal (Logic "H")	V_{IH}	5.5	V
Interface signal (Logic "L")	V_{IL}	−0.5	V
Supply voltage (Logic)	V_L	7	V
Supply voltage (Panel drive)	V_D	18	V
Operating temperature	Topr	0 to +55	°C
Storage temperature	Tstg	−25 to +70	°C

■ Corresponding connector:

HIF3BA-16D-2.54R (HIROSE) or equivalents

Outline Dimensions

(Unit:mm)



Connector
HIF3F-16PA-2.54DS (HIROSE ELECTRIC) or equivalents.

Electro-optical Characteristics

(Ta=25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	V_L	—	4.75	5.0	5.25	V
Supply corrent (Logic)	I_L	V_L=5V	100	—	450	mA
Supply voltage (Panel drive)	V_D	—	14.25	15.0	15.75	V
Supply current (Panel drive)	I_D	V_D=15V	50	—	550	mA
Power consumption	P_T	V_L=5V, V_D=15V	—	8	—	W
Luminance	B_{ON}	All dots lit	20	—	—	fL
Off luminance	B_{OFF}	All dots turned off	—	—	1.0	fL
Luminance distribution	ΔB_{DIS}	All dots lit	—	—	35	%

Interface Signals

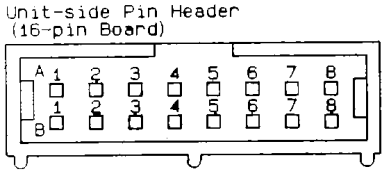
Pin No.	Symbol	Description
A-1	D_{IN}	Data signal
B-1	GND	Ground
A-2	CKD	Data transfer clock
B-2	GND	Ground
A-3	H.D	Horizontal sync. signal
B-3	GND	Ground
A-4	V.D	Vertical sync. signal
B-4	GND	Ground
A-5	GND	Ground
B-5	GND	Ground
A-6	GND	Ground
B-6	GND	Ground
A-7	V_L	+5V
B-7	V_L	+5V
A-8	V_D	+15V
B-8	V_D	+15V

Interface Timing Ratings

(Ta=25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Clock frequency	$1/T_{CL}$	4.4	—	7.5	MHz
Clock duty	$T_{CL}(H)/T_{CL}\times 100$	45	—	55	%
Horizontal sync. signal cycle time	T_H	62	—	75	μsec
Horizontal sync. signal blanking time	t_{HB}	2	—	—	μsec
Vertical sync. signal blanking time	t_{VB}	1	—	$N\times T_H$	μsec
Vertical sync. signal valid time	t_{VA}	$240\times T_H$	—	—	μsec
Frame frequency	$1/T_V$	50	60	63	Hz
Data signal delay time required	t_{DD}	0.01	—	T_{CL}	μsec
Horizontal sync. signal delay time required	t_{HD}	0.01	—	$T_{CL}/2$	μsec
Vertical sync. signal rise wait time	t_{VR}	4×62	—	—	μsec
Vertical sync. rise timing	t_{VH}	62	—	$T_H-t_{HB}+50$	μsec

Connector



Interface Timing Chart