

7-Bit 0.25dB Wideband Digital Step Attenuator

1 to 6000 MHz

DESCRIPTION

This document describes the specification for the F1956 Digital Step Attenuator. The F1956 is part of Renesas' *Glitch-Free™* family of DSAs optimized for the demanding requirements of Base Station (BTS) radio cards and numerous other non-BTS applications. This device is offered in compact 5×5 mm 32-pin package with 50Ω input and output impedance for ease of integration into the radio or RF system.

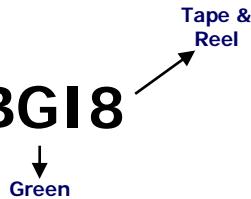
COMPETITIVE ADVANTAGE

The F1956 offers very high reliability due to its construction from a monolithic silicon die in a QFN package. The insertion loss is very low with minimal distortion. Additionally, the device is designed to have extremely accurate attenuations levels. These accurate attenuation level improves system SNR and/or ACLR by ensuring system gain is as close to targeted level as possible. Also, the very fast settling time in parallel mode is ideal for fast switching systems. Finally, the device is *Glitch-Free™* with less than 2dB of ringing across the attenuation range in stark contrast to competing DSAs that glitch as much as 10dB during MSB state changes.

- ✓ Lowest insertion loss for best SNR
- ✓ *Glitch-Free™* technology to protect PA or ADC during transitions between attenuation states.
- ✓ Extremely accurate attenuation levels
- ✓ Ultra-low distortion
- ✓ MSL1 and 2000V HBM ESD

ORDERING INFORMATION

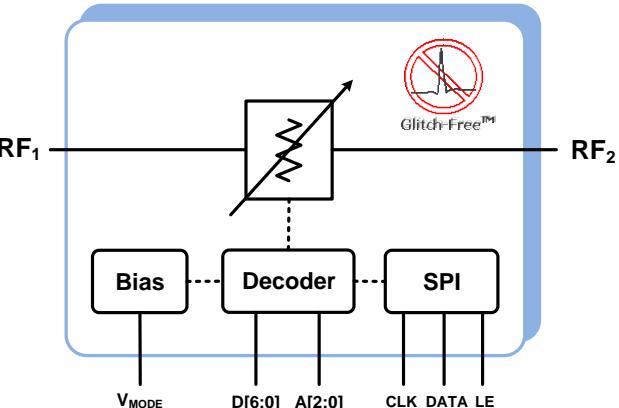
F1956NBG18



FEATURES

- Serial and 7-bit Parallel Interface
- 31.75dB Range
- 0.25dB steps
- *Glitch-Free™*: low transient overshoot
- 500ns settling time
- Ultra linear $> 64\text{dBm}$ IIP3
- Low Insertion Loss $< 1.7\text{dB}$ at 4GHz
- Attenuation error $< \pm 0.2\text{dB}$ at 4GHz
- Bi-directional RF use
- 3.3V or 5V Supply
- 1.8V or 3.3V control logic
- Low Current Consumption: $350\mu\text{A}$ typical
- -40°C to $+105^\circ\text{C}$ operating temperature
- 5×5 mm thin [32-QFN](#) package

FUNCTIONAL BLOCK DIAGRAM



Part# Details

| Part# | Freq Range (MHz) | Resolution / Range (dB) | Control | IL (dB) | Pinout |
|-------|------------------|-------------------------|-------------------|---------|----------------------------------|
| F1950 | 150 - 4000 | 0.25 / 31.75 | Parallel & Serial | 1.3 | PE43702 PE43701 |
| F1951 | 100 - 4000 | 0.50 / 31.5 | Serial Only | 1.2 | HMC305 |
| F1952 | 100 - 4000 | 0.50 / 15.5 | Serial Only | 0.9 | HMC305 |
| F1953 | 400 - 4000 | 0.50 / 31.5 | Parallel & Serial | 1.3 | PE4302 DAT-31R5 |
| F1956 | 1 - 6000 | 0.25 / 31.75 | Parallel & Serial | 1.4 | PE43705, PE43712, RFS43715 |
| F1912 | 1 - 4000 | 0.50 / 31.5 | Parallel & Serial | 1.6 | PE4312 PE4302 |

ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Min | Max | Units |
|--|-------------------|------|-----------------------------|-------|
| VDD to GND | V_{DD} | -0.3 | +5.5 | V |
| D[6:0], DATA, CLK, LE, A0, A1, A2, V _{MODE} | V _{CNTL} | -0.3 | Min ($V_{DD} + 0.3$, 3.9) | V |
| RF1, RF2 | V_{RF} | -0.3 | +0.3 | V |
| Maximum Input Power applied to RF1 or RF2 (>100 MHz) | P_{RF} | | +34 | dBm |
| Operating Case Temperature | | | 105 | °C |
| Continuous Power Dissipation | | | 1.5 | W |
| Maximum Junction Temperature | $T_{J\max}$ | | +150 | °C |
| Storage Temperature Range | T_{ST} | -65 | +150 | °C |
| Lead Temperature (soldering, 10s) | T_{LEAD} | | +260 | °C |
| Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2012) | V_{ESDHBM} | | 1500 (Class 1C) | V |
| ESD Voltage – CDM (Per JESD22-C101F) | V_{ESDCDM} | | 500 (Class C2) | V |

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

This product features proprietary protection circuitry. However, it may be damaged if subjected to high energy ESD. Please use proper ESD precautions when handling to avoid damage or loss of performance.

PACKAGE THERMAL AND MOISTURE CHARACTERISTICS

| | |
|---|--------|
| θ_{JA} (Junction – Ambient) | 40°C/W |
| θ_{JC} (Junction – Case) [The Case is defined as the exposed paddle] | 4°C/W |
| Moisture Sensitivity Rating (Per J-STD-020) | MSL1 |

F1956 RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|-----------------------------|-------------------|--|------|-----|--------------|-------|
| Supply Voltage(s) | V _{DD} | | 3.00 | | 5.25 | V |
| Operating Temperature Range | T _{CASE} | Case Temperature | -40 | | +105 | °C |
| Frequency Range | F _{RF} | | 1 | | 6000 | MHz |
| RF CW Input Power | P _{CW} | RF1 or RF2 | | | See Figure 1 | dBm |
| RF Peak Input Power | P _{peak} | RF1 Port, V _{DD} = 3.3V, T _{CASE} = 85°C, F _{RF} > 500MHz, WCDMA, 3GPP, Downlink, 64 DPCCH, Chip rate = 3.84MSPS, Avg. Pin = +22dBm | | | | |
| | | 1% | | | 28.9 | dBm |
| | | 0.1% | | | 30.7 | |
| | | 0.01% | | | 32.3 | |
| | | 0.001% | | | 33.2 | |
| RF Source Impedance | Z _{RF1} | Single-Ended | | 50 | | Ω |
| RF Load Impedance | Z _{RF0} | Single-Ended | | 50 | | Ω |

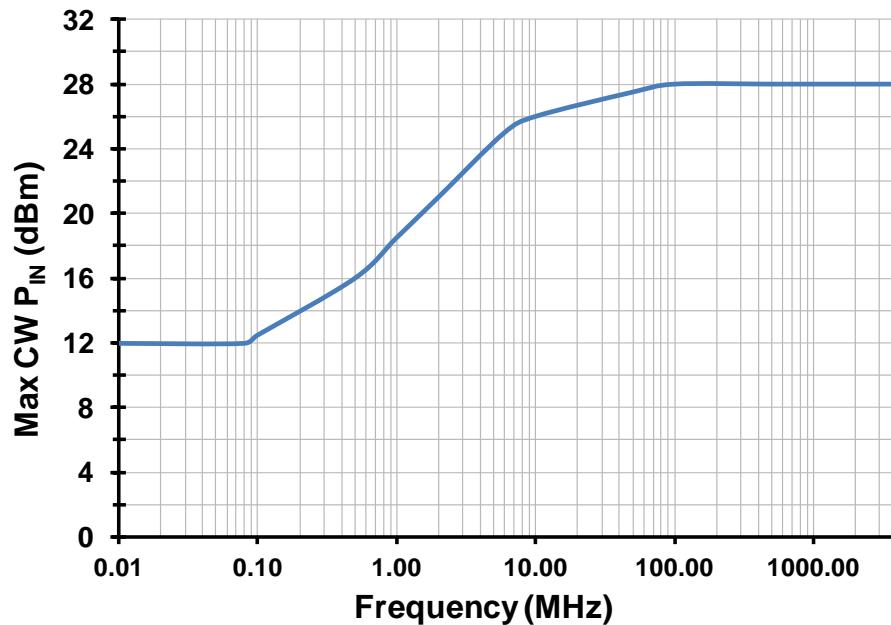


Figure 1. Maximum Operating RF input power vs Input Frequency

F1956 SPECIFICATION

Specifications apply at $V_{DD} = +3.3V$, $T_{CASE} = +25^{\circ}\text{C}$, $F_{RF} = 2\text{GHz}$, 0.25dB steps unless otherwise noted. Minimum Attenuation D[6:0] = [0000000], Maximum Attenuation D[6:0] = [1111111], EVKit losses are de-embedded unless otherwise noted.

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|--|------------------|--|-------------------|-------|----------|------------------|
| Logic Input High | V_{IH} | CLK, LE, DATA, D[6:0], A0, A1, A2, V_{MODE} | | | | |
| | | $3.0V \leq V_{DD} \leq 3.6V$ | 1.17 ² | | V_{DD} | V |
| | | $3.6V < V_{DD}$ | 1.17 ¹ | | 3.6 | |
| Logic Input Low | V_{IL} | CLK, LE, DATA, D[6:0], A0, A1, A2, V_{MODE} | | | 0.63 | V |
| Logic Current | I_{IH}, I_{IL} | Individual Pins | -95 | | +95 | μA |
| Supply Current | I_{DD} | | | 350 | 800 | μA |
| Attenuation Range | ATT_{RNG} | No missing codes | | 31.75 | | dB |
| Minimum Gain Step | LSB | $F_{RF} \leq 4.5\text{GHz}$ | | 0.25 | | dB |
| | | $F_{RF} \leq 6.5\text{GHz}$ | | 0.50 | | |
| | | $F_{RF} \leq 8.5\text{GHz}$ | | 1.00 | | |
| DSA Settling time | τ_{SET} | Max to Min Attenuation to settle to within 0.5dB of final value | | 0.9 | | μs |
| | | Min to Max Attenuation to settle to within 0.5dB of final value | | 1.8 | | |
| Video Feedthrough RF1, RF2 ports | VID_{FT} | Measured at RF ports with 2.5ns rise time, 0 to 3.3V control pulse | | 10 | | mV_{pp} |
| Maximum spurious level on any RF port ⁴ | $Spur_{MAX}$ | Spur Freq ~ 2.2MHz | | -140 | | dBm |
| Serial Clock Speed | F_{CLK} | SPI 3 wire bus | | | 25 | MHz |
| Parallel to Serial Setup | A | SPI 3 wire bus | 100 | | | ns |
| Serial Data Hold Time | B | SPI 3 wire bus | 10 | | | ns |
| LE Delay | C | SPI 3 wire bus Time from final serial clock rising edge | 10 | | | ns |
| Maximum Switching Rate | SW_{RATE} | | | 25 | | kHz |

Specification Notes:

- Note 1: Items in min/max columns in ***bold italics*** are guaranteed by Test.
- Note 2: Items in min/max columns that are not bold/italics are guaranteed by Design Characterization.
- Note 3: The input 0.1dB compression point is used as a linearity figure of merit. The recommended maximum input power is specified as the lesser of the two values from RF CW Power (Figure 1) and the RF Average Power (Recommended Operating Conditions Table).
- Note 4: Spurious due to on-chip negative voltage generator. Typical generator fundamental frequency is 2.2MHz.

F1956 SPECIFICATION (CONTINUED)

Specifications apply at $V_{DD} = +3.3V$, $T_{CASE} = +25^\circ C$, $F_{RF} = 2GHz$, 0.25dB steps unless otherwise noted. Minimum Attenuation D[6:0] = [0000000], Maximum Attenuation D[6:0] = [1111111], EVKit losses are de-embedded unless otherwise noted.

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|--|--------------------|--|-------------|------|-------------|-------|
| Insertion Loss | IL | 1MHz < $F_{RF} \leq 2GHz$ | | 1.3 | 1.8 | dB |
| | | 2GHz < $F_{RF} \leq 3GHz$ | | 1.3 | 1.9 | |
| | | 3GHz < $F_{RF} \leq 4GHz$ | | 1.6 | 2.2 | |
| | | 4GHz < $F_{RF} \leq 5GHz$ | | 2.1 | 2.6 | |
| | | 5GHz < $F_{RF} \leq 6GHz$ | | 2.6 | 3.0 | |
| Relative Phase (Amin vs. Amax) | $\Phi\Delta$ | $F_{RF} = 1GHz$ | | 12 | | deg |
| | | $F_{RF} = 2GHz$ | | 25 | | |
| | | $F_{RF} = 4GHz$ | | 55 | | |
| | | $F_{RF} = 6GHz$ | | 90 | | |
| Step Error (Differential Non-Linearity) | DNL | Max error between adjacent steps | | 0.10 | 0.19 | dB |
| Absolute Attenuation Error (Integral Non-Linearity) | INL | Max Error for state 19.75dB, $F_{RF} = 2GHz$ | -0.4 | 0.1 | +0.5 | dB |
| | | Max Error, over all states $F_{RF} = 2GHz$ | -0.8 | | +0.5 | |
| Input Return Loss | S ₁₁ | 1MHz < $F_{RF} \leq 2GHz$ | | 20 | 15 | dB |
| | | 2GHz < $F_{RF} \leq 4GHz$ | | 20 | 15 | |
| | | 4GHz < $F_{RF} \leq 6GHz$ | | 14 | 7 | |
| Output Return Loss | S ₂₂ | 1MHz < $F_{RF} \leq 2GHz$ | | 18 | 14 | dB |
| | | 2GHz < $F_{RF} \leq 4GHz$ | | 16 | 12 | |
| | | 4GHz < $F_{RF} \leq 6GHz$ | | 11 | 7 | |
| Input IP3 | IIP3 | P _{IN} = +10dBm per tone 50MHz Tone Separation | | | | |
| | | Attn = 0.00dB | | 64 | | dBm |
| | | Attn = 15.75dB | | 64 | | |
| | | Attn = 31.75dB | | 64 | | |
| | | Attn = 0.00dB P _{IN} = +22dBm per tone 1MHz Tone Separation | | | | |
| | | $F_{RF} = 0.7GHz$ | 60 | 63.4 | | dBm |
| | | $F_{RF} = 1.8GHz$ | 60 | 63.4 | | |
| | | $F_{RF} = 2.2GHz$ | 60 | 64.1 | | |
| | | $F_{RF} = 2.6GHz$ | 60 | 63.3 | | |
| Input 0.1dB Compression ³ | P _{0.1dB} | $F_{RF} = 2GHz$, Attn = 10dB | | 34.5 | | dBm |

Specification Notes:

- Note 1: Items in min/max columns in ***bold italics*** are guaranteed by Test.
- Note 2: Items in min/max columns that are not bold/italics are guaranteed by Design Characterization.
- Note 3: The input 0.1dB compression point is used as a linearity figure of merit. The recommended maximum input power is specified as the lesser of the two values from RF CW Power (Figure 1) and the RF Average Power (Recommended Operating Conditions Table).
- Note 4: Spurious due to on-chip negative voltage generator. Typical generator fundamental frequency is 2.2MHz.

PROGRAMMING OPTIONS

F1956 can be programmed using either the parallel or serial interface; selectable via V_{MODE} (pin 3). Serial mode is selected by floating V_{MODE} or pulling V_{MODE} to a logic high and parallel mode is selected by setting V_{MODE} to logic low.

SERIAL CONTROL MODE

F1956 Serial mode is selected by floating V_{MODE} (pin 3) or pulling it to logic high. The serial interface is a 16-bit shift register made up of two words. The first 8-bit word is the Attenuation word, which controls the DSA state. The second word is the address word, which uses only 3 of 8-bits that must match the hard wired A0-A2 programming in order to change the DSA state. If no external connections are made to A0 – A2 then internally they will default to 000 due to internal pull down resistors. If these 3 external preset address bits are not matched with the SPI loaded address bits then the current attenuator state will remain unchanged. This allows up to 8 serial-controlled devices to be used on a single board, which share a common DATA, CLK and LE.

When serial programming is used, all the parallel control input pins 26 – 32 can be left open or grounded. If a pin is grounded then an additional 25 μ A will be drawn from the voltage supply per pin.

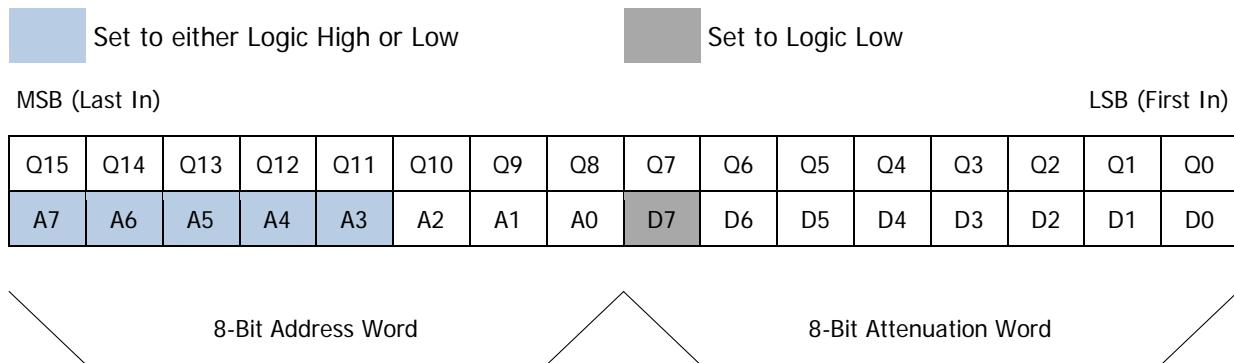


Figure 2. Two 8-bit words are comprised of 16bit serial in, parallel out shift register

Table 1. Truth Table for the Serial Address Word

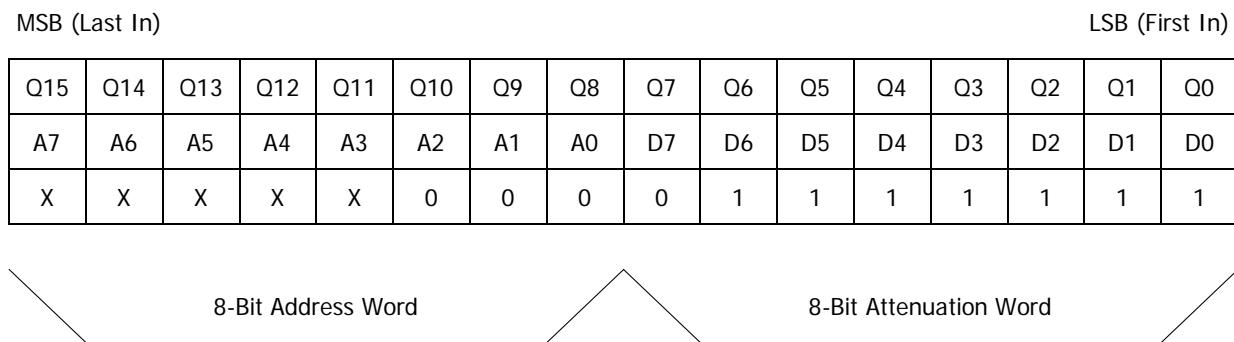
| A7 (MSB) | A6 | A5 | A4 | A3 | A2 | A1 | A0 | Address Setting |
|-------------|----|----|----|----|----|----|----|--------------------|
| X | X | X | X | X | 0 | 0 | 0 | 000 |
| X | X | X | X | X | 0 | 0 | 1 | 001 |
| X | X | X | X | X | 0 | 1 | 0 | 010 |
| X | X | X | X | X | 0 | 1 | 1 | 011 |
| X | X | X | X | X | 1 | 0 | 0 | 100 |
| X | X | X | X | X | 1 | 0 | 1 | 101 |
| X | X | X | X | X | 1 | 1 | 0 | 110 |
| X | X | X | X | X | 1 | 1 | 1 | 111 |

Table 2. Truth Table for the Serial Control Word

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 (LSB) | Attenuation (dB) |
|----|----|----|----|----|----|----|-------------|---------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0.25 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0.5 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 2 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 4 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 8 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 16 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 31.75 |

SERIAL MODE DEFAULT CONDITION

When the device is first powered up it will default to the **Maximum Attenuation** setting as described below: Note that for the F1956 in all cases logic high (1) has the attenuation stepped IN, while logic low (0) has the attenuation stepped OUT.

**Figure 3. Default register settings set for max attenuation and 000 Address Word****REGISTER TIMING DIAGRAM: (NOTE THE TIMING SPEC INTERVALS IN BLUE)**

With serial control, the F1956 can be programmed via the serial port on the rising edge of Latch Enable (LE) which loads the last 8 DATA line bits [formatted LSB (D0) first] resident in the SHIFT register followed by the Address Word into the ACTIVE register.

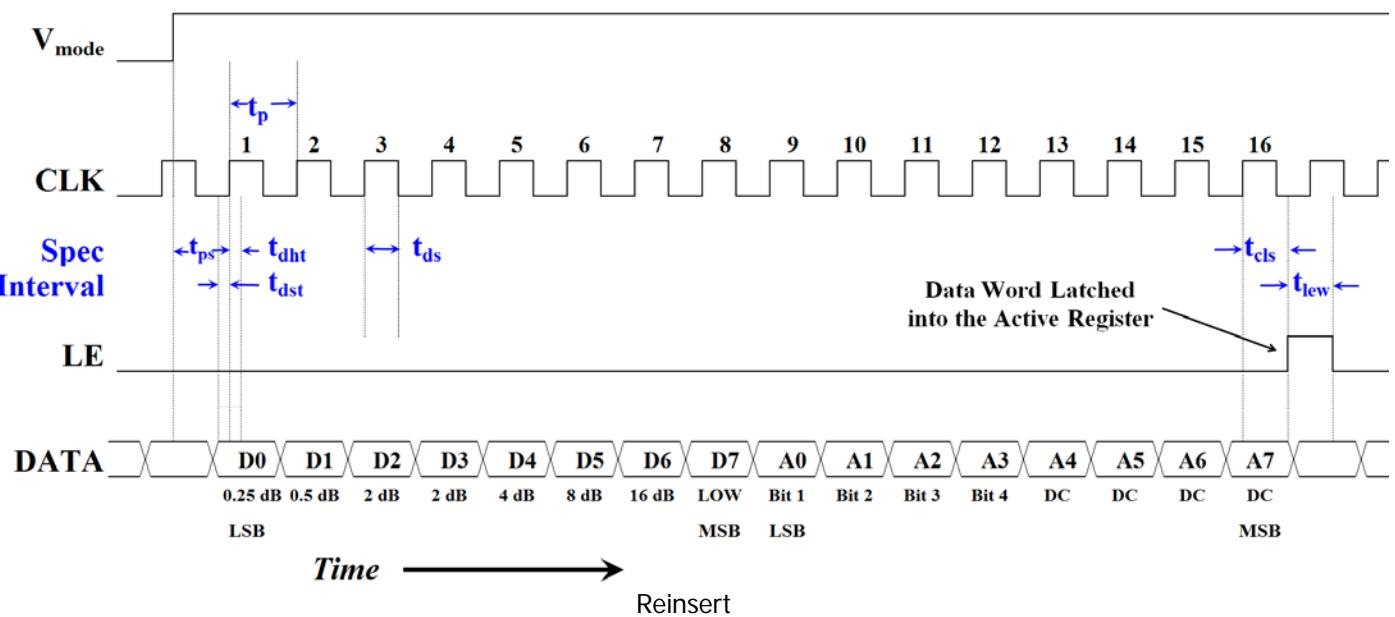


Figure 4. Serial Timing Diagram

Note - When Latch enable is high, the shift register is disabled and DATA is NOT continuously clocked into the shift register which minimizes noise. It is recommended that Latch enable be left high when the device is not being programmed.

Table 3. Serial Mode Timing Table

| Interval Symbol | Description | Min Spec | Max Spec | Units |
|------------------|---|----------|----------|-------|
| t _{ps} | Parallel to Serial Setup Time - From rising edge of Vmode to rising edge of CLK for D5 | 100 | | ns |
| t _p | Clock high pulse width | 10 | | ns |
| t _{cls} | LE Setup Time - From the rising edge of CLK pulse for D0 to LE rising edge minus half the clock period. | 10 | | ns |
| t _{lew} | LE pulse width | 30 | | ns |
| t _{dst} | Data Setup Time - From the starting edge of Data bit to rising edge of CLK | 10 | | ns |
| t _{dht} | Data Hold Time - From rising edge of CLK to falling edge of the Data bit. | 10 | | ns |

PARALLEL CONTROL MODE

For the F1956 the user has the option of running in one of two parallel modes. Direct Parallel Mode or Latched Parallel Mode.

Direct Parallel Mode:

Direct Parallel Mode is selected when V_{MODE} is a logic low and LE is a logic high. In this mode the device will immediately react to any voltage changes to the parallel control pins [pins 26 – 32]. Use direct parallel mode for the fastest settling time.

Latched Parallel Mode:

Latched Parallel Mode is selected when V_{MODE} is logic low and LE is toggled from logic low to high. To utilize Latched Parallel Mode:

- Set V_{MODE} is logic low.
- Set LE to logic low.
- Adjust pins [26, 27, 28, 29, 30, 31, 32] to the desired attenuation setting. (Note the device will not react to these pins while LE is a logic low).
- Pull LE to a logic high. The device will then transition to the attenuation settings reflected by pins D6 - D0.
- IF LE is pulled to a logic low then the attenuator will not change state.

Latched Parallel Mode implies a default state for when the device is first powered up with V_{MODE} set for logic low and LE logic low. In this case the default setting is MAXIMUM Attenuation.

Table 4. Truth Table for the Parallel Control Word

| D6 | D5 | D4 | D3 | D2 | D1 | D0 | Attenuation (dB) |
|----|----|----|----|----|----|----|------------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0.25 |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0.5 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 2 |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 4 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 8 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 16 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 31.75 |

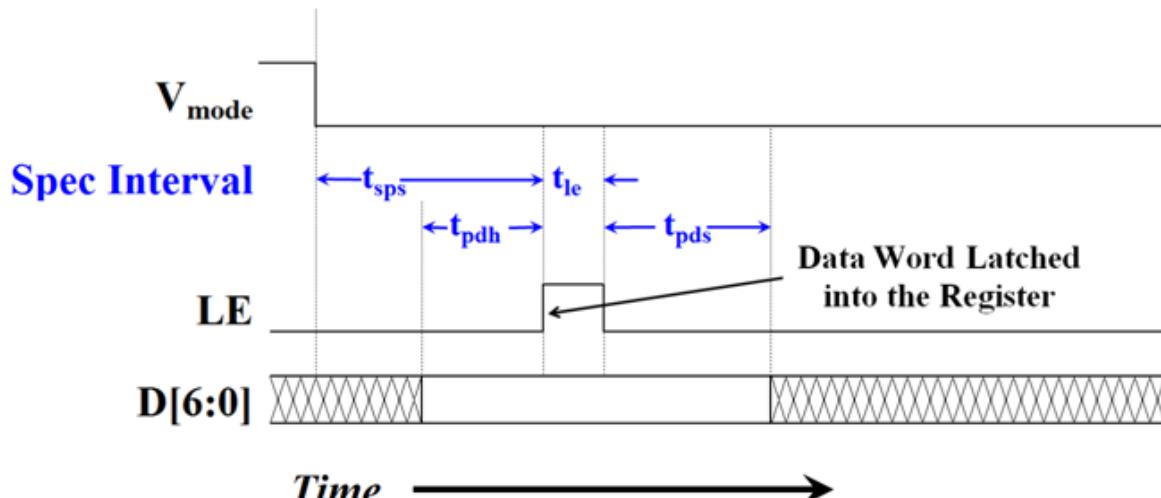


Figure 5. Latched Parallel Mode Timing Diagram

Table 5. Latched Parallel Mode Timing

| Interval Symbol | Description | Min Spec | Max Spec | Units |
|------------------------|------------------------------------|-----------------|-----------------|--------------|
| t_{sps} | Serial to Parallel Mode Setup Time | 100 | | ns |
| t_{pdh} | Parallel Data Hold Time | 10 | | ns |
| t_{le} | LE minimum pulse width | 10 | | ns |
| t_{pds} | Parallel Data Setup Time | 10 | | ns |

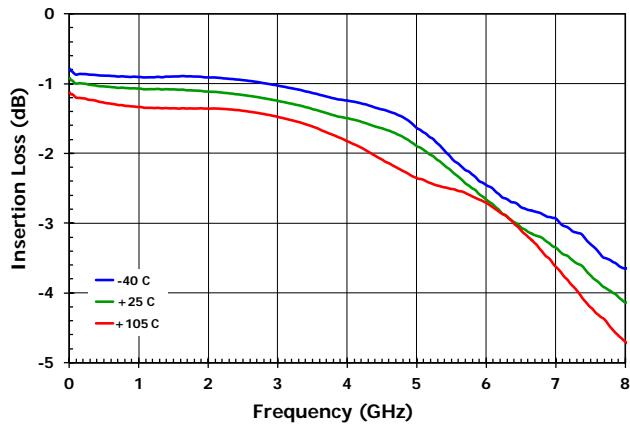
TYPICAL OPERATING CONDITIONS (TOC)

Unless otherwise noted for the TOC graphs on the following pages, the following conditions apply.

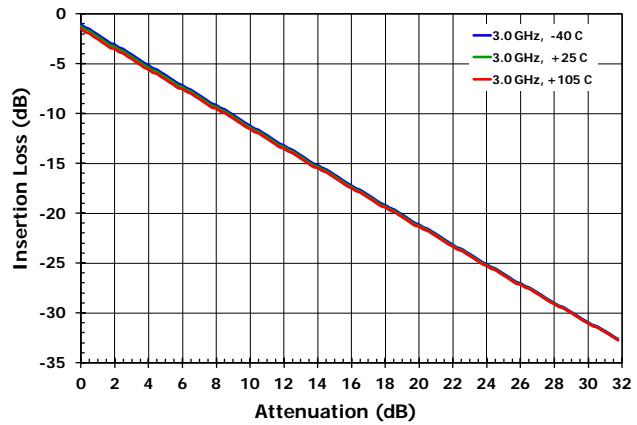
1. $V_{DD} = +3.30V$
2. $T_{CASE} = +25^{\circ}C$
3. 50 MHz Tone Space
4. Serial Control
5. $P_{IN} = 0dBm$
6. RF1 is the input port
7. Attenuation Setting = 0dB
8. EVKit losses (traces and connectors) are fully de-embedded

TYPICAL OPERATING CONDITIONS (1)

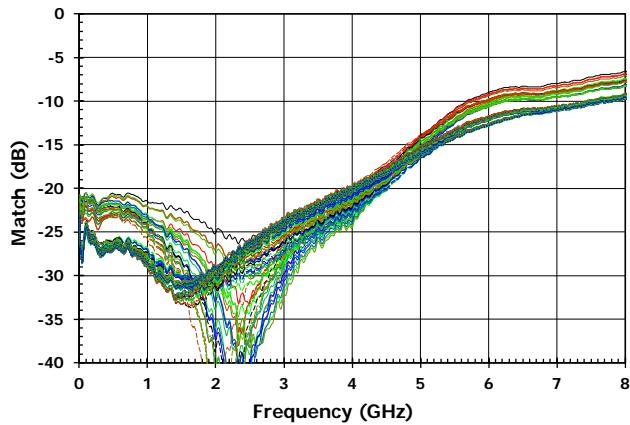
Insertion Loss vs Frequency



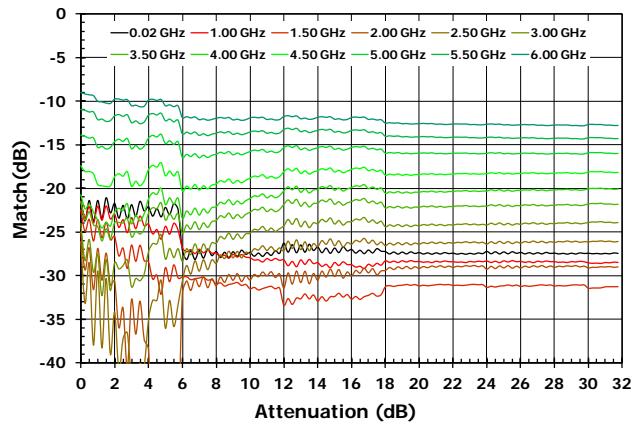
Insertion Loss vs Attenuation



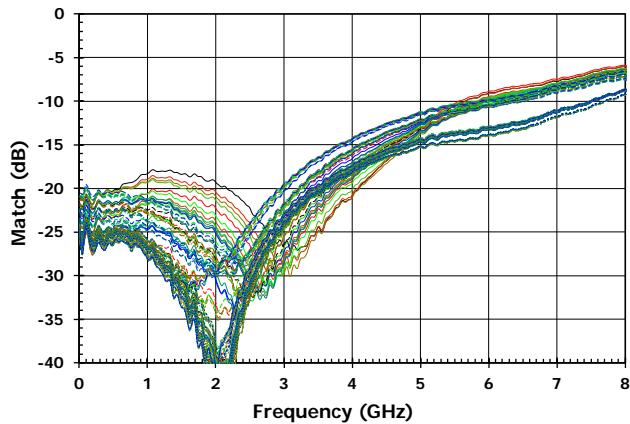
Input Return Loss vs Frequency [All States]



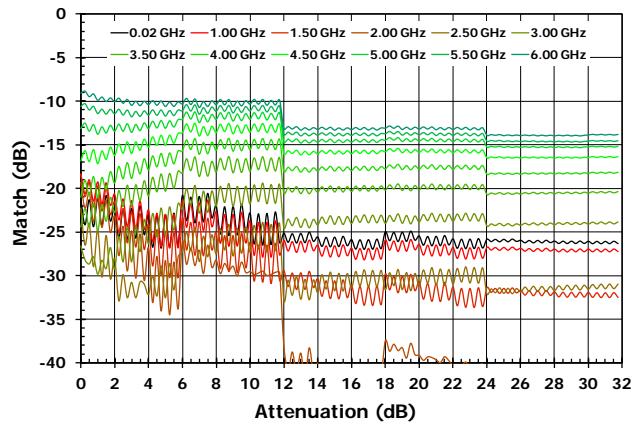
Input Return Loss vs Attenuation

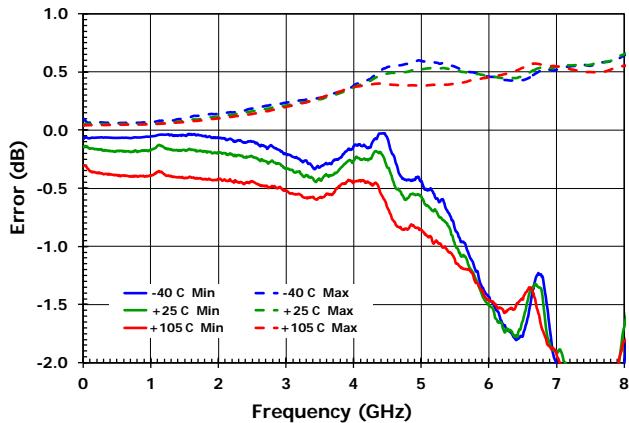
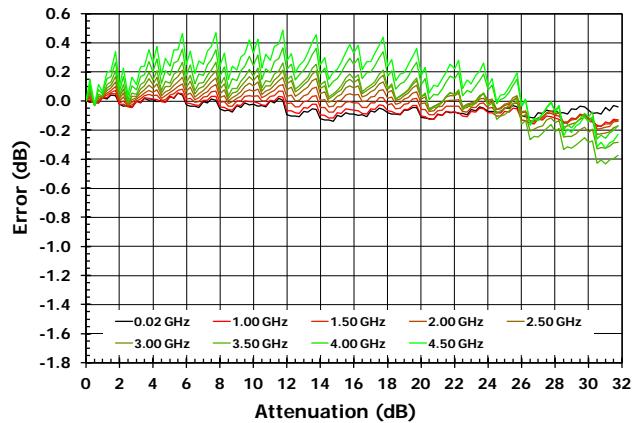
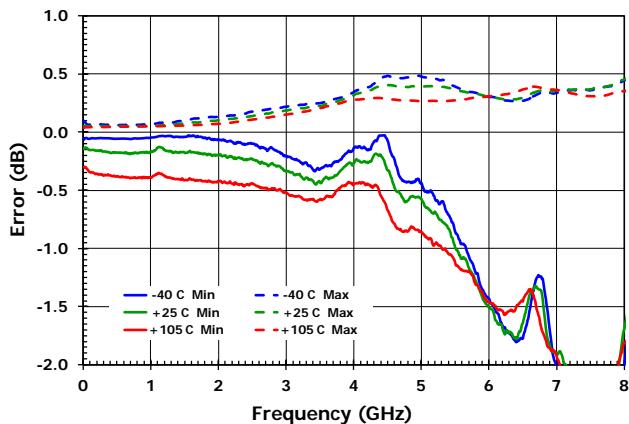
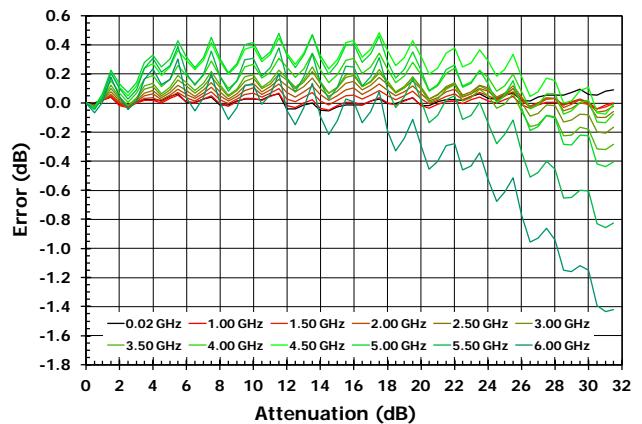
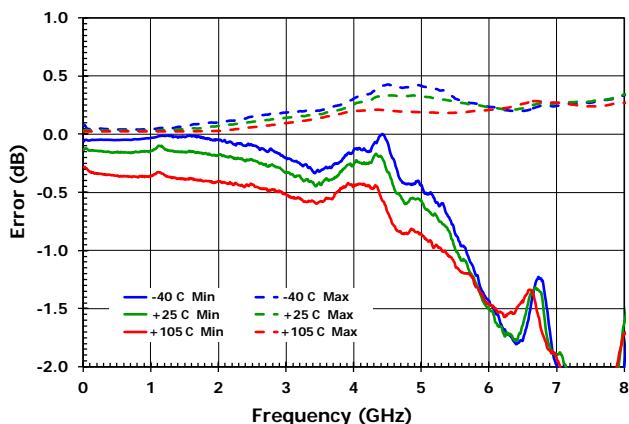
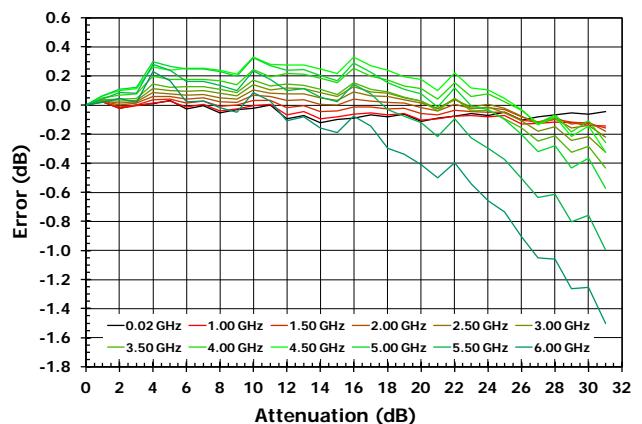


Output Return Loss vs Frequency [All States]



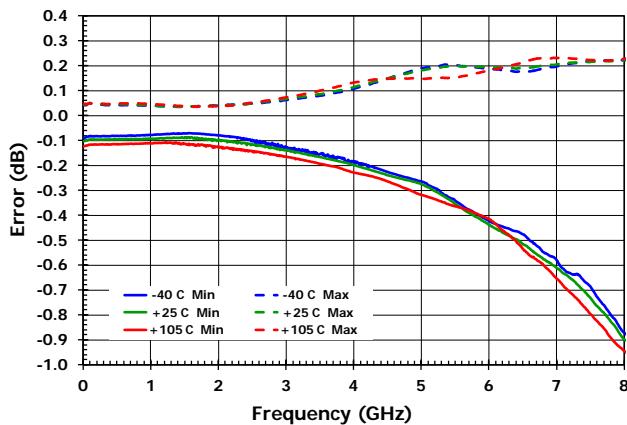
Output Return Loss vs Attenuation



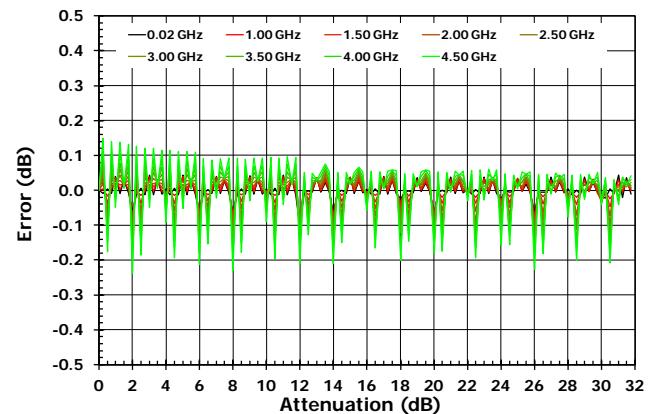
TYPICAL OPERATING CONDITIONS (2)**Worst Case Absolute Accuracy (LSB = 0.25dB)****Absolute Accuracy (LSB = 0.25dB)****Worst Case Absolute Accuracy (LSB = 0.50dB)****Absolute Accuracy (LSB = 0.50dB)****Worst Case Absolute Accuracy (LSB = 1.00dB)****Absolute Accuracy (LSB = 1.00dB)**

TYPICAL OPERATING CONDITIONS (3)

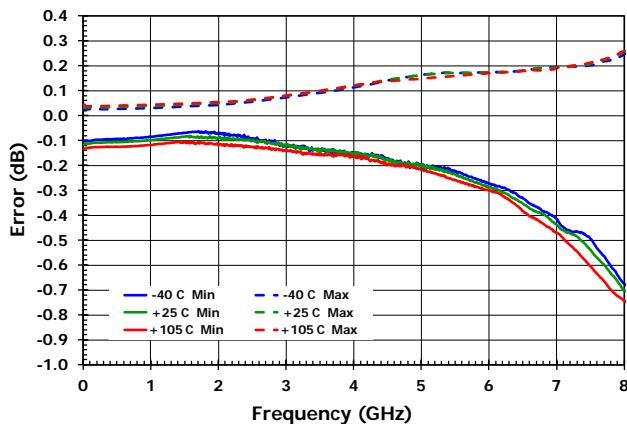
Worst Case Step Accuracy (LSB = 0.25dB)



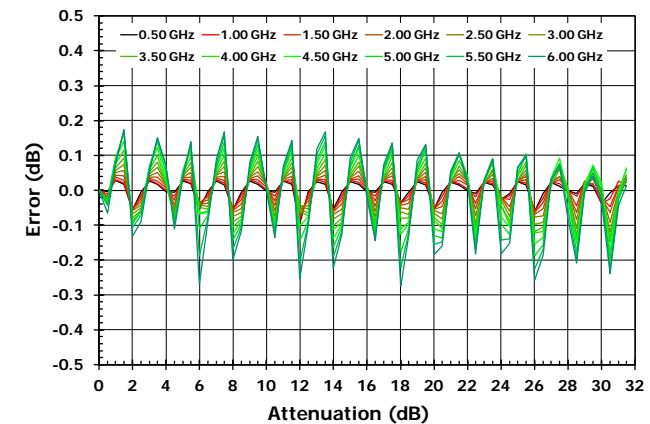
Step Accuracy (LSB = 0.25dB)



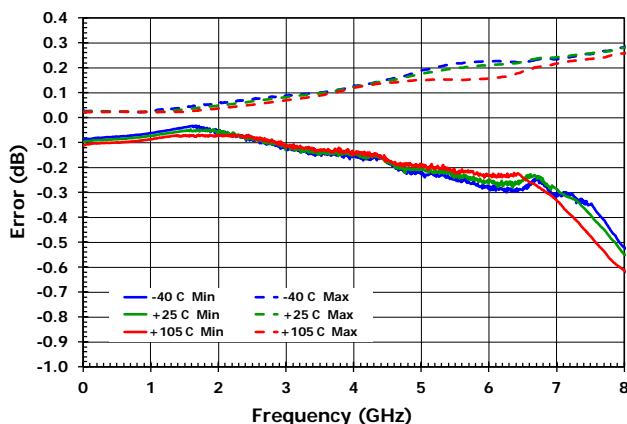
Worst Case Step Accuracy (LSB = 0.50dB)



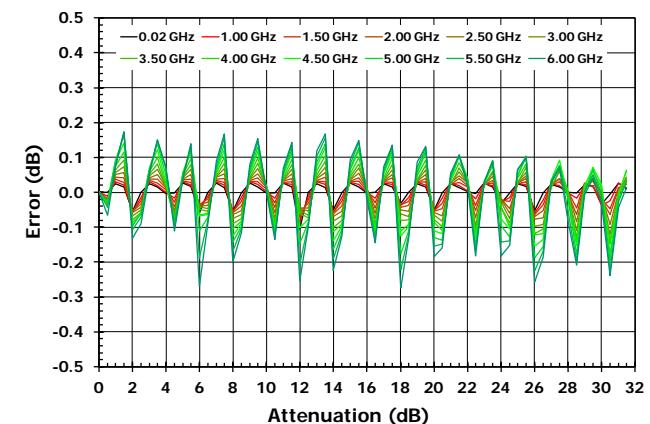
Step Accuracy (LSB = 0.50dB)



Worst Case Step Accuracy (LSB = 1.00dB)

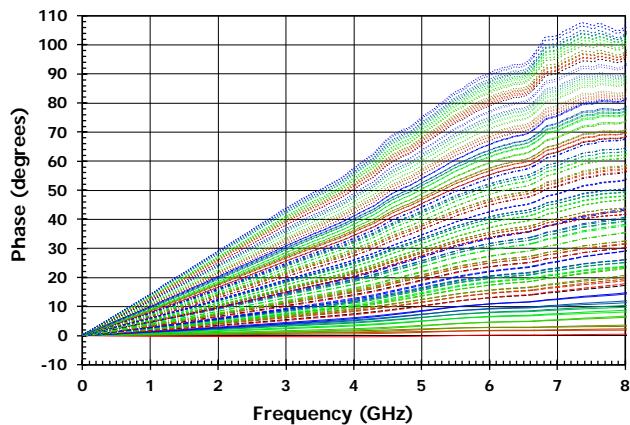


Step Accuracy (LSB = 1.00dB)

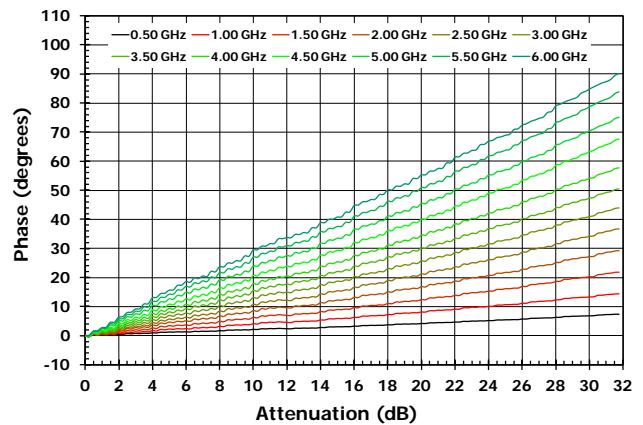


TYPICAL OPERATING CONDITIONS (4)

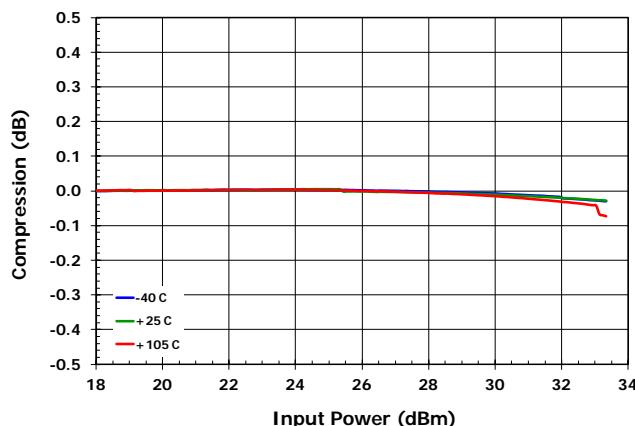
Relative Insertion Phase vs Frequency [All States]



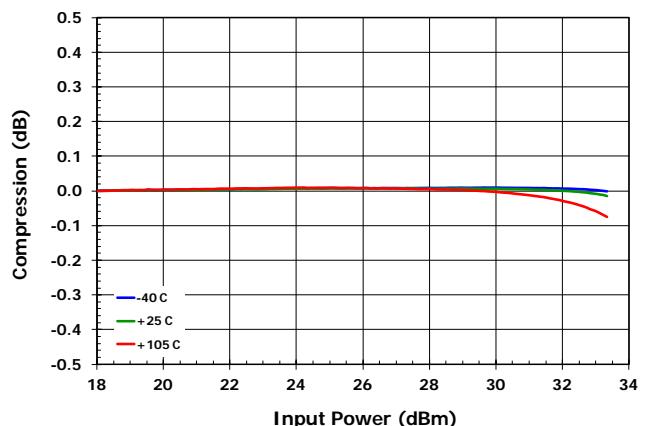
Relative Insertion Phase vs Attenuation



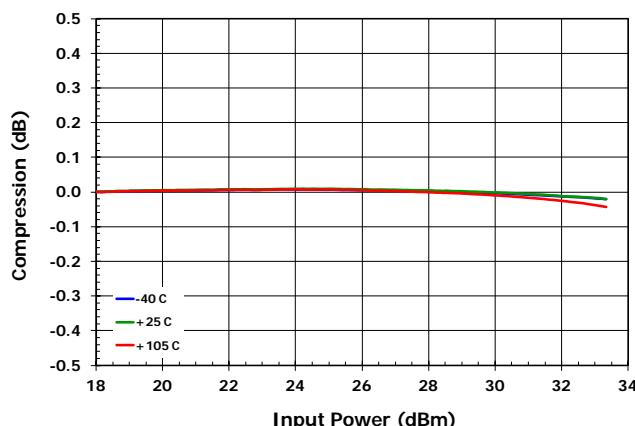
Input Compression (at 2GHz, Attn = 0dB)



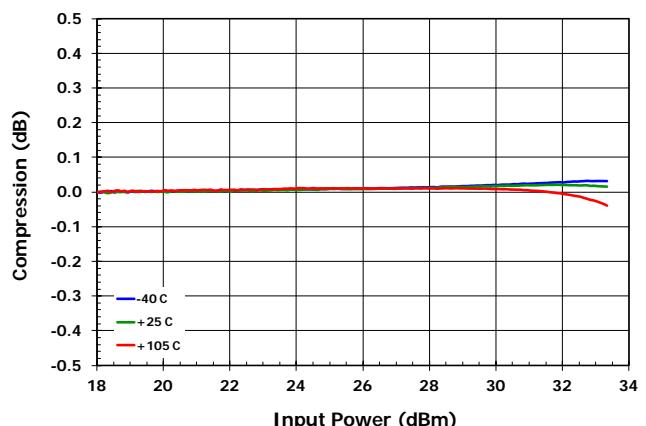
Input Compression (at 2GHz, Attn = 16dB)



Input Compression (at 2GHz, Attn = 4dB)

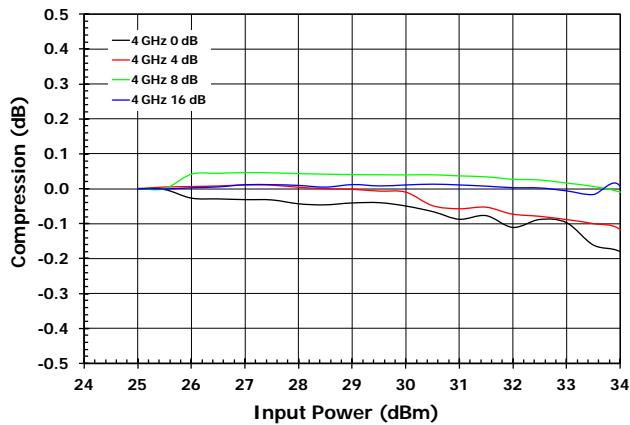


Input Compression (at 2GHz, Attn = 31.75dB)

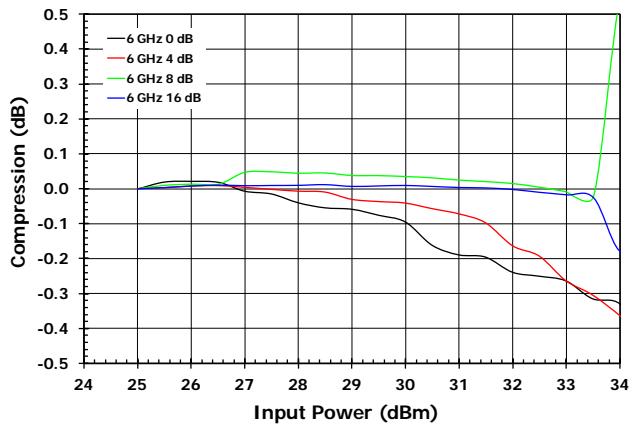


TYPICAL OPERATING CONDITIONS (5)

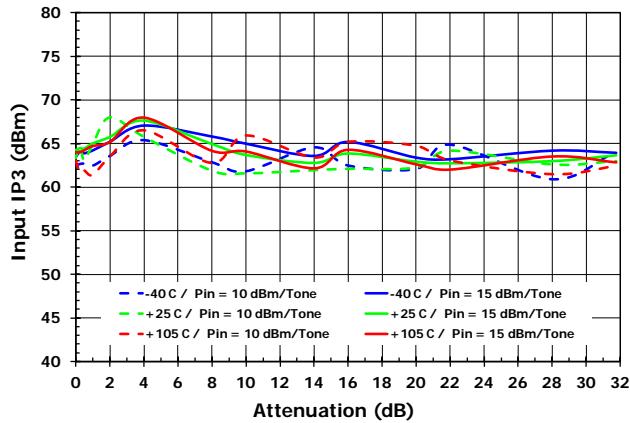
Input Compression (+25°C, 4GHz)



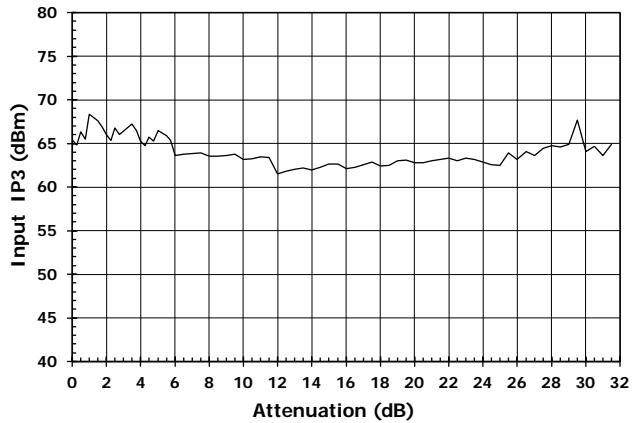
Input Compression (+25°C, 6GHz)



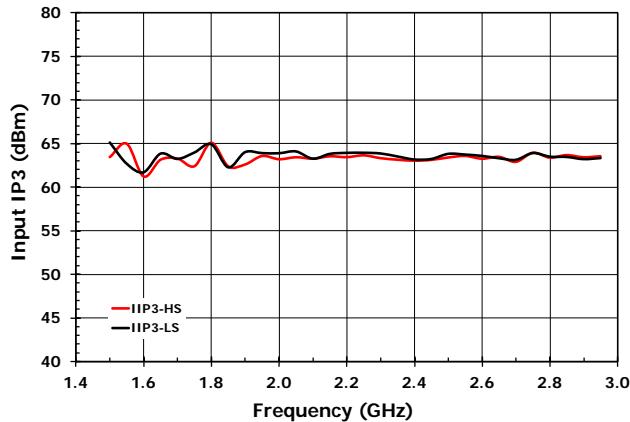
Input IP3 vs Attenuation [2GHz]



Input IP3 vs Attenuation [3.92GHz]



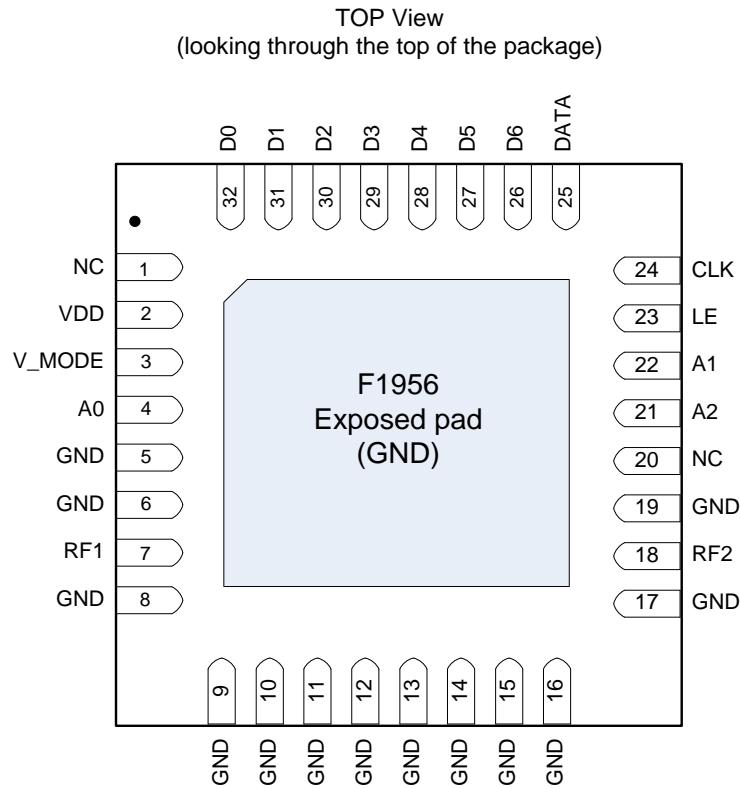
Input IP3 vs Frequency [Attn = 0dB, Pin = +22dBm]



PACKAGE OUTLINE DRAWINGS

The [package outline drawings](#) are located at the end of this document. The package information is the most current data available and is subject to change without revision of this document.

PIN DIAGRAM

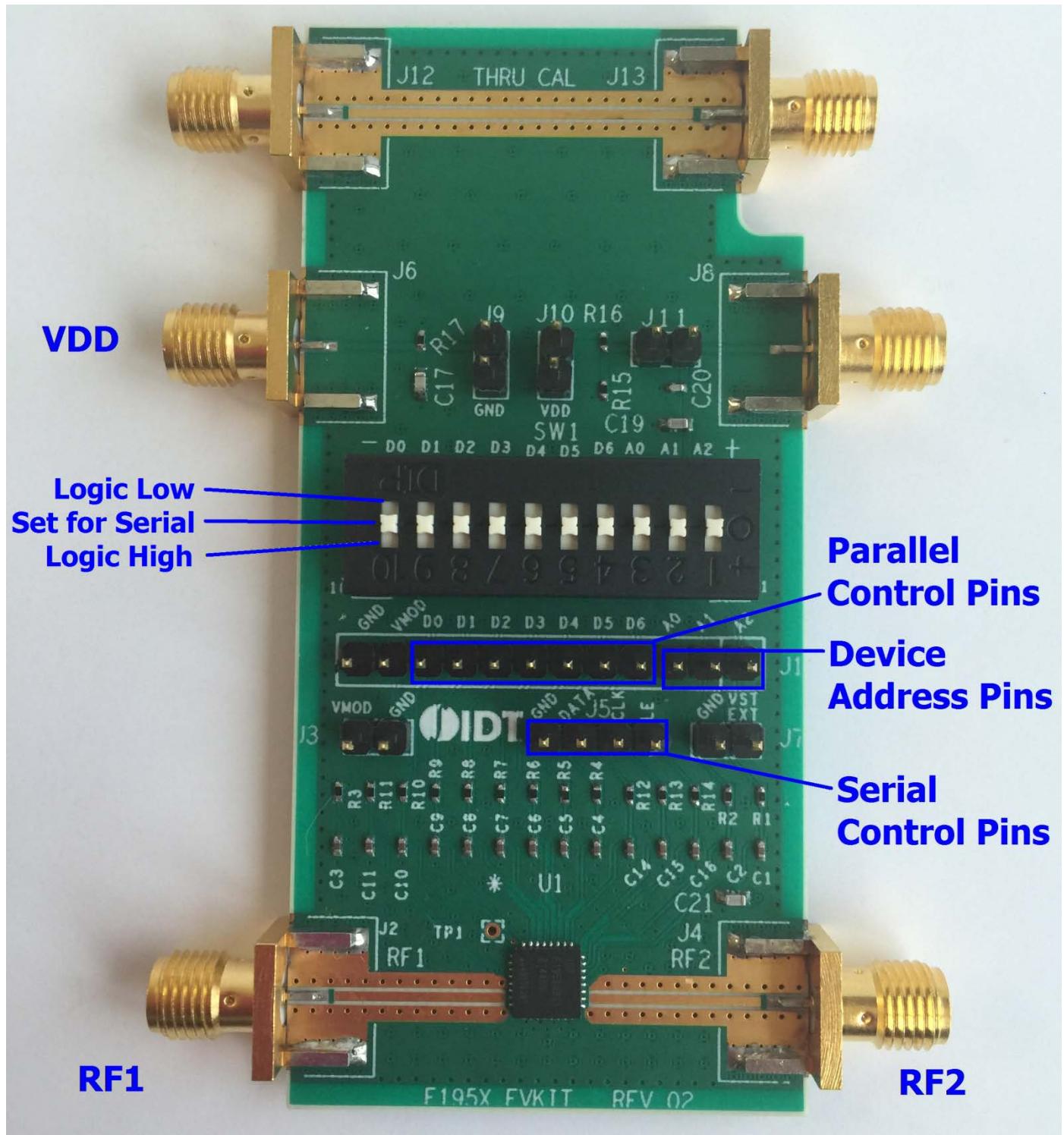


PIN DESCRIPTION

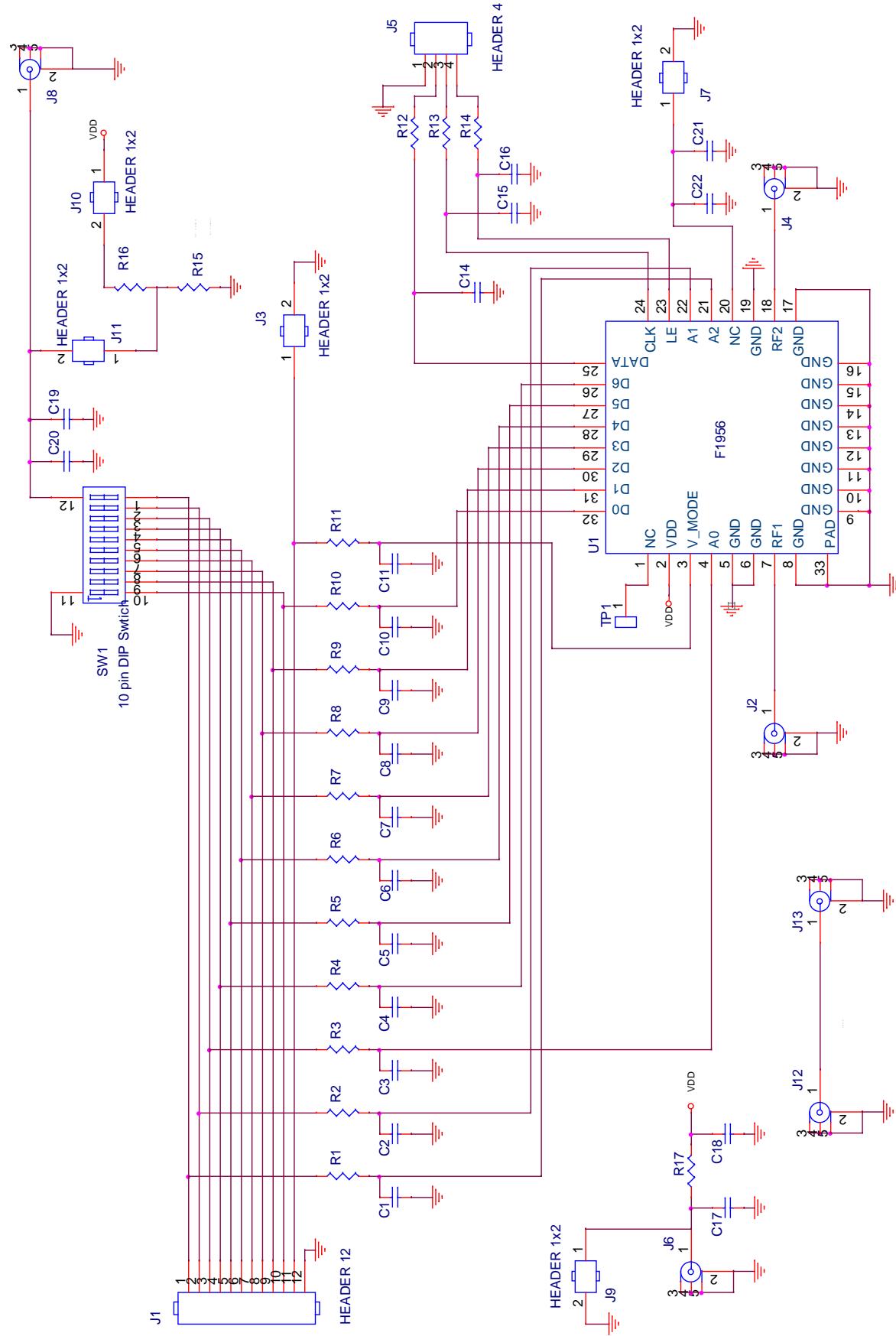
| Pin | Name | Function |
|------------|--------------------------------|--|
| 1 | DNC | This pin must be left open. |
| 2 | VDD | Main Supply. Use 3.3V or 5V. Bypass capacitor as close to pin as possible. |
| 3 | V _{MODE} ¹ | Logic low for parallel mode. Logic high or NC for serial mode. |
| 4 | A0 ² | Address bit A0 connection. |
| 5 | GND | Connect directly to paddle ground or as close as possible to pin with thru via. This pin is not internally connected |
| 6 | GND | Connect directly to paddle ground or as close as possible to pin with thru via. |
| 7 | RF1 | Device RF input or output (bi-directional). AC couple to this pin unless 0V DC. |
| 8 – 17 | GND | Connect each pin directly to paddle ground or as close as possible to pin with thru vias. |
| 18 | RF2 | Device RF input or output (bi-directional). AC couple to this pin unless 0V DC. |
| 19 | GND | Connect directly to paddle ground or as close as possible to pin with thru via. |
| 20 | NC | No internal connection. These pins can be left unconnected, voltage applied, or connected to ground (recommended). |
| 21 | A2 ² | Address bit A2 connection. |
| 22 | A1 ² | Address bit A1 connection. |
| 23 | LE ¹ | Serial interface latch enable input. |
| 24 | CLK ¹ | Serial interface clock input. |
| 25 | DATA ¹ | Serial interface data input. |
| 26 | D6 ¹ | Parallel control bit, 16dB. Ground pin if not used. |
| 27 | D5 ¹ | Parallel control bit, 8dB. Ground pin if not used. |
| 28 | D4 ¹ | Parallel control bit, 4dB. Ground pin if not used. |
| 29 | D3 ¹ | Parallel control bit, 2dB. Ground pin if not used. |
| 30 | D2 ¹ | Parallel control bit, 1dB. Ground pin if not used. |
| 31 | D1 ¹ | Parallel control bit, 0.5dB. Ground pin if not used. |
| 32 | D0 ¹ | Parallel control bit, 0.25dB. Ground pin if not used. |
| EP | Exposed Paddle | Connect to Ground with multiple vias for good thermal and RF performance. |

1. There is a 100kΩ pull-up resistor.
2. There is a 100kΩ pull-down resistor to ground.

EvKit PICTURE

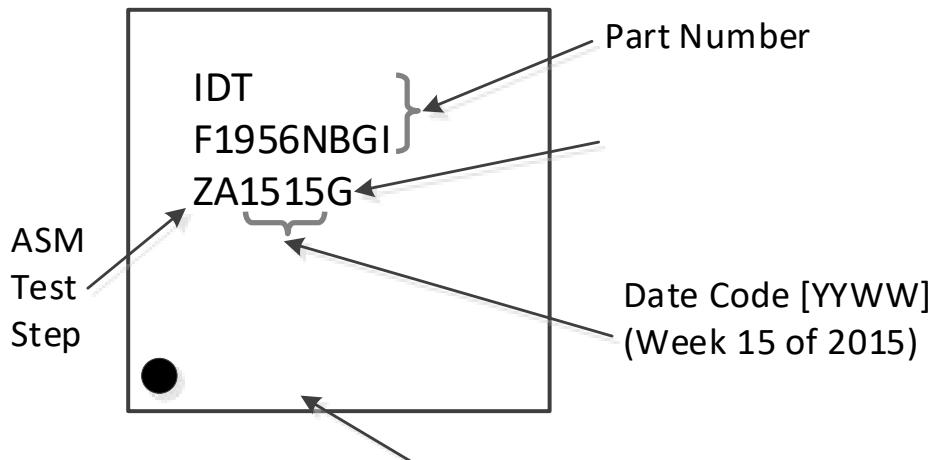


EVKIT / APPLICATIONS CIRCUIT



EVKIT BOM (REV 2)

| Item # | Part Reference | QTY | DESCRIPTION | Mfr. Part # | Mfr. |
|--------|--------------------------|-----|--|--------------------|-----------------|
| 1 | C1 - C11, C14, C15, C16 | 14 | 100pF $\pm 5\%$, 50V, COG Ceramic Capacitor (0402) | GRM1555C1H101J | MURATA |
| 2 | C18, C20, C22 | 3 | 1000pF $\pm 5\%$, 50V, COG Ceramic Capacitor (0402) | GRM1555C1H102J | MURATA |
| 3 | C17, C19, C21 | 3 | 10nF $\pm 5\%$, 50V, X7R Ceramic Capacitor (0603) | GRM188R71H103J | MURATA |
| 4 | R17 | 1 | 0Ω Resistors (0402) | ERJ-2GE0R00X | PANASONIC |
| 5 | R1 - R14 | 14 | 100Ω $\pm 1\%$, 1/10 W, Resistor (0402) | ERJ-2RKF1000X | PANASONIC |
| 6 | R15 | 1 | 6.98kΩ $\pm 5\%$, 1/10 W, Resistor (0402) | ERJ-2RKF6981X | PANASONIC |
| 7 | R16 | 1 | 10kΩ $\pm 1\%$, 1/10 W, Resistor (0402) | ERJ-2RKF1002X | PANASONIC |
| 8 | J3, J7, J9, J10, J11 | 5 | CONN HEADER VERT SGL 2 X 1 POS GOLD | 961102-6404-AR | 3M |
| 9 | J5 | 1 | CONN HEADER VERT SGL 4 X 1 POS GOLD | 961104-6404-AR | 3M |
| 10 | J1 | 1 | CONN HEADER VERT SGL 12 X 1 POS GOLD | 961112-6404-AR | 3M |
| 11 | J2, J4, J6, J8, J12, J13 | 6 | Edge Launch SMA (0.375 inch pitch ground, tab) | 142-0701-851 | Emerson Johnson |
| 12 | SW1 | 1 | SWITCH 10 POSITION DIP SWITCH | KAT1110E | E-Switch |
| 13 | U1 | 1 | DSA | F1956 | Renesas |
| 14 | | 1 | Printed Circuit Board | F1955 EVKit Rev 02 | Renesas |

TOP MARKINGS

APPLICATIONS INFORMATION

Power Supplies

A common V_{DD} power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than $1V/20\mu s$. In addition, all control pins should remain at 0V ($\pm 0.3V$) while the supply voltage ramps or while it returns to zero.

Digital Pin Voltage and Resistance Values

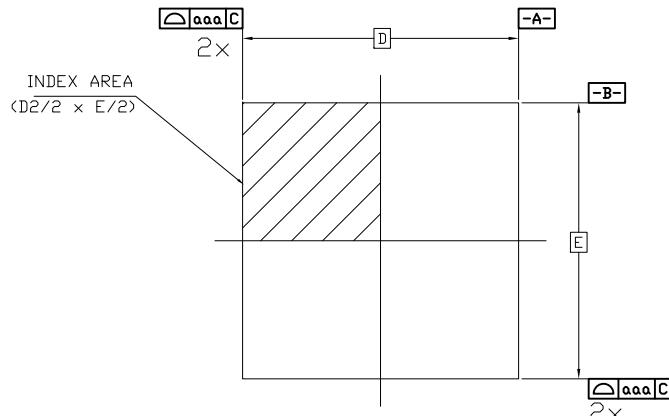
The following table provides open-circuit DC voltage referenced to ground and resistance values for each of the control pins listed.

| Pin | Name | Open Circuit DC Voltage | Internal Connection |
|------------|---------------|-------------------------|---|
| 3 | V_{MODE} | 2.5V | 100k Ω pull-up resistor to internally regulated 2.5V |
| 4, 21, 22 | A0, A2, A1 | 0V | 100k Ω resistor to GND |
| 23, 24, 25 | LE, CLK, DATA | 2.5V | 100k Ω pull-up resistor to internally regulated 2.5V |
| 26 – 32 | D6 – D0 | 2.5V | 100k Ω pull-up resistor to internally regulated 2.5V |

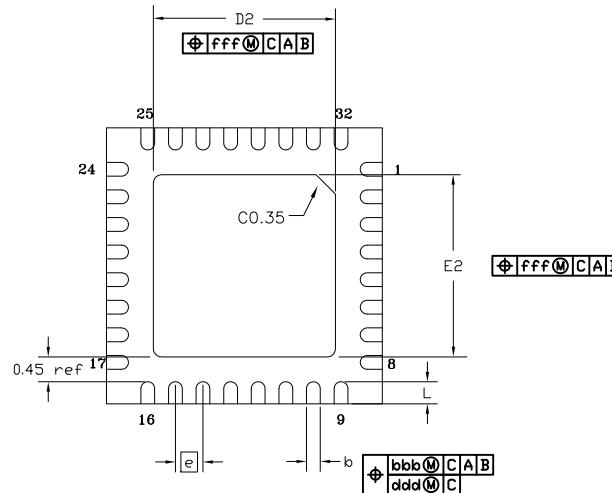
REVISION HISTORY

| Date | Description of Change |
|--------------------|--|
| May 22, 2015 | Initial release. |
| September 29, 2015 | <ul style="list-style-type: none">• Datasheet format update.• Added Maximum Average Power Rating |
| April 01, 2016 | <ul style="list-style-type: none">• Maximum operating frequency changed to 6GHz.• Added curves showing performance at higher frequencies. |
| February 23, 2021 | Rebranded to Renesas. |
| April 14, 2022 | Updated pin description table. |
| April 21, 2023 | Updated minimum and maximum specification limits for logic current in F1956 Specification table on page 4. |

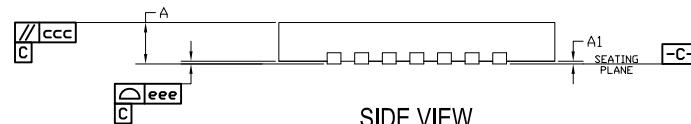
| REVISIONS | | | |
|-----------|-----------------|---------|----------|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 5/11/16 | JH |



TOP VIEW



BOTTOM VIEW



SIDE VIEW

| SYMBOL | DIMENSION | | |
|--------|-----------|------|------|
| | MIN | NOM | MAX |
| L | 0.30 | 0.40 | 0.50 |
| D | 5.00 | BSC | |
| E | 5.00 | BSC | |
| D2 | 3.20 | 3.30 | 3.40 |
| E2 | 3.20 | 3.30 | 3.40 |
| e | 0.50 | BSC | |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | .20 | .25 | .30 |
| aaa | | 0.10 | |
| bbb | | 0.10 | |
| ccc | | 0.10 | |
| ddd | | 0.05 | |
| eee | | 0.08 | |
| fff | | 0.10 | |

NOTES:

- ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
- ALL DIMENSIONS ARE IN MILLIMETERS.

TOLERANCES
UNLESS SPECIFIED
DECIMAL ANGULAR
 $X \pm .1$ $\pm 1^\circ$
 $XX \pm .05$
 $XXX \pm .030$

APPROVALS DATE
DRAWN *zac* 5/11/16
CHECKED

TITLE NB/NBG32 PACKAGE OUTLINE
5.0 x 5.0 mm BODY, EPAD 3.30mm SQ
0.50 mm PITCH QFN

SIZE DRAWING No.
C PSC-4348-02

REV
00

DO NOT SCALE DRAWING

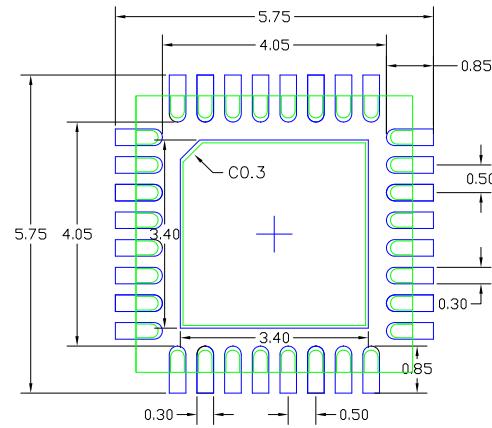
6024 SILVER CREEK
VALLEY ROAD, SAN JOSE,
CA 95138
PHONE: (408) 284-8200
FAX: (408) 284-3572



www.IDT.com

SHEET 1 OF 2

| REVISIONS | | | |
|-----------|-----------------|---------|----------|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 5/11/16 | JH |



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW, AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWN FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE, NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

| | | | |
|--|---------|---|-------------|
| TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR $X \pm .1$ $\pm 1^\circ$ $XX \pm .05$ $XXX \pm .030$ | | 6024 SILVER CREEK VALLEY ROAD, SAN JOSE, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-3572 | |
| APPROVALS | DATE | TITLE NB/NBG32 PACKAGE OUTLINE 5.0 x 5.0 mm BODY, EPAD 3.30mm SQ 0.50 mm PITCH QFN | |
| DRAWN <i>rac</i> | 5/11/16 | | |
| CHECKED | | SIZE | DRAWING No. |
| | | C | PSC-4348-02 |
| | | DO NOT SCALE DRAWING | |
| | | SHEET 2 OF 2 | |

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.