Data Communication Bus Interface for Modular Architecture of Small Satellites

M. Rizwan Mughal, Danilo Roascio, Leonardo M. Reyneri

Department of Electronics and Telecommunications, Politecnico Di Torino, Torino, Italy

Email: {muhammad.mughal, danilo.roascio, leonardo.reyneri}@polito.it

***Abstract*—This paper illustrates general data communication architecture of AraMiS project (Italian acronym standing for "modular architecture for small satellites) and inter-tile data communication bus interface structure of the small modular satellites. The dual redundant data bus will provide exchange of information in almost all operative conditions and connect all the electronic peripherals, supporting the data exchange speed required by the different sub-systems composing the satellite. The proposed architecture uses differential bus with galvanic isolation among all the connected modules in order to have fault tolerance, good signal integrity and to connect as many tiles in series or in parallel. The proposed structure has been tested in almost all possible fault conditions and the simulation and actual results show reliable transmission and reception of signal from one module to the other even under different types of fault conditions. System stability is guaranteed by the proposed characteristic of each subsystem in such a way that any number of modules can be connected to the communication bus without impairing overall performance and stability. This work presents the bus interface circuit located between the processor and the communication channel and also the fault tolerance analysis with different possible types of faults.**

***Index Terms*—**

I. Introduction

ONBOARD communication is one of the main issues in electronics system level development while working on university satellite mission. The basic architecture of AraMiS is based on one or more modular intelligent tiles [1]. Tiles or panel bodies have double function in the architecture: mechanical and functional. A single tile contains signal and power processing capabilities and six tiles are combined to form cubic shaped architecture.

At present, many fault-tolerant bus systems have been developed, realized and used for space applications [2-4]. Point-to-point communication structures are very reliable: a single fault or a node which starts generating data on the communication medium does not cause problems for all the system [5], but it results in high costs, volume and weight due to the number of wires. Data transmission using bus systems is cheaper, but also more sensitive to faults.

Several different standards for short range communications have been defined. Wireless communications employ standards such as IrDA, Blue-Tooth, Zig-Bee etc., and wired communications employ standards such as Universal Asynchronous Receiver Transmitter (UART), UART IrDA line mode, Serial Peripheral Interface (SPI), Inter Integrated Circuit (I2C) etc. [6-7]. Each of them has specific advantages and drawbacks. In space environment, the bus needs to be fault tolerant and operationally reliable.

Data communication using wireless approach on board the small satellites is still in the early stages as it is prone to much external interferences. In [8-9], the authors describe the analysis of using Optical wireless communication bus and discuss the use of this standard to exchange data between the sub-systems of a satellite.

Wired communication uses physical wires to transmit data across different subsystems. Using physical wires requires the electronic signals to be transmitted over a metal conductor. Currently, this is the most reliable way of transmitting/receiving data onboard the satellite missions. Depending on the protocol, either differential signaling or single ended signaling scheme can be used with wired communication. A differential signal [10] represents difference between two physical quantities. In differential signaling, the signal value is the difference between individual voltages whereas in single-ended signaling, 'ground' is used as voltage measurement reference. Differential signaling brings many advantages over single ended signaling such as tolerance to ground offsets, common mode rejection, resilience to outside electromagnetic interference and crosstalk, and cancelling of the magnetic field of each conductor. Since differential signaling only provides physical mechanism to transmit bits across the medium, any user defined encoding scheme can be sent/received across the low voltage differential signaling (LVDS) link.

AraMiS employs IrDA RZI (return to zero, inverted) encoding scheme with the proposed circuit. It is a coding format in which the encoder sends a pulse for every zero bit in the transmit bit stream. This coding scheme has been used because it is compatible with pulse transformers and it is easy to implement since it is the coding scheme used by IrDA line and available in many microprocessors. Next sections describe the bus interface structure that will ensure data to be transmitted on differential bus correctly.

978-1-4673-4688-7/12/$31.00 ©2012 IEEE

II. Cross Bus

Each tile incorporates solar panels on the external side and basic power routing, data routing and signal processing capabilities on the internal side. Multiple tiles interface through a proprietary self-configuring, dual-redundant, distributed power and data bus. By using modular tiles each having power and data routing capabilities, shape of the satellite can be configured according to payload needs. If payload requires, say e.g., 28V instead of typical tile voltage 14V, tiles can be added in series to have this voltage. If more current is needed, parallel configuration can be used. Usually power and data outputs of each tile use the same ground and the reference voltage level may be different between two tiles. Fig.1a shows typical way of interconnecting two tiles in series in order to obtain twice the tile voltage at the output. Let's assume that any data bus that uses common grounds between modules is used. Connecting *Gnd1* and *Gnd2* for data bus causes a short circuit (SC) between voltage *V2* and *Gnd2*, ultimately decreasing output voltage. In order to overcome this problem, we propose interface module that provides galvanic isolation between the tiles for inter tile data communication as shown in Fig 1b.

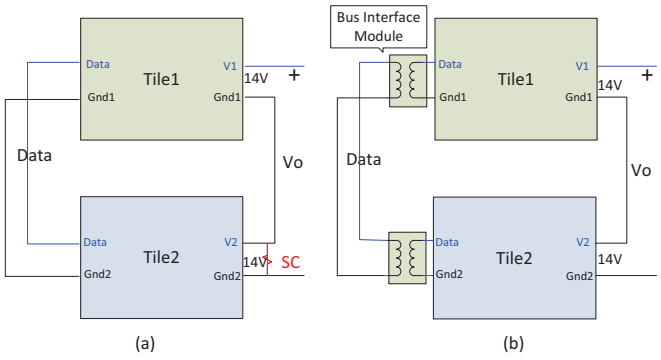


Fig. 1 Interconnecting two tiles in series (a) Typical (b) Proposed approach

In order to achieve high reliability and fault tolerance, an ad hoc interconnection system called cross bus has been proposed by authors of [1]. Fig.2a shows basic module for cross bus architecture and Fig.2b shows a network of basic modules connected with the bus; six tiles connected to form the cubic shaped small satellite. This is a fully redundant system since every node is always reachable unless it suffers four faults on different points which is quite rare even in space applications.

In Fig 2a, the controller sends data to be transmitted on the bus through differential buffer1and received data from differential buffer2 is sent to the receiver of the controller for further processing. Interconnecting modules of Fig 2(a) together, results in a network structure of six tiles labeled Fig.2(b).In the next sections, we present the detailed structure of the basic module i.e. transmitter, receiver and coupling.

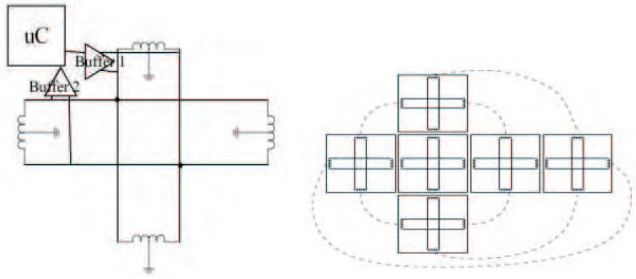


Fig. 2 Cross bus module (a) Single (b) Network of six [1]

III. Design of Interface Module

The bus interface circuit is connected between communication channel and microprocessor on each tile. Fig.3 illustrates the design of bus interface structure. The circuit employs an open drain Metal Oxide Semiconductor Field Effect Transistor which is used as a switching element. The transformer is used as coupling element and the differential receiver is used as a receiver to receive the pulsed signal.

A. Transmitter

AraMiS employ IrDA RZI coding scheme in communication bus therefore it is necessary to transmit pulsed signals onto the bus. The easiest way to generate pulsed waveform is to use a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) and the Gate terminal of the transistor to control current flow. In MOSFET, a voltage on oxide insulated gate induces a conducting channel between drain and source terminals. Switching frequency depends upon the frequency of input pulses. Input pulse of the controller is applied to the Gate of transistor that creates a current path from supply voltage to ground for the time the pulse is high. During the pulse, there is a change of voltage across primary side of the transformer that induces a voltage to its secondary side by the principle of mutual induction. The input signal of each module is pulse waveform (from tile's microcontroller), with maximum 1Mbps baud rate. An RC parallel circuit is placed in the current path from supply to ground as shown in Fig.3. Two main advantages are achieved by placing the RC circuit.

- At high frequency i.e. at switching frequency, the capacitor behaves like a short circuit according to (1)

$$Xc = \frac{1}{2\pi fC} \quad (1)$$

Where X_c =reactance in ohms (Ω)
f = frequency in Hz
C =Capacitance in farads

i.e. at high frequency, the reactance is negligible and it can be viewed as a short circuit across capacitor terminals. Effect of resistor is eliminated causing high amplitude current flow through primary side of transformer to ground path of Fig.3.

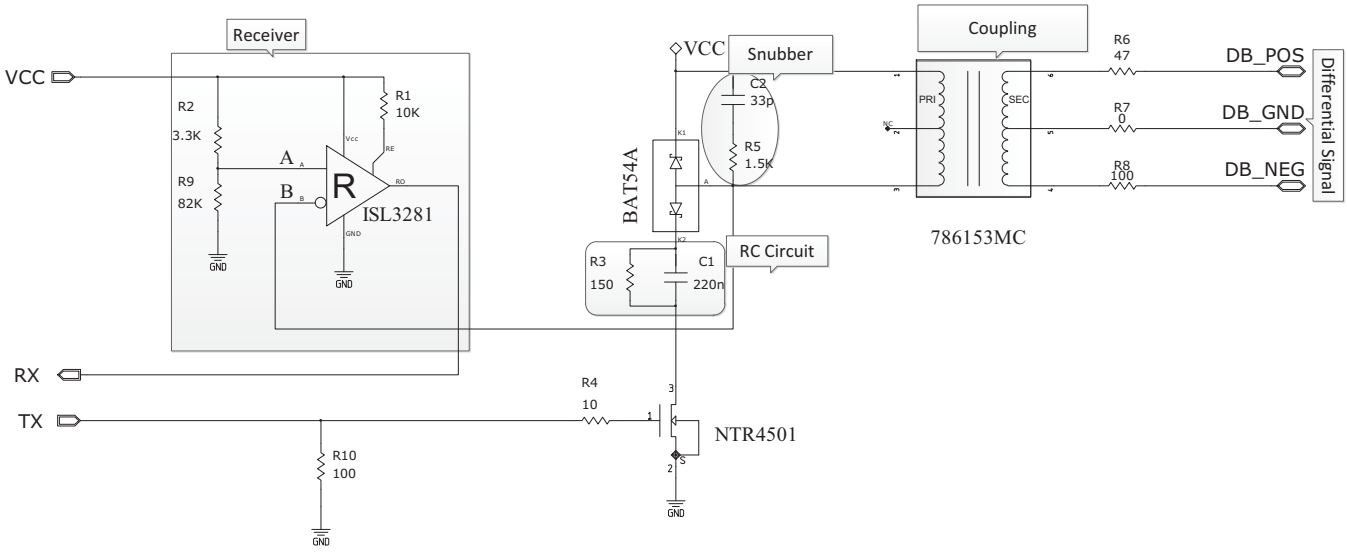


Fig. 3 Design of Bus Interface circuit

- In the event of faults i.e. when there is either continuous '1' across MOSFET gate terminal, there is zero frequency or steady DC. In this case capacitor becomes an open circuit and current flow through resistor only. We get a limited current with less amplitude and the devices get protected.

B. *Receiver*

The design of the receiver is based on a RS-485 receiver. Fig.3 shows receiver section with non-inverting input labelled as line *A* and the inverting input labelled as line *B*. Two wires carry the signal voltage and reference voltage. The receiver detects the difference between the two. Since most of the coupled noise is common to both wires, it cancels out. The receiver must see certain voltage difference between *A* and *B*. If *A* is greater than *B*, the receiver's output is logic high. If *B* is greater than *A*, the output is logic low. Fig.4 show plot of differential voltage at *B* compared with a fix voltage at *A* in the receiver section. As soon as voltage at *A* becomes higher than that on *B*, the receiver outputs a high pulse.

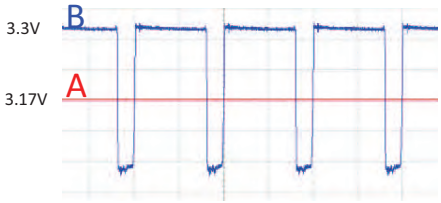


Fig. 4 Receiver inputs

Commercial low power receiver ISL3281E [11] is being used in proposed design. Receiver inputs feature a "Full Fail-Safe" design, which ensures logic high receive output if receiver inputs are floating, shorted, or terminated but undriven. Another main reason for choosing an RS485 receiver here is that it can withstand a common mode voltage far beyond the power rails, and this happens regularly with the circuit's configuration.

C. *Coupling*

For coupling purpose, pulse transformer is used because it is easy to connect with the signal controller, with RZI coding. The only limit of its use is the product of peak pulse voltage and the duration of the pulse (*V.t* product). Pulse transformers by definition have a duty cycle of less than 50%. The energy stored in the coil during the pulse must be damped out before the next coming pulse. In order to damp out the energy of the pulse, a commercial Schottky barrier diode, BAT54A [12] has been used as a Flyback diode across primary terminals of the transformer as shown in the Fig 3. Schottky barrier diode is a semiconductor diode with a low forward voltage drop (0.15V-0.45V) and a very fast switching action. The second schottky diode in the MOSFET branch is used to avoid ringing of the transformer/bus with drain to source capacitance, Cds; of the MOSFET. The lower voltage drop of the diode can also provide higher switching speed and better system efficiency. The proposed design uses commercial 786153MC pulse transformer [13].

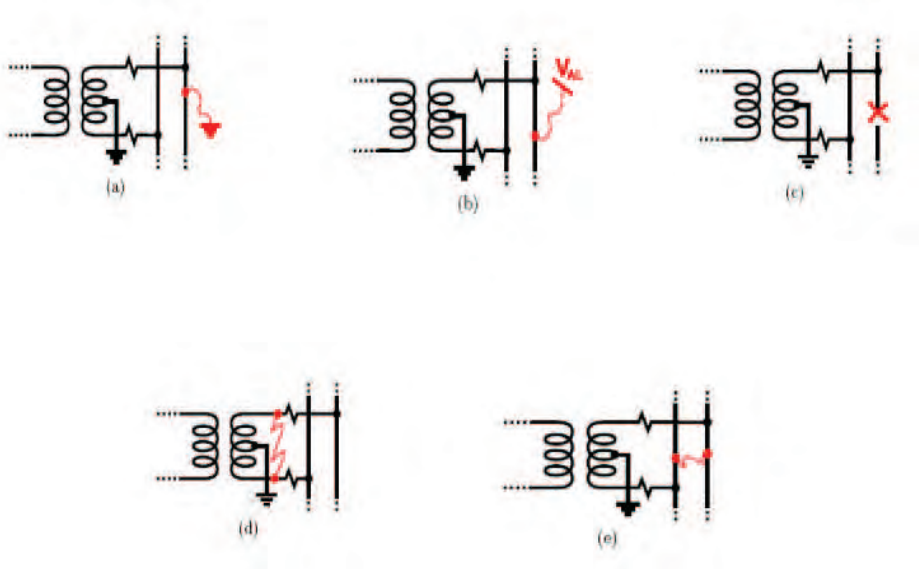


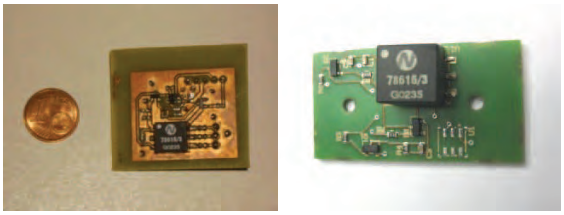
Fig. 5 Possible Types of Faults

D. *Snubber to Supress Ringing*

During the tests, the first non-ideal phenomenon is the ringing at the receiver part. Actually, this is due to the fact that Schottky diode during reverse bias behaves just like a capacitor and energy stored in the inductor i.e., transformer winding starts ringing with the capacitance of reverse biased schottky diode introducing oscillation therefore overshoot is encountered in the voltage waveform. A typical solution is to add an RC parallel snubber circuit to dump the ringing.

The basic function of snubber circuit is to absorb energy from the reactances in the circuit [14]. An RC snubber is proposed in our design to overcome the ringing problem as shown in Fig.3. The RC snubber damps the ringing and if snubber resistance is equal to the characteristics impedance of the resonant circuit $\sqrt{\frac{L}{C}}$ then resonant circuit will be critically damped and have no overshoot. The values of these R and C can be optimized experimentally.

The acutal fabricated module is shown in Fig.6 .This module is placed in a plug and play approach in each AraMis tile.



(a) (b)

Fig. 6 Implemented Bus Interface Module (a) Test circuit (b) Final Module

IV. Fault Analysis

As space environment is prone to faults, several types of faults can be encountered during the time when the satellite is in orbit [15]. Detailed fault analysis with all the possible types of faults is discussed in this section.The bus can tolerate the following types of faults

a) Short circuit between a conductor of the bus and the ground (see Fig.5a), the line that has been shorted with ground will have no voltage but the other one will continue to operate causing sufficient differential voltage but with reduced noise margin for the receivers to receive the signal correctly.

b) Short circuit between a conductor and a bus power supply (see Fig.5b) has the same effect as in the above case, but constant supply voltage on the line may damage the winding of the transformer because of the fact that the specific transformer winding may not be able to withstand supply voltage, the solution is to add a series resistance that prevents saturation of the core of the transformer and the bus continues to operate normally with the overhead of noise margins reduction.

c) Open circuit of one of the conductors (see Fig.5c), the system continues to operate because if one of the lines is down, the other one is operating normally. We reduce differential voltage and noise margin but the bus operates continuously.

d) Short-circuit of the secondary of a transformer, (see Fig.5d), the bus continues to operate normally and only the faulty unit will be isolated from the bus i.e. it will not receive any signal.

e) Short circuit of both conductors (see Fig.5e); in this case there is no voltage difference between the conductors of the bus but we still obtain differential voltage at the receivers because of the different values of the termination resistances. The expense is significant reduction of the noise margin.

According to this analysis, even in case of possible faults, the modules transmit and receive the data correctly. Therefore the proposed structure can provide fault tolerance at the expense of losing noise margin.

In order to demonstrate the fault analysis, we connected six modules across the bus and then measured mean differential voltages on each receiver in standard situation and then with possible fault condition. Fig.7 shows the block diagram of interconnected modules.In the block diagram, module 2 is used as transmitter and all others are receivers. Failure condition always happens at module 4.

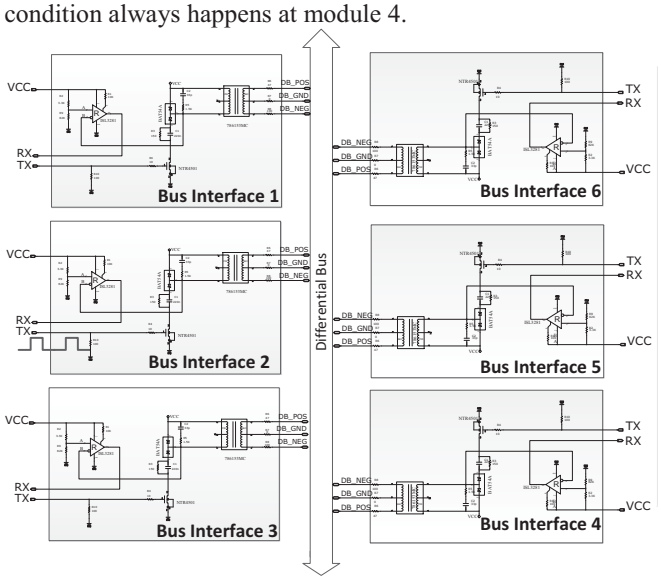


Fig. 7 Block Diagram of connecting six modules

Table I summarizes the mean voltage on the inverting terminal of each receiver i.e. at line *B* of each reveiver in normal operation and with all possible faults. Under circumstances when there is no activity on the bus , the mean value on line *B* remains at constant 3.3V i.e. at supply voltage. Under normal activity , the higher differential voltage causes more drop of supply voltage, ultimately reducing the mean voltage.

TABLE I

Failure Type Module No.	No fault	Fault (a)	Fault (b)	Fault (c)	Fault (d)	Fault (e)
1	2.7V	2.85V	2.80V	2.85V	3.1V	3.25V
2	*2.5V*	*2.5V*	*2.5V*	*2.5V*	*2.5V*	*2.5V*
3	2.7V	2.85V	2.85V	2.8V	2.7V	3.15
4	2.7V	2.9V	2.85V	2.8V	0V	3.2V
5	2.7V	2.9V	2.85V	2.8V	2.7V	3.0V
6	2.7V	2.9V	2.85V	2.8V	2.7V	3.0V

The data of Table I is obtained by using the proposed bus interface circuit with all types of faults listed in Fig.5. The resulted waveforms of interconnecting modules of interface circuit are shown in Fig.8 (a) through (e) in the same order as they had been discussed in Fig. 5.

This differential voltage is compared with a fixed voltage through a voltage divider (on inverting terminal *A*) as can be shown in basic interface circuit in Fig.3. Depending upon the difference between *A* and *B*, the receiver generates the output voltage pulses accordingly. Input waveform is shown in yellow trace. There is a high differential voltage on the bus in case of faults (a) and (b). Shortening of both the conductors together causes worst decrease in the differential voltage but the mean differential voltage will increase in this case. It is apparent from column (e) of Table I.

Since Table I lists the mean voltage at the inverting terminal

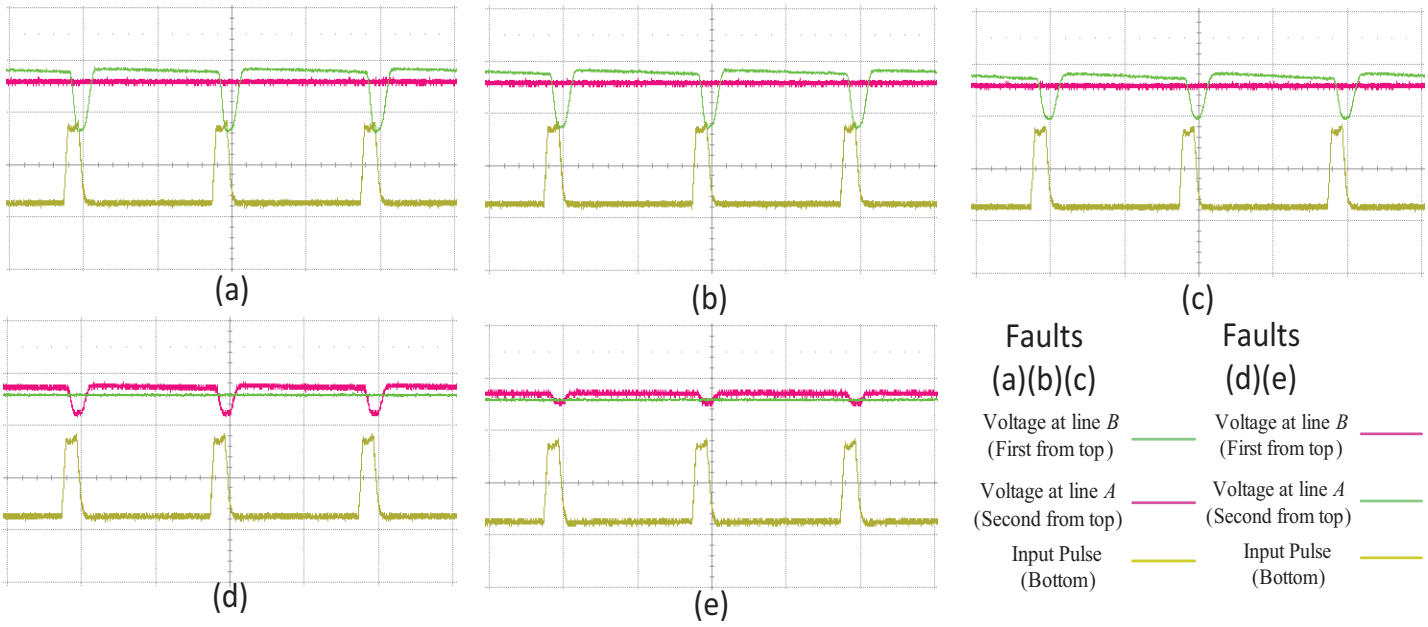


Fig. 8 Fault analysis with proposed bus interface circuit

of each receiver, it is apparent from Table I results and Fig. 8 that this input stays at supply voltage i.e. 3.3V and as soon as there is differential signal (referred to negative terminal of bus DB_NEG), the level drops below 3.3V. In case of no fault, the high differential signal causes more drop and ultimately we get relatively low mean voltage on the inverting terminal as it can be seen from Table I. Mean value across inverting terminal of the differential receiver is about 2.7V in case of no faults on the bus. Every fault situation causes reduction in mean voltage according to how severe it is. In case of fault (e), which is the most severe fault, there is a very minor differential signal and a very minor drop in the mean voltage as is apparent from column (e). Since in this demonstration, fault condition happen at module 4 only, it is quite clear from the data in table that we don't get any voltage at the receiver of module 4 when fault (d) happens on it. Since module 2 is used as transmitter in our demonstration, its receiver receives the best differential voltage in any case as it has not to do anything with the faults.

Fig.9 shows the performance analysis interface circuit. A random bit sequence generated by MSP430 UART [16] is applied to the transmit pin TX of module 2. The yellow trace show the input transmit stream and blue trace show the voltage level received on the receiver pin RX of the module 4. The transmit and receive behavior has been tested with random sequence of bits transmitted on the bus with and without fault conditions. The results show no delay in the reception of bit sequence and also acceptable bit error rate.

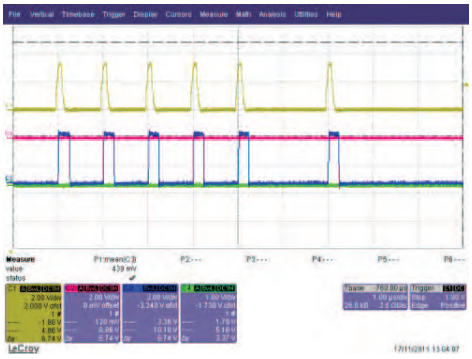


Fig. 9 Transmit and Receive of Random Bit Sequence

V. Conclusion

In this work we have shown the use of intelligent modular tiles and COTS components to design a fault tolerant system which is the basic aim of AraMiS project i.e. to achieve fault tolerance from COTS components and also the modular design.

The data communication interface module has been tested with MSP430 microprocessor at different transmission baud rates and it has shown maximum transmission and reception error within the protocol limits. In this work, we only tested the module using IrDA RZI encoding scheme. In future, we will test this circuit with all possible wired transmission encoding schemes (like 8B10B etc.) and also by modifying the proposed circuit to have only radiation hardened LED and use wireless solution instead of employing differential signaling and pulse transformers.

References

[1] Stefano Speretta, Leonardo M. Reyneri, Claudio Sanso´e, Maurizio Tranchero, Claudio Passerone, Dante Del Corso.; , " Modular architecture for satellites," 58th International Astronautical Congress , Hyderabad, India, 24 - 28 September 2007

[2] Tai, A.T.; Chau, S.N.; Alkalai, L.; "COTS-based fault tolerance in deep space: Qualitative and quantitative analyses of a bus network architecture," High-Assurance Systems Engineering, 1999. Proceedings. 4th IEEE International Symposium on, vol., no., pp.97-104, 1999.

[3] Chandler, G.D.; McClure, D.T.; Hishmeh, S.F.; Lumpp, J.E.; Carter, J.B.; Malphrus, B.K.; Erb, D.M.; Hutchison, W.C.; Strickler, G.R.; Cutler, J.W.; Twiggs, R.J.; , "Development of an Off-the-Shelf Bus for Small Satellites," Aerospace Conference, 2007 IEEE , vol., no., pp.1-16, 3-10 March 2007.

[4] Addaim, A.; Kherras, A.; Zantou, B.;, "Design of Store and Forward Data Collection Low-cost Nanosatellite," Aerospace Conference, 2007 IEEE , vol., no., pp.1-10, 3-10 March 2007.

[5] Temple, C.; "Avoiding the babbling-idiot failure in a time-triggered communication system," Fault-Tolerant Computing, 1998. Digest of Papers. Twenty-Eighth Annual International Symposium on, vol., no., pp.218-227, 23-25 June 1998.

[6] Leens, F.; , "An introduction to I2C and SPI protocols," Instrumentation & Measurement Magazine, IEEE , vol.12, no.1, pp.8-13, February 2009

[7] Johnson, D.; "Implementing serial bus interfaces with general purpose digital instrumentation," AUTOTESTCON, 2009 IEEE, vol., no., pp.125-129, 14-17 Sept. 2009.

[8] Stefano Speretta,Danilo Roascio, Leonardo M. Reyneri, C. Sansoè, Maurizio Tranchero, Claudio Passerone, Dante Del Corso,"Optical-Based data communication bus for satellites",Actaastronautica(2009).

[9] Meitzler, R.C.; Schneider, W.; Conde, R.;, "IRCOMM: spacecraft free-space optical bus development," Aerospace Conference, 2005 IEEE , vol., no., pp.1583-1588, 5-12 March 2005.

[10] Benedetto, J.M.; Oliver, A.; , "High-speed data transmission for spaceborne applications," Radiation Effects Data Workshop, 2001 IEEE , vol., no., pp.67-71, 2001

[11] ISL3281E datasheet, Online: http://www.intersil.com/data/fn/fn6543.pdf.

[12] BAT54 Schottky Diodes datasheet, Online: http://www.fairchildsemi.com/ds/BA/BAT54C.pdf

[13] Rhombus Industries Inc. Pulse Transformers, Transformer equivalent circuit, 2008. Online:http://www.rhombus-ind.com/app-note/circuit.pdf.

[14] Philip C. Todd ;"snubber circuits: Theory, Design and Applications",May93

[15] Danilo Roascio, "Sottosistema di comunicazione tollerante ai guasti per satellite," Masters. dissertation, Dept. Elect. Eng., Politecnico Di Torino., Italy, 2008

[16] T. Instruments, "MSP430 User's Guide," Texas Instruments, Tech. Rep.,SLAU208H, Dec 2010