CSE 664 Introduction to System-on-Chip Design
FINAL EXAM
Submit one single pdf or word file

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1. **Which of the following statements are TRUE? Mark true or false in the provided space** (6 points)

   False_ The nonrecurrent (NRE) cost for designing an integrate chip is decreasing with the progress of semiconductor technology.

   True_ We should not use NMOS to pass VDD because this will forward-bias its parasitic junction diode and cause DC current.

   False To improve performance of a combinational gate, the fastest input signal must be connected to the transistor that is closest to the output.

   True_ A gate with a regenerative property can suppress noise.

   True_ A larger transistor has smaller resistance.

   True_ The purpose of having setup constraints for D flip-flops is to make sure that there is enough time for the input to settle down in the bistable circuit to avoid metastability.

2. **Because the capacitance of a transistor is proportional to its size, to improve the speed of this design, one of the CSE664 students decided to change all transistors to a minimum size to reduce the RC delay. Do you agree with him/her?**
Briefly explain your answer. (5 points)

I would disagree with this student. While this may improve speed at a transistor-level, the resistance of each transistor would increase, making the power requirements troubling. Additionally, this design does not take into account the asymmetric response of PMOS and NMOS transistors, so the pull-up network strength would suffer relative to the pull-down. Finally, this design might not take into account other effective ways of reducing RC delay such as buffering with inverter chains.

3. **How will the delay of a wire change if its length is doubled?**
Briefly explain your answer. (5 points)

The delay of a wire is determined by its capacitance. We know that the equation for the internal capacitance of a wire includes a multiplication by its length, so the C_{int} will double. The fringe capacitance of the wire is scaled by twice the length, so the C_{fringe} will be four times larger. As the total capacitance of the wire = C_{int} + C_{fringe}, we can see that after doubling the length of the wire:

$C_{wire\_after} = 2(C_{int\_prev} + 4C_{fringe\_prev})$

4. **You are given the layout of an inverter implemented as a static complementary CMOS gate. Assume that the gate has symmetrical response. Its γ (i.e., C_{int}/C_g ratio) is 1.5. The propagation delay of this inverter is 300 ps if there is no fan-out.**
    a. If using this inverter to drive a load C_L that is 96 times as large as C_{int}, what will be the propagation delay? (10 points)
    b. Two extra inverters are inserted before the load mentioned in (a) to boost the driving strength to make a three-stage buffer chain. How large should those two inverters be chosen so that the total delay is minimized? What is the path delay in this case? (10 points)

A: $T_p = 300(1+ 96 / 1.5) = 300(64) = 19200$ ns = **19.2µs**

B: The size of these inverters should be half and one-quarter the size of the original inverter.
$T_p = 3*300(1+3Root(96) / 1.5) = 600(1+ 4.58 / 1.5) = 600(4.05) = 2431$ns = **2.431µs**

5. **Design a static complementary CMOS gate for logic function: $\overline{ab + c}$.**

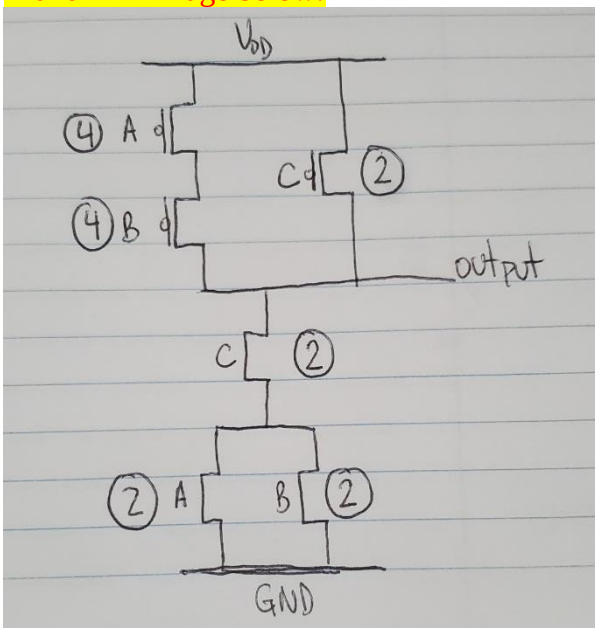
   a. Draw the transistor level schematic; (10 points)

   b. Size the transistors so that each PDN and PUN has the same resistance as an inverter with 2:1 PMOS and NMOS size; (5 points)

   c. Which input pattern gives the longest tphl? How about tplh? (5 points)

   d. Assume that the external load capacitance is 1pF, the diffusion capacitance of a unit size PMOS/NMOS is 0.2pF. The equivalent resistance of NMOS and PMOS with L/W=1 are 15KΩ and 30KΩ respectively. Estimate the worst case tphl and tplh using Elmore model. (5 points)

A and B in image below:



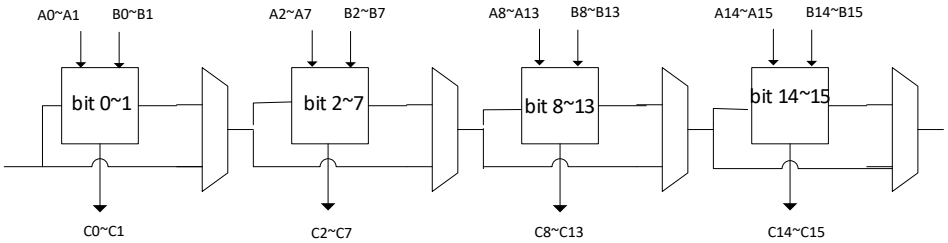
C: Worst Pull-Up Input: **[ABC] 001**
Worst Pull-Down Input: **[ABC] 101**

D: **worst case tphl** = $C_n*R_{an} + C_l*2R_n + C_p*(R_{bp} + R_{cp})$= 0.2*15/2 + 1(2*15/2) + 0.2(30/2 + 30/4) = 1.5 + 15 + 4.5 = **21µs**
Worst case tplh = $C_n*R_{cn} + C_l*(R_{ap} + R_{bp}) + C_p*R_{ap}$ = 0.2*15/2 + 1*2*30/4 + 0.2*30/4 = 1.5 + 15 + 1.5 = **18µs**

6. **You are given a carry-bypass adder as shown in** Error! Reference source not found.**below. Let t_c = 2 ns be the delay for carry logic in each bit slide, t_s = 3 ns be the delay for sum logic, and t_{by} =0.5 ns be the delay for the bypass MUX.**

a. What is the worst-case delay of this adder? Which input pattern will cause this delay? (5 points)

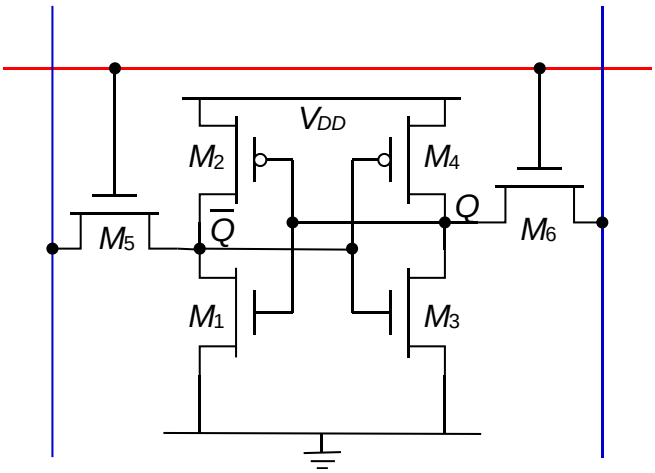
b. If the input is 0x0FF0 + 0x1177, how long will it take for the adder to calculate the output? (10 points)



a. Worst case input for this adder is 0xF777, which will not allow the use of any bypasses. It will take $t_{byp} = 4t_{carry} + 3t_{carry} + 3t_{carry} + 3t_{carry} + t_{sum} = 4(2) + 3(3(2)) + 3 = 8 + 18 + 3 =$ **29ns**

b. This would take $0t_{carry} + 2tbyp + 3t_{carry} + t_{sum} = 2(0.5) + 3(2) + 3 = 1 + 6 + 3 =$ **10ns**

7. **Consider the following circuit. Where will you possibly see this? Consider the transistors M1, M2, and M5. Which one has the largest size? Which has the smallest size?** (4 points)



We would see this circuit as an implementation of an SRAM cell. The largest transistor is M2, since it is PMOS and needs to be ~2x the size of M1 for a symmetric response. We must have M1 > M5 to prevent a conflicting state when both are active. Therefore the smallest transistor is M5. **Overall: M2 > M1 > M5**