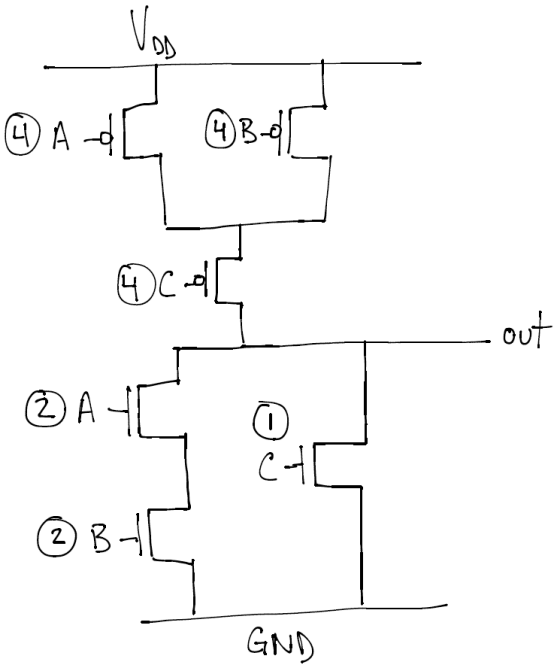
HW #3

(Lecture 4, 5 and 7)

Design a static complementary CMOS gate for logic function: $\overline{ab + c}$.

(1) Draw the transistor level schematic;

(2) Size the transistors so that each PDN and PUN has the same resistance as an inverter with 2:1 PMOS and NMOS size; See sizing on drawing



(3) Which input pattern gives the longest tphl? How about tplh?

[Format ABC] Longest tphl: 110 Longest tplh: 100

(4) Assume that the external load capacitance is 1pF, the diffusion capacitance of a unit size PMOS/NMOS is 0.2pF. The equivalent resistance of NMOS and PMOS with L/W=1 are 15KΩ and 30KΩ respectively. Estimate the worst case tphl and tplh using Elmore model.

Longest tphl = $R_{cp}*C_p + R_{bn}*C_n + (R_{an} + R_{bn})*C_l$

= (30/4)*0.2 + (15/2)*0.2 + (15/2 + 15/2)*1 = 7.5*0.2 + 7.5*0.2 + 15*1 = **18µs**

Longest tplh = $R_{bp}*C_p + (R_{bp} + R_{cp})*C_l + (R_{an} + R_{cn})*C_n$

= (30/4)*0.2 + (30/4 + 30/4)*1 + (15/2 + 15)*0.2 = 7.5*0.2 + 15*1 + 22.5*0.2 = **21µs**