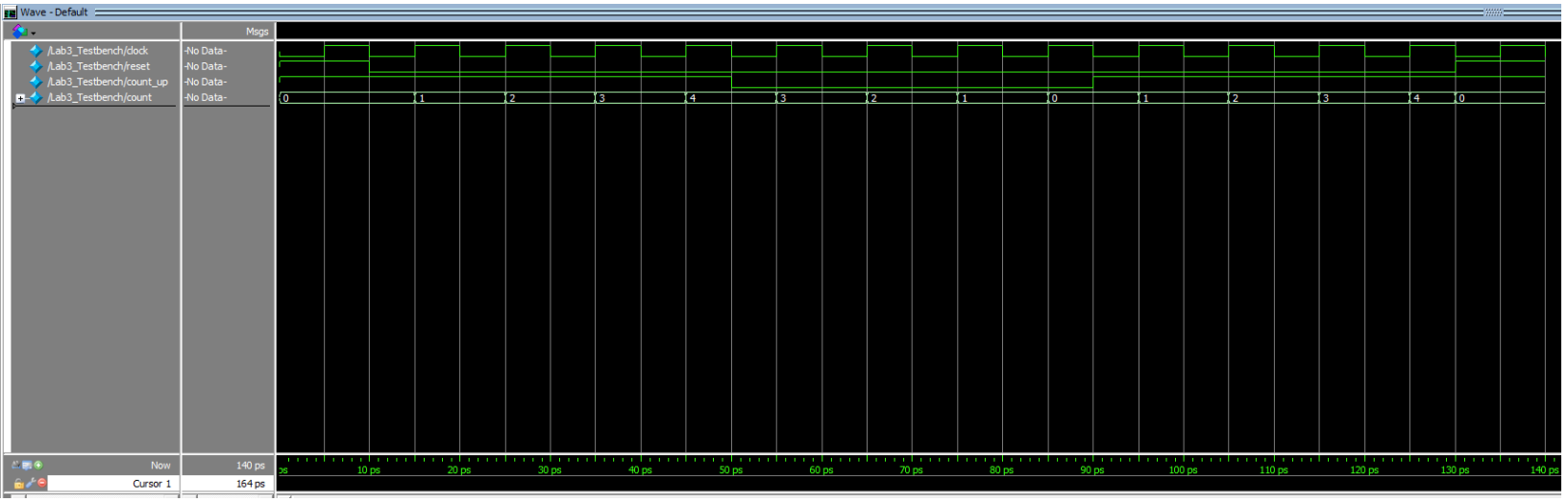
COUNTER:

```
module updown_counter_4bit (input clock, reset, count_up, output reg
[3:0]count);
      always @(posedge clock or posedge reset)
      begin
                  if (reset)
                  count = 4'b0000;
                  else
                  if (count_up)
                        count = count + 1;
                  else
                        count = count - 1;
      end
endmodule
```

TESTBENCH:

```
module Lab3_Testbench();

reg clock, reset, count_up;
wire [3:0] count;

updown_counter_4bit counter (clock, reset, count_up, count);

initial begin

clock = 0;
reset = 1;
count_up = 1;

forever #5 clock = ~clock;

end

initial begin

#10 reset = 0;
#120 reset = 1;

end

initial begin

#50 count_up = 0;
#40 count_up = 1;

end

endmodule
```


Wave - Default
Msgs
/Lab3_Testbench/clock
/Lab3_Testbench/reset
/Lab3_Testbench/count_up
/Lab3_Testbench/count
-No Data-
-No Data-
-No Data-
-No Data-
0
1
2
3
4
3
2
1
0
1
2
3
4
0
Now
140 ps
Cursor 1
164 ps
10 ps
20 ps
30 ps
40 ps
50 ps
60 ps
70 ps
80 ps
90 ps
100 ps
110 ps
120 ps
130 ps
140 ps