Outline for paper

* Interests in this technology started around the 2000s
  + Looking to avoid issues of pipeline hazards
  + Power consumption concerns
* Basic overview
  + Asynchronous processors are composed of separate logical units that process work on demand and communicate with each other via communication protocols to verify that data transfer occurs properly rather than a global clock
  + Allows for more modularity in chip development – can improve one component at a time without having to focus solely on the bottleneck operation before decreasing the clock cycle time.
* Concepts:
  + What does a processor look like when fully async?
  + What applications of asyc circuits are there for specific processes?
    - Async communication meshes are waaaay faster than buses, especially for analog sensors, like visual sensors.
    - Fully async is great for low workload, low power requirement systems that are long-running /IoT applications.
    - Smaller footprint for async since there is less routing of clocking
  + My proposal – using an asynchronous sensor network processor for stand-alone VR headsets, such as Oculus Quest. These applications are sensitive to power consumption requirements as well as overheating concerns, and have to process a huge amount of visual information non-stop to stay coordinated. Can even be combined with the neural linkages to make recognition of physical hazards more rapid.
* **Design concepts:**
* AMULET
  + The third in a pioneer series of async processors that showed feasibility of them vs synchronous
  + Displayed the benefits of less Electromagnetic interference since there is no chip-wide clock (good for sensors!) and power control.
* Exploiting synchronous for async circuits fpga
  + It has been shown to be possible to use fpga to produce async circuits
  + For proposal of solution? Fpga for field sensors is a good combo
* SAMIPS
  + Concurrent Sequential Processes (CSP) used to simulate the processor
  + GALS (Globally Async, Locally Sync)
  + 32 bit processor
  + Handles data hazards by storing which data is in use and alerting when the instruction is read.
  + Control hazards are handled by “coloring” the processor – instructions must have the same color as the overall processor in order to me accepted into the next stage. Flushes the pipeline if you guess wrong.
* **Low energy / iot**
  + SNAP/LE
    - Sensor Network Asynchronous Processor / Low Energy
    - Optimized for sensor network applications – bit filtering, event scheduling ,etc
    - Focus on very low wakeup / sleep times to be responsive but also save power
    - Can run at 23MIPS (0.6V) to 200MIPS (1.8 V)
  + BitSNAP
    - A variation of SNAP/LE that trades off the ability to ramp up the voltage for better performance and standardizes extremely low power consumption at all times
    - Uses a bit-serial datapath vs the 16-bit parallel datapath in SNAP
      * Async is good at handling dynamic datapath sizes
      * Hardware implementation is smaller, further improving power efficiency due to leakage at submicron chip creation
  + Low Power GPS Baseband Processor
    - Improves on Standard GPS receivers of the time by reducing power consumption
    - Allows for continuous operation that was not possible before due to overheating and battery concerns
    - GPS receivers are already split into the RF component (highly power optimized), and the Digital Signal Processing (DSP) component (not yet optimized)
    - Propose a further segmentation of constant sensor input processing (async) and the triangulations and logical processing of the signals (synchronous)
  + FIR Implementation Case Study (Finite Impulse Response)
    - Notes that the typical synchronous approach to limiting power consumption is to reduce clock speed. This is detrimental for real-time sensor applications, where sample rate must be high, or analogue.
    - Roughly 61% reduction in power consumption and 43% reduction in chip area at the expense of performance
* **Brain stuff**
  + DYNAPs
    - Using asynchronous circuits to convey sensor information in real-time, such that there is implied information from the timing of the inputs, which is not possible with clocked systems.
    - These systems also have a very large fan-in and fan-out network, so optimizing connections from each neuron is critical. Async protocols means any number could be communicating vs limit of a bus (either limit connects or make one really big)
    - Mimicing the structure of the problem to be run is helpful for efficient performance.
    - Able to achieve very dense neuron network and route it on-chip
  + Digital Neurosynaptic Core
    - Previous approaches to hardware-level neural modelling focus on density to approach realism
    - This opts for a setup that is programmable, since the synapses are generalized to a consistent set of components analogous to a typical Processor (crossbar memory kept in the neurons)
    - Allows for separation of hardware and software development, normally tough for async applications
  + Hardware-Software Co-Design for Brain-Computer Interfaces
    - Brain-Computer Interfaces (BCI)
    - Focuses on processing signals from medical devices implanted in patients’ brain tissue
    - Must be low-power and not overhead, since its implanted in the brain
    - Many applications are closed loop – read, process, and act on information
    - Must be configurable to different diseases and patient profiles