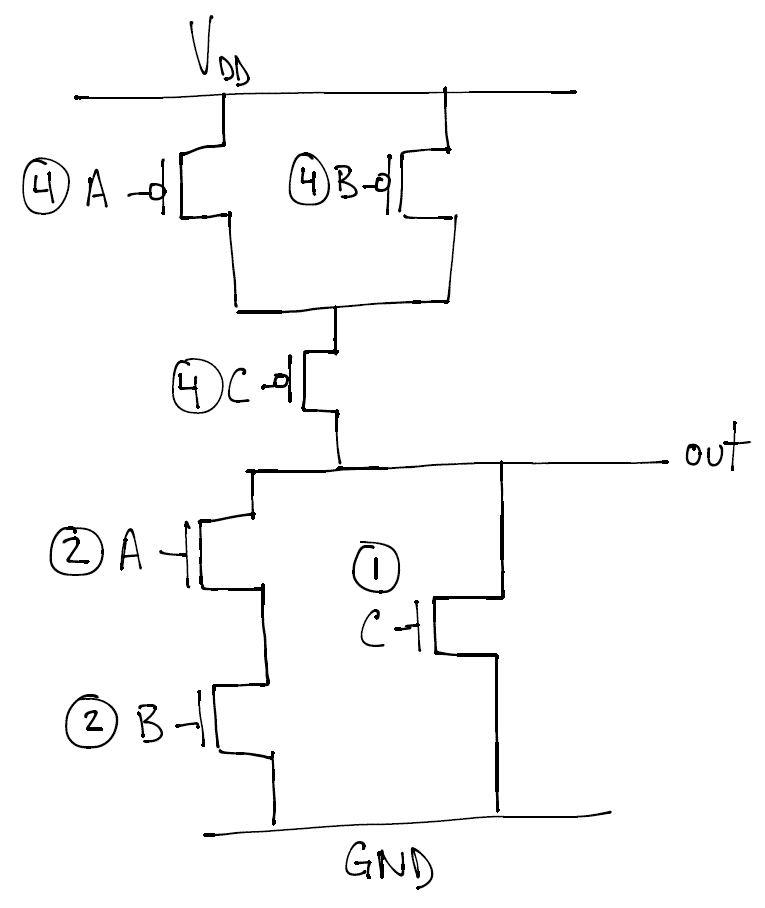
**HW #3**

(Lecture 4, 5 and 7)

Design a static complementary CMOS gate for logic function: .

(1) Draw the transistor level schematic;

(2) Size the transistors so that each PDN and PUN has the same resistance as an inverter with 2:1 PMOS and NMOS size; See sizing on drawing



(3) Which input pattern gives the longest tphl? How about tplh?

[Format ABC] Longest tphl: 110 Longest tplh: 100

(4) Assume that the external load capacitance is 1pF, the diffusion capacitance of a unit size PMOS/NMOS is 0.2pF. The equivalent resistance of NMOS and PMOS with L/W=1 are 15KΩ and 30KΩ respectively. Estimate the worst case tphl and tplh using Elmore model.

Longest tphl = Rcp\*Cp + Rbn\*Cn + (Ran + Rbn)\*Cl

= (30/4)\*0.2 + (15/2)\*0.2 + (15/2 + 15/2)\*1 = 7.5\*0.2 + 7.5\*0.2 + 15\*1 = **18μs**

Longest tplh = Rbp\*Cp + (Rbp + Rcp)\*Cl + (Ran + Rcn)\*Cn

= (30/4)\*0.2 + (30/4 + 30/4)\*1 + (15/2 + 15)\*0.2 = 7.5\*0.2 + 15\*1 + 22.5\*0.2 = **21μs**