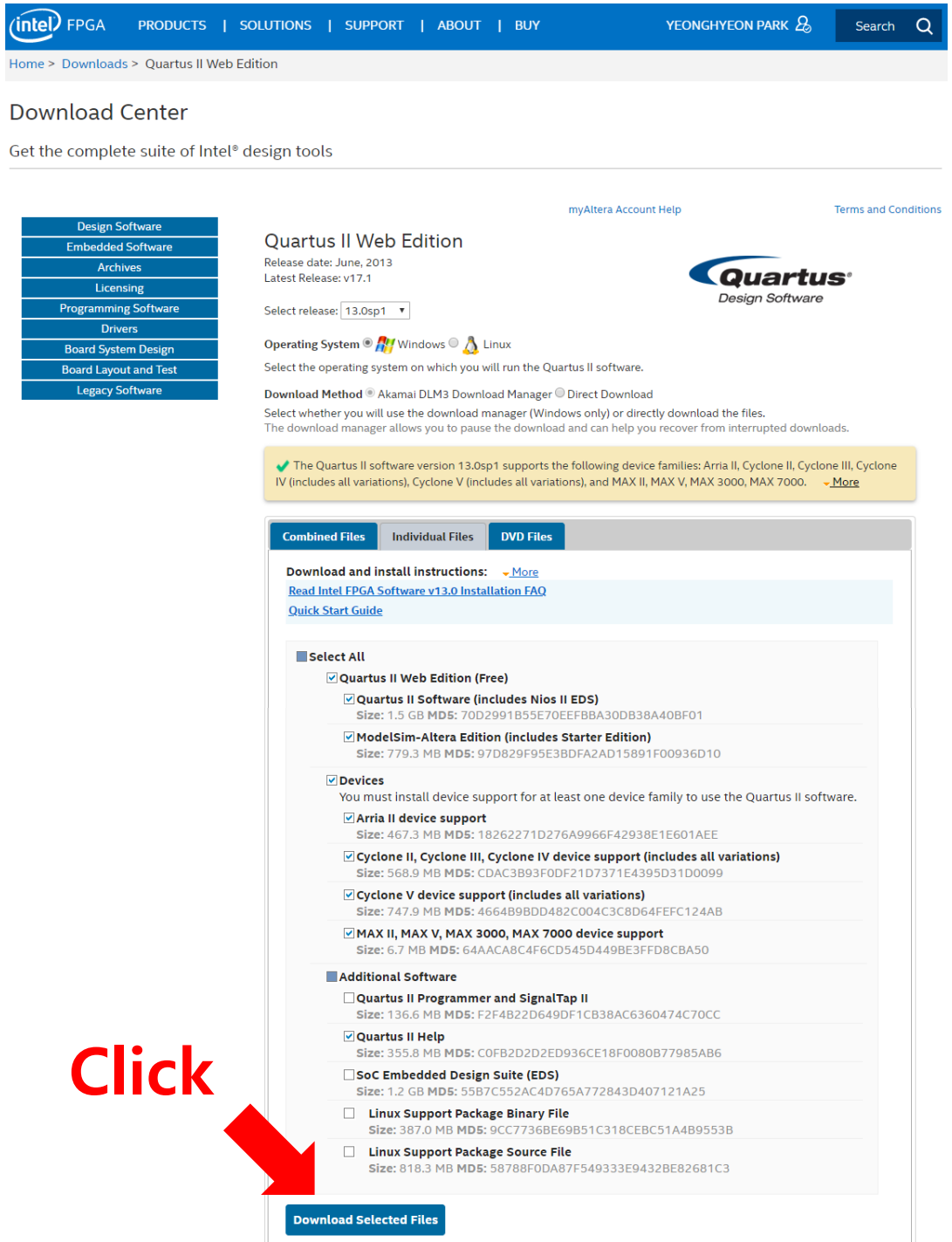
논리회로 및 실험

2주차



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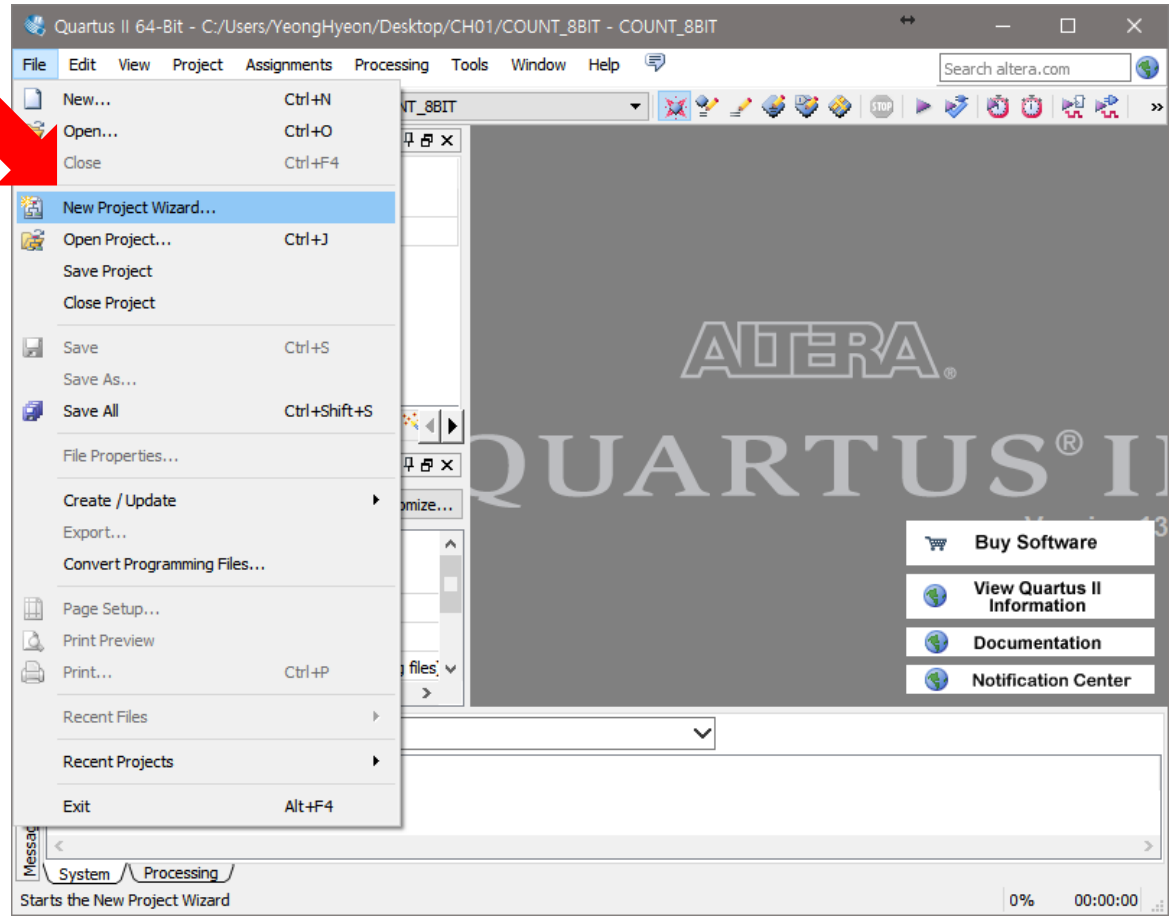
1 in Performance & Productivity
for CPLD, FPGA, SoC FPGA, and HardCopy® ASIC designs
Design Software v13.0
QUARTUS® II
ALTERA
MEASURABLE ADVANTAGE™

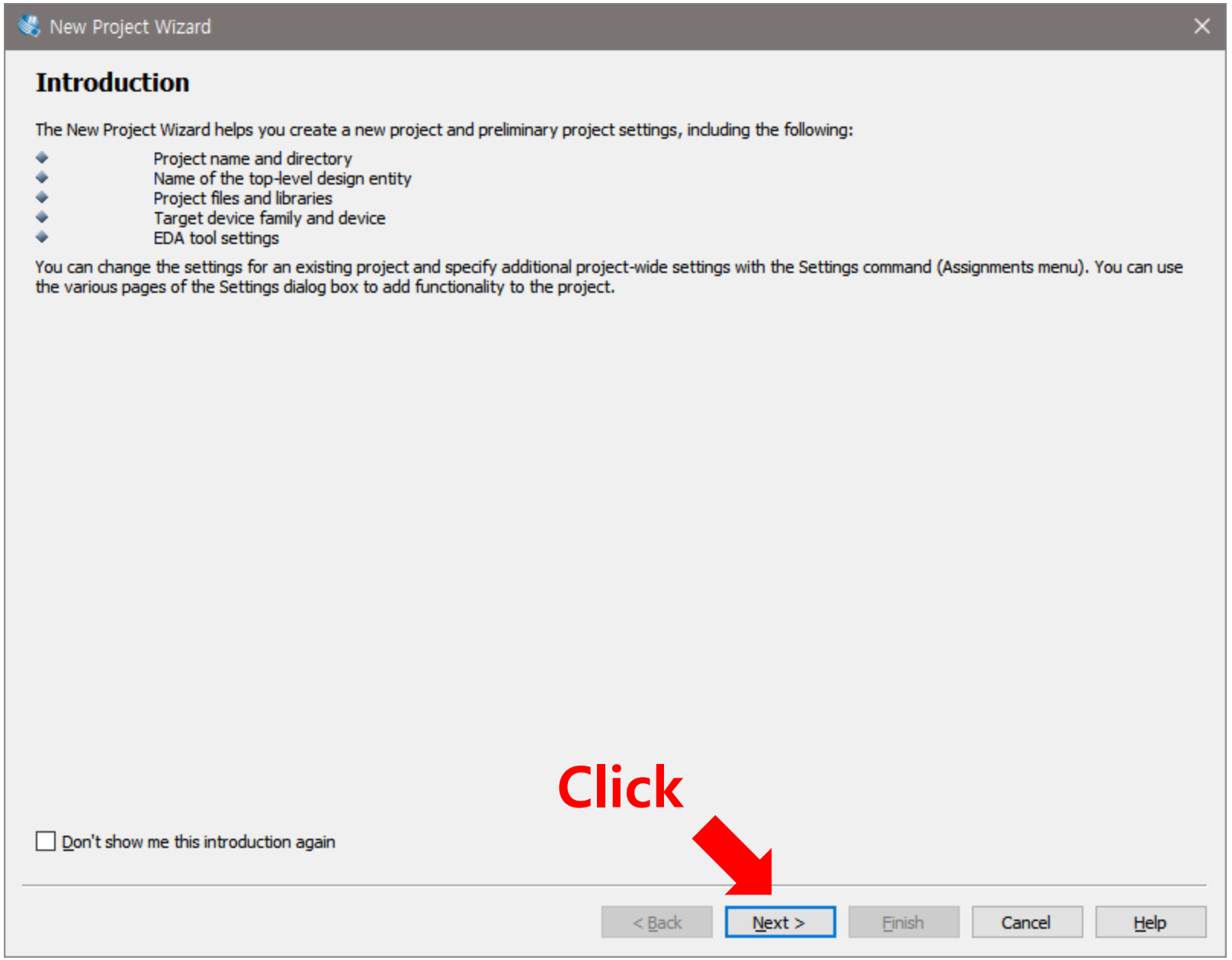
방법 1

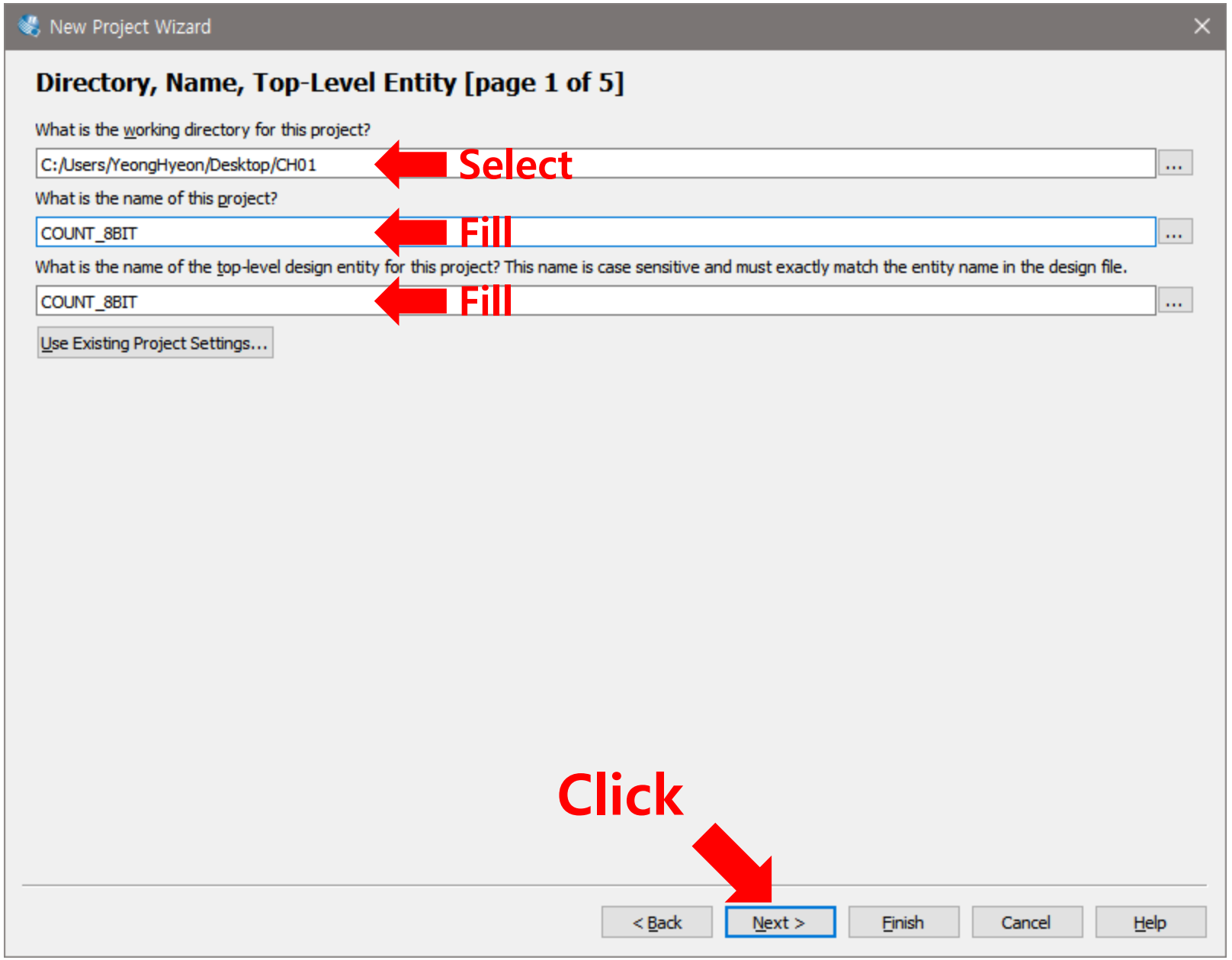
Click

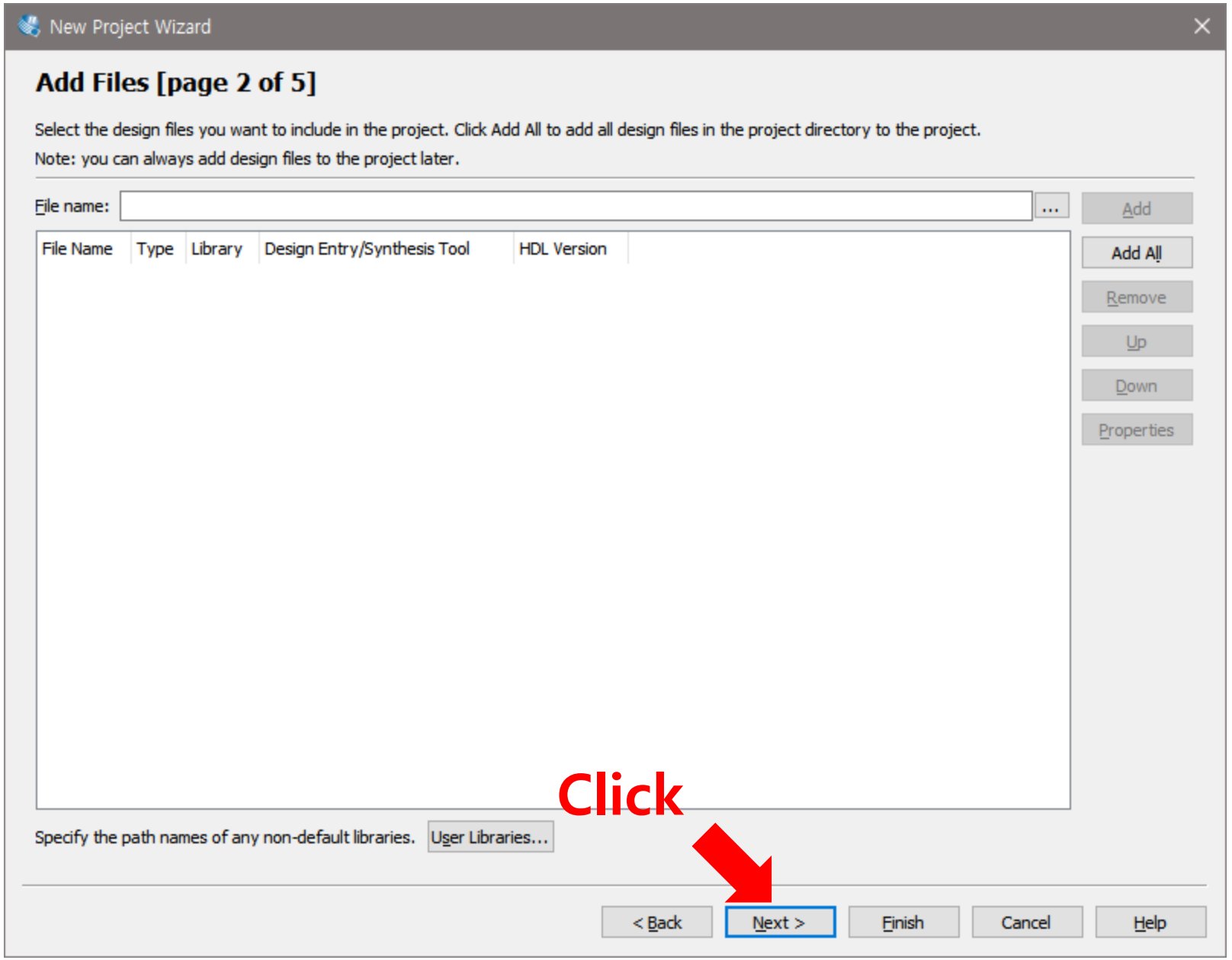
방법 2

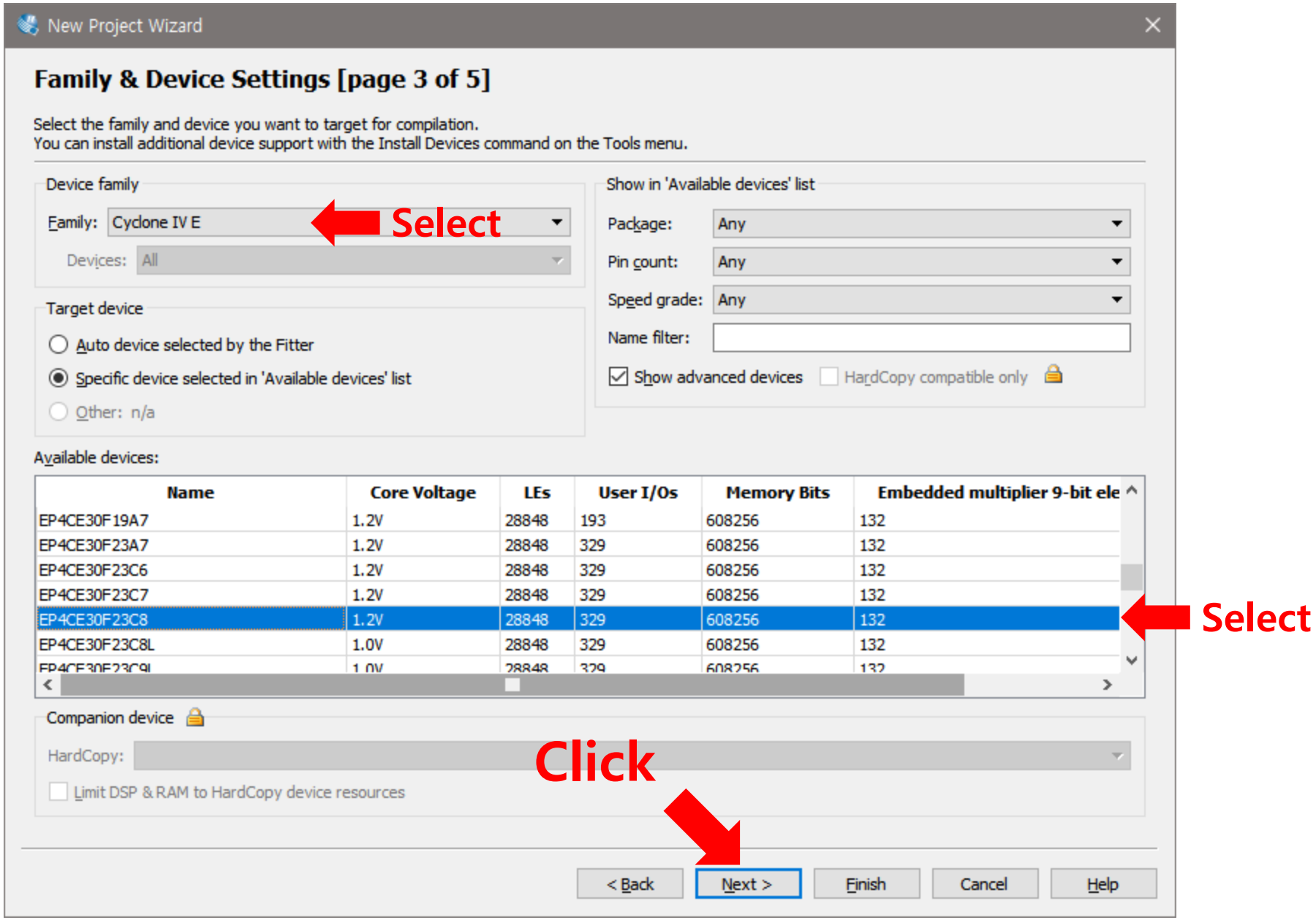
Click

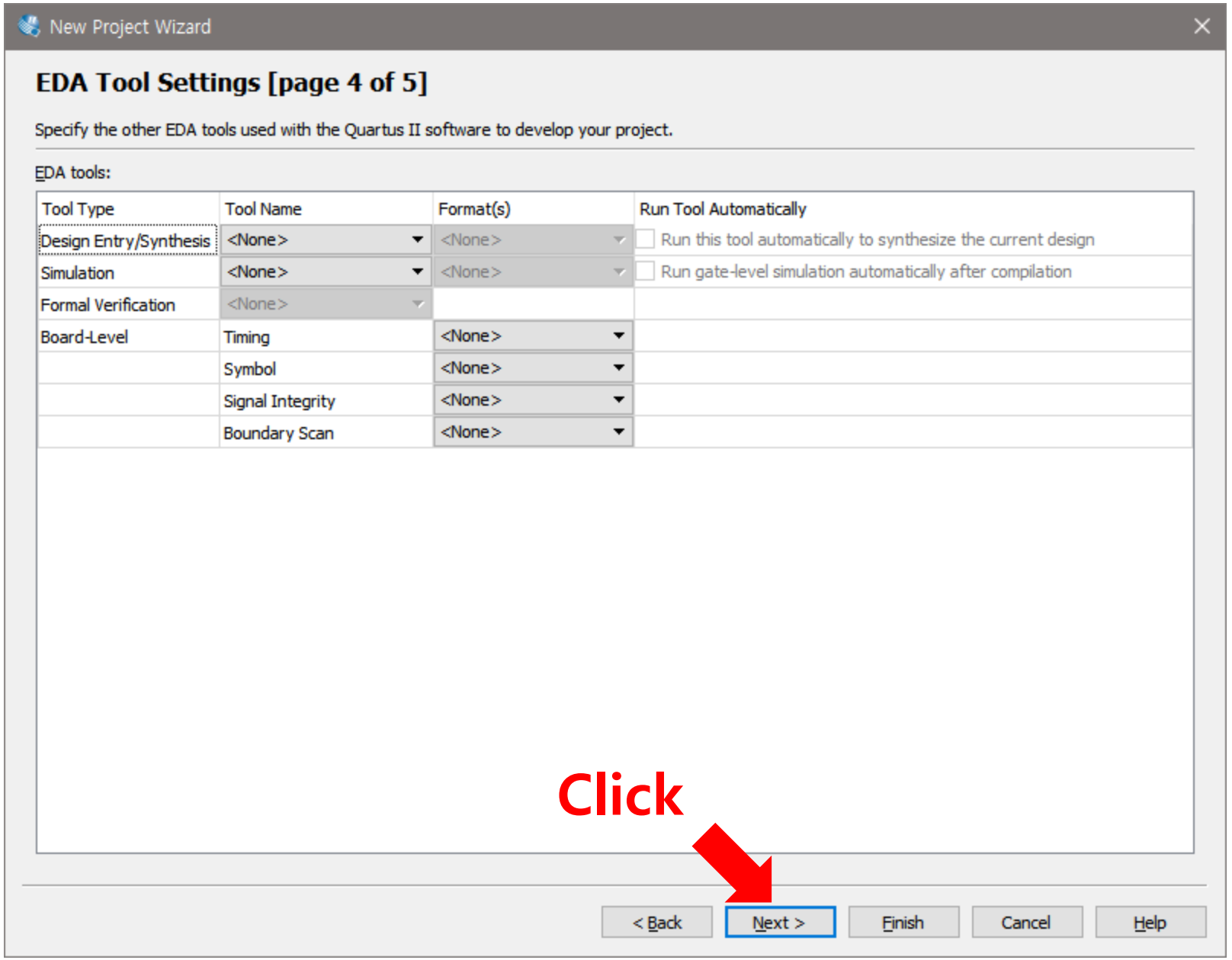


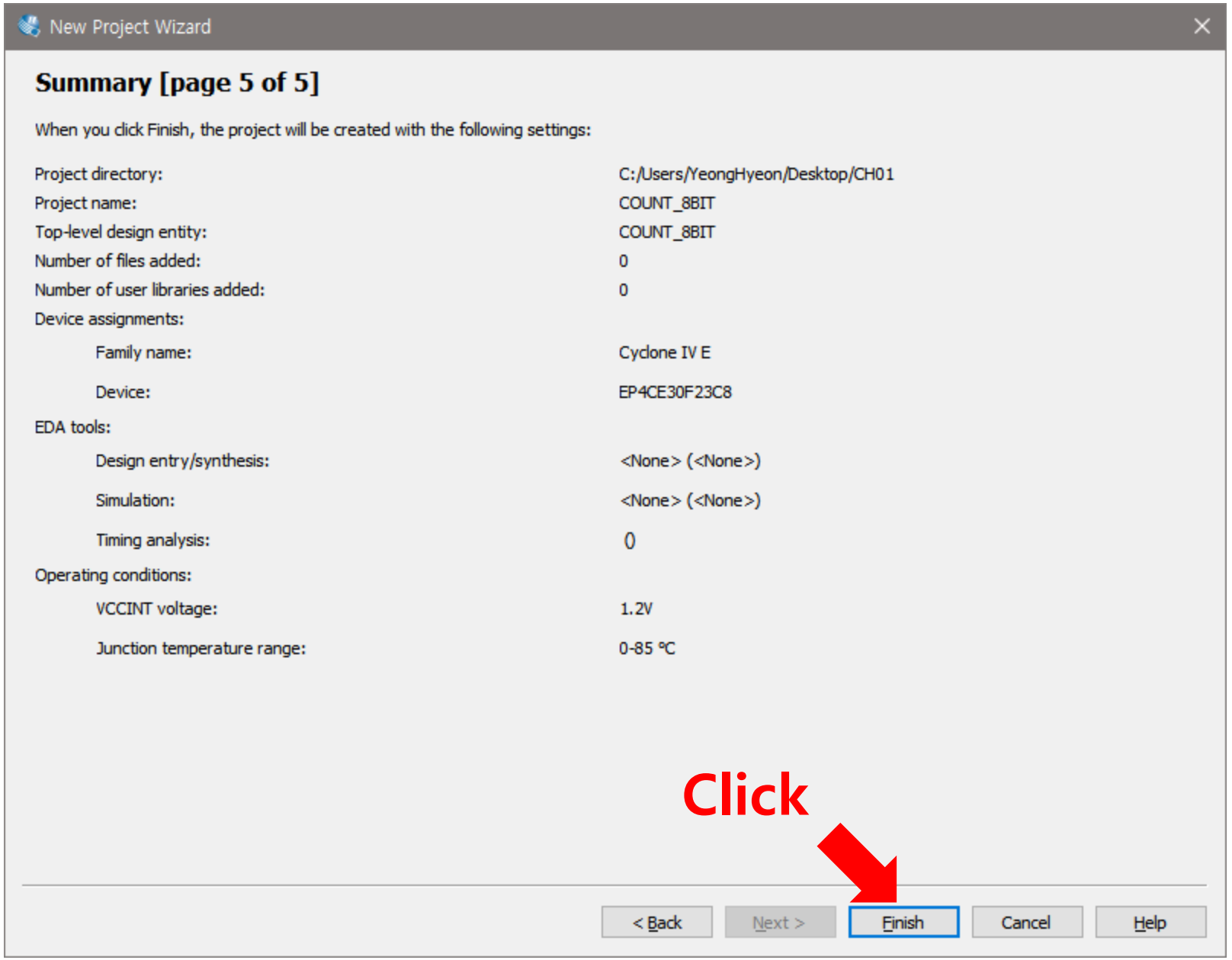

New Project Wizard
Introduction
The New Project Wizard helps you create a new project and preliminary project settings, including the following:
Project name and directory
Name of the top-level design entity
Project files and libraries
Target device family and device
EDA tool settings
You can change the settings for an existing project and specify additional project-wide settings with the Settings command (Assignments menu). You can use the various pages of the Settings dialog box to add functionality to the project.
Click
Don't show me this introduction again
< Back
Next >
Finish
Cancel
Help


New Project Wizard
Directory, Name, Top-Level Entity [page 1 of 5]
What is the working directory for this project?
C:/Users/YeongHyeon/Desktop/CH01
Select
What is the name of this project?
COUNT_8BIT
Fill
What is the name of the top-level design entity for this project? This name is case sensitive and must exactly match the entity name in the design file.
COUNT_8BIT
Fill
Use Existing Project Settings...
Click
< Back
Next >
Finish
Cancel
Help

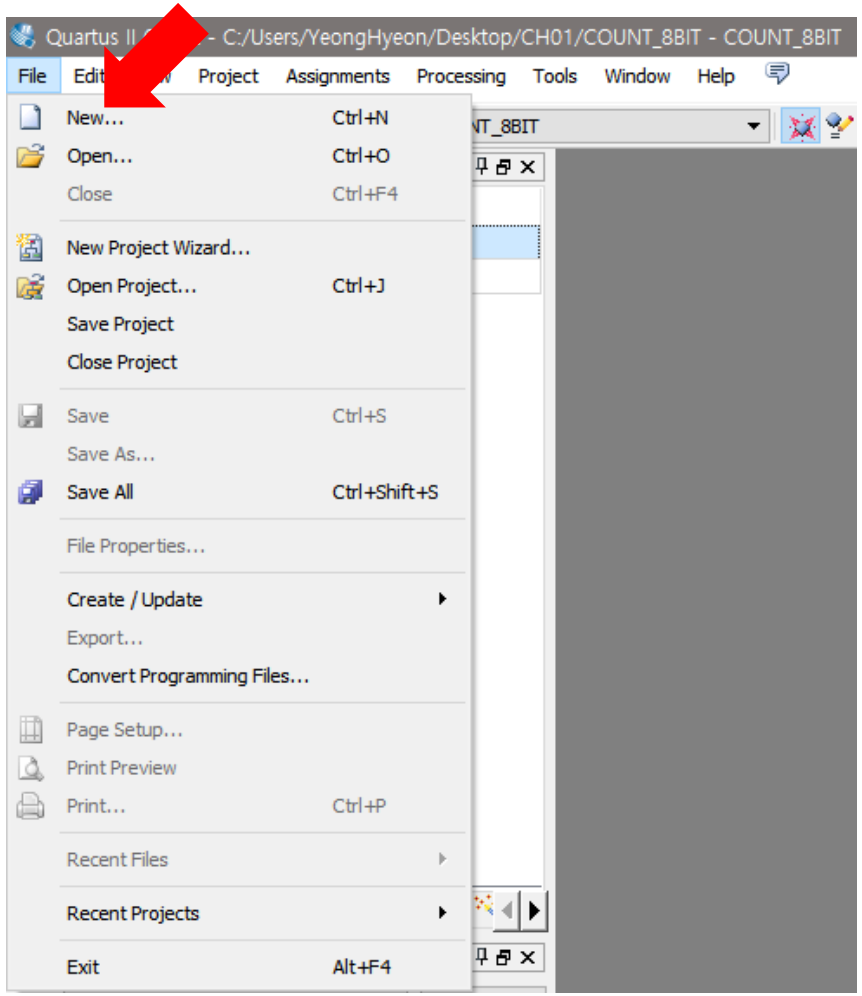

New Project Wizard
Add Files [page 2 of 5]
Select the design files you want to include in the project. Click Add All to add all design files in the project directory to the project.
Note: you can always add design files to the project later.
File name:
...
Add
Add All
Remove
Up
Down
Properties
File Name
Type
Library
Design Entry/Synthesis Tool
HDL Version
Click
Specify the path names of any non-default libraries.
User Libraries...
< Back
Next >
Finish
Cancel
Help


New Project Wizard
Family & Device Settings [page 3 of 5]
Select the family and device you want to target for compilation.
You can install additional device support with the Install Devices command on the Tools menu.
Device family
Family: Cyclone IV E
Select
Devices: All
Target device
Auto device selected by the Fitter
Specific device selected in 'Available devices' list
Other: n/a
Show in 'Available devices' list
Package: Any
Pin count: Any
Speed grade: Any
Name filter:
Show advanced devices
HardCopy compatible only
Available devices:
Name | Core Voltage | LEs | User I/Os | Memory Bits | Embedded multiplier 9-bit ele
EP4CE30F19A7 | 1.2V | 28848 | 193 | 608256 | 132
EP4CE30F23A7 | 1.2V | 28848 | 329 | 608256 | 132
EP4CE30F23C6 | 1.2V | 28848 | 329 | 608256 | 132
EP4CE30F23C7 | 1.2V | 28848 | 329 | 608256 | 132
EP4CE30F23C8 | 1.2V | 28848 | 329 | 608256 | 132
EP4CE30F23C8L | 1.0V | 28848 | 329 | 608256 | 132
Select
Companion device
HardCopy:
Limit DSP & RAM to HardCopy device resources
Click
< Back
Next >
Finish
Cancel
Help

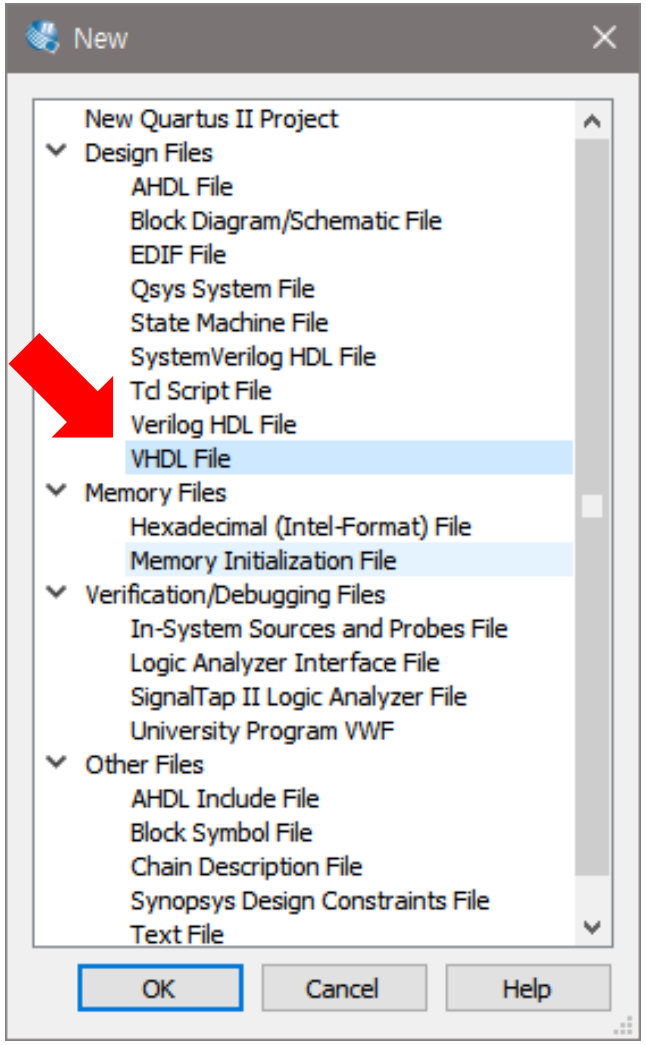

New Project Wizard
EDA Tool Settings [page 4 of 5]
Specify the other EDA tools used with the Quartus II software to develop your project.
EDA tools:
Tool Type
Tool Name
Format(s)
Run Tool Automatically
Design Entry/Synthesis
<None>
<None>
Run this tool automatically to synthesize the current design
Simulation
<None>
<None>
Run gate-level simulation automatically after compilation
Formal Verification
<None>
Board-Level
Timing
<None>
Symbol
<None>
Signal Integrity
<None>
Boundary Scan
<None>
Click
< Back
Next >
Finish
Cancel
Help


New Project Wizard
Summary [page 5 of 5]
When you click Finish, the project will be created with the following settings:
Project directory: C:/Users/YeongHyeon/Desktop/CH01
Project name: COUNT_8BIT
Top-level design entity: COUNT_8BIT
Number of files added: 0
Number of user libraries added: 0
Device assignments:
Family name: Cyclone IV E
Device: EP4CE30F23C8
EDA tools:
Design entry/synthesis: <None> (<None>)
Simulation: <None> (<None>)
Timing analysis: 0
Operating conditions:
VCCINT voltage: 1.2V
Junction temperature range: 0-85 °C
Click
< Back
Next >
Finish
Cancel
Help

Click


Quartus II - C:/Users/YeongHyeon/Desktop/CH01/COUNT_8BIT - COUNT_8BIT
File
Edit
Project
Assignments
Processing
Tools
Window
Help
New... Ctrl+N
Open... Ctrl+O
Close Ctrl+F4
New Project Wizard...
Open Project... Ctrl+J
Save Project
Close Project
Save Ctrl+S
Save As...
Save All Ctrl+Shift+S
File Properties...
Create / Update
Export...
Convert Programming Files...
Page Setup...
Print Preview
Print... Ctrl+P
Recent Files
Recent Projects
Exit Alt+F4

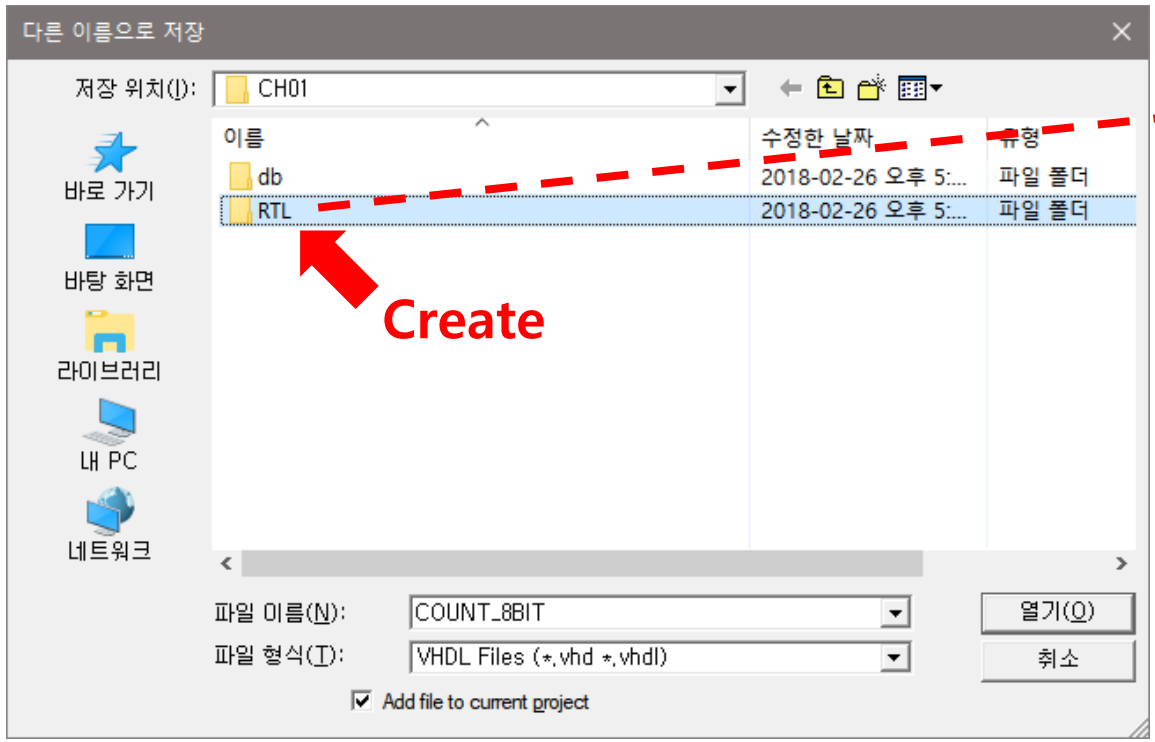
Click

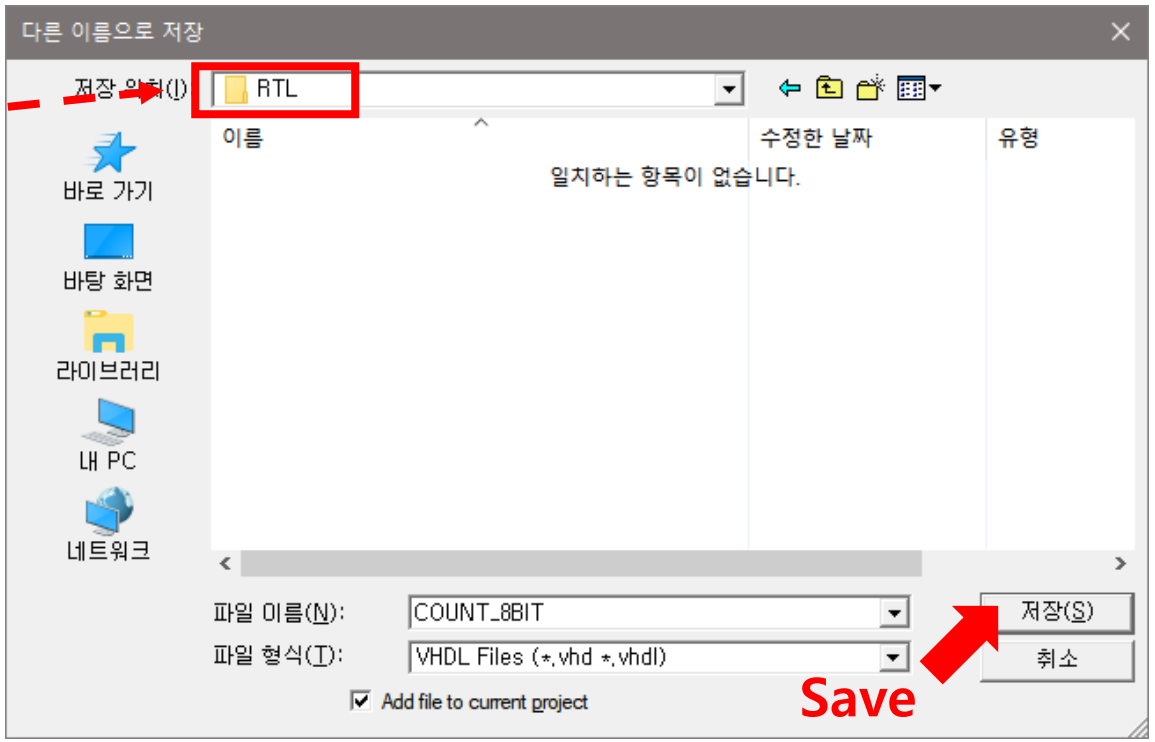

New
New Quartus II Project
Design Files
AHDL File
Block Diagram/Schematic File
EDIF File
Qsys System File
State Machine File
SystemVerilog HDL File
Tcl Script File
Verilog HDL File
VHDL File
Memory Files
Hexadecimal (Intel-Format) File
Memory Initialization File
Verification/Debugging Files
In-System Sources and Probes File
Logic Analyzer Interface File
SignalTap II Logic Analyzer File
University Program VWF
Other Files
AHDL Include File
Block Symbol File
Chain Description File
Synopsys Design Constraints File
Text File
OK
Cancel
Help

Vhdl1.vhd*

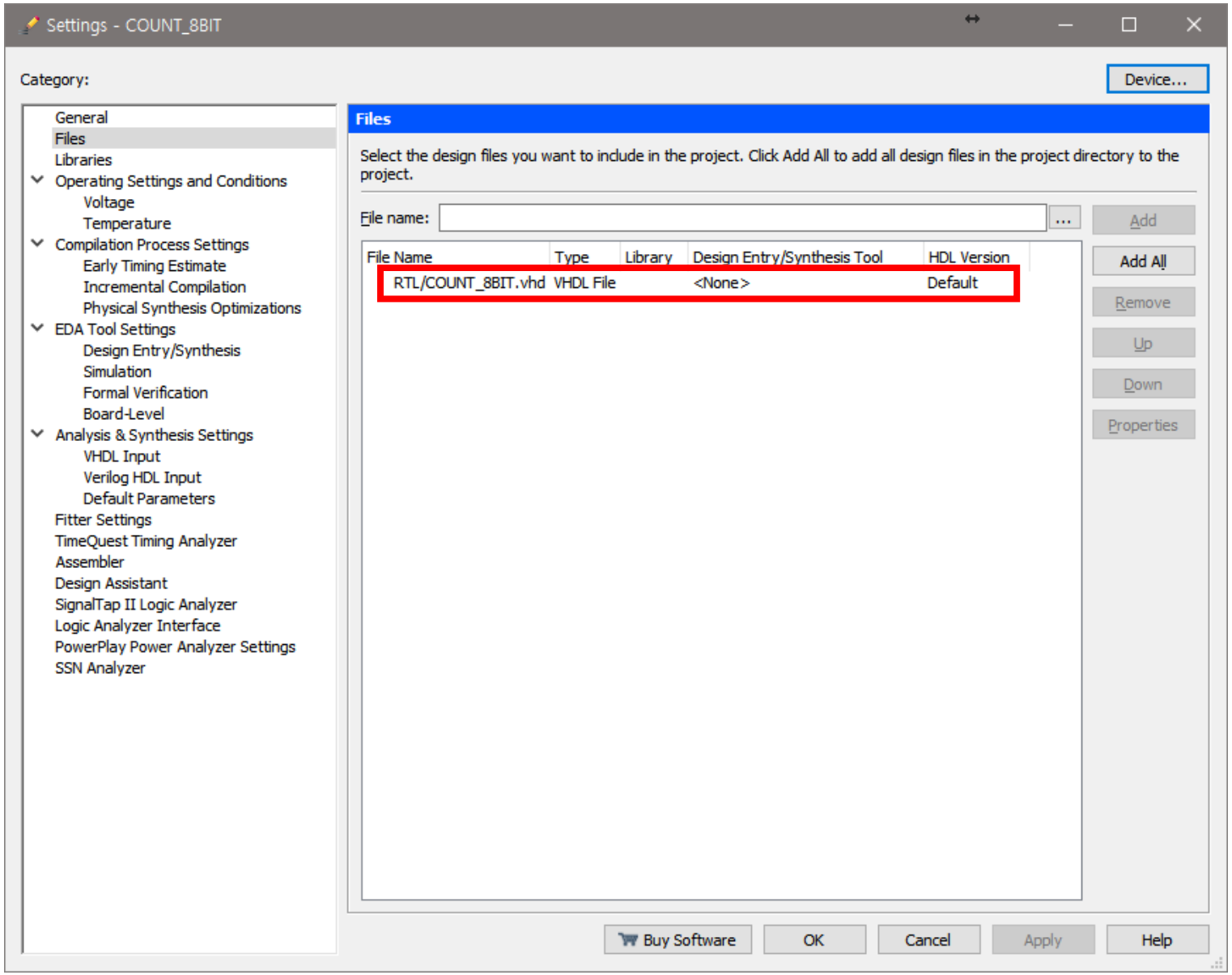
```
1  --COUNT_8BIT.VD
2
3  LIBRARY IEEE;
4  USE IEEE.STD_LOGIC_1164.ALL;
5  USE IEEE.STD_LOGIC_UNSIGNED.ALL;
6
7  ENTITY COUNT_8BIT IS
8  PORT(
9     RESETN:IN STD_LOGIC; --RESET
10    CLK:IN STD_LOGIC; --CLOCK BUTTON
11
12    COUNT_OUT:OUT STD_LOGIC_VECTOR(7 DOWNTO 0)    --LED OUTPUT
13 );
14 END COUNT_8BIT;
15
16 ARCHITECTURE HB OF COUNT_8BIT IS
17
18 SIGNAL CNT_8BIT:STD_LOGIC_VECTOR(7 DOWNTO 0);
19
20 BEGIN
21
22 PROCESS(RESETN, CLK)
23 BEGIN
24    IF RESETN='1' THEN
25       CNT_8BIT<=(OTHERS=>'0');
26    ELSIF CLK'EVENT AND CLK='1' THEN
27       IF CNT_8BIT="11111111" THEN
28          CNT_8BIT<=(OTHERS=>'0');
29       ELSE
30          CNT_8BIT<=CNT_8BIT+1;
31       END IF;
32    END IF;
33 END PROCESS;
34
35 COUNT_OUT<=CNT_8BIT;
36
37 END HB;
```

Ctrl + S

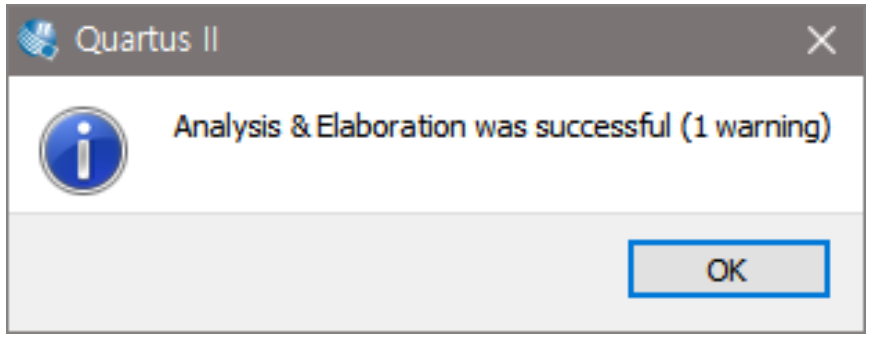

다른 이름으로 저장
저장 위치(I):
CH01
바로 가기
바탕 화면
라이브러리
내 PC
네트워크
이름
수정한 날짜
유형
db
2018-02-26 오후 5:...
파일 폴더
RTL
2018-02-26 오후 5:...
파일 폴더
Create
파일 이름(N):
COUNT_8BIT
파일 형식(T):
VHDL Files (*.vhd *.vhdl)
열기(O)
취소
Add file to current project


다른 이름으로 저장
저장 위치(I):
RTL
바로 가기
바탕 화면
라이브러리
내 PC
네트워크
이름
수정한 날짜
유형
일치하는 항목이 없습니다.
파일 이름(N):
COUNT_8BIT
파일 형식(T):
VHDL Files (*.vhd *.vhdl)
저장(S)
취소
Add file to current project
Save

Project > Add/remove Files in Project



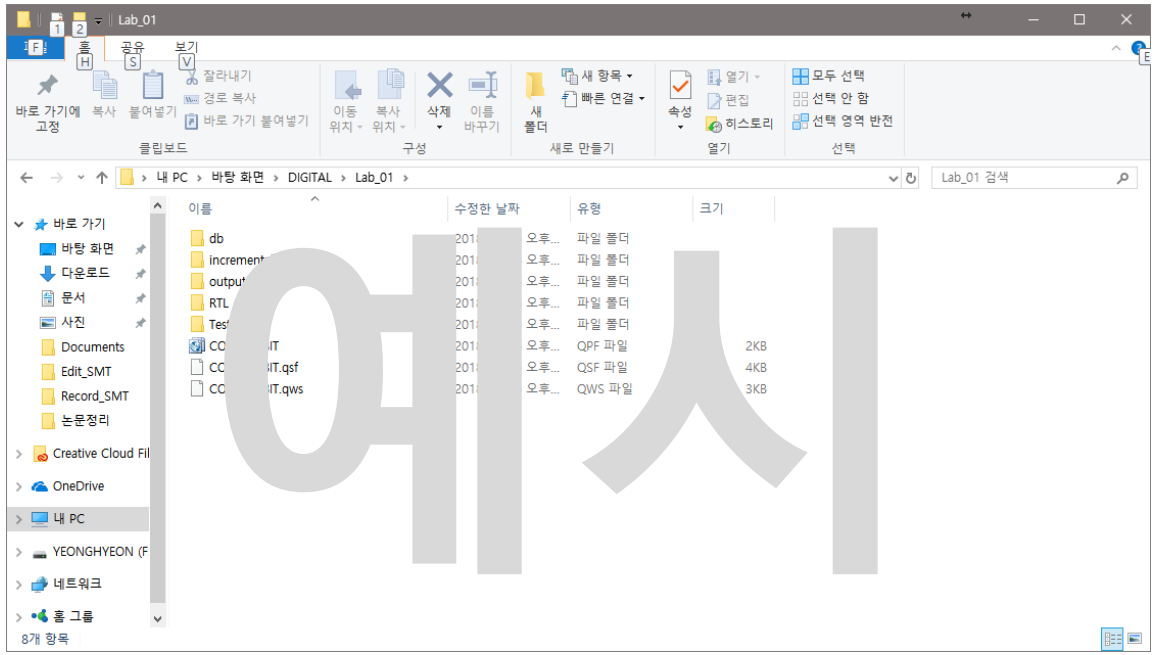
Processing > Start > Start Analysis & Elaboration



Report

결과

- 프로젝트 디렉토리 캡쳐
- 소스코드 첨부 및 설명



예비

- 없음