

# 논리회로 및 실험

4주차

### AND GATE

INPUT		OUTPUT
A	B	A AND B
0	0	0
0	1	0
1	0	0
1	1	1

### OR GATE

INPUT		OUTPUT
A	B	A OR B
0	0	0
0	1	1
1	0	1
1	1	1




### XOR GATE

INPUT		OUTPUT
A	B	A XOR B
0	0	0
0	1	1
1	0	1
1	1	0

```
//GATE.V
```

```
module GATE(  
    A,B,  
    X,Y,Z  
);
```

```
input A,B;  
output X,Y,Z;
```

```
assign X=A  B;  
assign Y=A  B;  
assign Z=A  B;
```

```
endmodule
```

Report

Report not available

Groups

Report

Tasks

Run Anal

Early Pin

Early

Run

Expo

Change

Show

Show

Show

Show

Show

Show

Show

Show

Show

Show

Show

Show

Show

Show

Show

Show

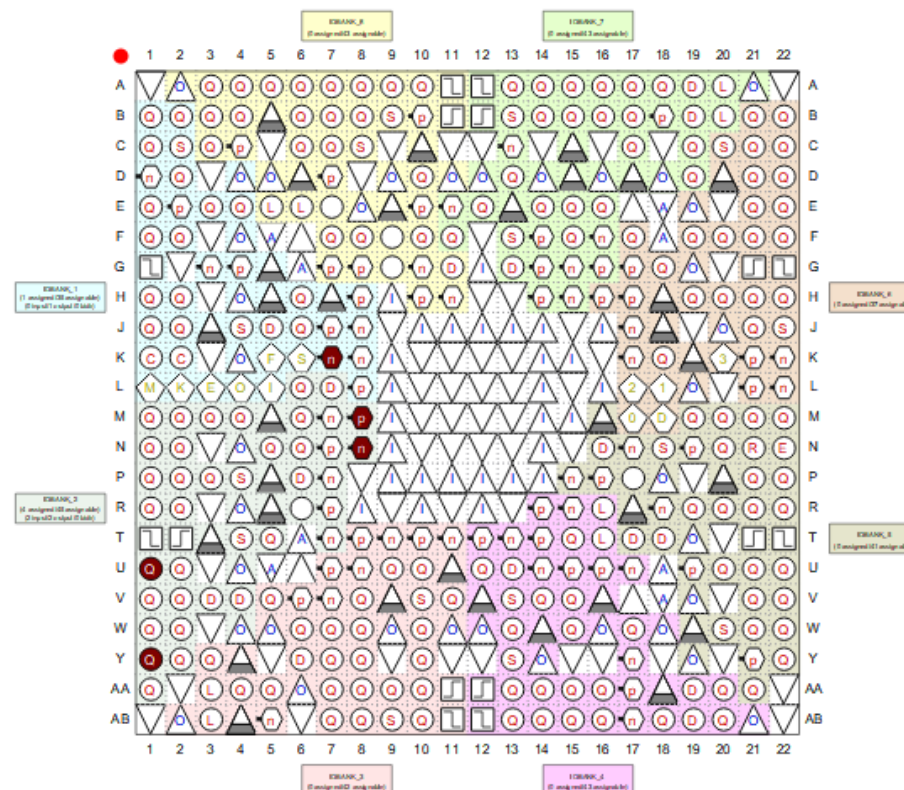
Show

Show

Show

Show

Show

Top View - Wire Bond  
Cyclone IV E - EP4CE30F23C8

Named: \* Filter: Pins: all

Node Name	Direction	Location	I/O Bank	VREF Group	Fitter Location	I/O Standard	Reserved	Current Strength	Slew Rate	Differential Pa
in A	Input	PIN_U1	2	B2_N1	PIN_U1	2.5 V (default)		8mA (default)		
in B	Input	PIN_Y1	2	B2_N2	PIN_Y1	2.5 V (default)		8mA (default)		
out X	Output	PIN_K7	1	B1_N2	PIN_K7	2.5 V (default)		8mA (default)	2 (default)	
out Y	Output	PIN_M8	2	B2_N1	PIN_M8	2.5 V (default)		8mA (default)	2 (default)	
out Z	Output	PIN_N8	2	B2_N2	PIN_N8	2.5 V (default)		8mA (default)	2 (default)	
<<new node>>										

All Pins

