논리회로 및 실험

5주차

NAND GATE

INPUT		OUTPUT
A	B	A NAND B
0	0	1
0	1	1
1	0	1
1	1	0

NOR GATE

INPUT		OUTPUT
A	B	A NOR B
0	0	1
0	1	0
1	0	0
1	1	0

XNOR GATE

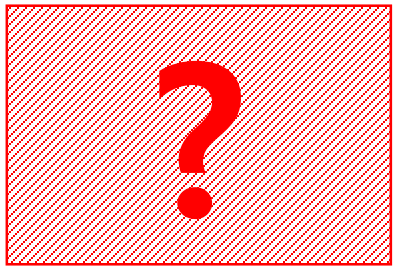
Input		Output
A	B	A XNOR B
0	0	1
0	1	0
1	0	0
1	1	1

```
//GATE.V

module GATE(
        A,B,
        X,Y,Z
);

input A,B;
output X,Y,Z;

assign X=
assign Y=
assign Z=
```




```
;
;
;

endmodule
```