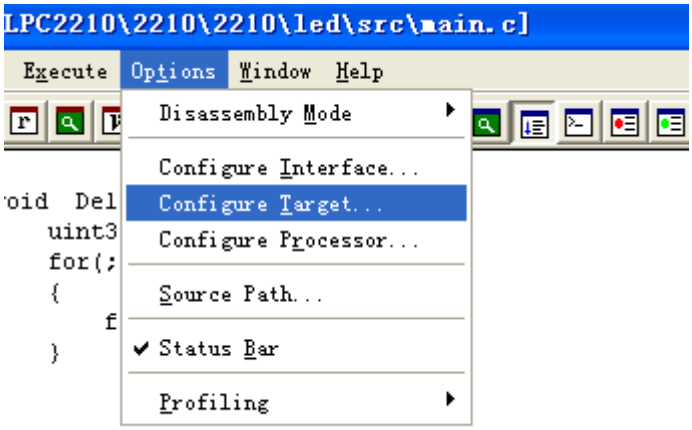
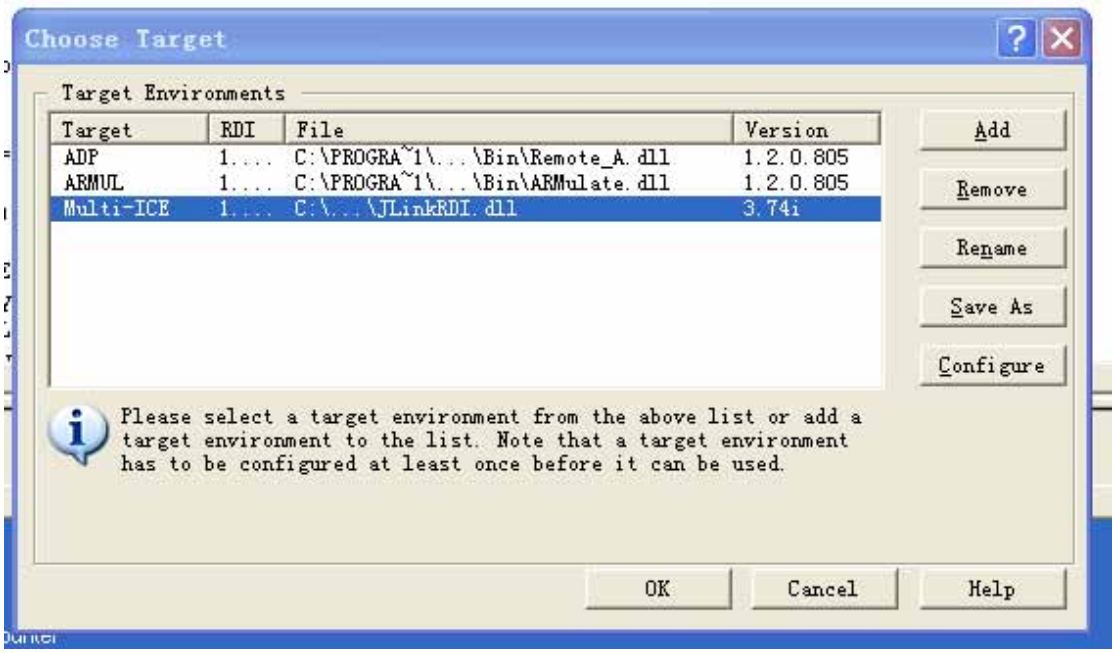
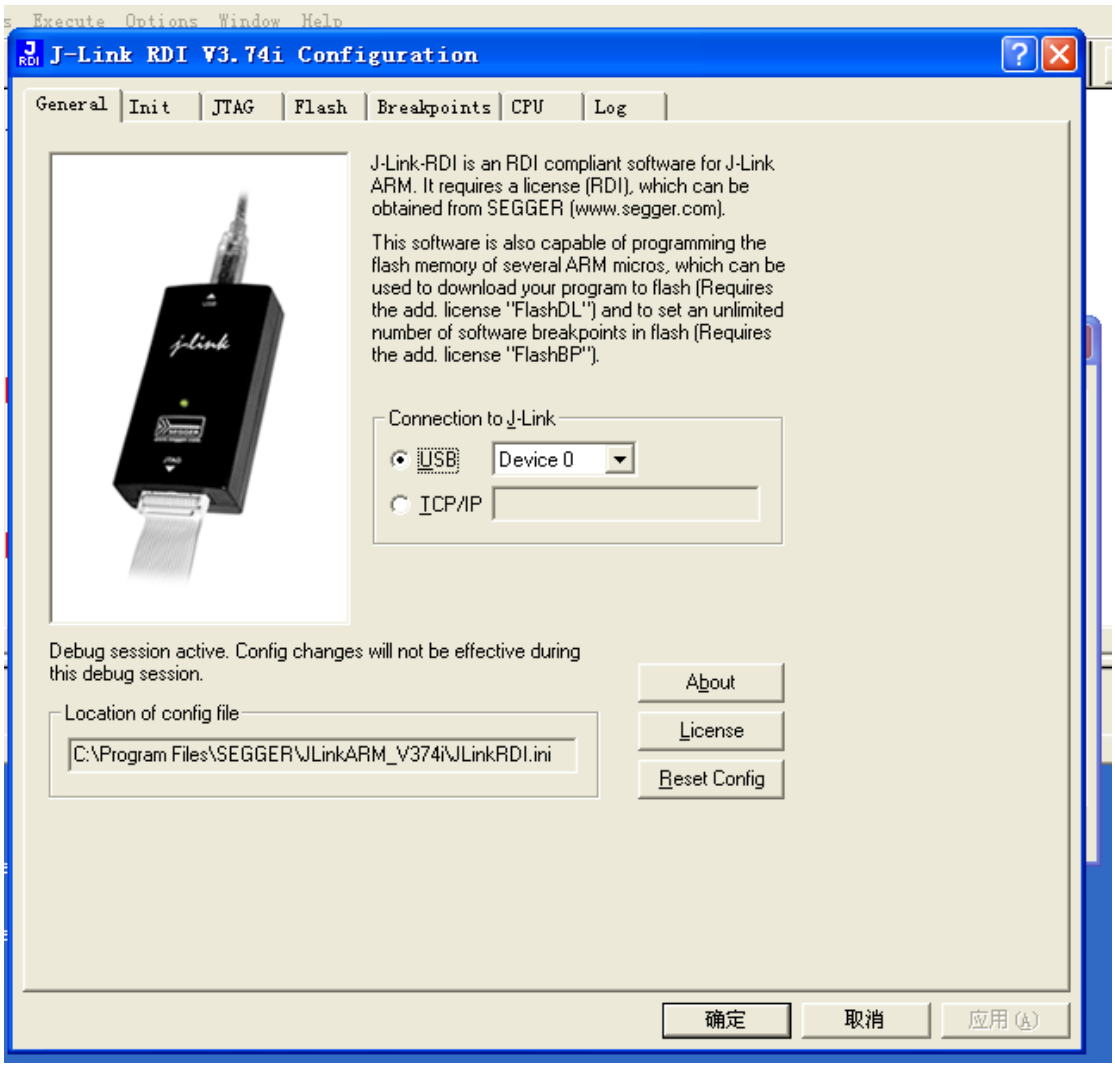
JLINK 在 ADS 下调试 LPC2210 相关说明

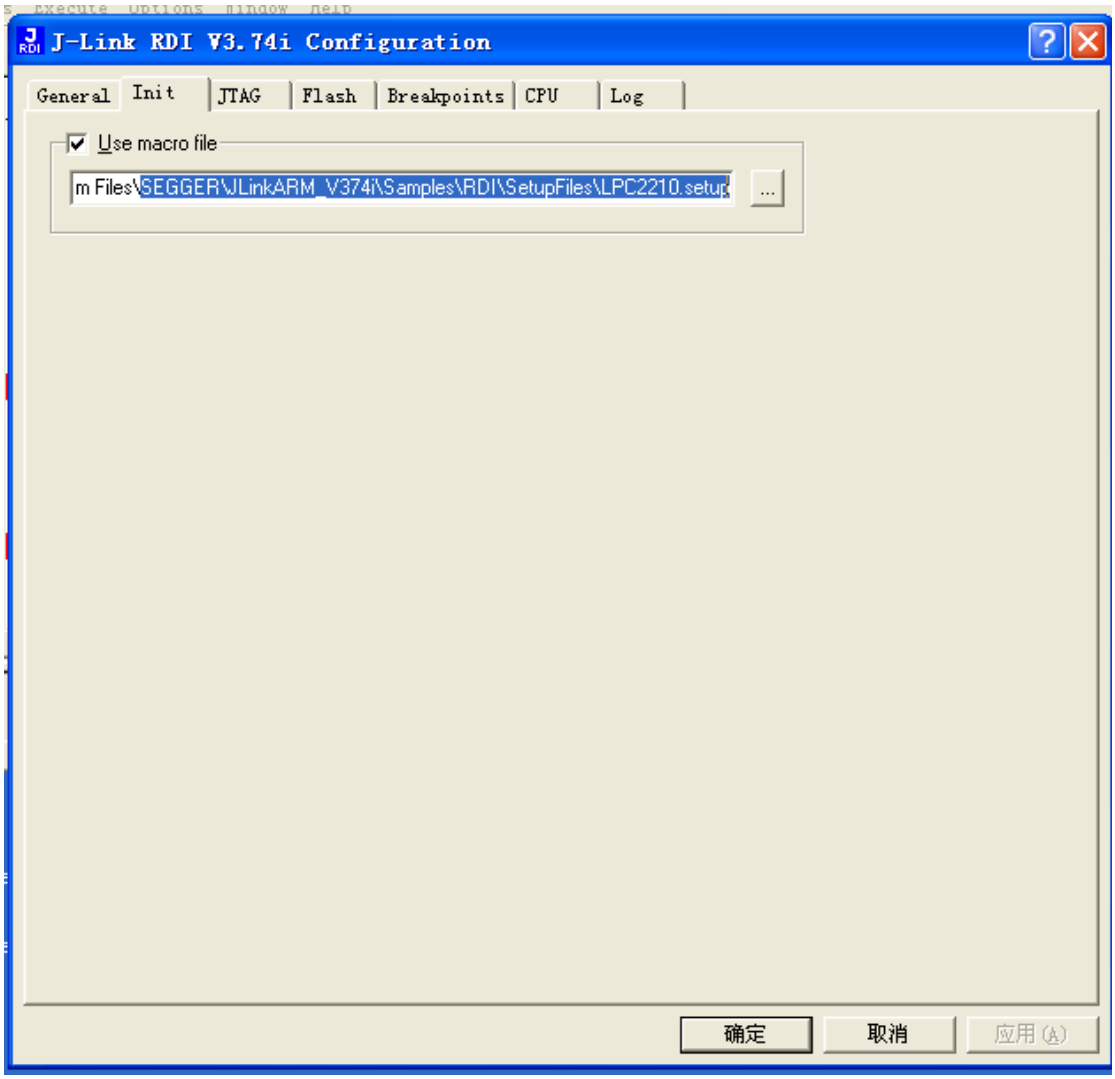
在 RAM 中调试的设置：







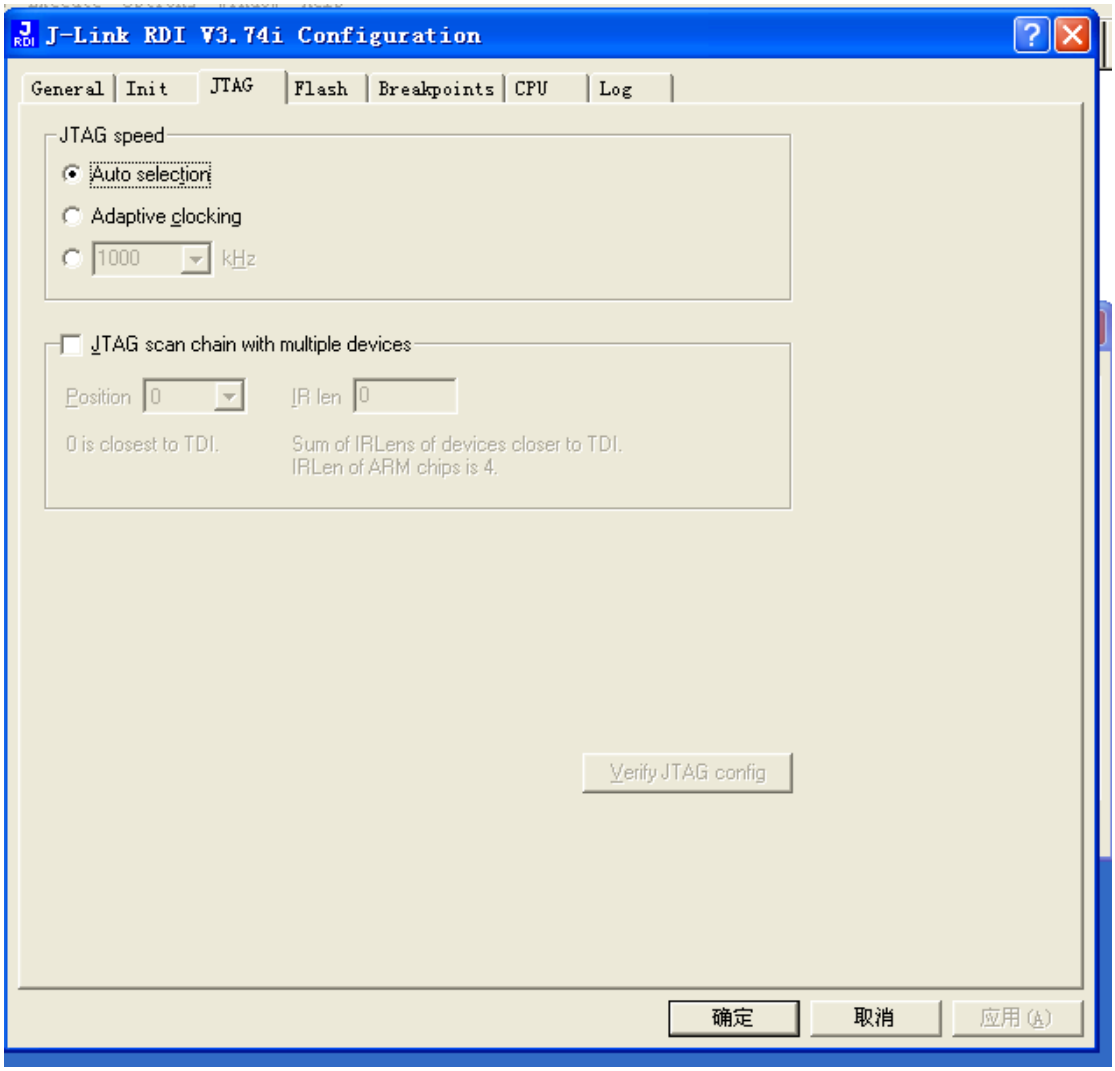
自己写了个 SETUP 文件

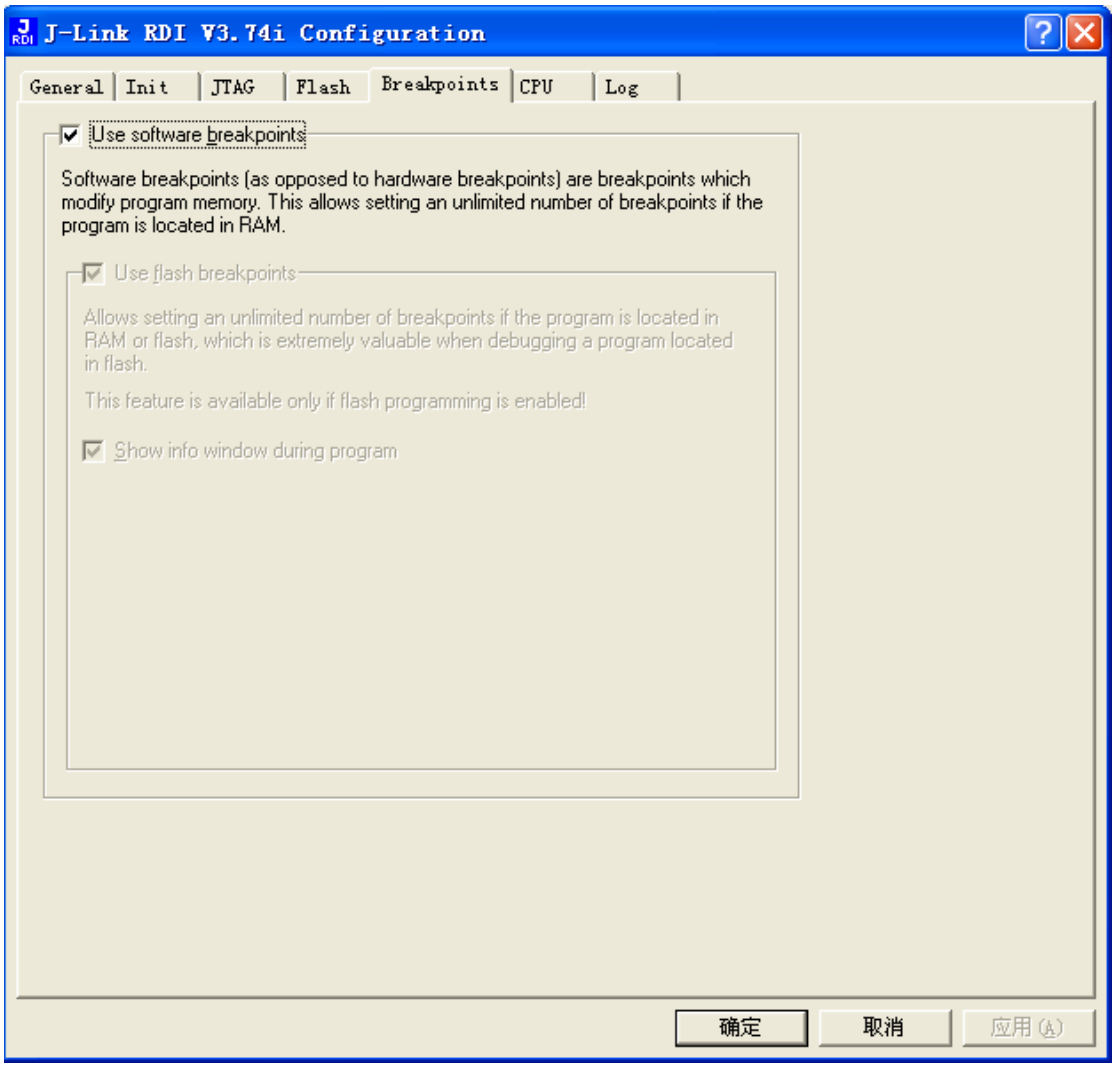


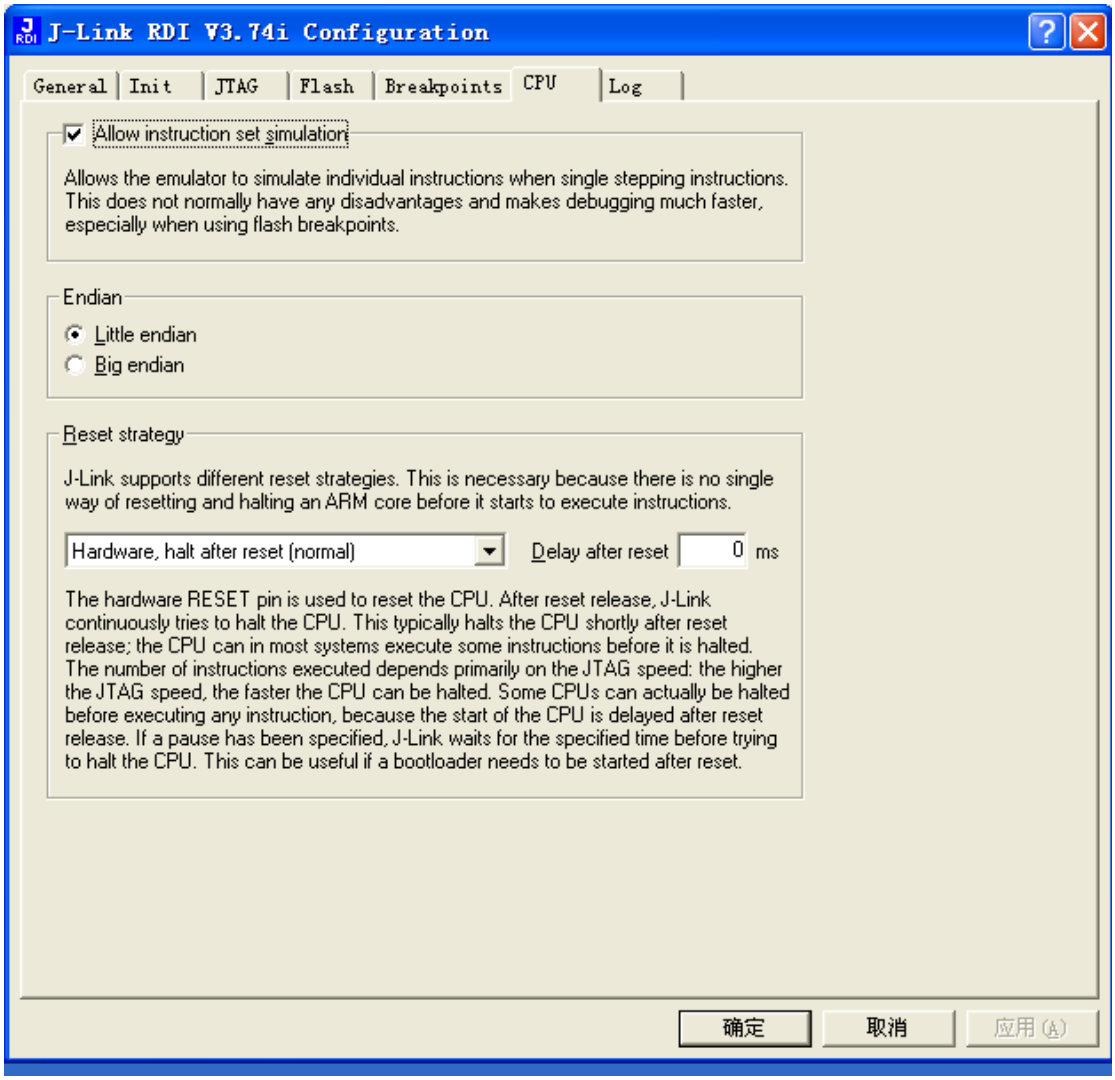
SETUP 的内容如下：

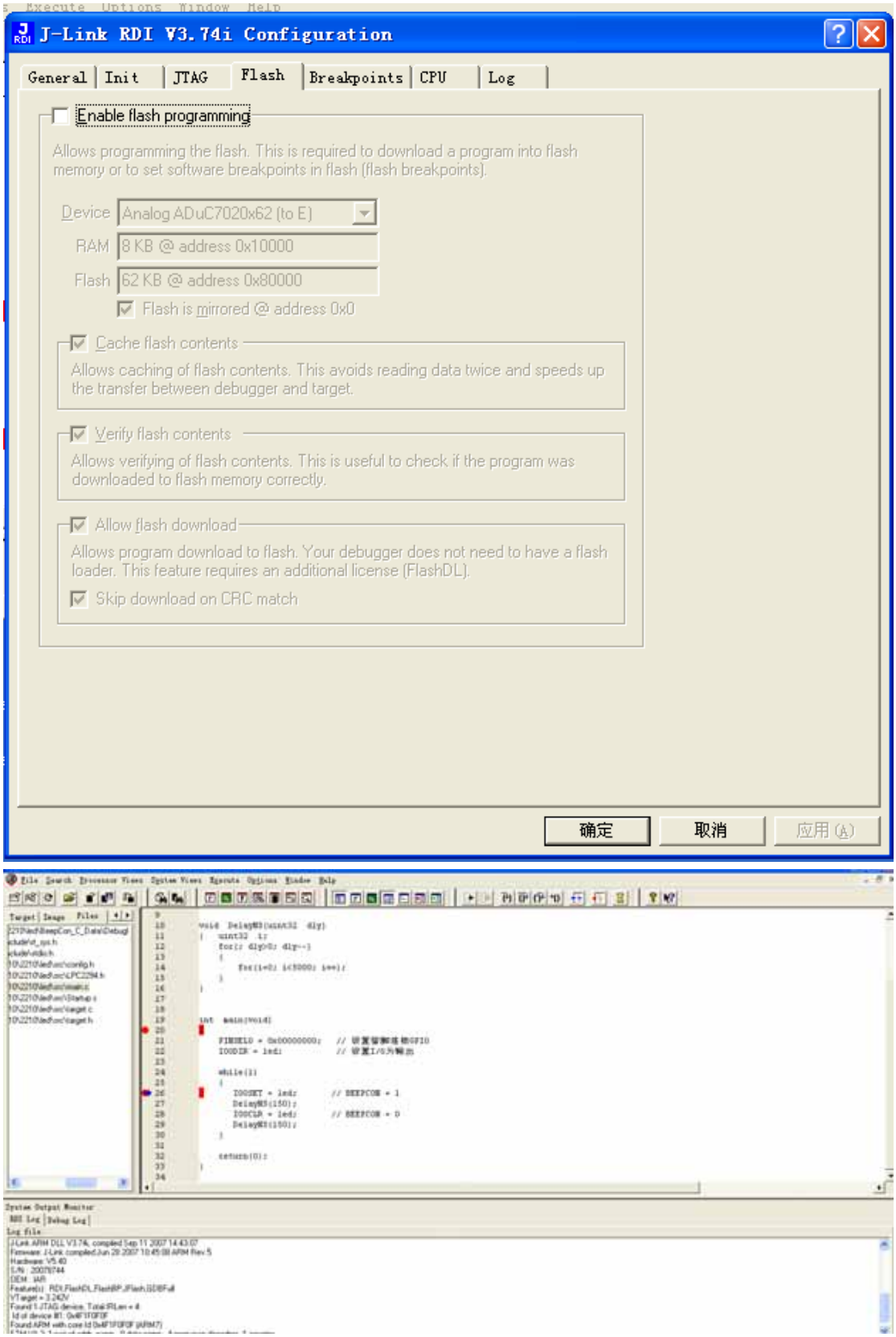
```
SetJTAGSpeed(30);
Reset(0);
DisableChecks();
Write32(0xE01FC080, 0x00000000);          // Disable PLL
Write32(0xE002C014, 0x0F814914);          // PINSEL2
Write32(0xFFE00000, 0x10001460);          // BCFG0
Write32(0xFFE00004, 0x10001460);          // BCFG1
Write32(0xFFE00008, 0x1000FFEF);          // BCFG2
Write32(0xFFE0000C, 0x10001C61);          // BCFG3

EnableChecks();
SetJTAGSpeed(1000);
```

其它选项不用理会，按默认即可。

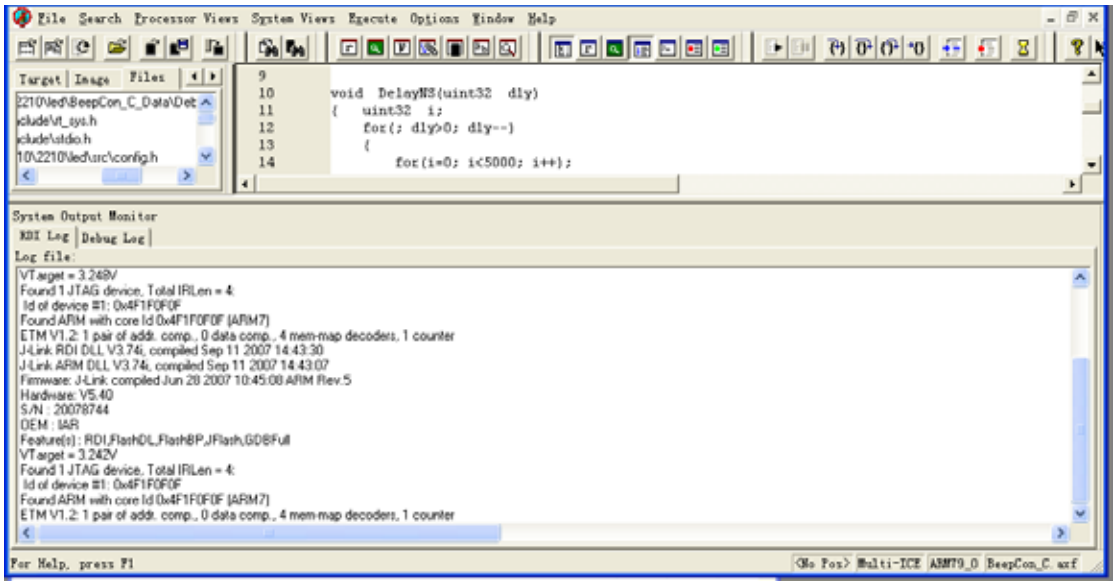



J-Link RDI V3.74i Configuration
General
Init
JTAG
Flash
Breakpoints
CPU
Log
Use software breakpoints
Software breakpoints (as opposed to hardware breakpoints) are breakpoints which modify program memory. This allows setting an unlimited number of breakpoints if the program is located in RAM.
Use flash breakpoints
Allows setting an unlimited number of breakpoints if the program is located in RAM or flash, which is extremely valuable when debugging a program located in flash.
This feature is available only if flash programming is enabled!
Show info window during program
确定
取消
应用(A)


J-Link RDI V3.74i Configuration
General
Init
JTAG
Flash
Breakpoints
CPU
Log
Allow instruction set simulation
Allows the emulator to simulate individual instructions when single stepping instructions. This does not normally have any disadvantages and makes debugging much faster, especially when using flash breakpoints.
Endian
Little endian
Big endian
Reset strategy
J-Link supports different reset strategies. This is necessary because there is no single way of resetting and halting an ARM core before it starts to execute instructions.
Hardware, halt after reset (normal)
Delay after reset
0
ms
The hardware RESET pin is used to reset the CPU. After reset release, J-Link continuously tries to halt the CPU. This typically halts the CPU shortly after reset release; the CPU can in most systems execute some instructions before it is halted. The number of instructions executed depends primarily on the JTAG speed: the higher the JTAG speed, the faster the CPU can be halted. Some CPUs can actually be halted before executing any instruction, because the start of the CPU is delayed after reset release. If a pause has been specified, J-Link waits for the specified time before trying to halt the CPU. This can be useful if a bootloader needs to be started after reset.
确定
取消
应用 (A)


Execute Options Window Help
J-Link RDI V3.74i Configuration
General
Init
JTAG
Flash
Breakpoints
CPU
Log
Enable flash programming
Allows programming the flash. This is required to download a program into flash memory or to set software breakpoints in flash (flash breakpoints).
Device
Analog ADuC7020x62 (to E)
RAM
8 KB @ address 0x10000
Flash
62 KB @ address 0x80000
Flash is mirrored @ address 0x0
Cache flash contents
Allows caching of flash contents. This avoids reading data twice and speeds up the transfer between debugger and target.
Verify flash contents
Allows verifying of flash contents. This is useful to check if the program was downloaded to flash memory correctly.
Allow flash download
Allows program download to flash. Your debugger does not need to have a flash loader. This feature requires an additional license (FlashDL).
Skip download on CRC match
确定
取消
应用 (A)

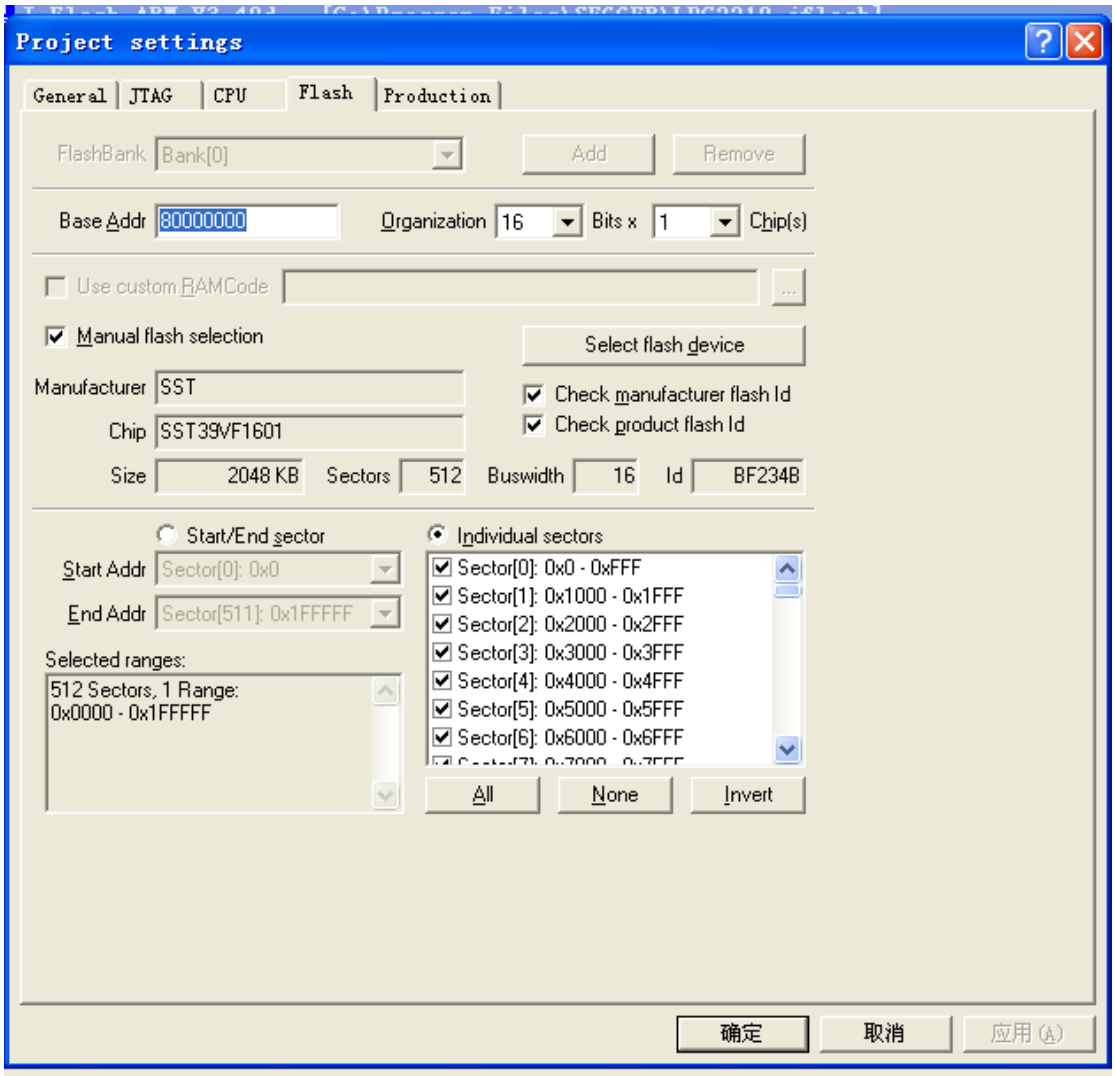
调试信息：

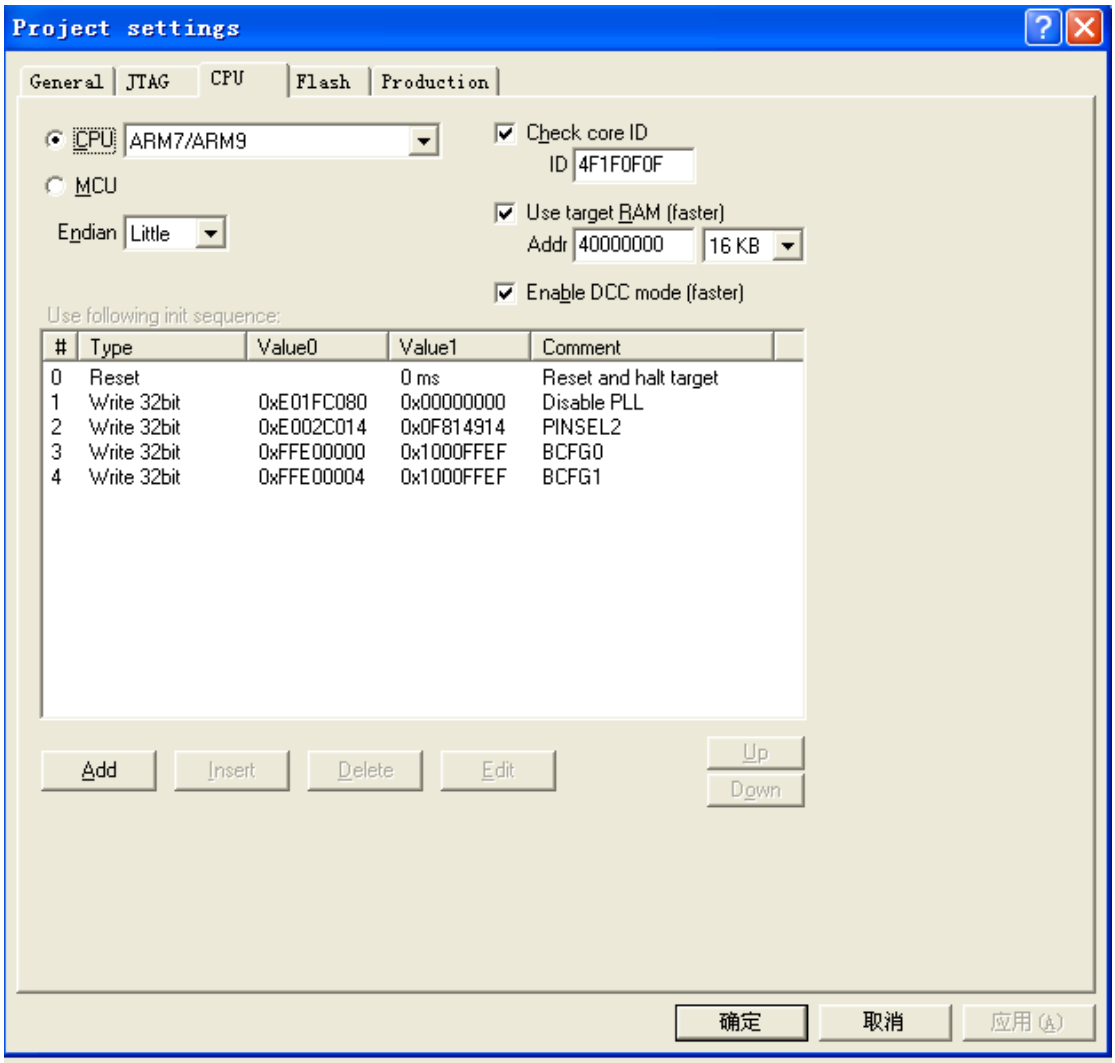


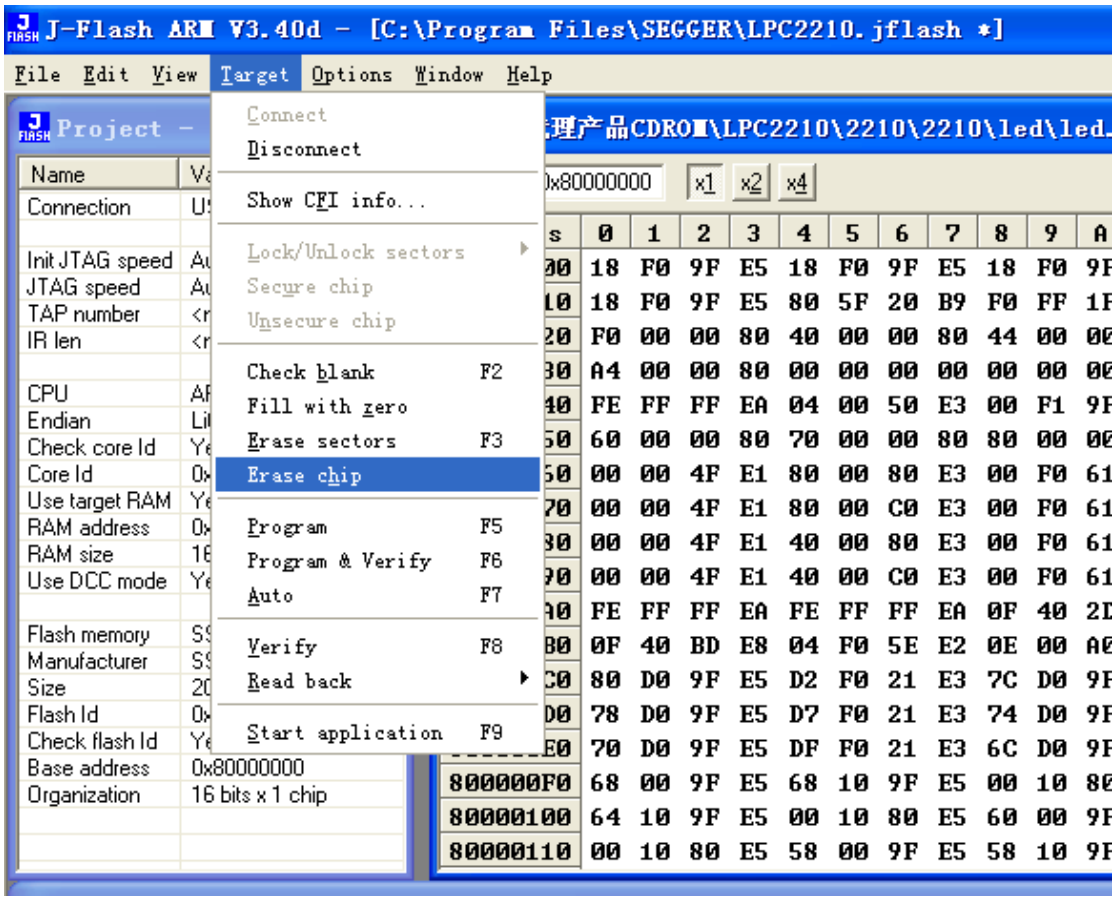
ARM RDI 1.5.1 -> ASYNC RDI Protocol Converter ADS v1.2 [Build number 805]. Copyright (c) ARM Limited 2001.
J-Link RDI DLL V3.74i, compiled Sep 11 2007 14:43:30
J-Link ARM DLL V3.74i, compiled Sep 11 2007 14:43:07
Firmware: J-Link compiled Jun 28 2007 10:45:08 ARM Rev.5
Hardware: V5.40
S/N : 20078744
OEM : IAR
Feature(s) : RDI,FlashDL,FlashBP,JFlash,GDBFull
VTarget = 3.248V
Found 1 JTAG device, Total IRLen = 4:
  Id of device #1: 0x4F1F0F0F
Found ARM with core Id 0x4F1F0F0F (ARM7)
ETM V1.2: 1 pair of addr. comp., 0 data comp., 4 mem-map decoders, 1 counter
J-Link RDI DLL V3.74i, compiled Sep 11 2007 14:43:30
J-Link ARM DLL V3.74i, compiled Sep 11 2007 14:43:07
Firmware: J-Link compiled Jun 28 2007 10:45:08 ARM Rev.5
Hardware: V5.40
S/N : 20078744
OEM : IAR
Feature(s) : RDI,FlashDL,FlashBP,JFlash,GDBFull
VTarget = 3.242V
Found 1 JTAG device, Total IRLen = 4:
  Id of device #1: 0x4F1F0F0F
Found ARM with core Id 0x4F1F0F0F (ARM7)
ETM V1.2: 1 pair of addr. comp., 0 data comp., 4 mem-map decoders, 1 counter

FLASH 烧写

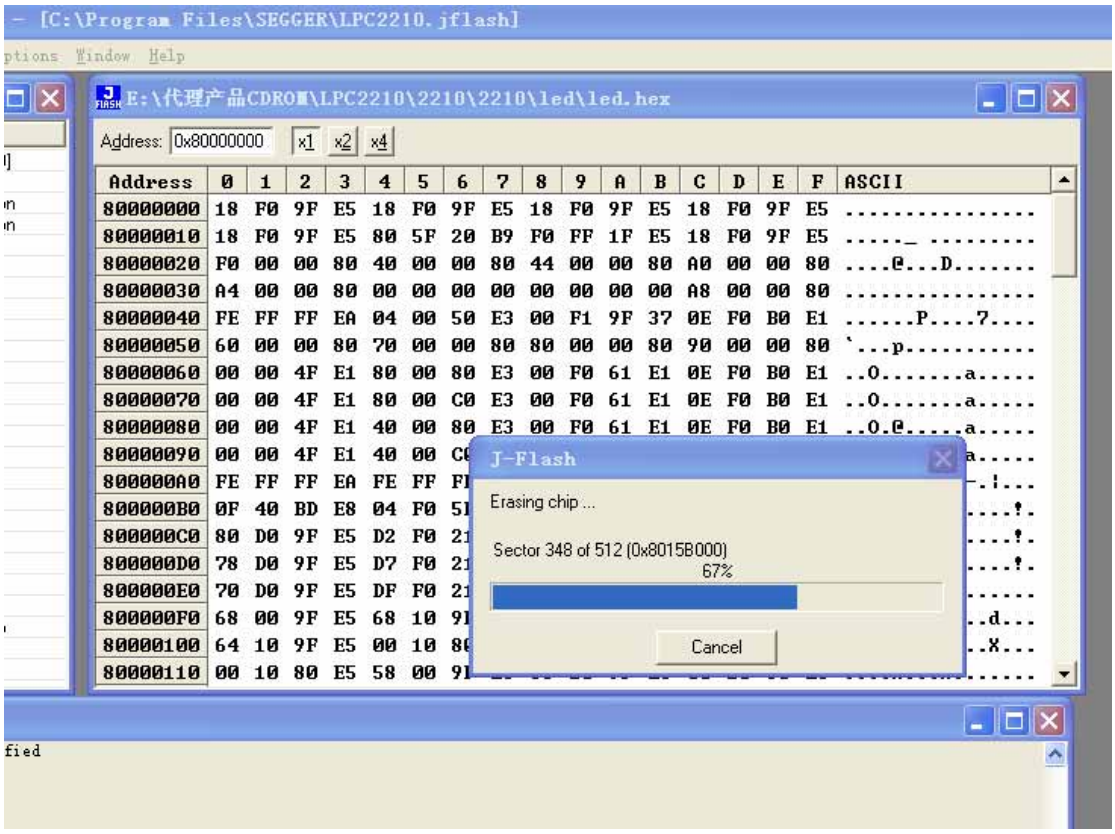
对于 FLASH 的烧录 SST39VF1601 系列建议用 Setup_JLinkARM_V340d.zip 来烧录；较为稳定，在新版本的 Setup_JLinkARM 对 SST 的 FLASH 算法有改变，其它的不会。

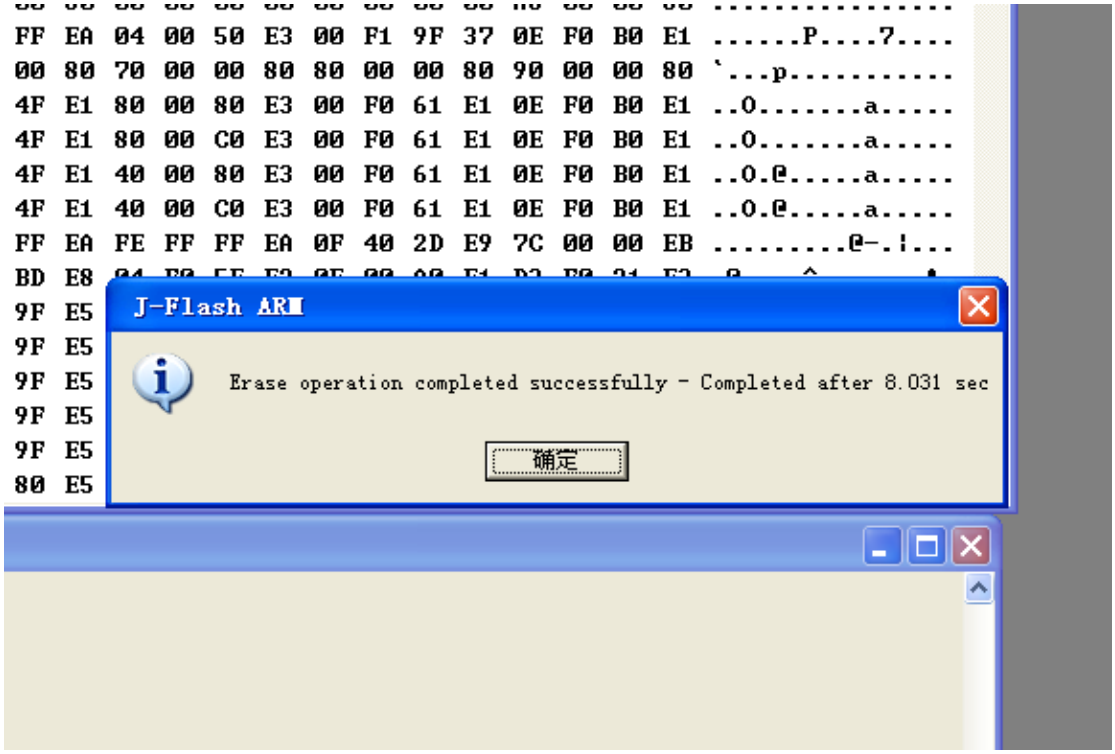


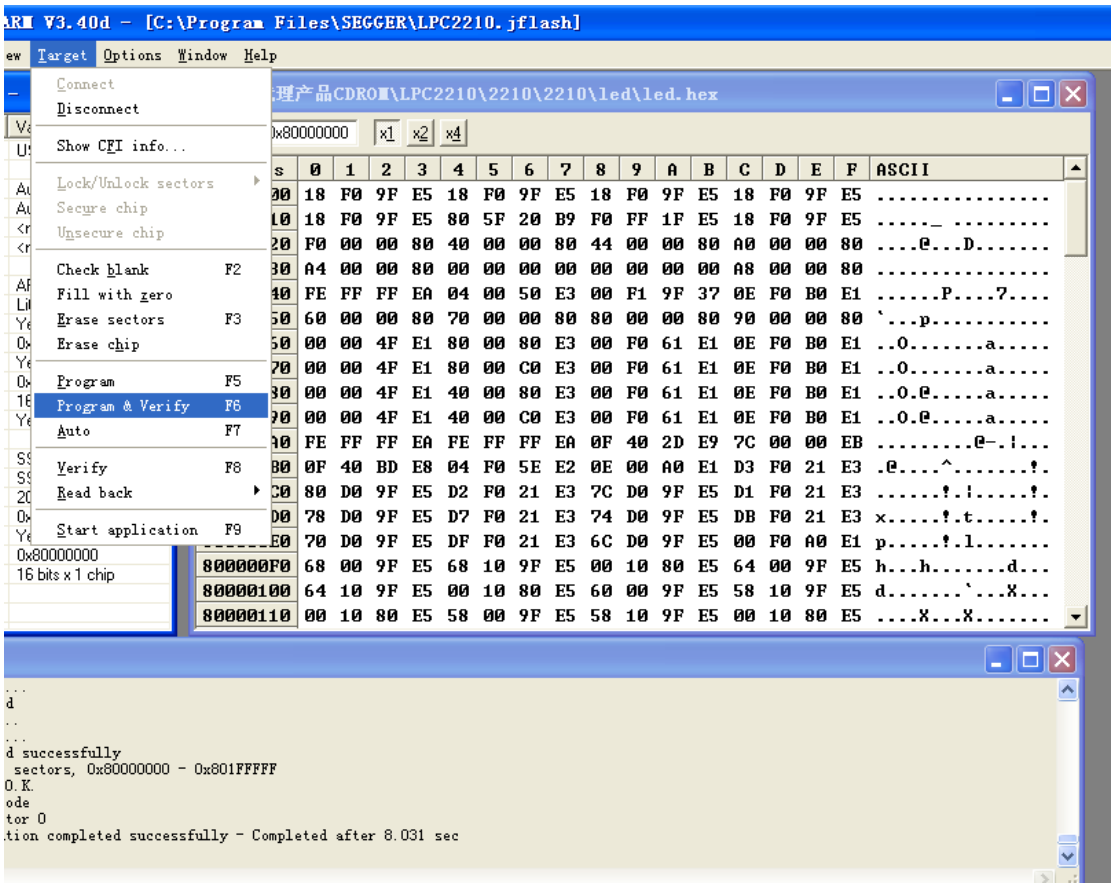

Project settings
General
JTAG
CPU
Flash
Production
CPU
ARM7/ARM9
MCU
Endian
Little
Check core ID
ID
4F1F0F0F
Use target RAM (faster)
Addr
40000000
16 KB
Enable DCC mode (faster)
Use following init sequence:
Type Value0 Value1 Comment
0 Reset 0 ms Reset and halt target
1 Write 32bit 0xE01FC080 0x00000000 Disable PLL
2 Write 32bit 0xE002C014 0x0F814914 PINSEL2
3 Write 32bit 0xFFE00000 0x1000FFEF BCFG0
4 Write 32bit 0xFFE00004 0x1000FFEF BCFG1
Add
Insert
Delete
Edit
Up
Down
确定
取消
应用 (A)

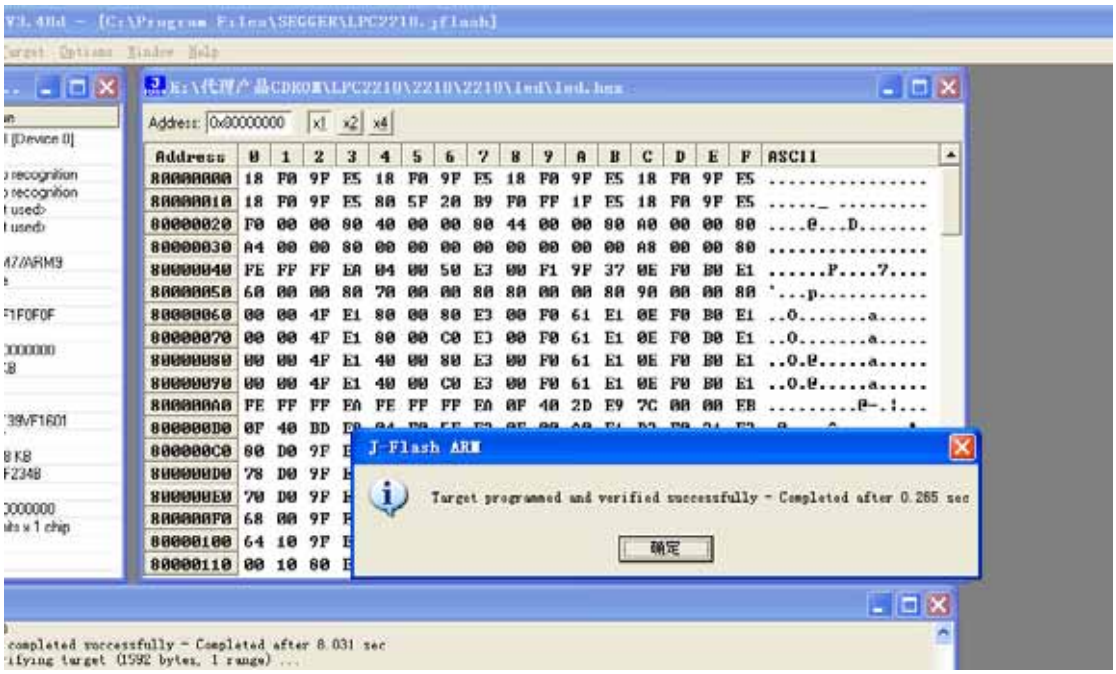

J-Flash ARM V3.40d - [C:\Program Files\SEGGER\LPC2210.jflash *]
File Edit View Target Options Window Help
Project
Connect
Disconnect
Show CFI info...
Lock/Unlock sectors
Secure chip
Unsecure chip
Check blank F2
Fill with zero
Erase sectors F3
Erase chip
Program F5
Program & Verify F6
Auto F7
Verify F8
Read back
Start application F9
Name
Connection
Init JTAG speed
JTAG speed
TAP number
IR len
CPU
Endian
Check core Id
Core Id
Use target RAM
RAM address
RAM size
Use DCC mode
Flash memory
Manufacturer
Size
Flash Id
Check flash Id
Base address 0x80000000
Organization 16 bits x 1 chip
0x80000000
x1 x2 x4

接下来擦除 FLASH


E:\代理产品CDROM\LPC2210\2210\2210\led\led.hex
Address: 0x80000000
x1 x2 x4
J-Flash
Erasing chip ...
Sector 348 of 512 (0x8015B000)
67%
Cancel


J-Flash ARM
Erase operation completed successfully - Completed after 8.031 sec
确定

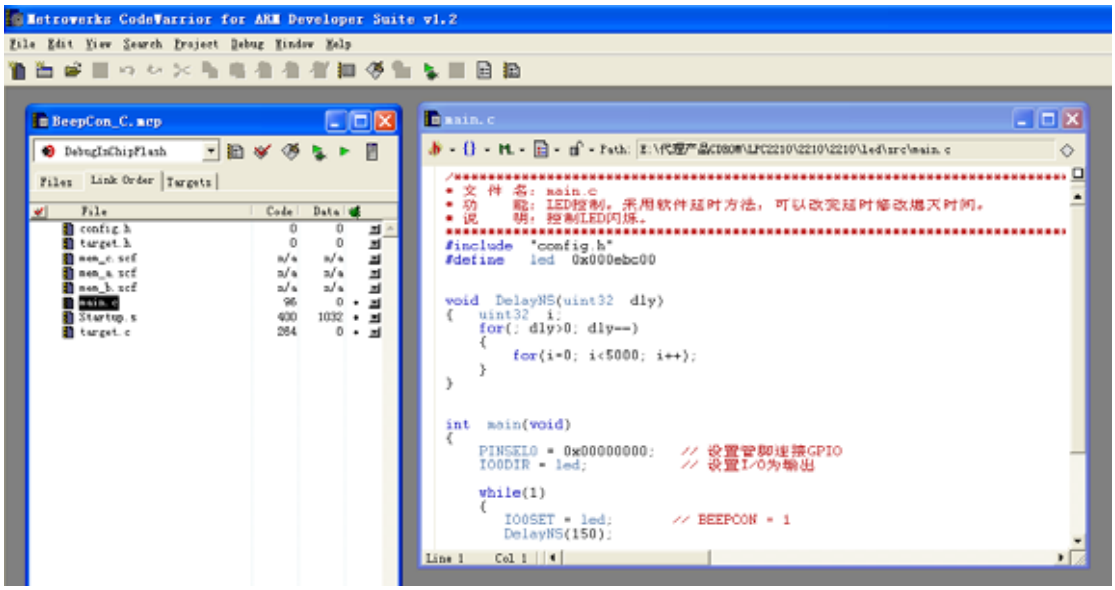

ARM V3.40d - [C:\Program Files\SEGGER\LPC2210.jflash]
Target Options Window Help
Connect
Disconnect
Show CFI info...
Lock/Unlock sectors
Secure chip
Unsecure chip
Check blank F2
Fill with zero
Erase sectors F3
Erase chip
Program F5
Program & Verify F6
Auto F7
Verify F8
Read back
Start application F9
0x80000000
16 bits x 1 chip
d successfully
sectors, 0x80000000 - 0x801FFFFF
O.K.
ode
tor 0
tion completed successfully - Completed after 8.031 sec



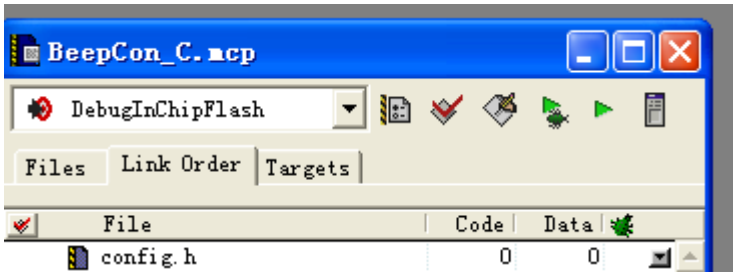
烧录一闪而过…….

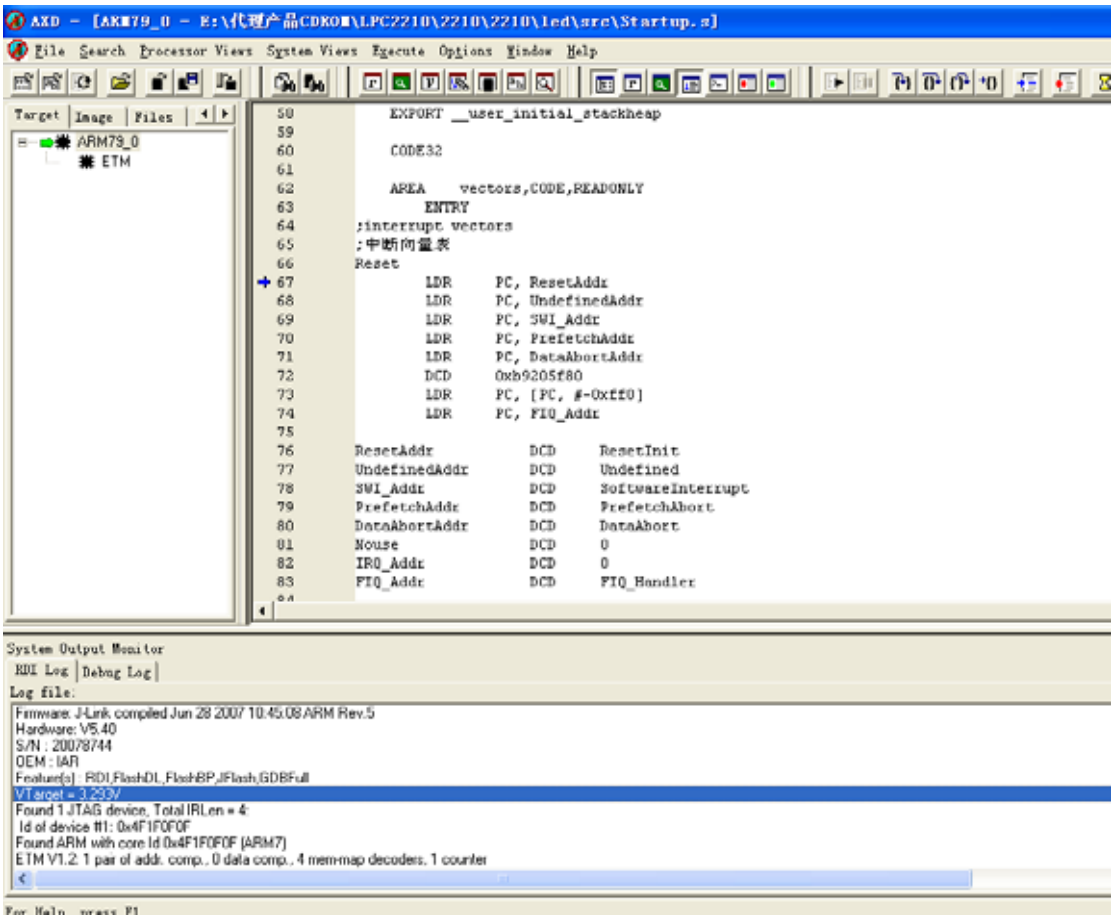
FLASH 调试也是同理，但先要用 JFLASH 烧录 FLASH 然后再调试。
和 RAM 差不多。
只是入口不同。。。

打开工程：

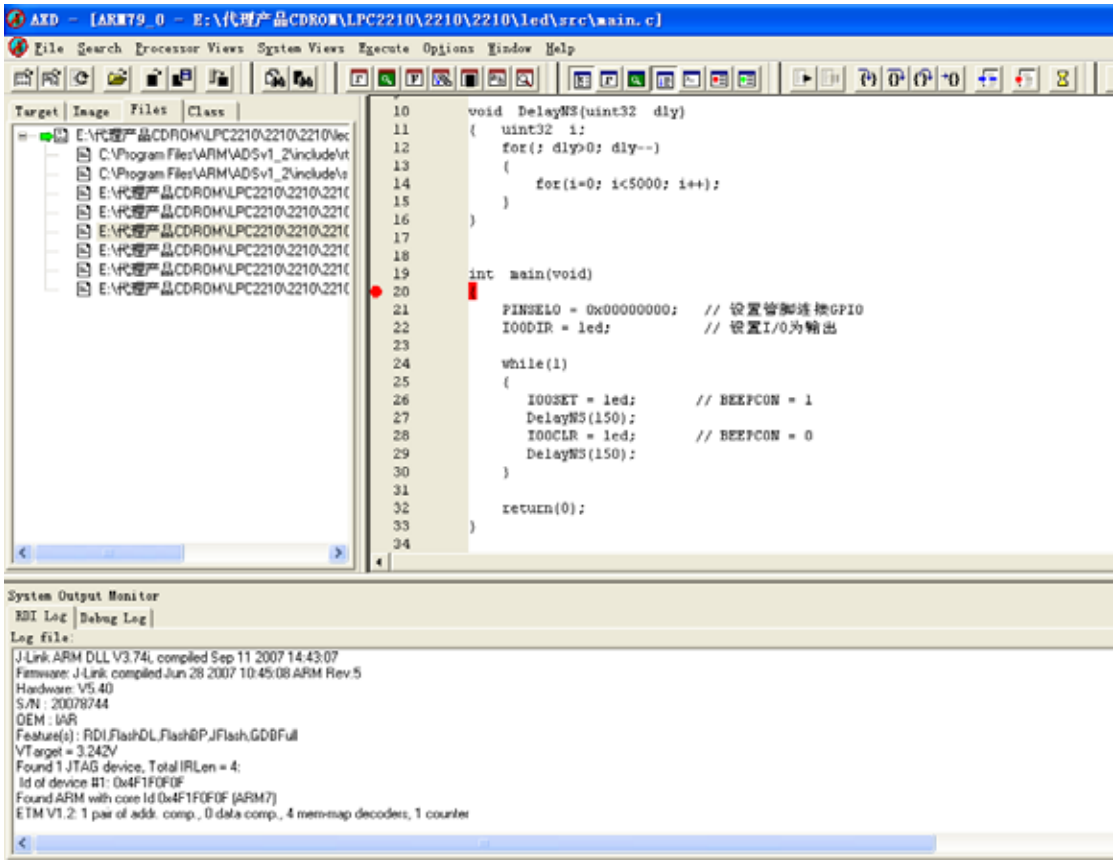

Metrowerks CodeWarrior for ARM Developer Suite v1.2
File Edit View Search Project Debug Window Help
BeepCon_C.mcp
DebugInChipFlash
Files Link Order Targets
File Code Data
config.h 0 0
target.h 0 0
mem_c.scf n/a n/a
mem_a.scf n/a n/a
mem_b.scf n/a n/a
main.c 96 0
Startup.s 400 1032
target.c 284 0
main.c
Path: E:\代理产品\ARM\LPC2210\2210\2210\led\src\main.c
/*****
* 文 件 名: main.c
* 功 能: LED控制，采用软件延时方法，可以改变延时修改熄灭时间。
* 说 明: 控制LED闪烁。
*****/
#include "config.h"
#define led 0x000ebc00
void DelayNS(uint32 dly)
{ uint32 i;
for(; dly>0; dly--)
{
for(i=0; i<5000; i++);
}
}
int main(void)
{
PINSEL0 = 0x00000000; // 设置管脚连接GPIO
IO0DIR = led; // 设置I/O为输出
while(1)
{
IO0SET = led; // BEEPCON = 1
DelayNS(150);
Line 1 Col 1

选择 FLASH 调试

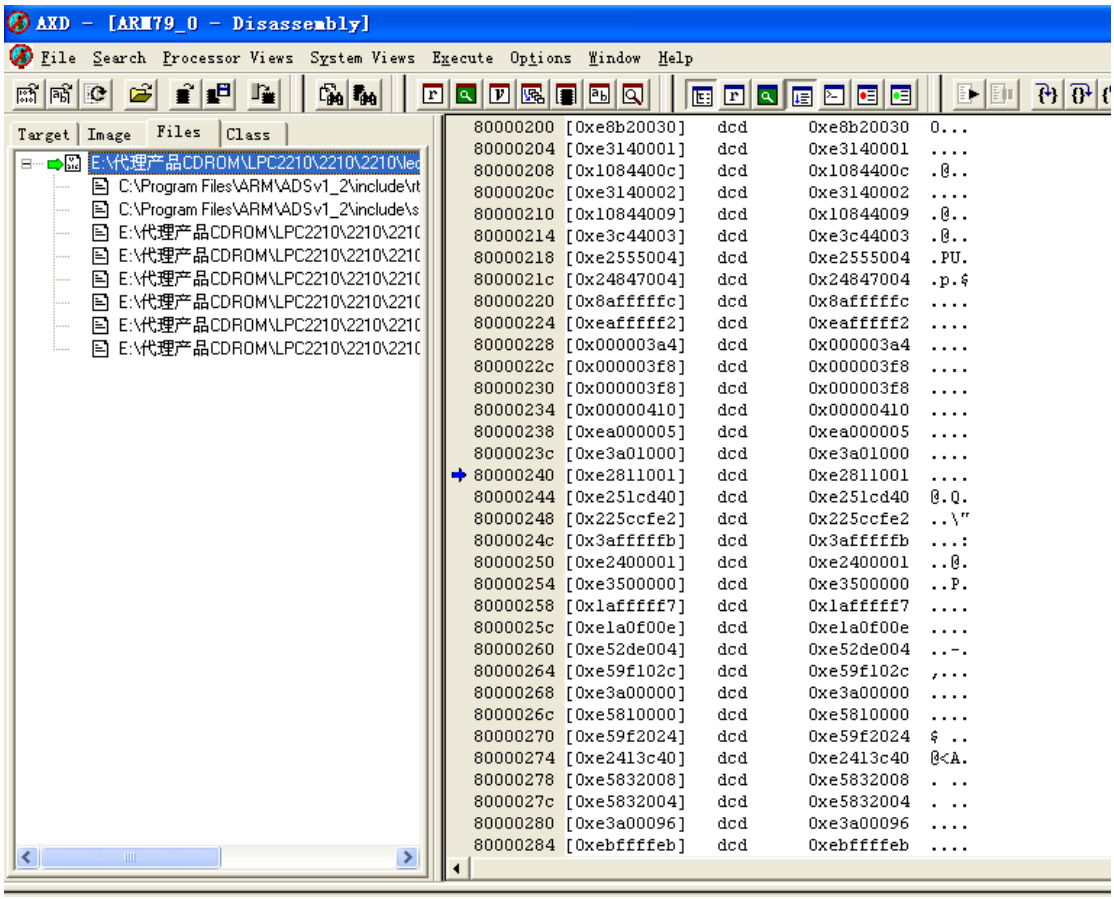

BeepCon_C.mcp
DebugInChipFlash
Files
Link Order
Targets
File
Code
Data
config.h
0
0


AXD - [ARM79_0 - E:\代理产品CDKO■\LPC2210\2210\2210\led\src\Startup.s]
File Search Processor Views System Views Execute Options Window Help
Target Image Files
ARM79_0
ETM
50 EXPORT __user_initial_stackheap
59
60 CODE32
61
62 AREA vectors,CODE,READONLY
63 ENTRY
64 ;interrupt vectors
65 ;中断向量表
66 Reset
67 LDR PC, ResetAddr
68 LDR PC, UndefinedAddr
69 LDR PC, SWI_Addr
70 LDR PC, PrefetchAddr
71 LDR PC, DataAbortAddr
72 DCD 0xb9205f80
73 LDR PC, [PC, #-0xff0]
74 LDR PC, FIQ_Addr
75
76 ResetAddr DCD ResetInit
77 UndefinedAddr DCD Undefined
78 SWI_Addr DCD SoftwareInterrupt
79 PrefetchAddr DCD PrefetchAbort
80 DataAbortAddr DCD DataAbort
81 Nouse DCD 0
82 IRQ_Addr DCD 0
83 FIQ_Addr DCD FIQ_Handler
System Output Monitor
RDI Log Debug Log
Log file:
Firmware: J-Link compiled Jun 28 2007 10:45:08 ARM Rev.5
Hardware: V5.40
S/N : 20078744
OEM : IAR
Feature(s) : RDI,FlashDL,FlashBP,JFlash,GDBFull
VTarget = 3.293V
Found 1 JTAG device, Total IRLen = 4:
Id of device #1: 0x4F1F0F0F
Found ARM with core Id 0x4F1F0F0F (ARM7)
ETM V1.2: 1 pair of addr. comp., 0 data comp., 4 mem-map decoders, 1 counter

运行到断点处：


AXD - [ARM7_0 - E:\代理产品CDROM\LPC2210\2210\2210\led\src\main.c]
File Search Processor Views System Views Execute Options Window Help
Target Image Files Class
E:\代理产品CDROM\LPC2210\2210\2210\led
C:\Program Files\ARM\ADSv1_2\include\st
C:\Program Files\ARM\ADSv1_2\include\s
E:\代理产品CDROM\LPC2210\2210\2210\
E:\代理产品CDROM\LPC2210\2210\2210\
E:\代理产品CDROM\LPC2210\2210\2210\
E:\代理产品CDROM\LPC2210\2210\2210\
E:\代理产品CDROM\LPC2210\2210\2210\
E:\代理产品CDROM\LPC2210\2210\2210\
10 void DelayNS(uint32 dly)
11 { uint32 i;
12 for(; dly>0; dly--)
13 {
14 for(i=0; i<5000; i++);
15 }
16 }
17
18
19 int main(void)
20 {
21 PINSEL0 = 0x00000000; // 设置管脚连接GPIO
22 IO0DIR = led; // 设置I/O为输出
23
24 while(1)
25 {
26 IO0SET = led; // BEEPCON = 1
27 DelayNS(150);
28 IO0CLR = led; // BEEPCON = 0
29 DelayNS(150);
30 }
31
32 return(0);
33 }
34
System Output Monitor
RDI Log Debug Log
Log file:
J-Link ARM DLL V3.74i, compiled Sep 11 2007 14:43:07
Firmware: J-Link compiled Jun 28 2007 10:45:08 ARM Rev.5
Hardware: V5.40
S/N : 20078744
OEM : IAR
Feature(s) : RDI,FlashDL,Flash0P,JFlash,GDBFull
VTarget = 3.242V
Found 1 JTAG device, Total IRLen = 4:
Id of device #1: 0x4F1F0F0F
Found ARM with core Id 0x4F1F0F0F (ARM7)
ETM V1.2: 1 pair of addr. comp., 0 data comp., 4 mem-map decoders, 1 counter

全速后按暂停



关于 INI 配置，
也是根据工程文件中的 startup.s 来进行的

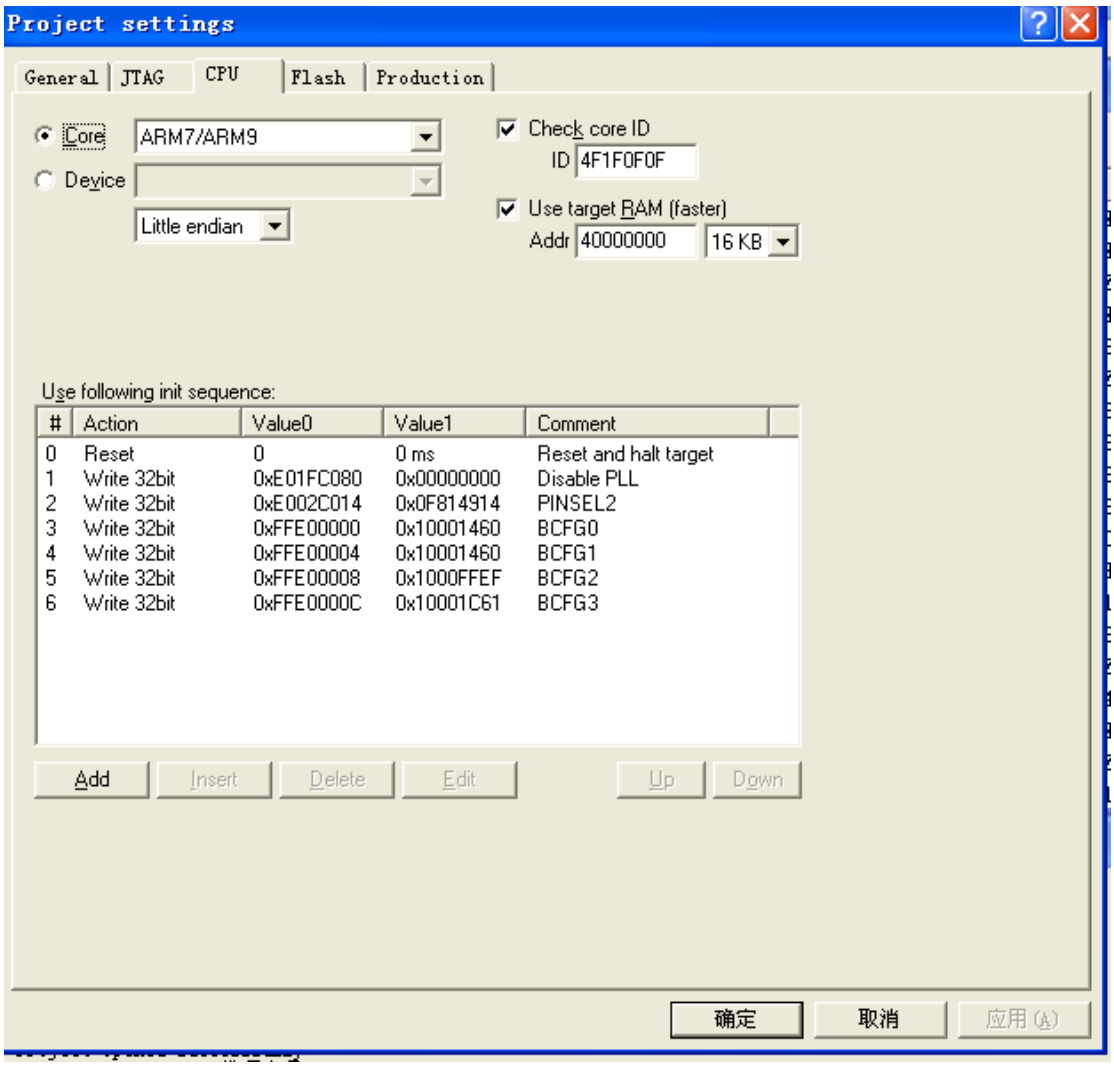
```
;/* Define the Bus Speed */
BCFG0          EQU      0xFFE00000        ;// Control Word of BANK0 / CS0
BCFG1          EQU      0xFFE00004        ;// Control Word of BANK1 / CS1
BCFG2          EQU      0xFFE00008        ;// Control Word of BANK2 / CS2
BCFG3          EQU      0xFFE0000C        ;// Control Word of BANK3 / CS3

BCFG_08DEF     EQU          0x00000000        ;//   8Bit Bus
BCFG_16DEF     EQU          0x10000400        ;// 16Bit Bus
BCFG_32DEF     EQU          0x20000400        ;// 32Bit Bus


;//                                  |      IDCY      |      WST1      |      WST2
;//                                  | Idle width | Read width | Write width
;//                                  | 0x00 ~ 0x0f| 0x00 ~ 0x1f| 0x00~0x1f
BCFG_FLASH     EQU          (BCFG_16DEF | (0x00<<00) | (0x03<<05) | (0x02<<11))     ;//
For 90ns Flash
BCFG_PSRAM     EQU       (BCFG_16DEF | (0x00<<00) | (0x03<<05) | (0x02<<11))     ;// For
```

70ns PSRAM
BCFG_CS2 EQU (BCFG_16DEF | (0x0f<<00) | (0x1f<<05) | (0x1f<<11)) ;// Blank
BCFG_CS3 EQU (BCFG_16DEF | (0x01<<00) | (0x03<<05) | (0x03<<11)) ;// For Peripheral Equipment

ResetInit
;Initial extenal bus controller.
;初始化外部总线控制器，根据目标板决定配置

```
    LDR     R0, =PINSEL2
IF :DEF: EN_CRP
    LDR     R1, =0x0f814910
ELSE
    LDR     R1, =0x0f814914
ENDIF
    STR     R1, [R0]

    LDR     R0, =BCFG0
    LDR     R1, =BCFG_FLASH
    STR     R1, [R0]

    LDR     R0, =BCFG1
    LDR     R1, =BCFG_PSRAM
    STR     R1, [R0]

    LDR     R0, =BCFG2
    LDR     R1, =BCFG_CS2
    STR     R1, [R0]

    LDR     R0, =BCFG3
    LDR     R1, =BCFG_CS3
    STR     R1, [R0]
```

对应就是：



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2007-09-18

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