**计算机组织与系统结构实习报告 Lab 2.2**

**Part I: RISC-V多周期模拟器**

1. 基于实现的RISC-V ISA，给出指令各阶段的寄存器传输级描述。每类指令举1-2个例子即可。

R-TYPE:

and rd, rs1, rs

共分4个阶段

取指：inst[31:0] <- memory[PC], PC <- PC +4

译码：opcode = 0x33, func3 = 0x7, func7 = 0x00, raddr1 = inst[19:15], raddr2 = inst[24:20], waddr = inst[11:7]

执行：ALUop = 12(R型与操作), ALUout = REG[raddr1] & REG[raddr2]

写回：RegWrite = 1, wdata = ALUout

I-TYPE:

andi rd, rs1, imm

共分4个阶段

取指：inst[31:0] <- memory[PC], PC <- PC +4

译码：opcode = 0x13, func3 = 0x7, raddr1 = inst[19:15], waddr = inst[11:7], imm[11:0] = inst[31:20]

执行：ALUop = 23(I型与操作), ALUout = REG[raddr1] & imm

写回：RegWrite = 1, wdata = ALUout

ld rd, offset(rs1)

共分5阶段

取指：inst[31:0] <- memory[PC], PC <- PC +4

译码：opcode = 0x03, func3 = 0x3, raddr1 = inst[19:15], waddr = inst[11:7], imm[11:0] = inst[31:20]

执行：ALUop = 16, ALUout = REG[raddr1] + imm

访存：MemRead = 1, val = memory[ALUout]

写回：RegWrite = 1, wdata = val

S-TYPE:

sd rs2, offset(rs1)

共分4阶段

取指：inst[31:0] <- memory[PC], PC <- PC +4

译码：opcode = 0x23, func3 = 0x3, raddr1 = inst[19:15], raddr2 = inst[24:20], imm[11:5] = inst[31:25], imm[4:0] = inst[11:7]

执行：ALUop = 30, ALUout = REG[raddr1] + imm

访存：MemWrite = 1, memory[ALUout] = REG[raddr2]

SB-TYPE:

beq rs1, rs2, offset

共分3阶段

取指：inst[31:0] <- memory[PC], PC <- PC +4

译码：opcode = 0x63, func3 = 0x0, raddr1 = inst[19:15], raddr2 = inst[24:20], imm[12] = inst[31], imm[11] = inst[7], imm[10:5] = inst[30:25], imm[4:1] = inst[11:8], imm[0] = 0

执行：ALUop = 31, if(REG[raddr1] == REG[raddr2]) PC = temp\_PC + imm

U-TYPE:

auipc rd, offset

共分4阶段

取指：inst[31:0] <- memory[PC], PC <- PC +4

译码：opcode = 0x17, waddr = inst[11:7], imm = inst[31:12]<<12

执行：ALUop = 35, ALUout = temp\_PC + imm

写回：RegWrite = 1, wdata = ALUout

UJ-TYPE:

jal rd, imm

共分4阶段

取指：inst[31:0] <- memory[PC]

译码：opcode = 0x6f, waddr = inst[11:7], imm[20] = inst[31], imm[19:12] = inst[19:12], imm[11] = inst[20], imm[10:1] = inst[30:21], imm[0] = 0

执行：ALUop = 37, ALUout = temp\_PC + 4, PC = temp\_PC + imm

写回：RegWrite = 1, wdata = ALUout