2021/12/07

Project 2 – Cell-Based Layout Design

11010CS312000
Introduction of Integrated Circuit Design, NTHU

Outline

- Cell-Based Design
- Standard Cell Setting
- Cell Duplication for Logic Function
- Example
- Project
- Grading

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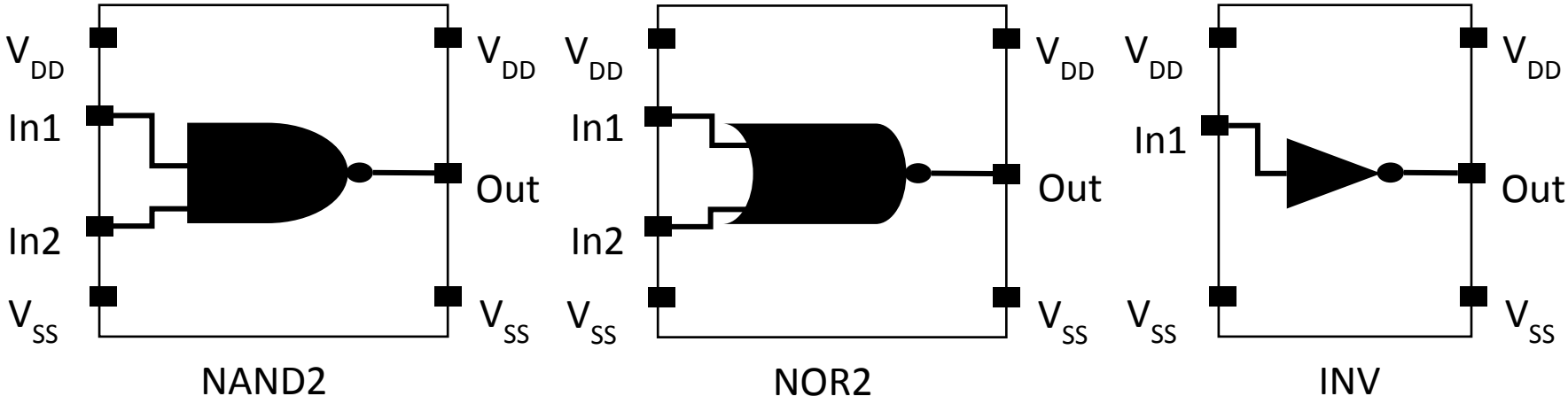
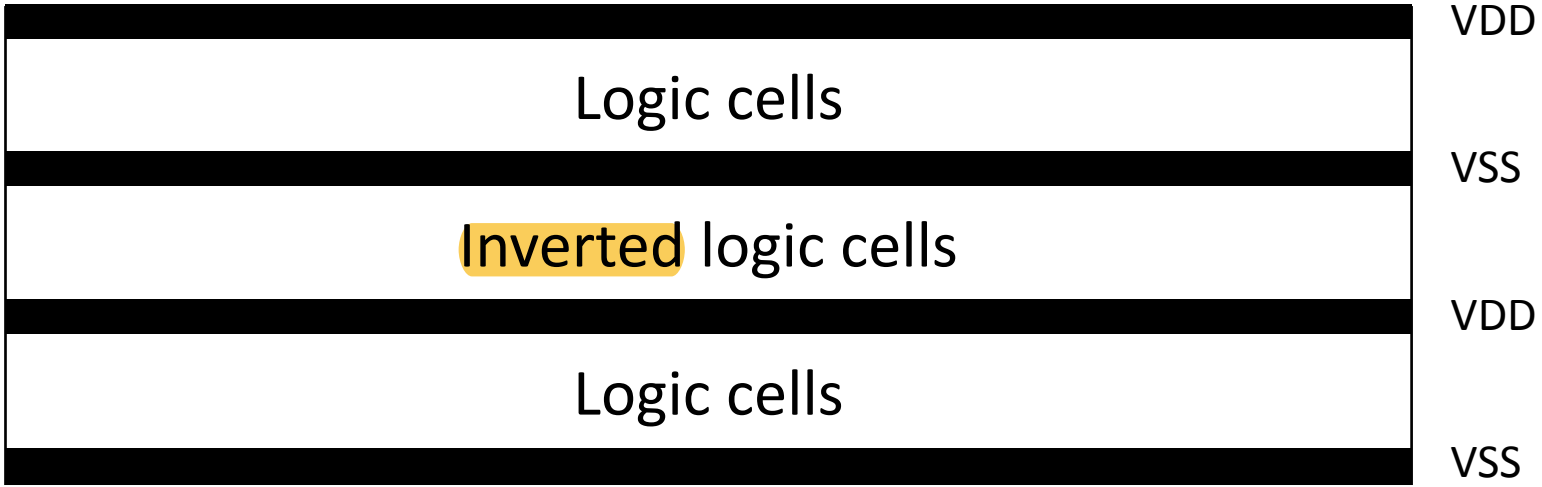
Cell-Based Design (1)

- Based on the idea of hierarchical design
- Do not care about the internal details at the cell-level design



Cell-Based Design (2)

- Weinberger image array



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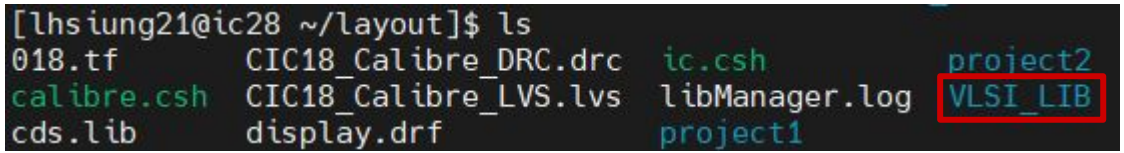
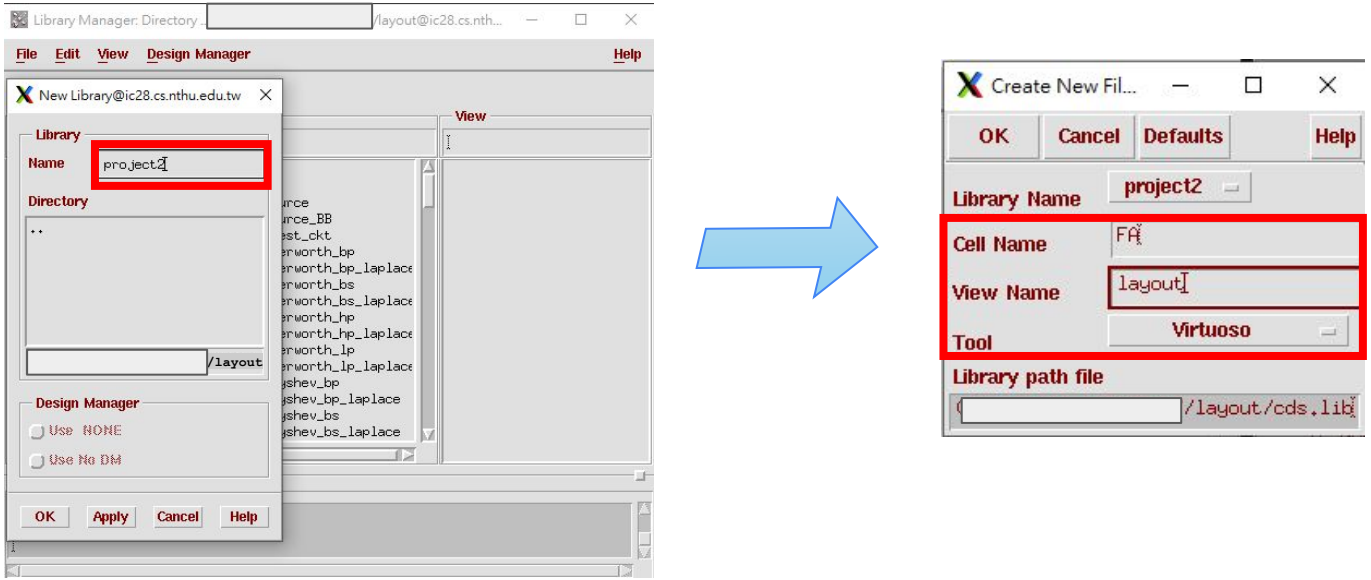
Library Prepared

- Upload library “VLSI_LIB” to workstation
  - ~/layout/VLSI_LIB
- You may use the same directory used in Project1 since the environment settings are still the same, i.e., DRC, LVS rule files, calibre.csh and 018.tf etc. are also necessary.

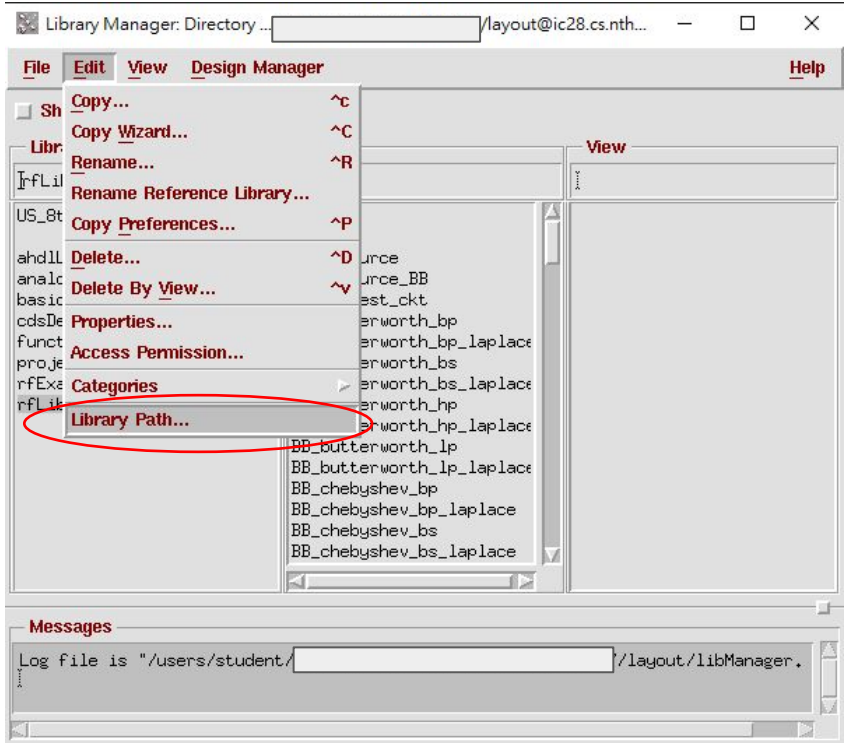


New Project Library Creation

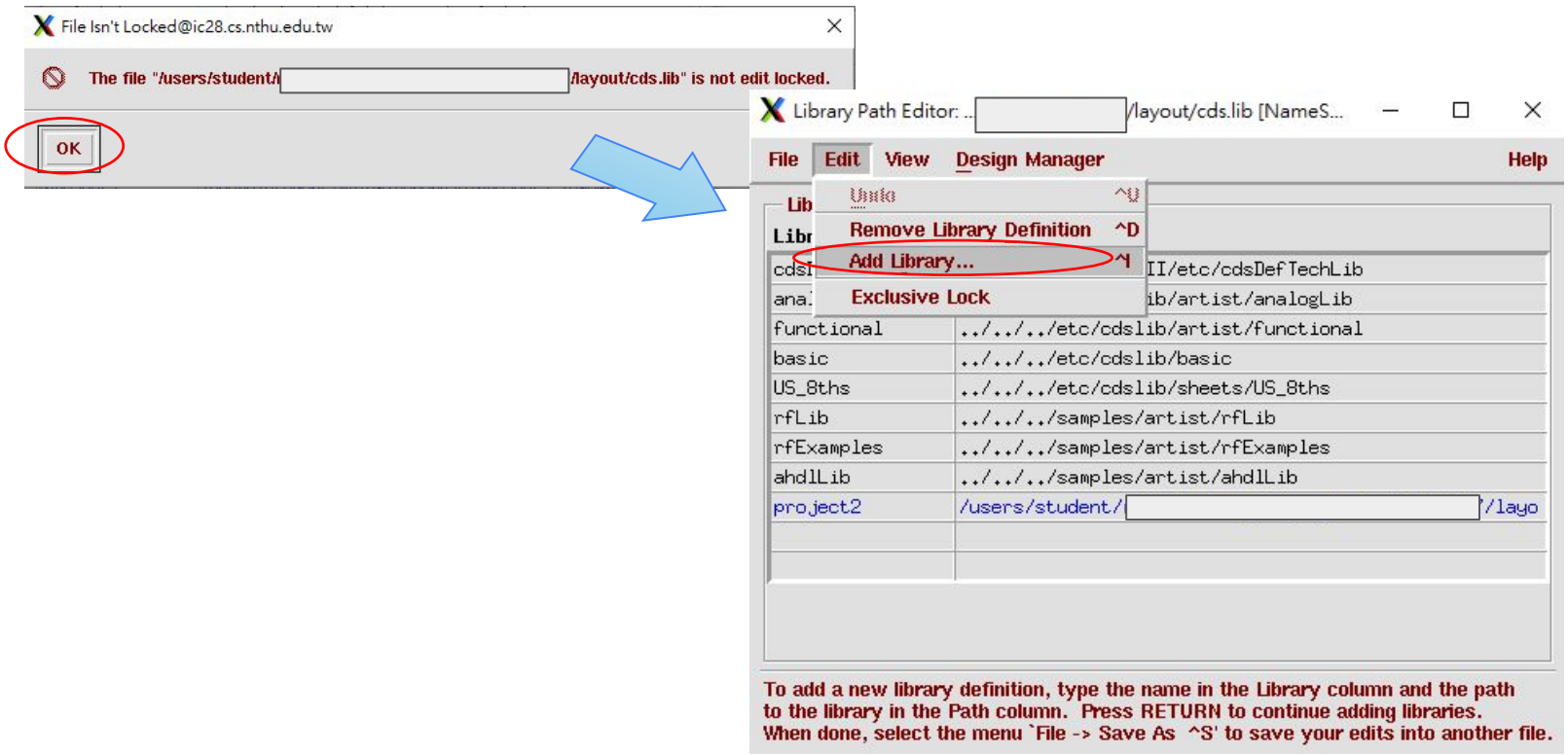
- Please refer the slides of Project1
  - Create a library named “project2”
  - Create a cell view named “FA”



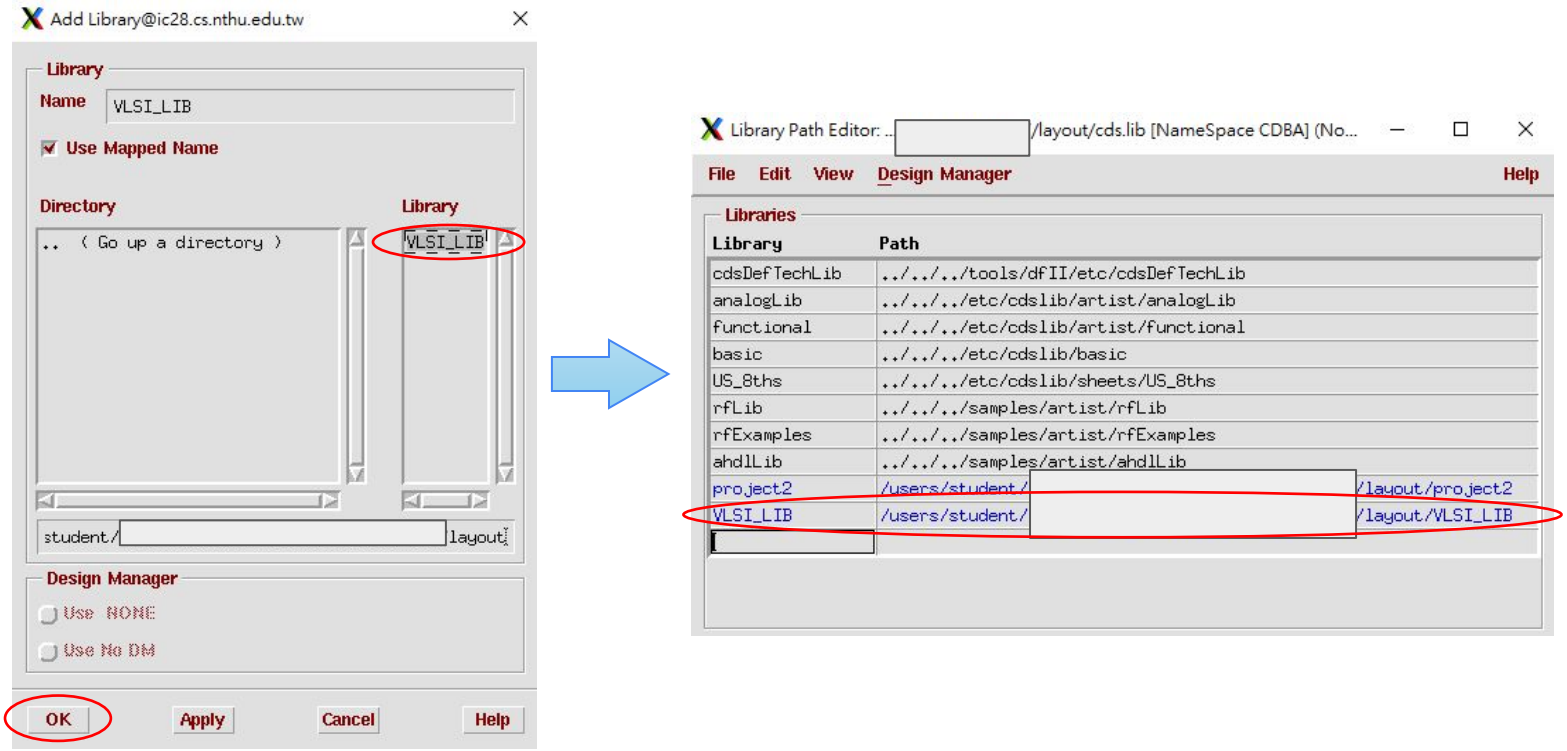
Set Library Path (1)



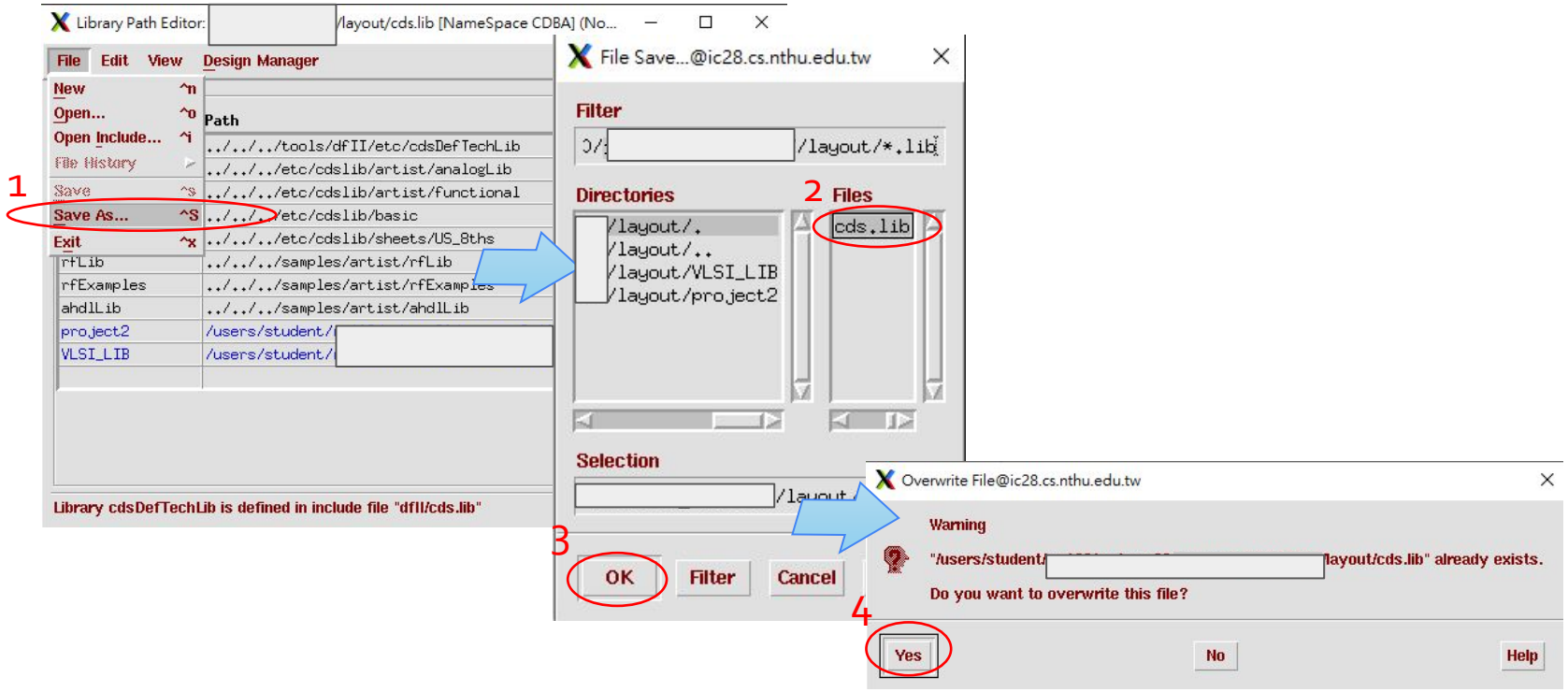
Set Library Path (2)



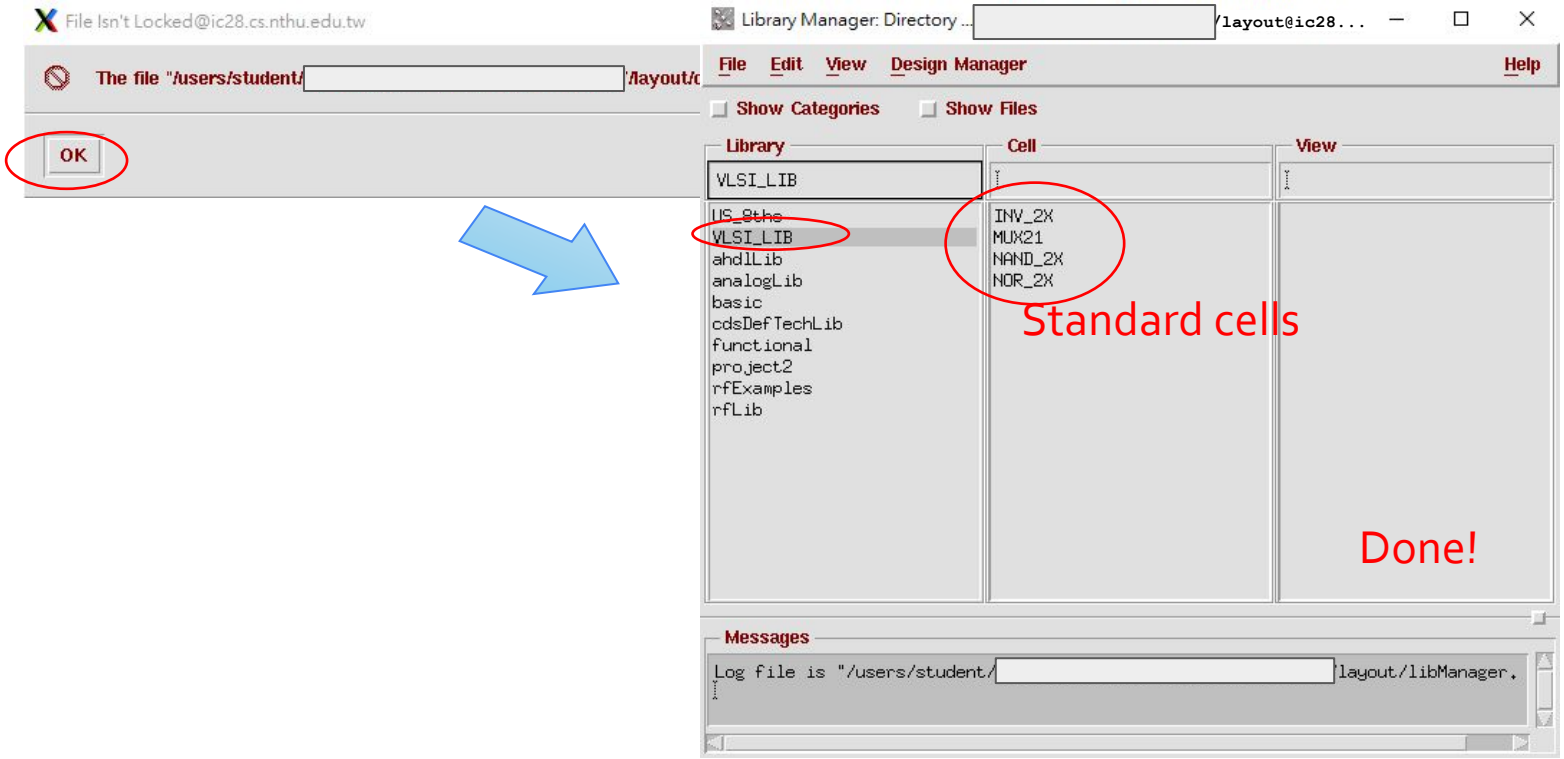
Set Library Path (3)



Set Library Path (4)



Set Library Path (5)



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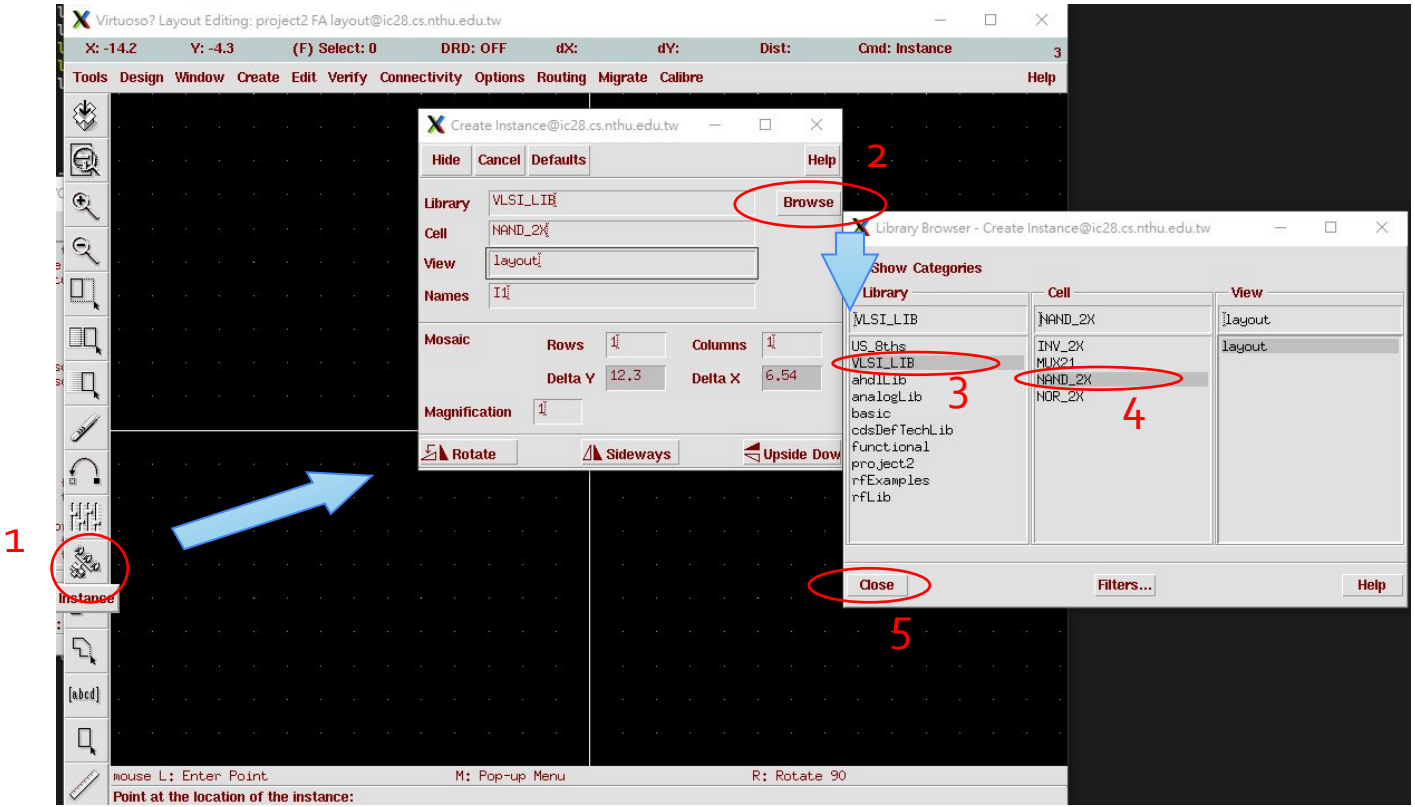
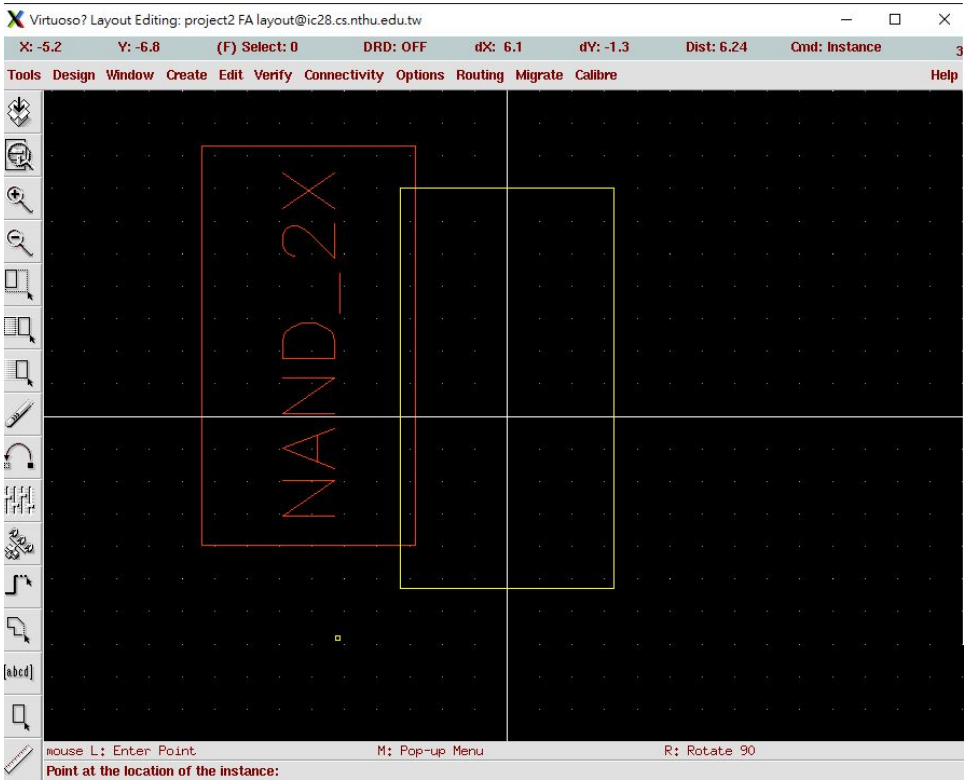
Instance Creation (1)

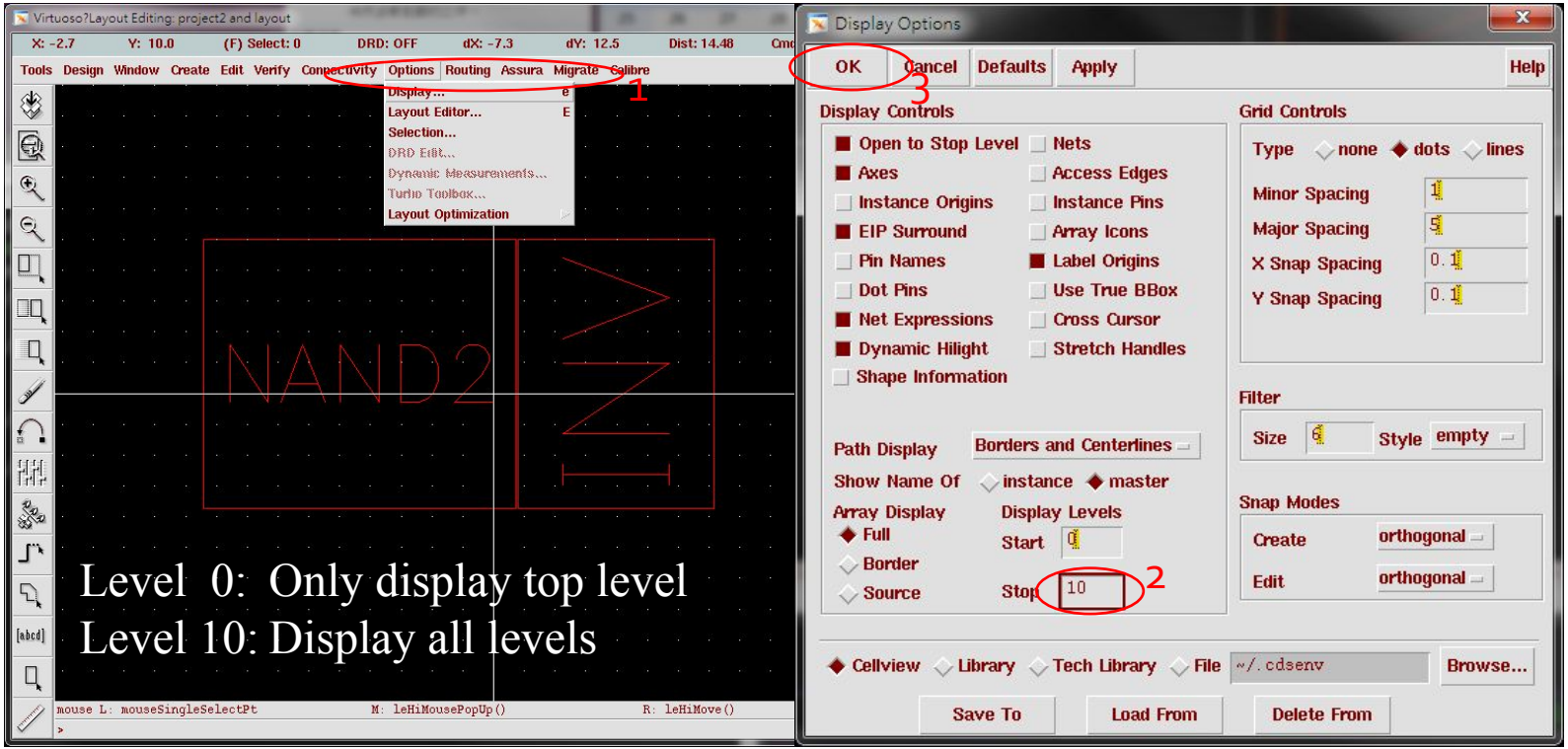


Instance Creation (2)

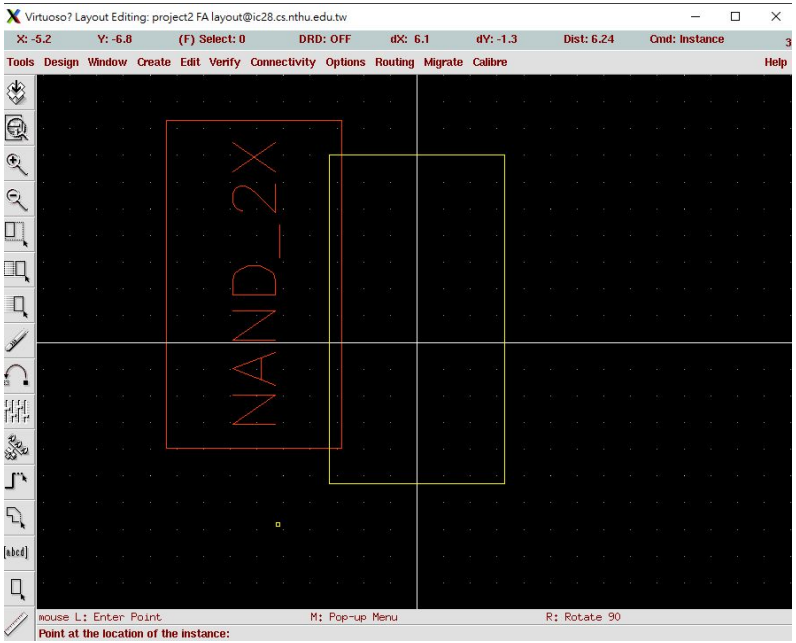


- Left click to place the cell.

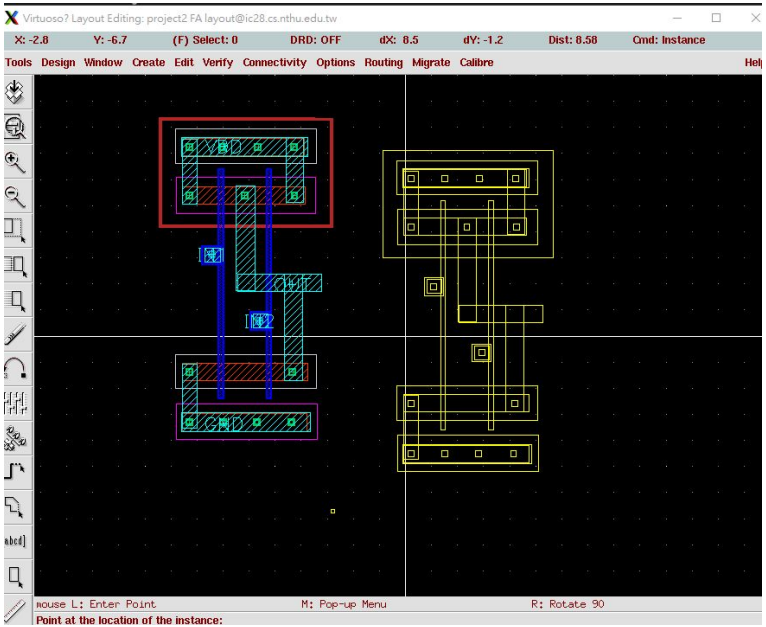
Instance Creation (3)



Instance Creation (4)



Display level 0



Display level 10

Hotkey - Display level

Cadence Virtuoso Layout Hotkeys

	Category	Action	Hotkey
VIEW	ZOOM	IN	cntl+z
		OUT	shift+Z
	FIT	Fit whole layout to exiting window	f
	VIEW HIERARCHY	MORE DETAIL	shift+F
		LESS DETAIL	cntl+f
	REDRAW	---	cntl+r
EDIT	STRETCH	---	s
	MOVE	---	m
	COPY	---	c
	UNDO	---	u
	SELECT ALL	Select all objects on the window	cntl +a
	DESELECT ALL	Deselects all selected objects	cntl +d
MISC	PROPERTIES	Show properties of selected object	q
	RULER	CREATE	k
		DELETE ALL	shift+K
	HIERARCHY	DESCEND	shift+X
		RETURN	shift+B

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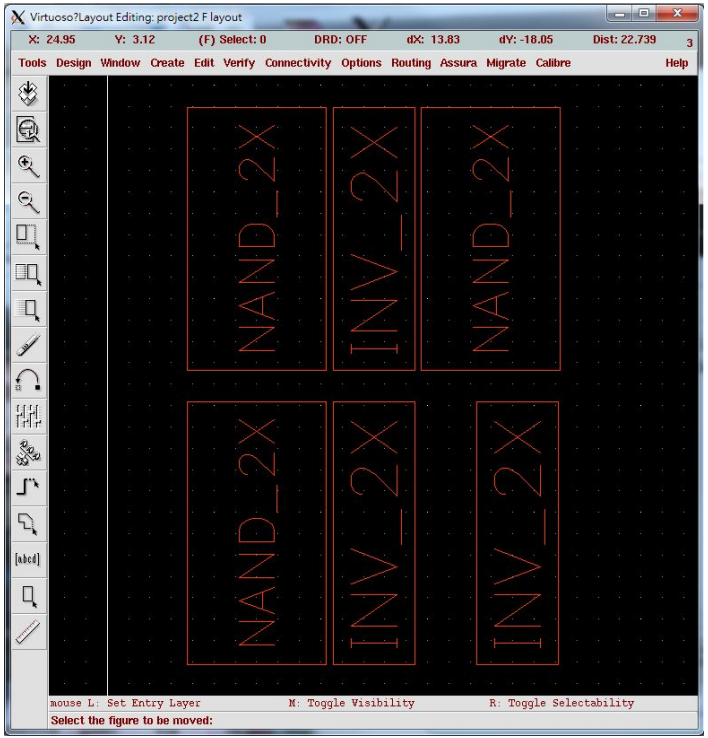
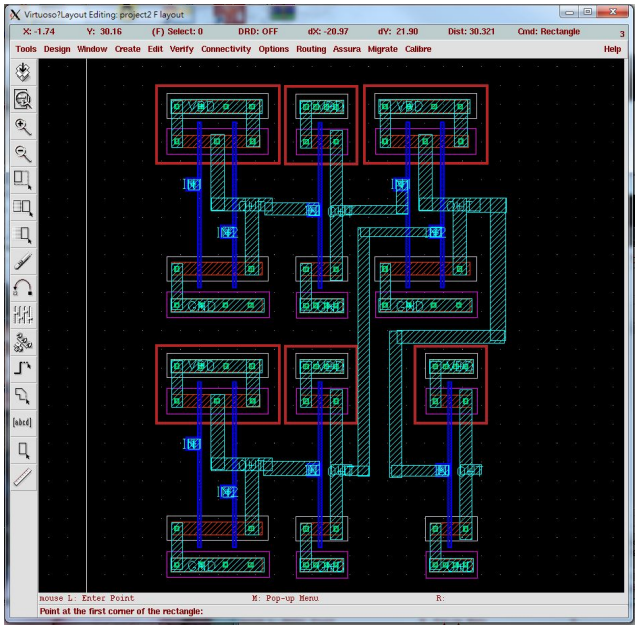
Example: f = a * b * c * d (1)

Cell duplication

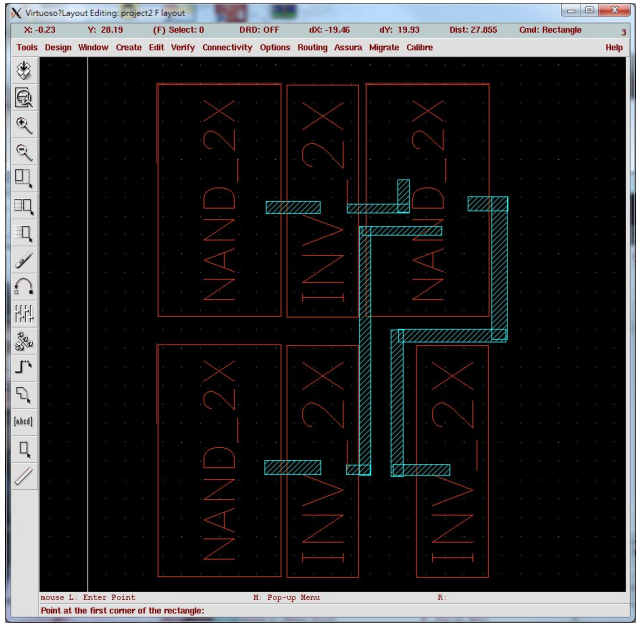


Example: f = a * b * c * d (2)

Metal wire connection



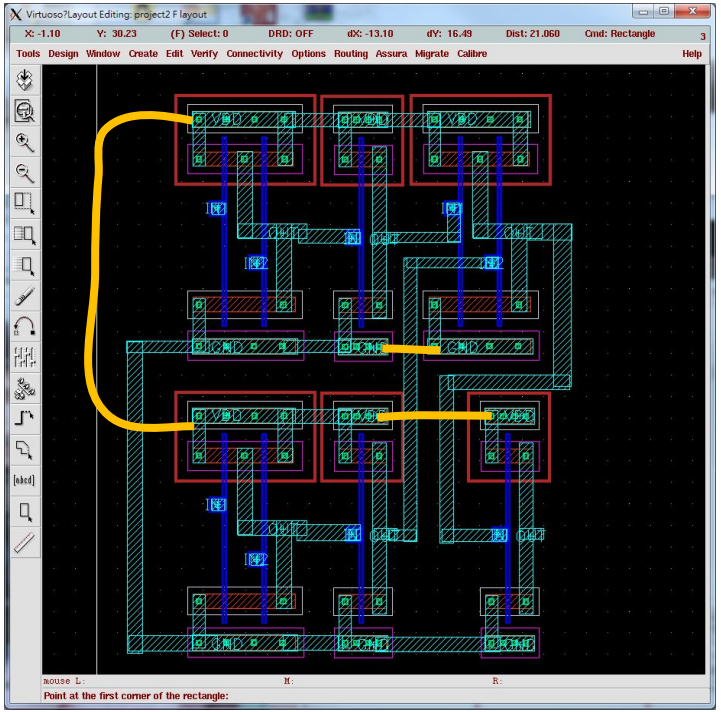
Display level 10



Display level 0

Example: f = a * b * c * d (3)

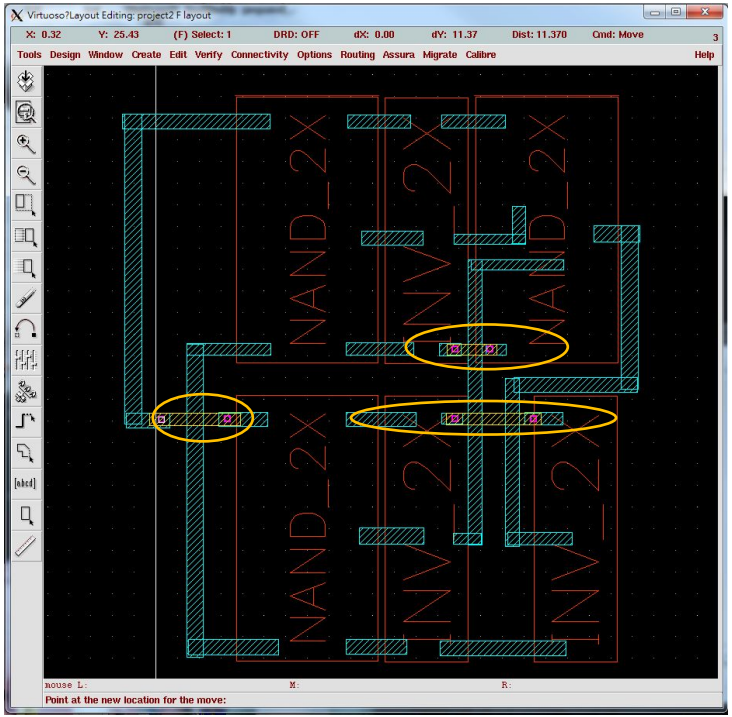
Vdd / Gnd Connection **by metal 1**



- You **cannot just** use metal 1 to connect these segments —— .
- It causes unexpected shorts to other metal 1!

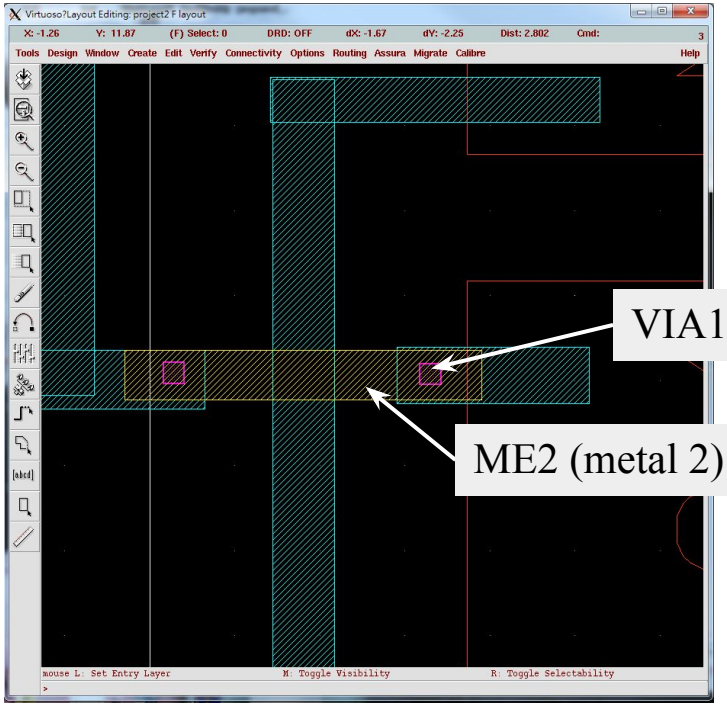
Example: f = a * b * c * d (4)

Vdd / Gnd Connection **by metal 2**



Example: f = a * b * c * d (5)

Vdd / Gnd Connection **by metal 2**



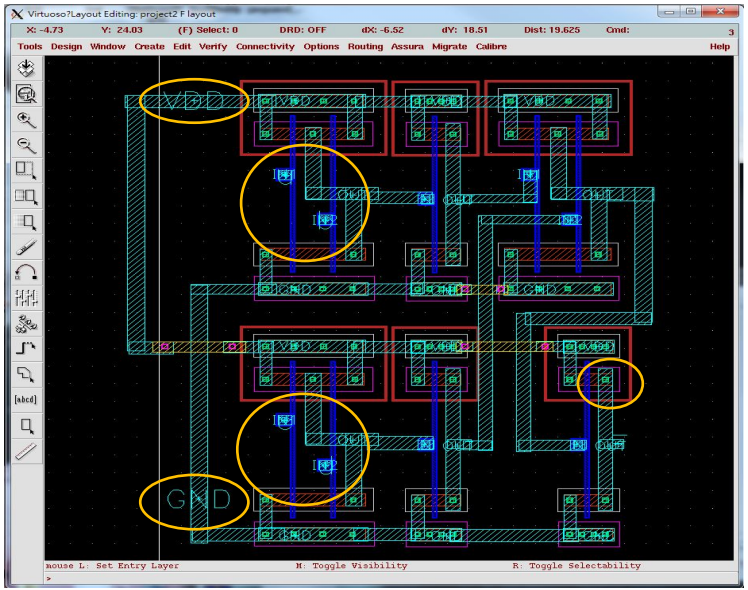
Size of VIA must be
0.25um * 0.25um

VIA1

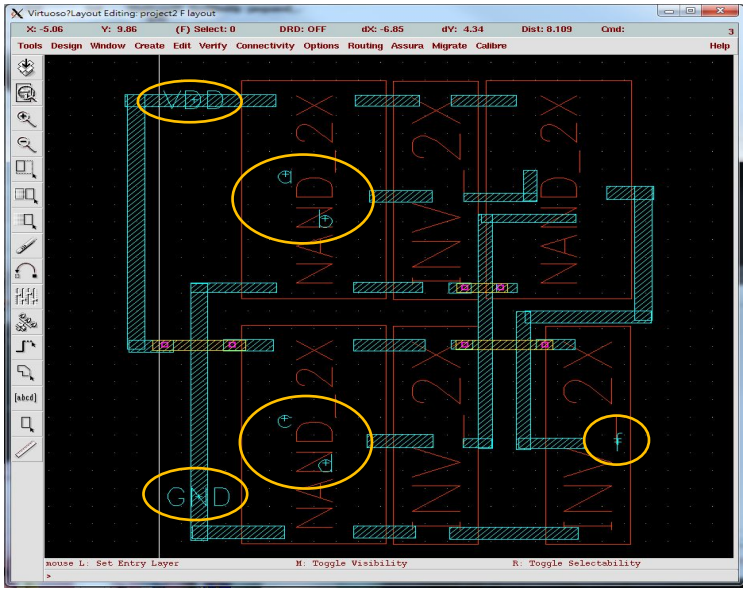
ME2 (metal 2)

Example: f = a * b * c * d (6)

Labels in standard cells are different from current cell!
*P.S. You should display **level zero** for checking*



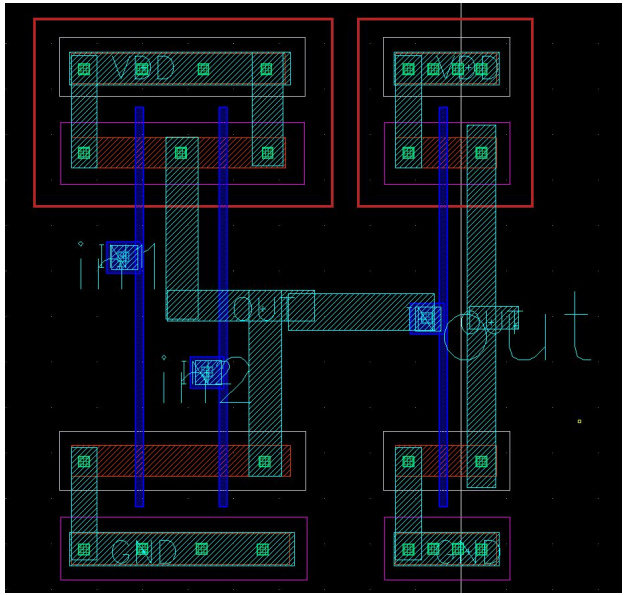
Display level 10



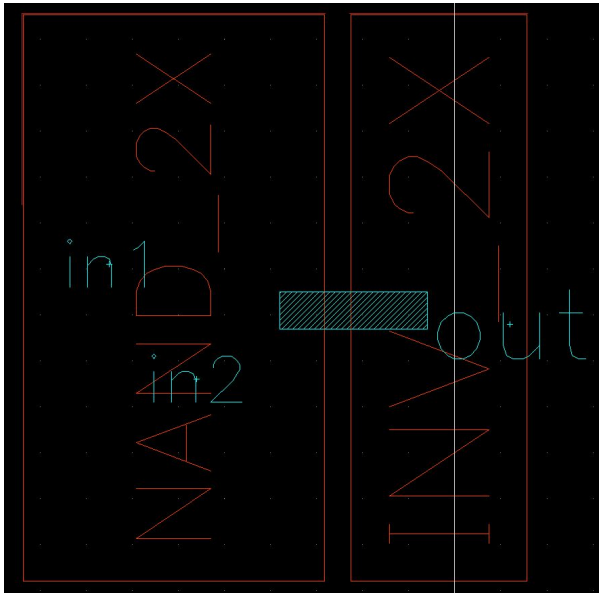
Display level 0

Another clearer example: out = in1 * in2

Labels in standard cells are different from current cell!
*P.S. You should display **level zero** for checking*



Display level 10



Display level 0

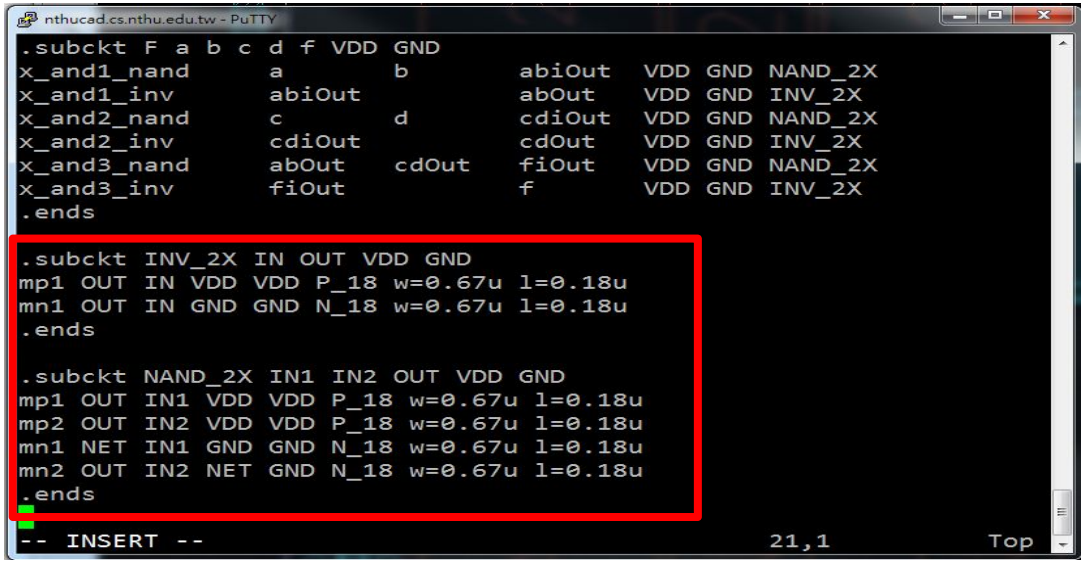
Example: f = a * b * c * d (7)

- Schematic file “ADDER3.src.net”
- “x” represents the cell (subcircuit call)
  - x_[name_as_you_like] [Pin 1] [Pin 2] … [Pin N] [Cell_type_name]
- E.g.

```
.subckt  F  a  b  c  d  f  VDD  GND
x_and1_nand    a       b       abiOut VDD   GND    NAND_2X
x_and1_inv     abiOut  abOut   VDD    GND   INV_2X
x_and2_nand    c       d       cdiOut VDD   GND    NAND_2X
x_and2_inv     cdiOut  cdOut   VDD    GND   INV_2X
x_and3_nand    abOut   cdOut   fiOut  VDD   GND    NAND_2X
x_and3_inv     fiOut   f       VDD    GND   INV_2X
.ends
```

Example: f = a * b * c * d (8)

- Definition of standard cells also needs to be put into schematic file.
- You can find standard definition at `VLSI_LIB/[Cell_name]`
  - E.g. `VLSI_LIB/NAND_2X/NAND2X.src.net`



Outline

- Cell-Based Design
- Standard Cell Setting
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- Example
- Project
  - Step 1: 2x1 multiplexer
  - Step 2: 1-bit full adder
  - Step 3: 3-bit carry select adder
- Grading

Project Requirements

Step 1: Design a 2x1 multiplexer: MUX21 (already given in `VLSI_LIB`)

- Use cell-based design
- Pass DRC and LVS

Step 2: Design a 1-bit full adder: FA

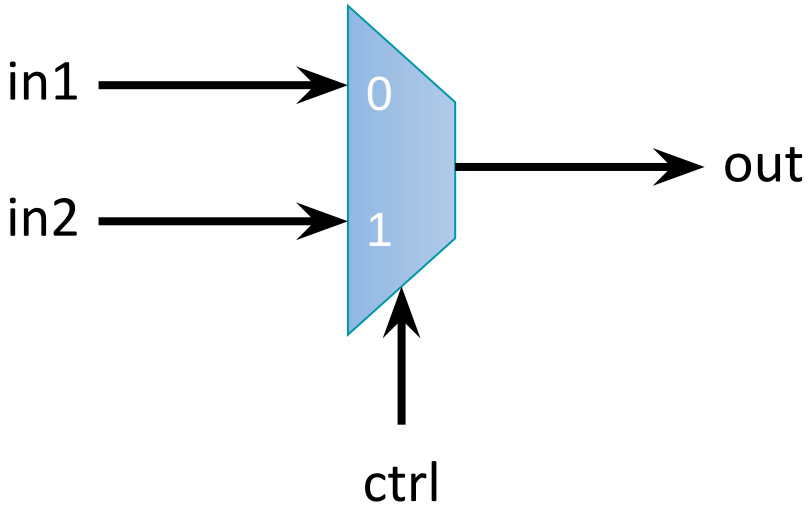
- Use cell-based design
- Pass DRC and LVS

Step 3: Design a 3-bit carry select adder: ADDER3

- Design a transistor-level schematic yourself
- Draw a cell-based layout (reuse your full_adder & MUX)
- Pass DRC and LVS

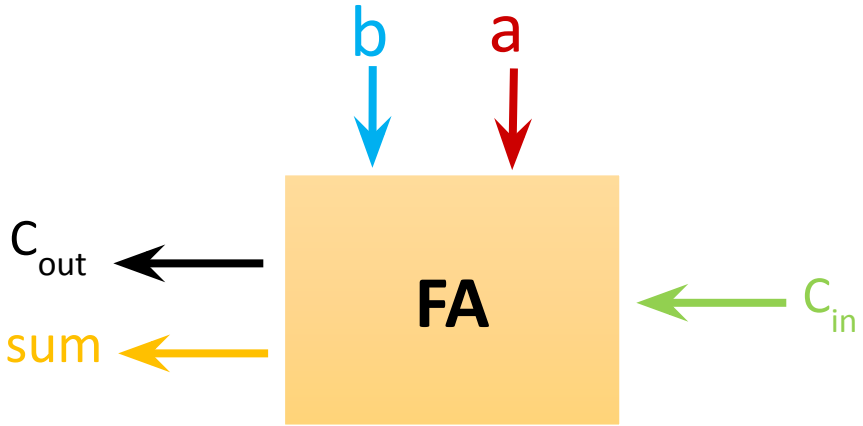
Step 1: 2x1 Multiplexer

- Cell name: MUX21 (given in `VLSI_LIB`)
- Input
  - in1
  - in2
  - ctrl
- Output
  - out
- Function
  - out = (ctrl == 0) ? in1 : in2



Step 2: 1-bit Full Adder

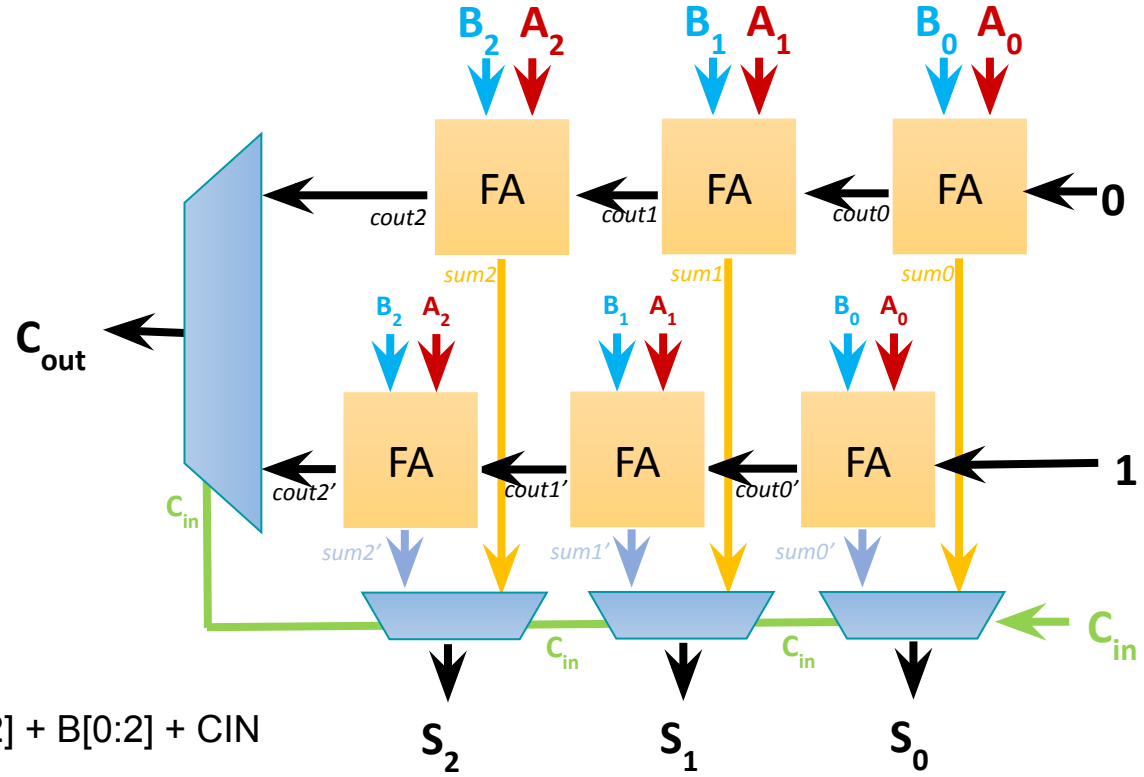
- Cell name: FA
- Input
  - a
  - b
  - c_in
- Output
  - c_out
  - sum
- Function
  - { c_out , sum } = a + b + c_in



Inputs			Outputs	
A	B	C – IN	Sum	C - Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Step 3: 3-bit Carry Select Adder

- Cell name: ADDER3
- Input
  - A[0:2]: A0, A1, A2
  - B[0:2]: B0, B1, B2
  - CIN
- Output
  - S[0:2]: S0, S1, S2
  - COUT
- Function
  - { COUT , S[0:2] } = A[0:2] + B[0:2] + CIN



Transistor Schematic

- Schematic format
  - Cell and port name should be named as follows
  - I/O port must be ***in order***

```
.subckt ADDER3 A0 A1 A2 B0 B1 B2 CIN S0 S1 S2 COUT VDD GND
    ...
.ends

.subckt FA a b c_in sum c_out VDD GND
    ...
.ends

.subckt MUX21 in1 in2 ctrl out VDD GND
    ...
.ends
    ...
```

Layout

- Labels should be **STRICTLY** named as follows.
  - Cell name
    - ADDER3
  - Input
    - A0, A1, A2, B0, B1, B2, CIN, VDD, GND
  - Output
    - S0, S1, S2, COUT
  - No naming constraint to internal signals
  - You can use only metal layer 1 and 2 (ME1 & ME2)

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Report

- Your report should contain the following content, and you can add more as you wish.
  - Your NAME and STUDENT ID
  - FIVE screenclips:
    - Layout with rulers (BOTH display *level 10* and *level 0*)
    - DRC summary report
    - The message of passing LVS... ✓[CORRECT]☺
    - LVS schematic (the text file, ADDER3.src.net)
  - What else did you do to enhance your layout quality?
  - What have you learned from this homework? What problem(s) have you encountered in this homework?

Grading (1)

- Submission deadline: 2021/12/31 (Fri.) 23:59
- TWO files to upload:
  1. A `.pdf` format report
  2. A `.tar.gz` file includes all files in directory `layout`.

     You can use the following command to compress your directory on a workstation:

     ```
     $ tar -zcvf [Student_ID]_project2.tar.gz ./layout
     ```

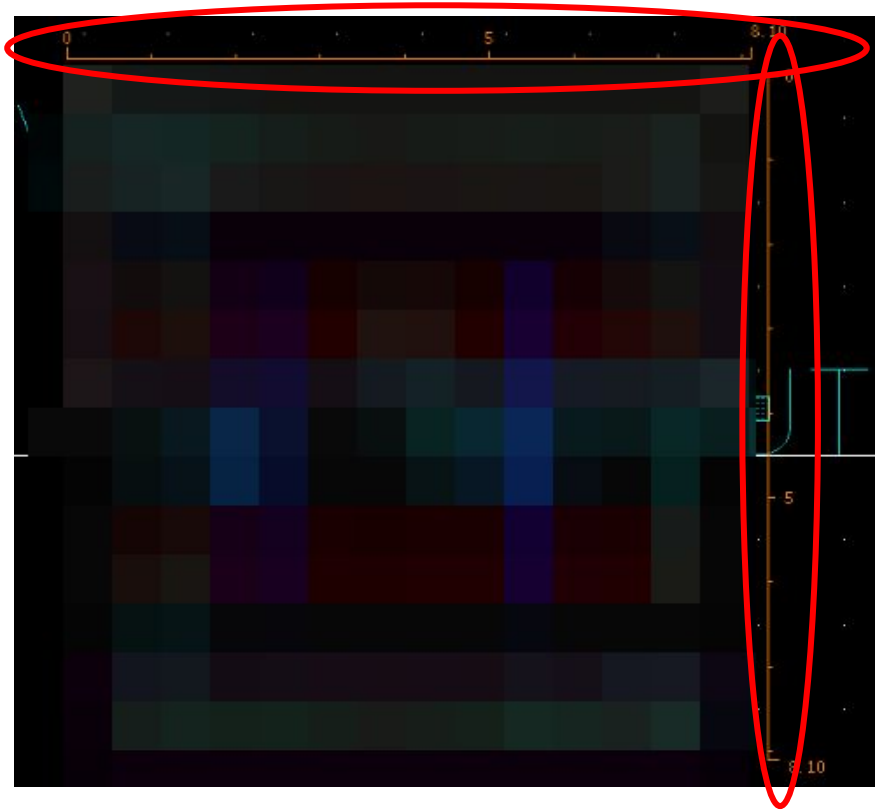
     (More compress & extraction commands: http://note.drx.tw/2008/04/command.html)
- Upload *1.* and *2.* to *eeclass*
  - Name the files as "`[StudentID]_report2.pdf`" and "`[StudentID]_project2.tar.gz`", repectively.

Grading (2)

- Score breakdown
  - Layout Area 30% (以全班1/3、2/3為分界，給予三等級分數)
  - DRC pass 20%
  - Layout 20%
  - LVS schematic 20%
  - Report 10%
  - Uploading date
    - Early bird bonus: Extra 10 points for submission before 2021/12/24 (Fri.) 23:59
    - No late submission

Layout with Rulers to Show Area

- No ruler: -10 points
- Ruler must not be too large or too small.



Notice

- File Naming
  - Library name: project2
  - Cell: FA, ADDER3
  - LVS netlist name: ADDER3.src.net
- Submission after deadline → 0 point
- Plagiarism → 0 point
- Dishonest contents in the report → 0 point