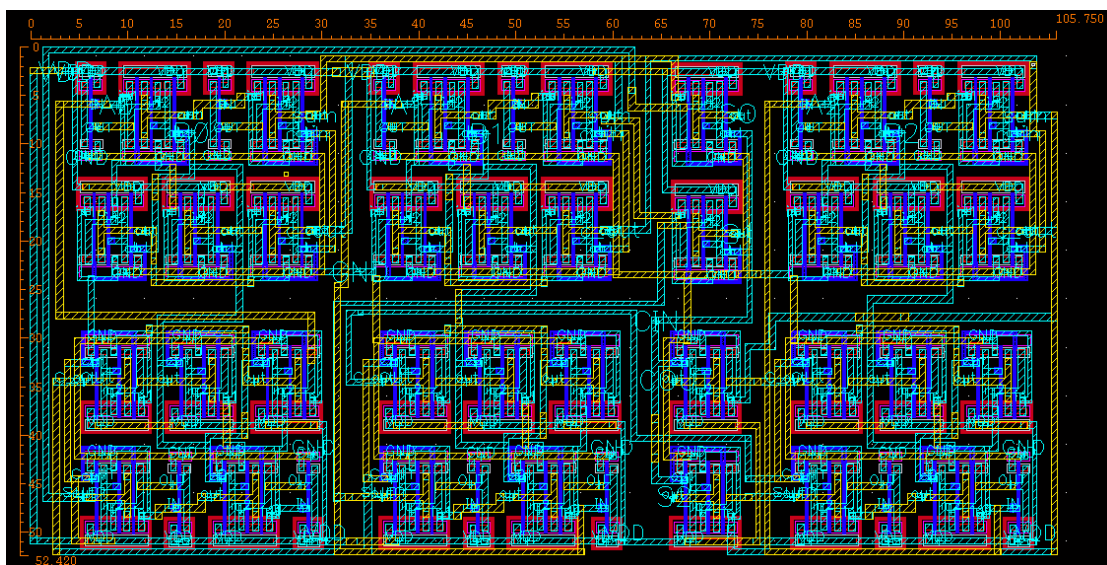
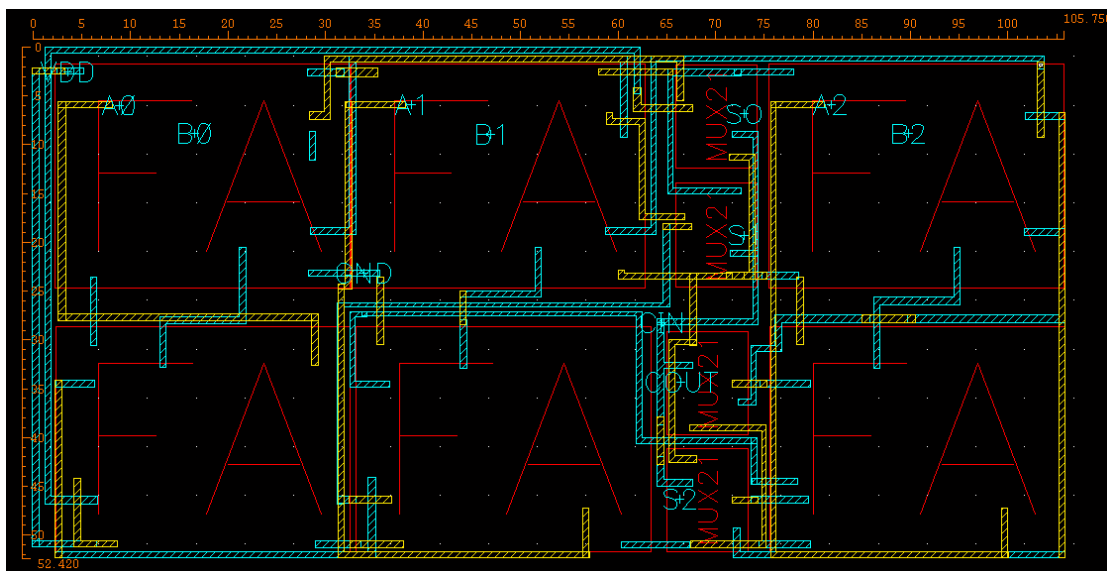


積體電路設計概論 Project2

107062103 王依婷

I. 5 Screenshots :

- Layout with ruler



- DRC summary report

```

DRC Summary Report - ADDER3.drc.summary
File Edit Options Windows

RULECHECK SLOT.S2_M3 ..... NOT EXECUTED
RULECHECK SLOT.S3_M3 ..... NOT EXECUTED
RULECHECK SLOT.W1_M4 ..... NOT EXECUTED
RULECHECK SLOT.W2_M4 ..... NOT EXECUTED
RULECHECK SLOT.S1_M4 ..... NOT EXECUTED
RULECHECK SLOT.S2_M4 ..... NOT EXECUTED
RULECHECK SLOT.S3_M4 ..... NOT EXECUTED
RULECHECK SLOT.W1_M5 ..... NOT EXECUTED
RULECHECK SLOT.W2_M5 ..... NOT EXECUTED
RULECHECK SLOT.S1_M5 ..... NOT EXECUTED
RULECHECK SLOT.S2_M5 ..... NOT EXECUTED
RULECHECK SLOT.S3_M5 ..... NOT EXECUTED
RULECHECK SLOT.W1_M6 ..... NOT EXECUTED
RULECHECK SLOT.W2_M6 ..... NOT EXECUTED
RULECHECK SLOT.S1_M6 ..... NOT EXECUTED
RULECHECK SLOT.S2_M6 ..... NOT EXECUTED
RULECHECK SLOT.S3_M6 ..... NOT EXECUTED

-----
--- RULECHECK RESULTS STATISTICS (BY CELL)
---
-----
--- SUMMARY
---
TOTAL CPU Time: 0
TOTAL REAL Time: 1
TOTAL Original Layer Geometries: 258 (2460)
TOTAL DRC RuleChecks Executed: 234
TOTAL DRC Results Generated: 0 (0)

Edit Row 1 Col 1

```

- LVS passing message

[illegible]

- LVS schematic

```

ADD3.src.net
.subckt ADDER3 A0 A1 A2 B0 B1 B2 CIN S0 S1 S2 COUT VDD GND
x_fa0 A0 B0 GND sum0 cout0 VDD GND FA
x_fa1 A1 B1 cout0 sum1 cout1 VDD GND FA
x_fa2 A2 B2 cout1 sum2 cout2 VDD GND FA
x_fa3 A0 B0 VDD sum3 cout3 VDD GND FA
x_fa4 A1 B1 cout3 sum4 cout4 VDD GND FA
x_fa5 A2 B2 cout4 sum5 cout5 VDD GND FA
x_mux0 sum0 sum3 CIN S0 VDD GND MUX21
x_mux1 sum1 sum4 CIN S1 VDD GND MUX21
x_mux2 sum2 sum5 CIN S2 VDD GND MUX21
x_mux3 cout2 cout5 CIN COUT VDD GND MUX21
.ends

.subckt FA a b c_in sum c_out VDD GND
x_inv0 a inv_a VDD GND INV_2X
x_mux0 a inv_a b r0 VDD GND MUX21
x_inv1 r0 inv_r0 VDD GND INV_2X
x_mux1 r0 inv_r0 c_in sum VDD GND MUX21
x_mux2 GND a b r1 VDD GND MUX21
x_mux3 a VDD b r2 VDD GND MUX21
x_mux4 r1 r2 c_in c_out VDD GND MUX21
.ends

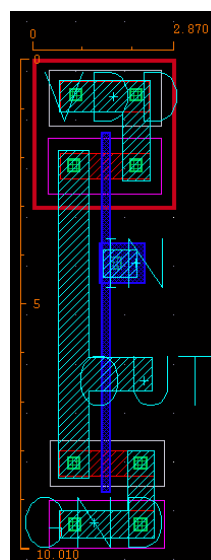
.subckt MUX21 in1 in2 ctrl out VDD GND
mp0 invctrl ctrl VDD VDD P_18 w=0.57u l=0.18u
mn0 invctrl ctrl GND GND N_18 w=0.50u l=0.18u
mp1 out ctrl in1 VDD P_18 w=0.57u l=0.18u
mn1 in1 invctrl out GND N_18 w=0.50u l=0.18u
mp2 out invctrl in2 VDD P_18 w=0.57u l=0.18u
mn2 in2 ctrl out GND N_18 w=0.50u l=0.18u
.ends

.subckt INV_2X IN OUT VDD GND
mp0 OUT IN VDD VDD P_18 w=0.53u l=0.18u
mn0 OUT IN GND GND N_18 w=0.51u l=0.18u
.ends

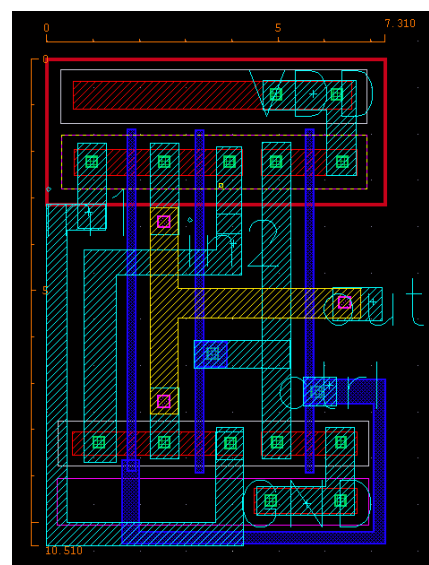
```

II. Other discussion

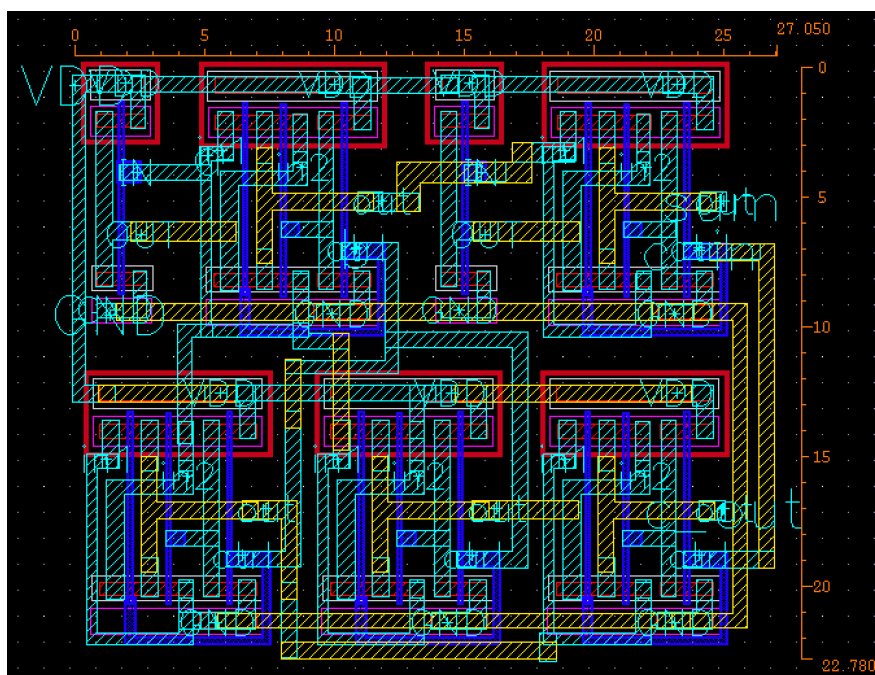
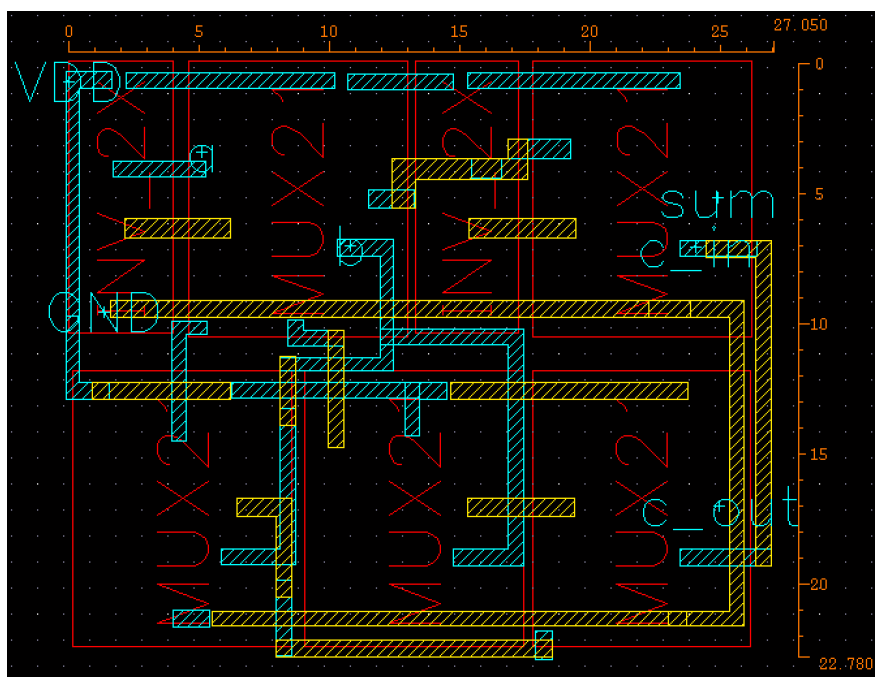
在這次的作業中我沒有使用 standard cell library 裡面的 cell，因為 library 裡面的 cell 其實比較大，改成自己繪製了 inverter，再用來它和 transmission gate 組合成 2-to-1 的 MUX，之後再組合成 full adder，最後形成 ADDER3。以下分別是 inverter、MUX、full adder 的 layout 圖，還有參考的電路圖（LVS 檔案的話其實有包含在 ADDER3 裡面了，所以不再附上）。



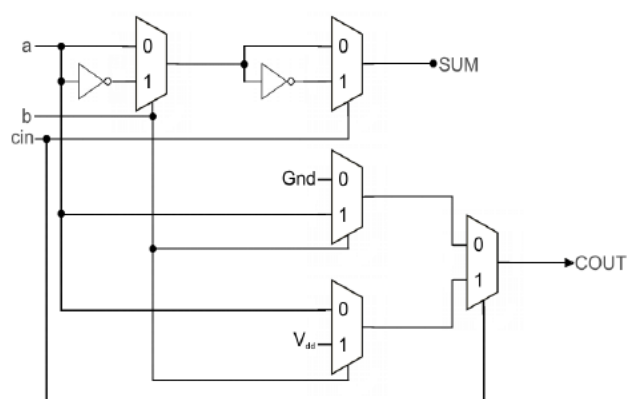
(a) inverter



(b) 2-to-1 MUX



(c) 1-bit full adder



(d) 參考的 full adder 圖

我覺得 project2 和 project1 的規模差非常多，在 inverter、MUX、FA 每一層級都要檢查沒問題才能繼續做下去，等到畫到最後 ADDER3 時 layout 已經變得非常複雜！一開始 LVS 一直不過，慢慢檢查才發現在很多小地方不小心漏掉一些，比如我漏畫很多 via 等，最後也覺得有 debug 出了一些條理，感覺更熟悉畫 layout 了！這次也自己畫了 cell 來使用，讓 area 減少不少，蠻有成就感的。