

2021/10/26

# Project 1 – Custom Layout Design

11010CS312000  
Introduction of Integrated Circuit Design, NTHU

# Full-Custom Design Flow

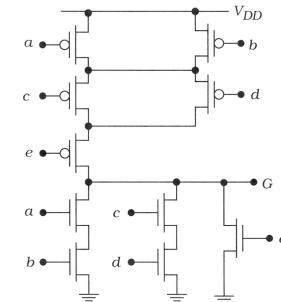
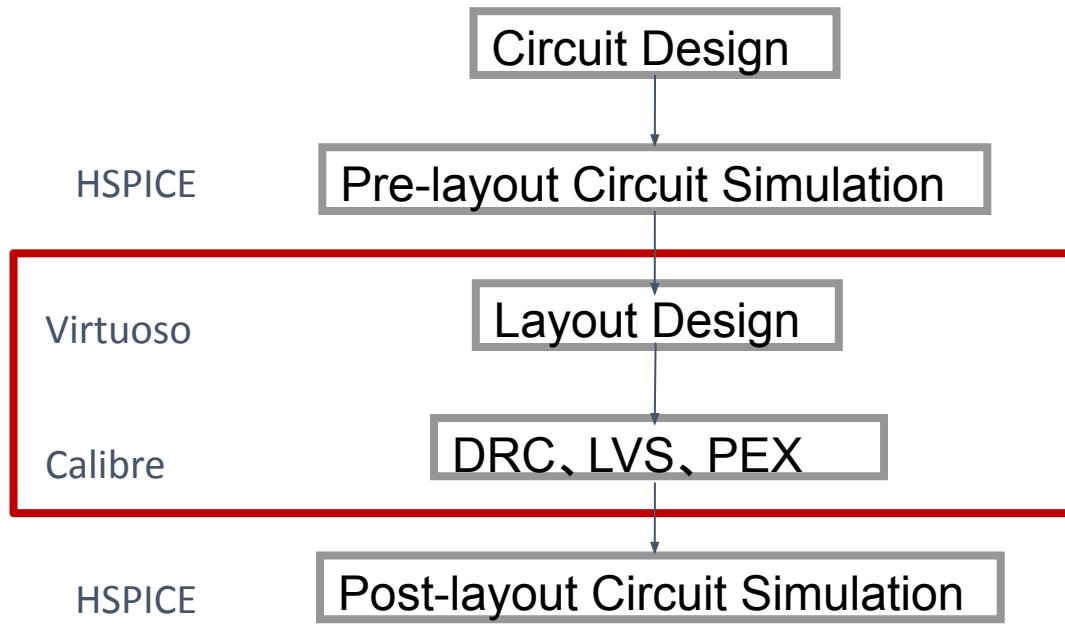
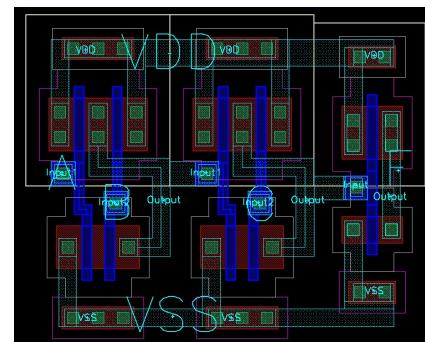


Figure 2.55 Final circuit for the bubble-pushing example



# Outline

- Environment Setup
- Virtuoso
- Inverter
- DRC & LVS
- Project

# Outline

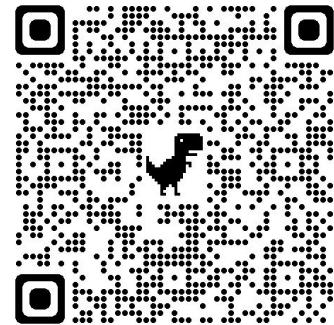
- Environment Setup

- Virtuoso
- Inverter
- DRC & LVS
- Project

# Environment Setup

## CAD Server Account Application

- 指導老師或授課老師: 何宗易
- 申請帳號類別: 課程修課學生
- 課程名稱: 積體電路設計概論
- [https://docs.google.com/forms/d/1FOoLwbFab\\_nJ-RL0py8MLrndOQLPOtIsZBp\\_mS-cp4Y](https://docs.google.com/forms/d/1FOoLwbFab_nJ-RL0py8MLrndOQLPOtIsZBp_mS-cp4Y)



# Environment Setup

## Prepared Files

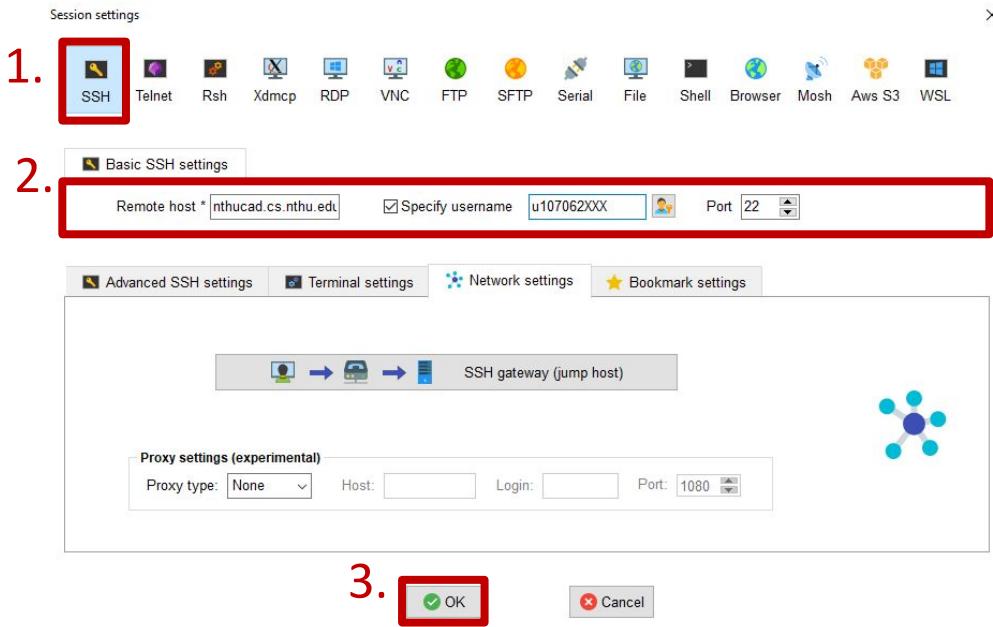
- Download from eeclass
  - <https://eeclass.nthu.edu.tw/>
- Download files
  - Project1.pdf
  - prepared\_file.zip

- 018.tf
  - This file is a large data file that specifies all of the technology-dependent parameters associated with that particular library.
- display.drf
  - Containing layer display information.
- CIC18\_Calibre\_DRC
  - Containing rules used for DRC.
- CIC18\_Calibre\_LVS
  - Containing rules used for LVS.
- .cdsinit
  - Setting searching paths of existing libraries.
- calibre.csh

# Environment Setup

## Workstation Setup

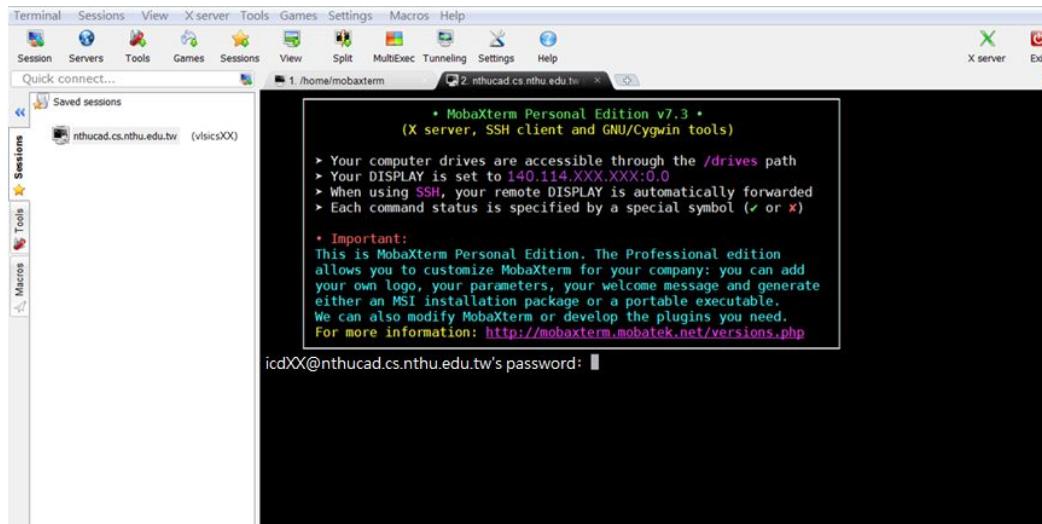
- Enter the following fields
  - Remote host : nthucad.cs.nthu.edu.tw
  - Specify username : u + 學號 (your account)
  - Port : 22
- Click “OK”



# Environment Setup

## Login at the First Time

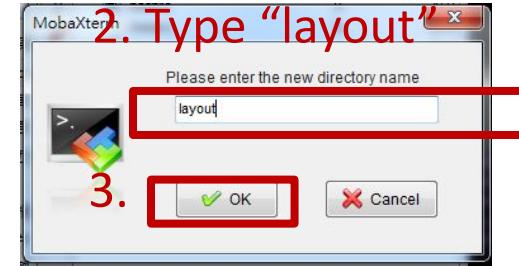
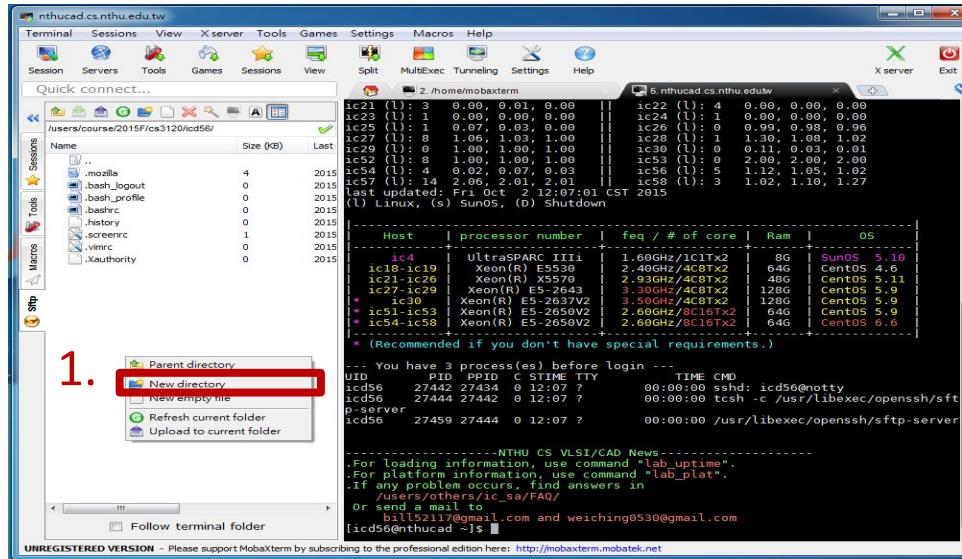
- Key in your **initial password** from your e-mail
- Use **yppasswd** to change your password



# Environment Setup

## Uploading Prepared Files

- Right click to create new directory `layout` or by command line  
**“`mkdir layout`”**

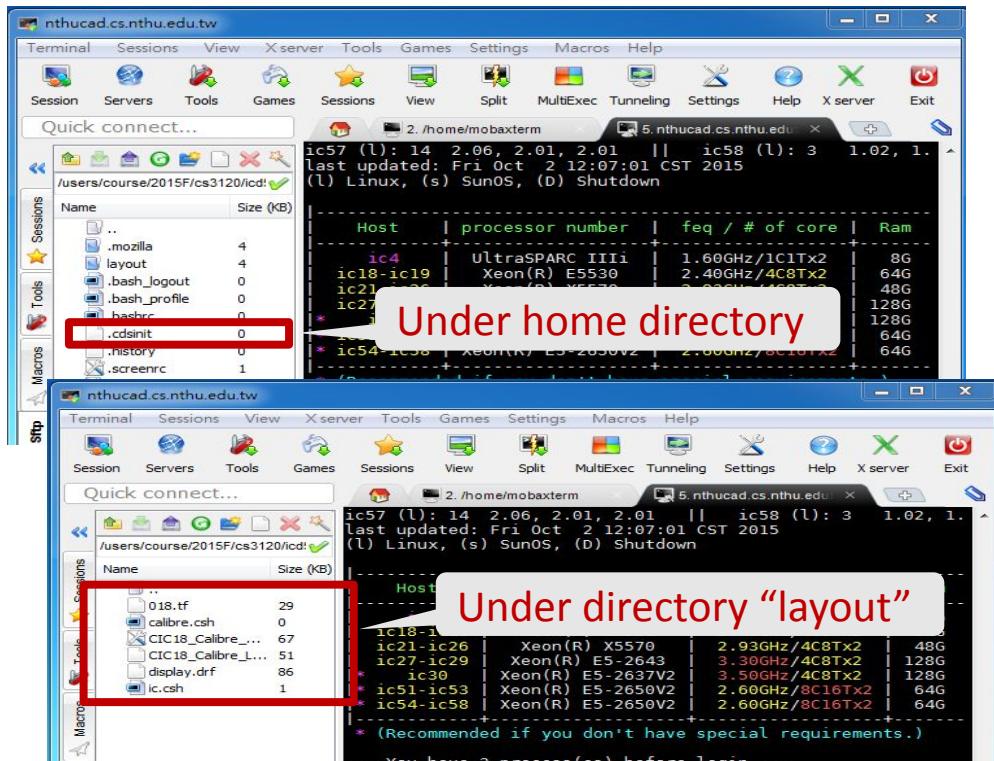


3.

# Environment Setup

## Uploading Prepared Files (Cont.)

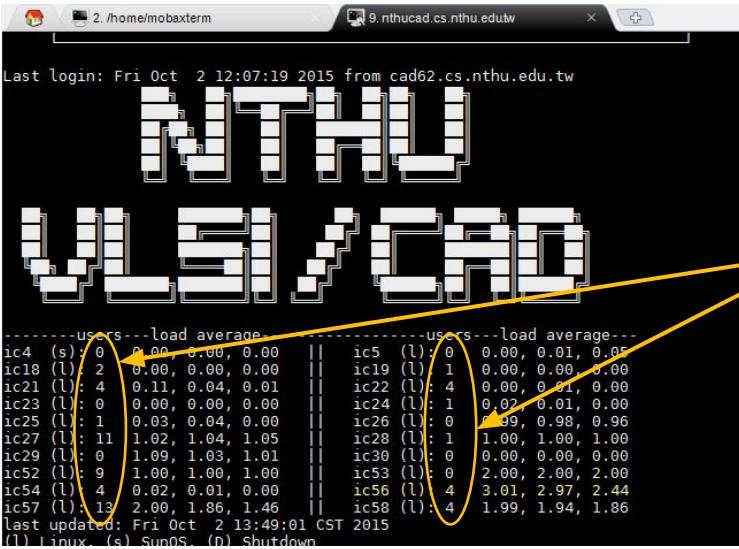
- Home directory
  - .cdsinit
- Directory “layout”
  - 018.tf
  - display.drf
  - CIC18\_Calibre\_DRC
  - CIC18\_Calibre\_LVS
  - calibre.csh
  - ic.csh



# Environment Setup

## Connecting to Workstation

- Select the workstation range from **ic27, ic51, ic56 to ic58**
- Find a workstation that has less user



The screenshot shows a terminal window with two tabs. The active tab displays the NTHU logo in a blocky, pixelated font. Below the logo, a user list is shown:

| User     | Load Average        |
|----------|---------------------|
| ic4 (s)  | 0 0.00, 0.00, 0.00  |
| ic18 (l) | 2 0.00, 0.00, 0.00  |
| ic21 (l) | 4 0.11, 0.04, 0.01  |
| ic23 (l) | 0 0.00, 0.00, 0.00  |
| ic25 (l) | 1 0.03, 0.04, 0.00  |
| ic27 (l) | 11 1.02, 1.04, 1.05 |
| ic29 (l) | 0 1.09, 1.03, 1.01  |
| ic52 (l) | 9 1.00, 1.00, 1.00  |
| ic54 (l) | 4 0.02, 0.01, 0.00  |
| ic57 (l) | 13 2.00, 1.86, 1.46 |
| ic5 (l)  | 0 0.00, 0.01, 0.00  |
| ic19 (l) | 1 0.00, 0.00, 0.00  |
| ic22 (l) | 4 0.00, 0.01, 0.00  |
| ic24 (l) | 1 0.07, 0.01, 0.00  |
| ic26 (l) | 0 0.99, 0.98, 0.96  |
| ic28 (l) | 1 1.00, 1.00, 1.00  |
| ic30 (l) | 0 0.00, 0.00, 0.00  |
| ic53 (l) | 0 2.00, 2.00, 2.00  |
| ic56 (l) | 4 3.01, 2.97, 2.44  |
| ic58 (l) | 4 1.99, 1.94, 1.86  |

A yellow arrow points from the text "# of users on the workstation" to the user count column of the table.

Last login: Fri Oct 2 12:07:19 2015 from cad62.cs.nthu.edu.tw

(l) Linux, (s) SunOS, (d) Shutdown

# Environment Setup

## Connecting to Workstation (Cont.)

- SSH Connection

```
$ ssh -X icXX
```

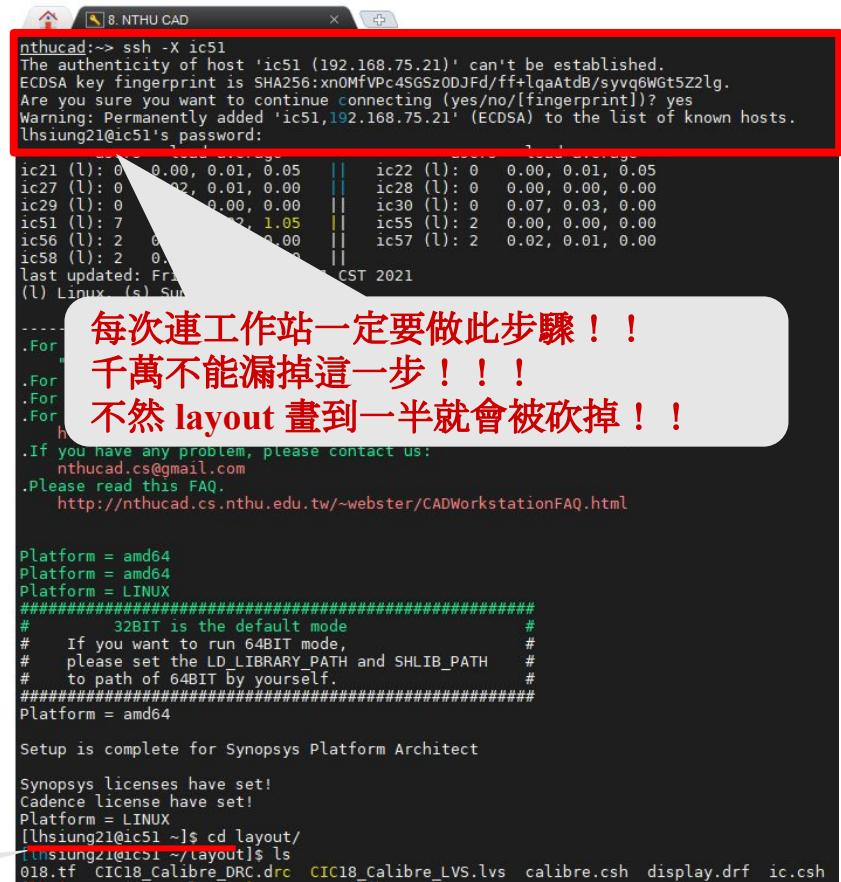
- Go into your working directory layout.

```
$ cd layout
```

- You can use ls command to see all files in the directory.

```
$ ls
```

注意有沒有變成 [XXX@icXX ~]\$



```
nthucad:~> ssh -X ic51
The authenticity of host 'ic51 (192.168.75.21)' can't be established.
ECDSA key fingerprint is SHA256:xn0MfVpc4SGSz0DJFd/ff+lqaAtdB/syvq6WGT5Z2lg.
Are you sure you want to continue connecting (yes/no/[fingerprint])? yes
Warning: Permanently added 'ic51,192.168.75.21' (ECDSA) to the list of known hosts.
lhsiung21@ic51's password:
```

```
ic21 (l): 0 0.00, 0.01, 0.05 ||| ic22 (l): 0 0.00, 0.01, 0.05
ic27 (l): 0 0.02, 0.01, 0.00 ||| ic28 (l): 0 0.00, 0.00, 0.00
ic29 (l): 0 0.00, 0.00, 0.00 ||| ic30 (l): 0 0.07, 0.03, 0.00
ic51 (l): 7 0.02, 1.05 ||| ic55 (l): 2 0.00, 0.00, 0.00
ic56 (l): 2 0.00, 0.00, 0.00 ||| ic57 (l): 2 0.02, 0.01, 0.00
ic58 (l): 2 0.00, 0.00, 0.00 |||
last updated: Fri Jul 24 14:53:21 CST 2021
(l) Linux (s) Sun
```

```
.For
.For
.For
.For
.h
.If you have any problem, please contact us:
    nthucad.cs@gmail.com
.Please read this FAQ.
    http://nthucad.cs.nthu.edu.tw/~webster/CADWorkstationFAQ.html
```

```
Platform = amd64
Platform = amd64
Platform = LINUX
#####
# 32BIT is the default mode
# If you want to run 64BIT mode,
# please set the LD_LIBRARY_PATH and SHLIB_PATH
# to path of 64BIT by yourself.
#####
Platform = amd64

Setup is complete for Synopsys Platform Architect

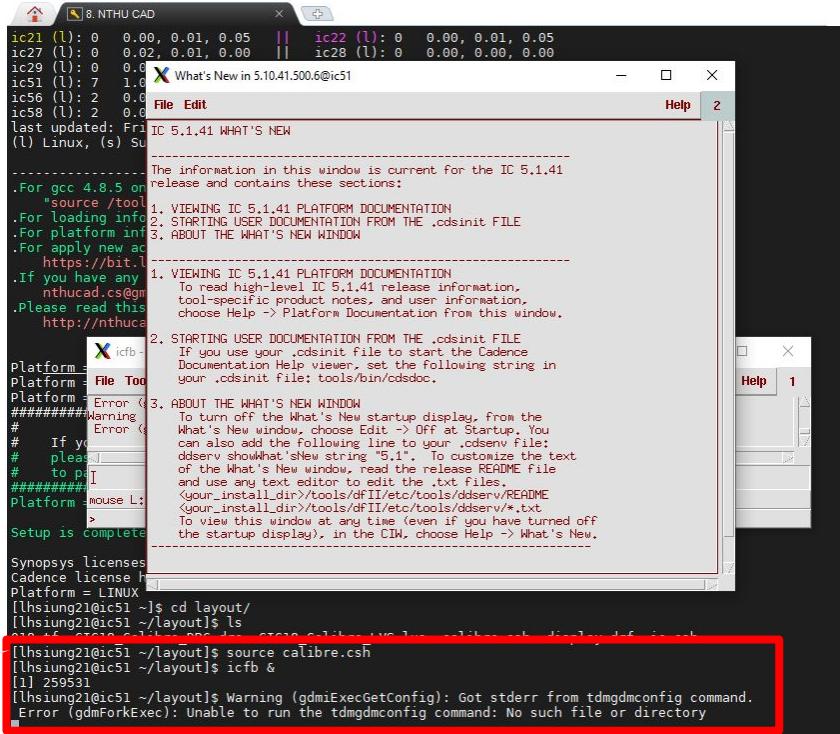
Synopsys licenses have set!
Cadence license have set!
Platform = LINUX
[lhsiung21@ic51 ~]$ cd layout/
[lsiung21@ic51 ~]ls
018.tf CIC18_Calibre_DRC.drc CIC18_Calibre_LVS.lvs calibre.csh display.drf ic.csh
```

# Environment Setup

## Open Platform

- Initialize the environment  
    \$ source calibre.csh
- Open the Viewing IC Platform  
    \$ icfb &

執行完會跳出 VIEWING IC PLATFORM



```
ic21 (l): 0  0.00, 0.01, 0.05 || ic22 (l): 0  0.00, 0.01, 0.05
ic27 (l): 0  0.02, 0.01, 0.00 || ic28 (l): 0  0.00, 0.00, 0.00
ic29 (l): 0  0.0
ic51 (l): 7  1.0
ic56 (l): 2  0.0
ic58 (l): 2  0.0
last updated: Fri IC 5.1.41 WHAT'S NEW
(l) Linux, (s) SunOS
The information in this window is current for the IC 5.1.41
release and contains these sections:
1. VIEWING IC 5.1.41 PLATFORM DOCUMENTATION
2. STARTING USER DOCUMENTATION FROM THE .cdsinit FILE
3. ABOUT THE WHAT'S NEW WINDOW
-----[redacted]-----[redacted]
1. VIEWING IC 5.1.41 PLATFORM DOCUMENTATION
To read high-level IC 5.1.41 release information,
tool-specific product notes, and user information,
choose Help->Platform Documentation from this window.
2. STARTING USER DOCUMENTATION FROM THE .cdsinit FILE
If you use your .cdsinit file to start the Cadence
Documentation Help viewer, set the following string in
your .cdsinit file: tools/bin/cdsdoc.
3. ABOUT THE WHAT'S NEW WINDOW
To turn off the What's New startup display, From the
What's New window, choose Edit->Off at Startup.
You can also add the following line to your .cdsenv file:
ddserv whatshow=shew string "5.1". To customize the text
of the What's New window, read the release README file
and use any text editor to edit the .txt files.
<your_install_dir>/tools/dfII/etc/tools/ddserv/*.txt
To view this window at any time (even if you have turned off
the startup display), in the CIM, choose Help->What's New.
-----[redacted]-----[redacted]
Platform = File Tools
Platform = Error (1)
#####
# Warning
# Error (1)
# If you
# please
# to pi
#####
Platform = mouse L:
Setup is complete
Synopsys licenses
Cadence license
Platform = LINUX
[lhsiung2@ic51 ~]$ cd layout/
[lhsiung2@ic51 ~]/layout$ ls
[lhsiung2@ic51 ~]/layout$ source calibre.csh
[lhsiung2@ic51 ~]/layout$ icfb &
[1] 259531
[lhsiung2@ic51 ~]/layout$ Warning (gdmExecGetConfig): Got stderr from tdmgdmcconfig command.
>Error (gdmForExec): Unable to run the tdmgdmcconfig command: No such file or directory
```

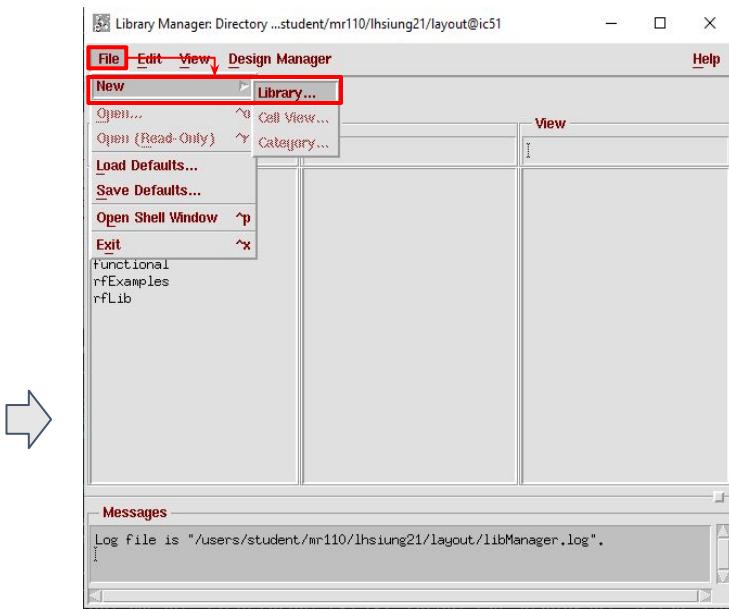
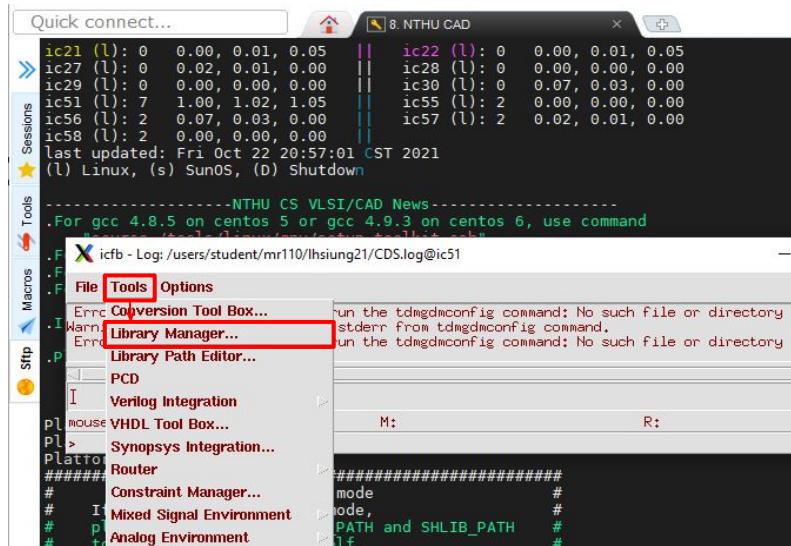
# Outline

- Environment Setup
- Virtuoso
- Inverter
- DRC & LVS
- Project

# Virtuoso

## Open Virtuoso

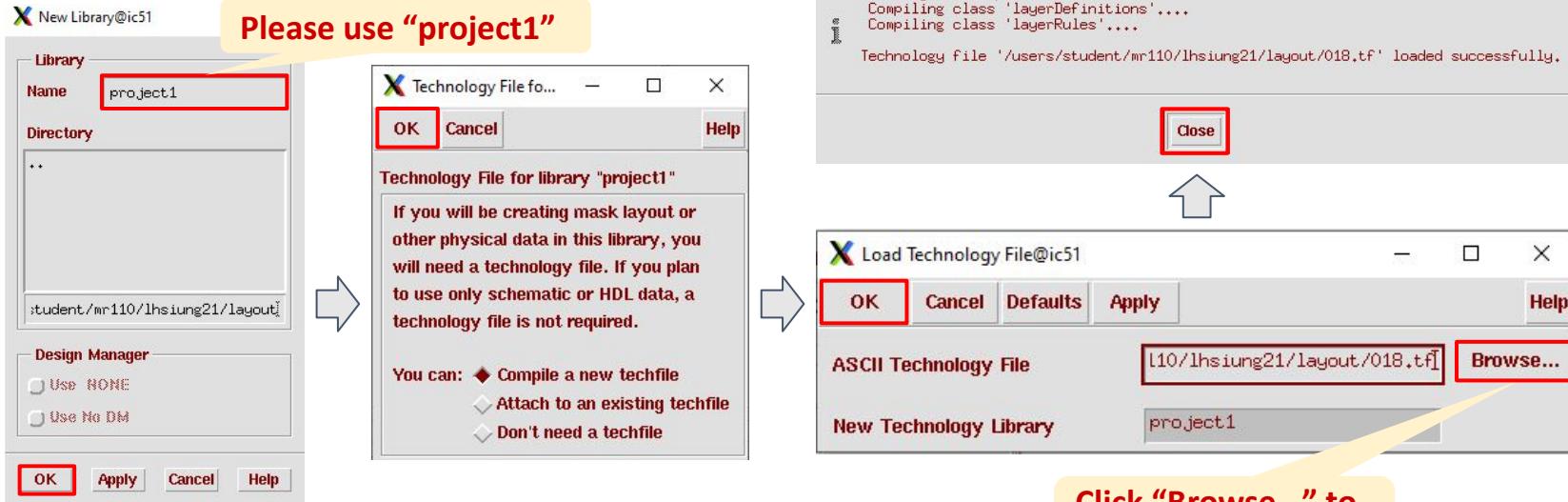
- Tool -> Library Manager
- File -> New -> Library



# Virtuoso

## Open Virtuoso (Cont.)

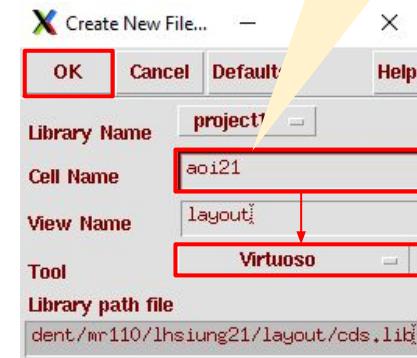
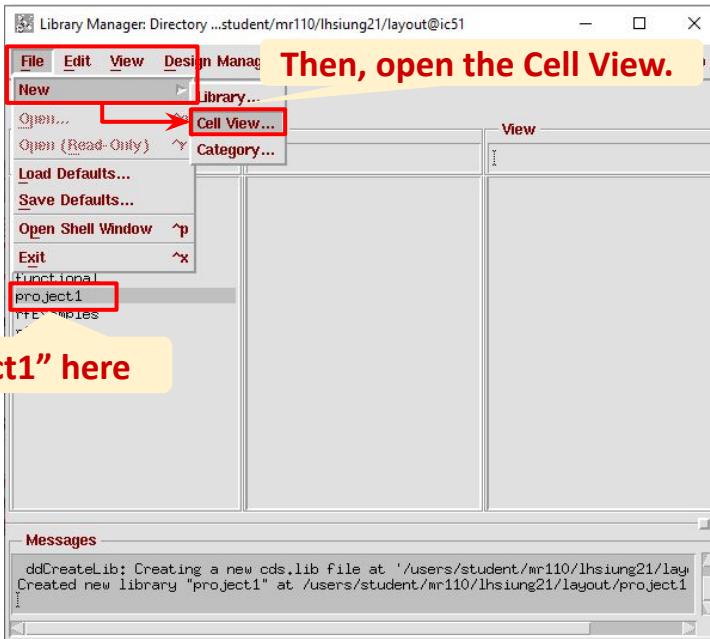
- Follow the steps showing below.



# Virtuoso

## Open Virtuoso (Cont.)

- Follow the steps showing below.



Cell Name: aoi21  
View Name: layout  
Tool: Virtuoso

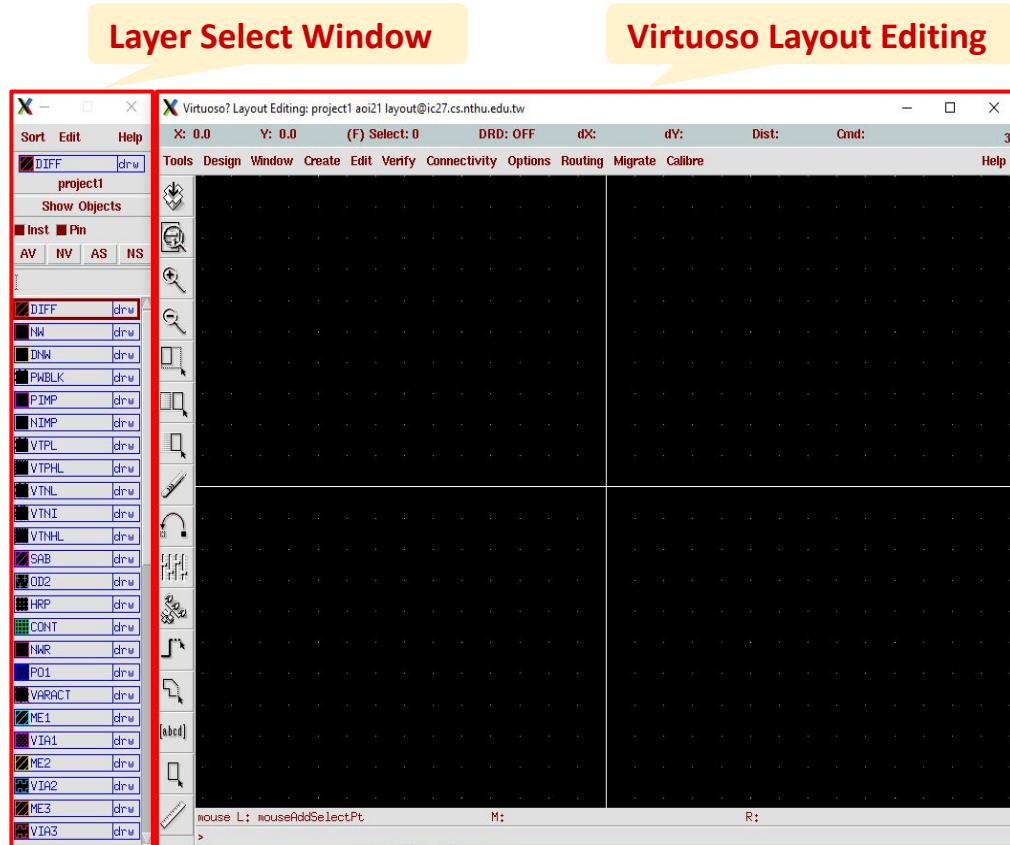
# Virtuoso

## Layer Select Window (LSW)

- The LSW allows you to choose the layer on which you create objects, set which layers are selectable and set layer visibility.

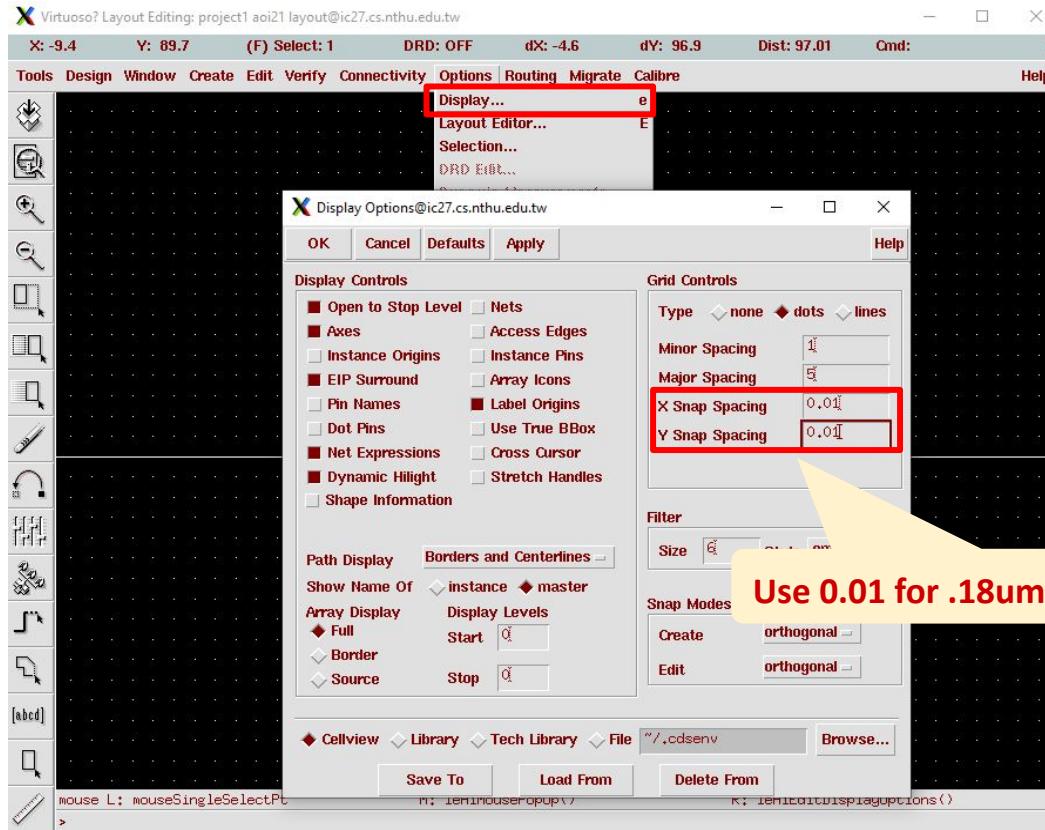
## Virtuoso Layout Editing

- Perform the place and route of the inverter layout.



# Virtuoso

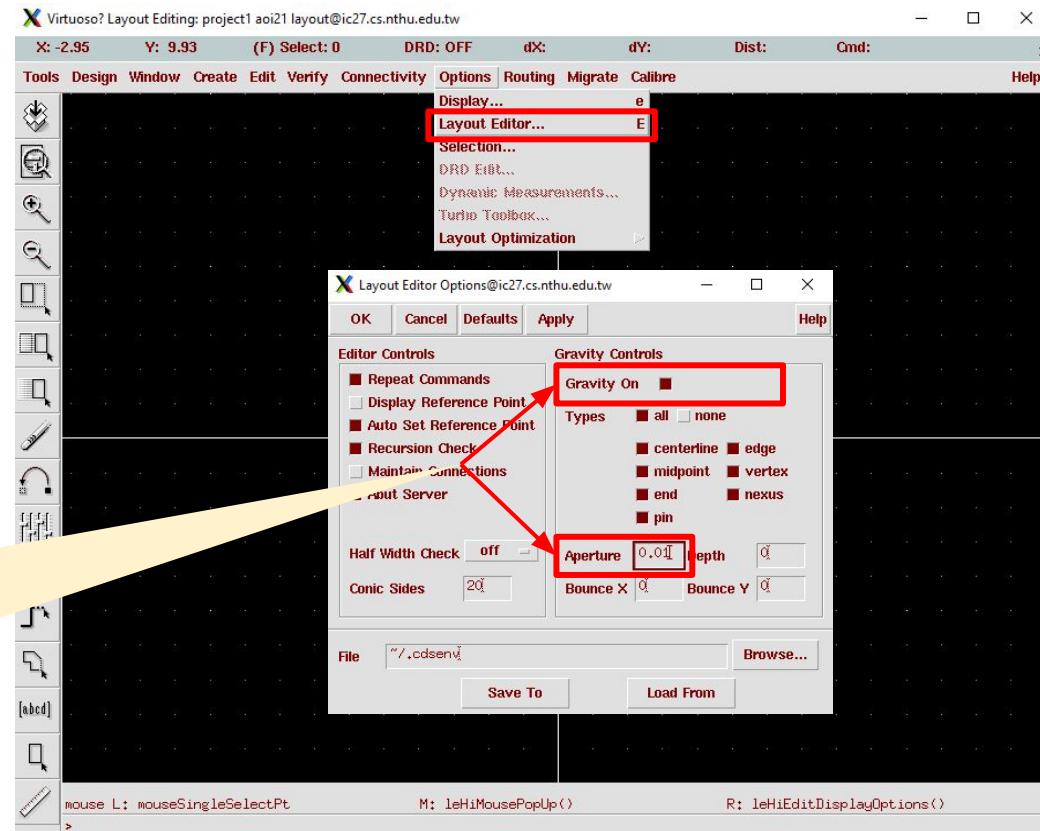
## Accuracy



# Virtuoso

## Accuracy

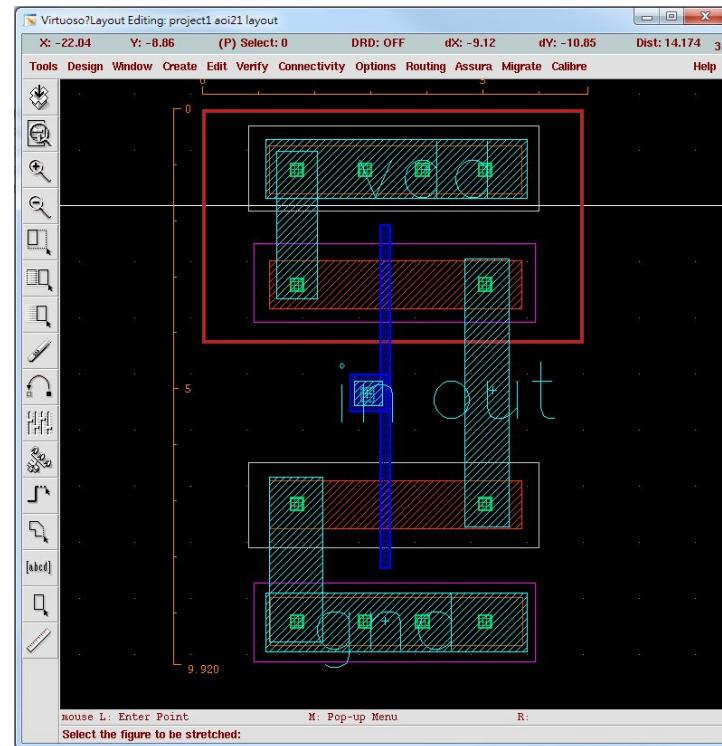
**Snap configuration:**  
Set 0.01um as the snapping distance to an object.  
**Gravity On** to activate the function.



# Virtuoso

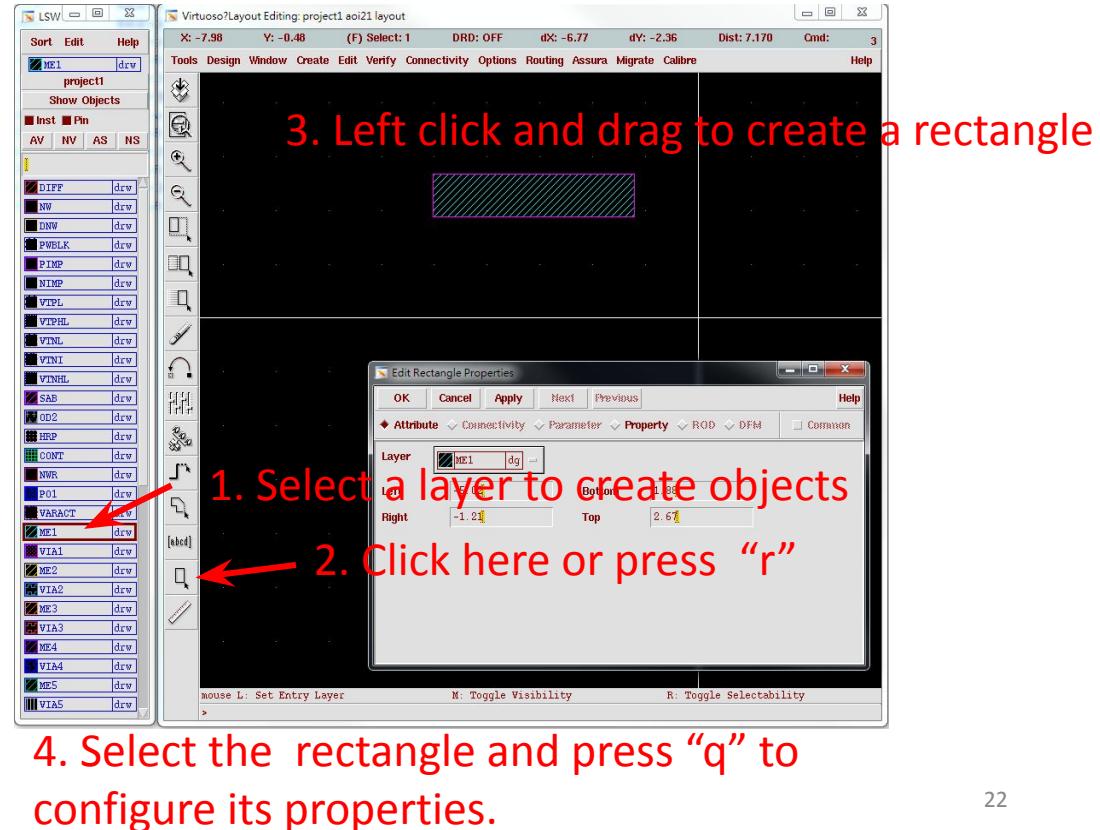
## Ruler

- Layout area
  - Measurement by using **RULER**
  - “k” // Turn ruler
  - “Esc” // Turn off
  - “shift + k” // Erase



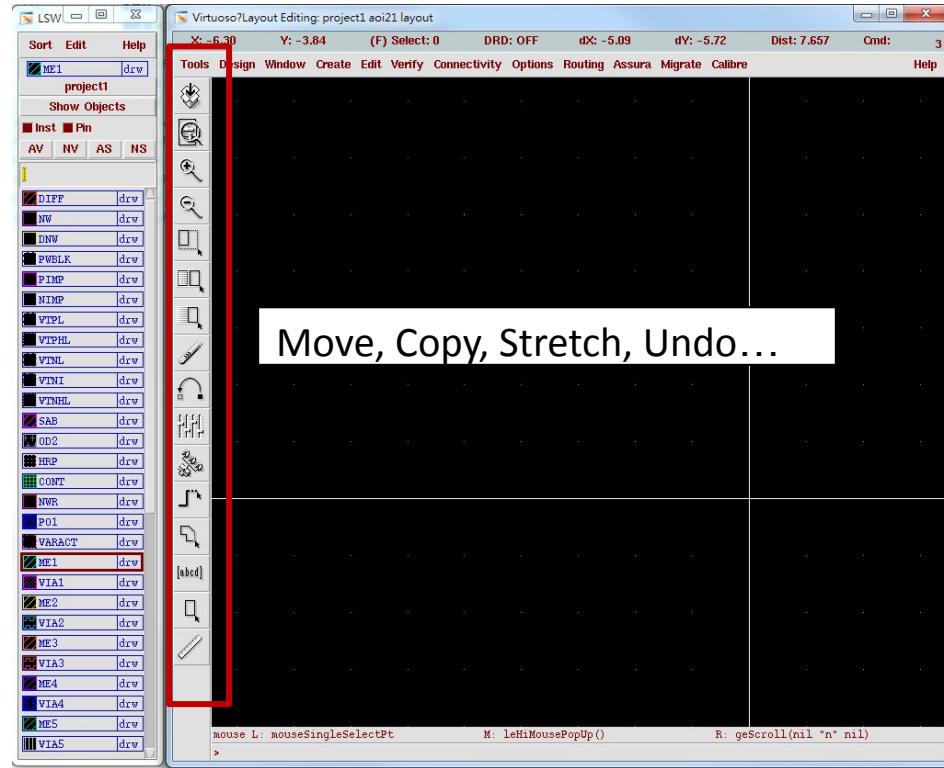
# Virtuoso

## Rectangle



# Virtuoso

## Other Practical Tools



# Virtuoso

## Mouse Click

- Left: Tool dependant
- Middle: Pop-up menu (e.g. Properties)
- Right: Tool dependant

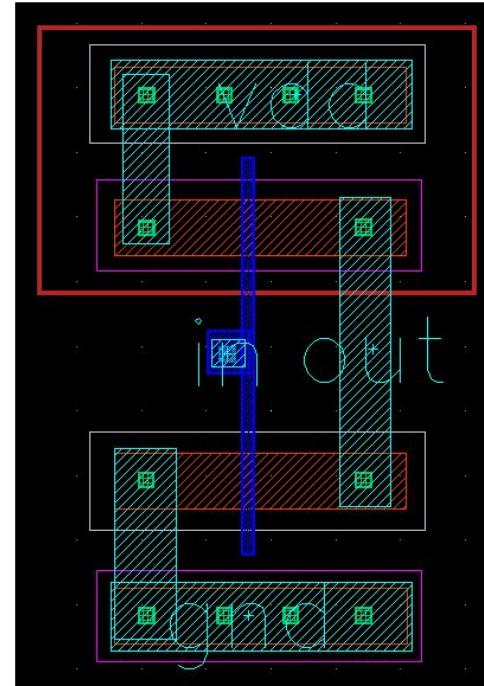
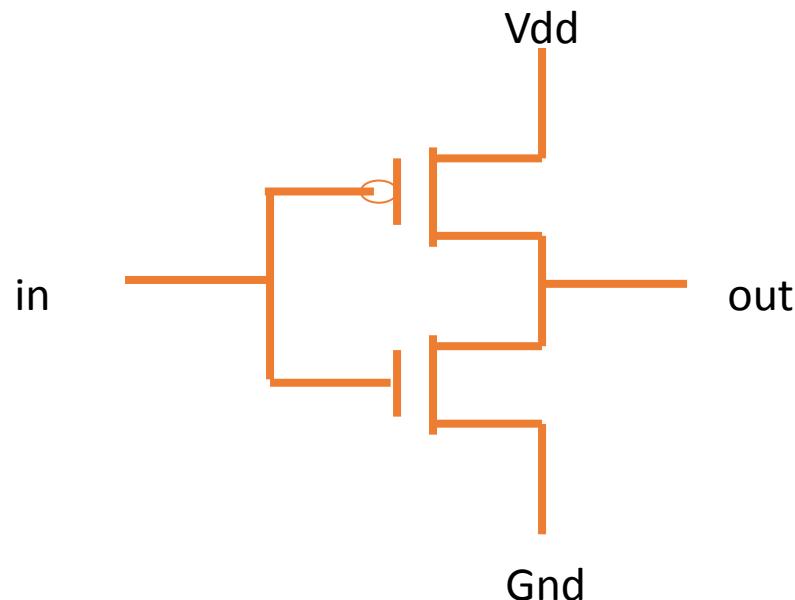


# Outline

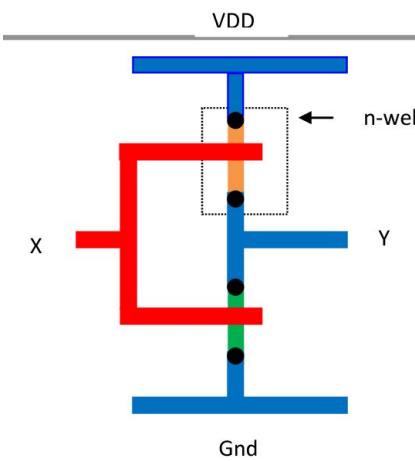
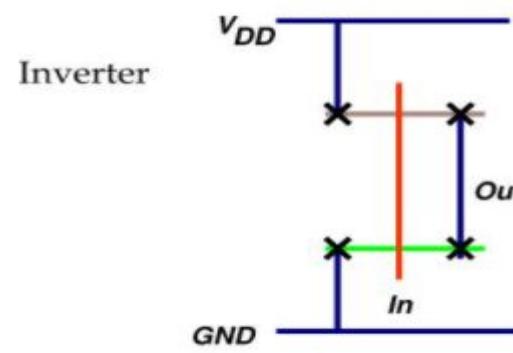
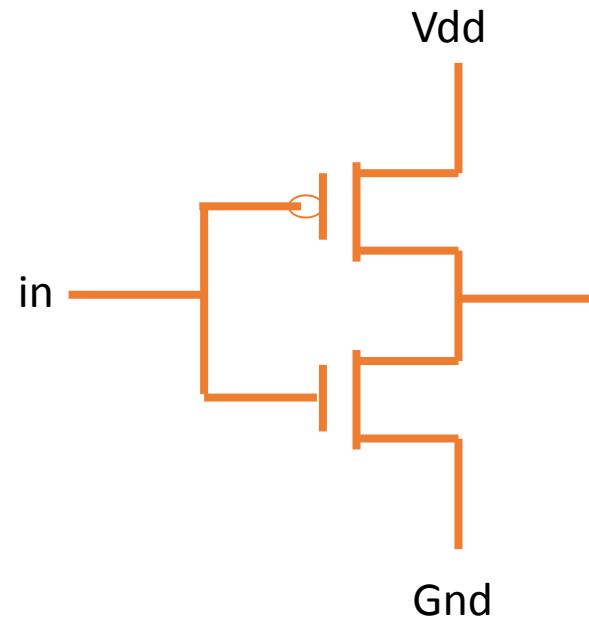
- Environment Setup
- Virtuoso
- Inverter**
- DRC & LVS
- Project

# Inverter layout

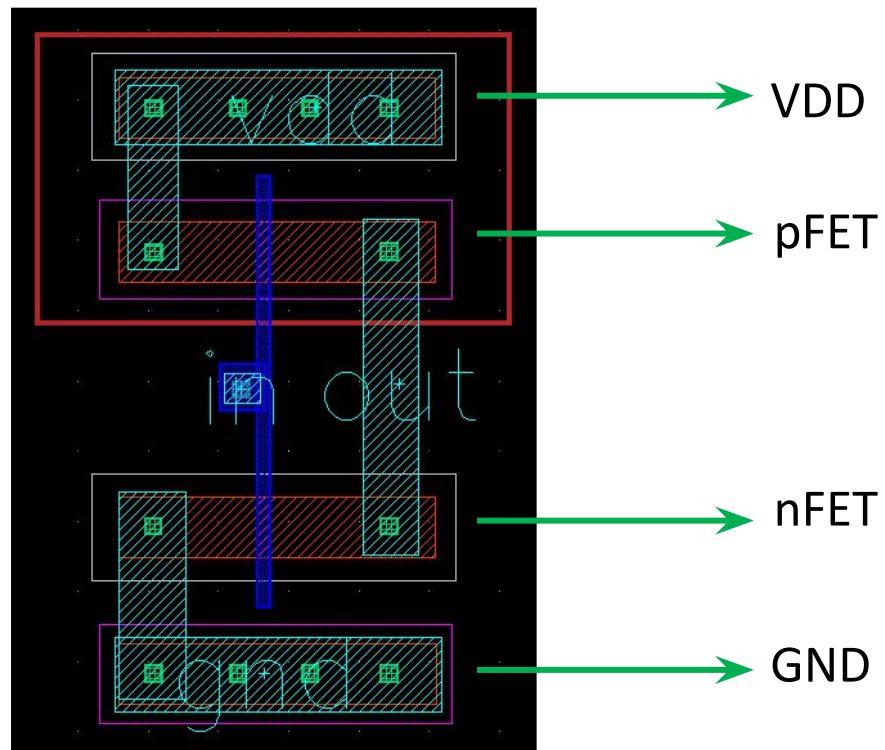
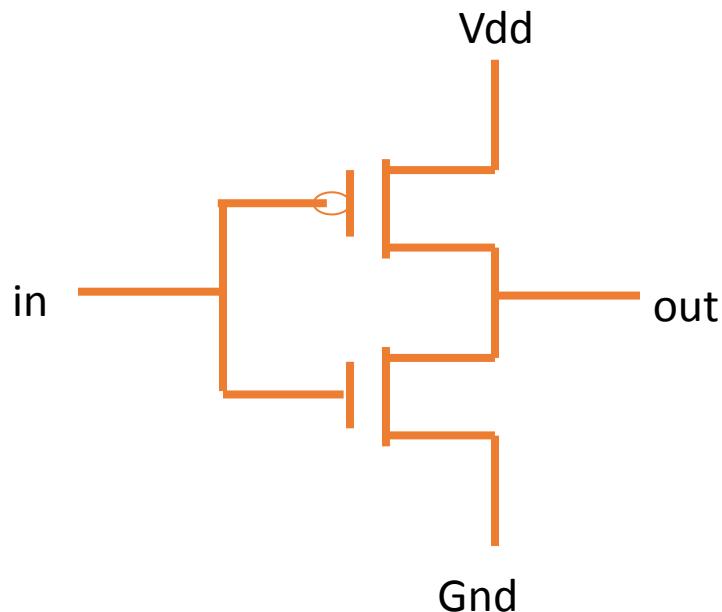
\*以下範例圖片僅供參考，實際 rectangle 大小請遵守後面投影片之規範



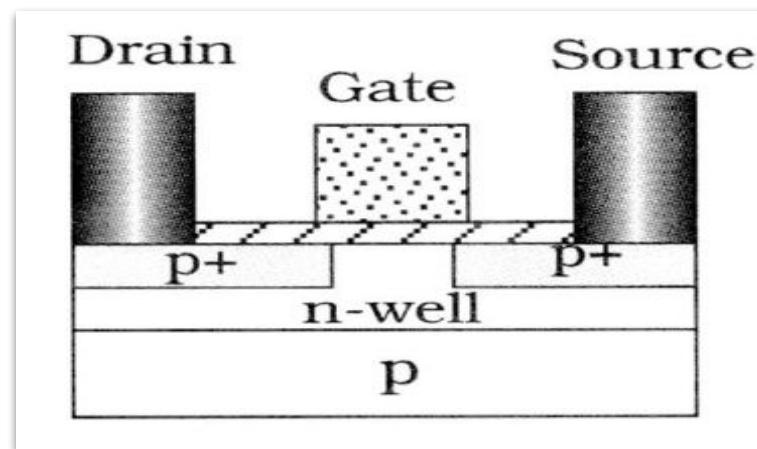
# Inverter stick diagram



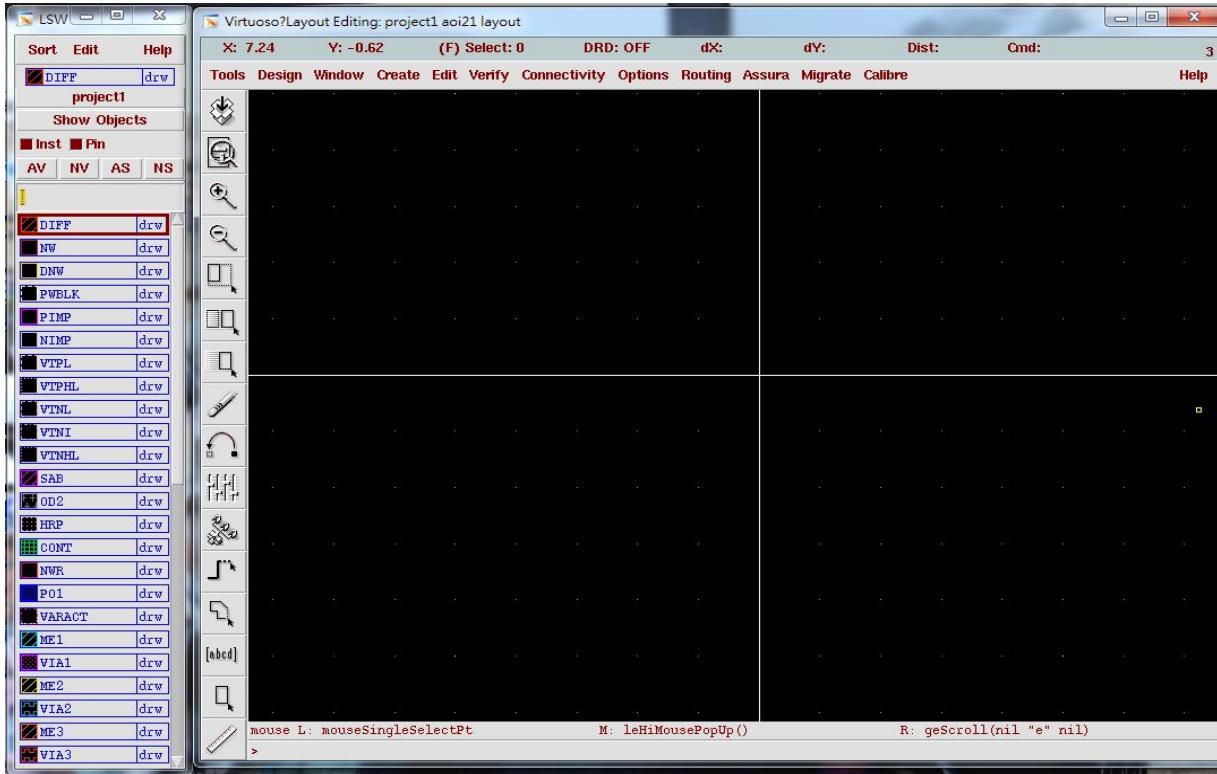
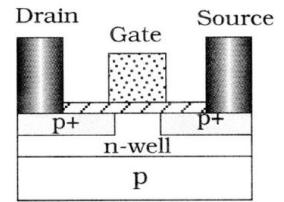
# Inverter layout



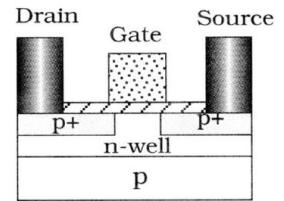
# pFET



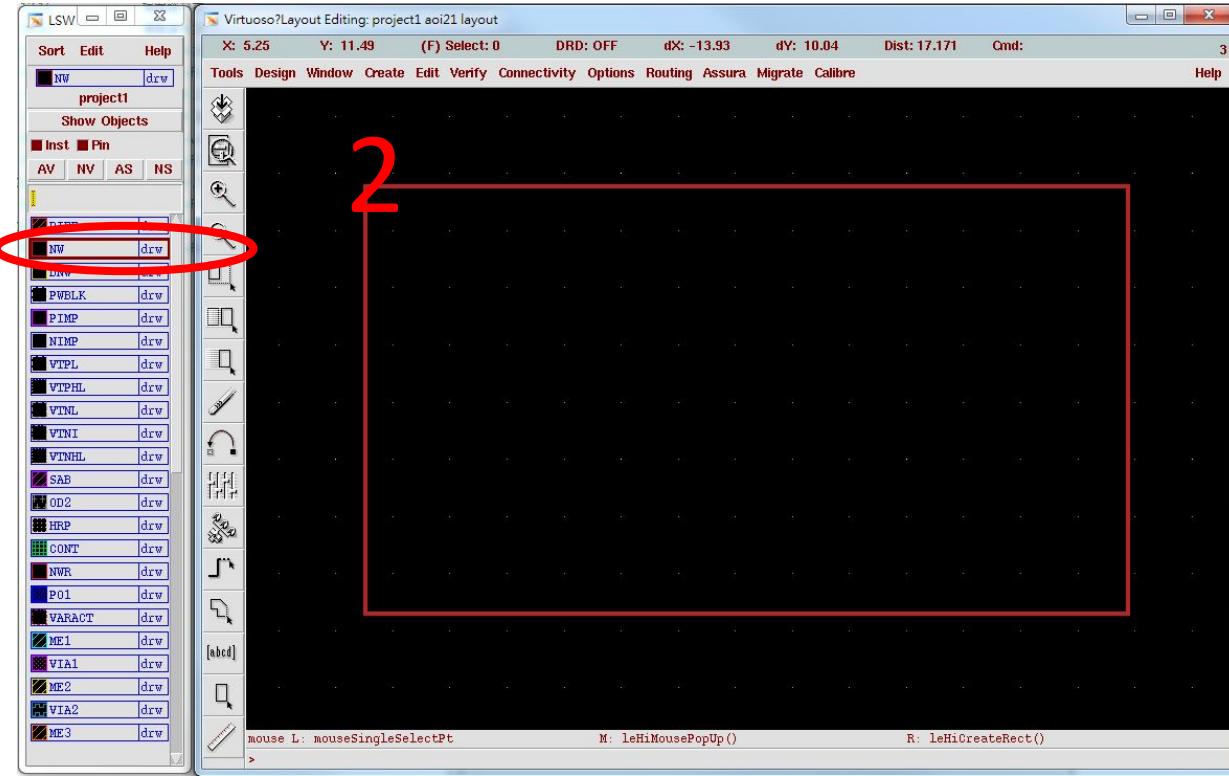
# p-substrate



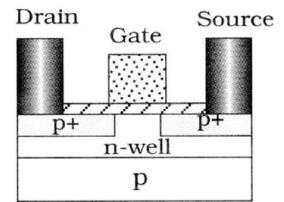
# n-well (NW)



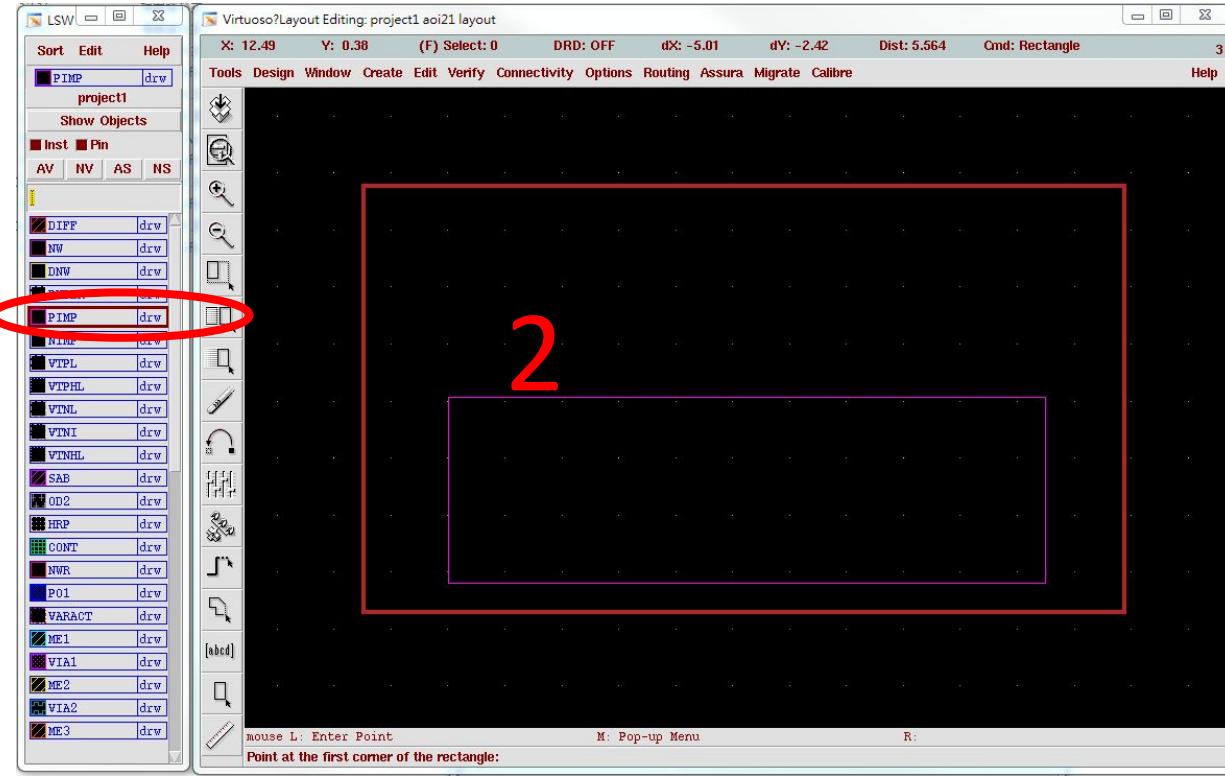
1



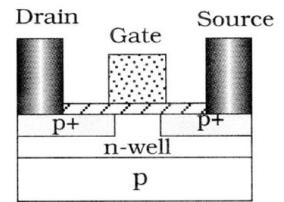
# P+ (PIMP)



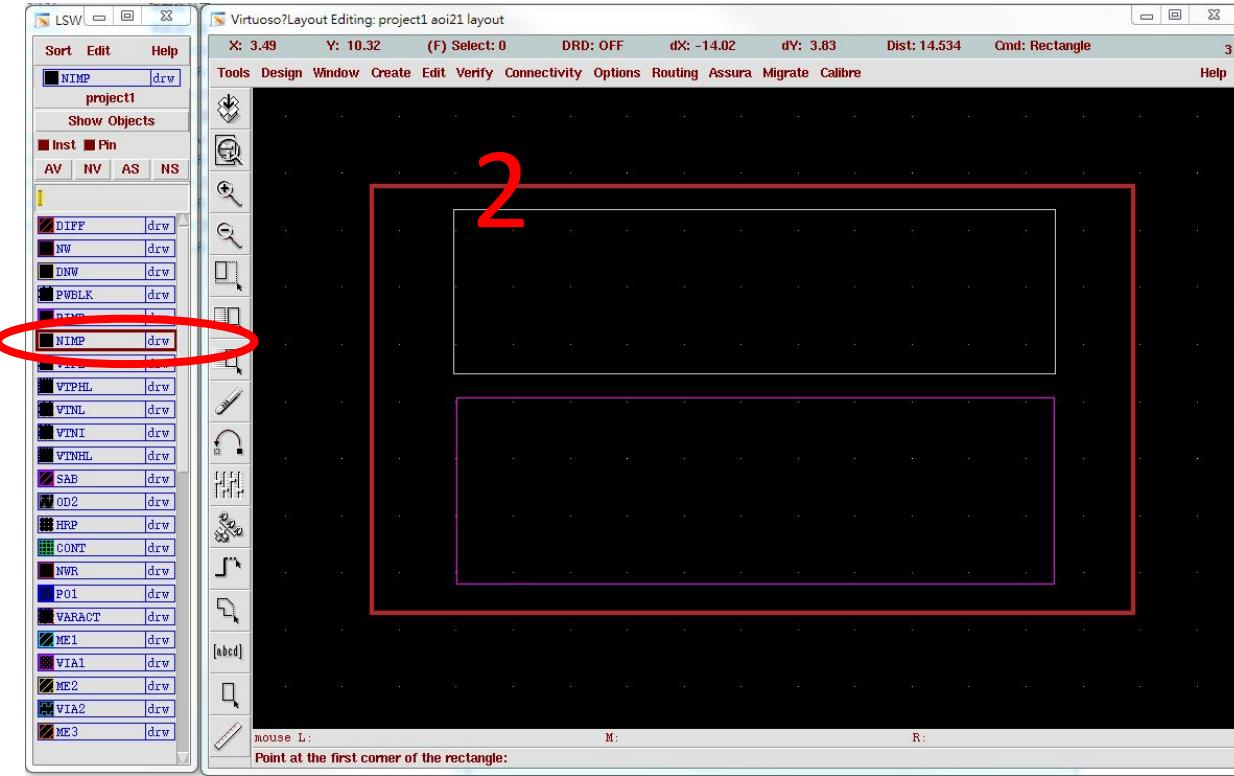
1



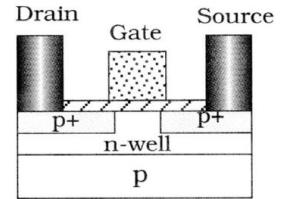
# N+ (NIMP)



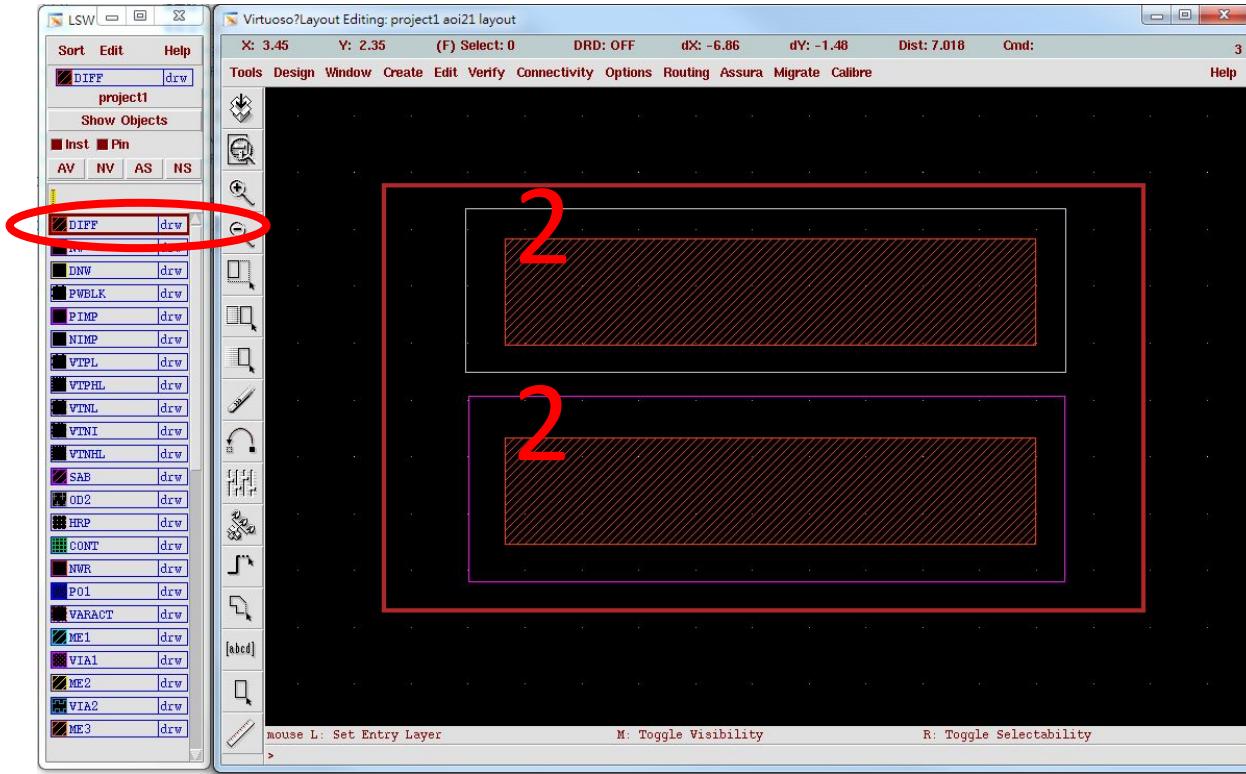
1



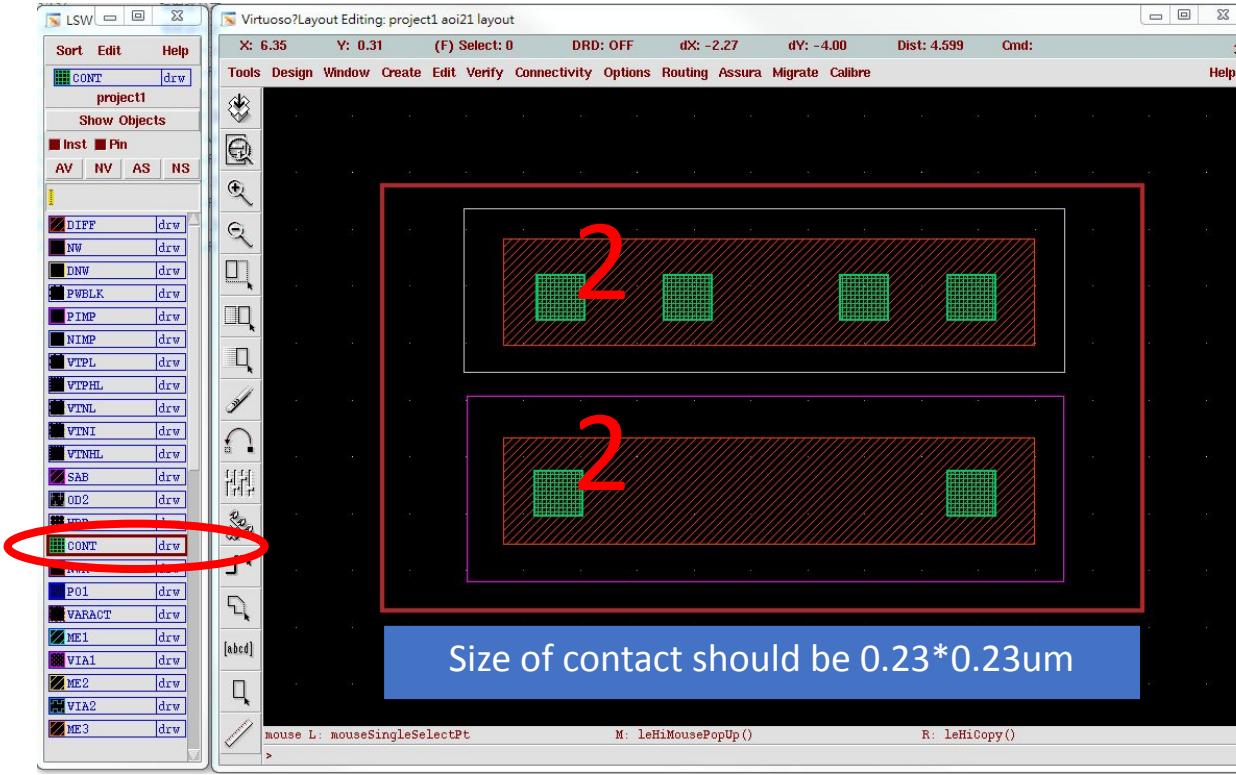
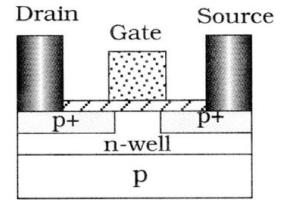
# Active (DIFF)



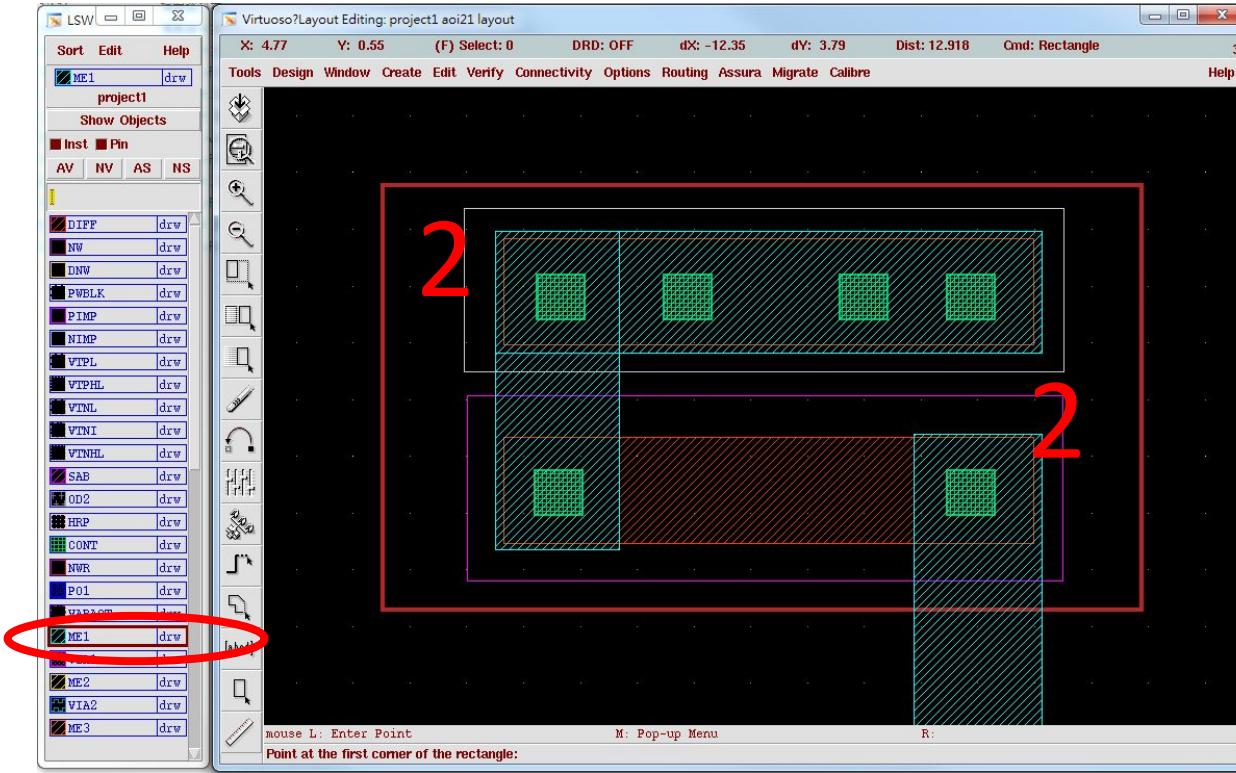
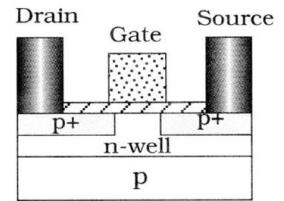
1



# Contact (CONT)

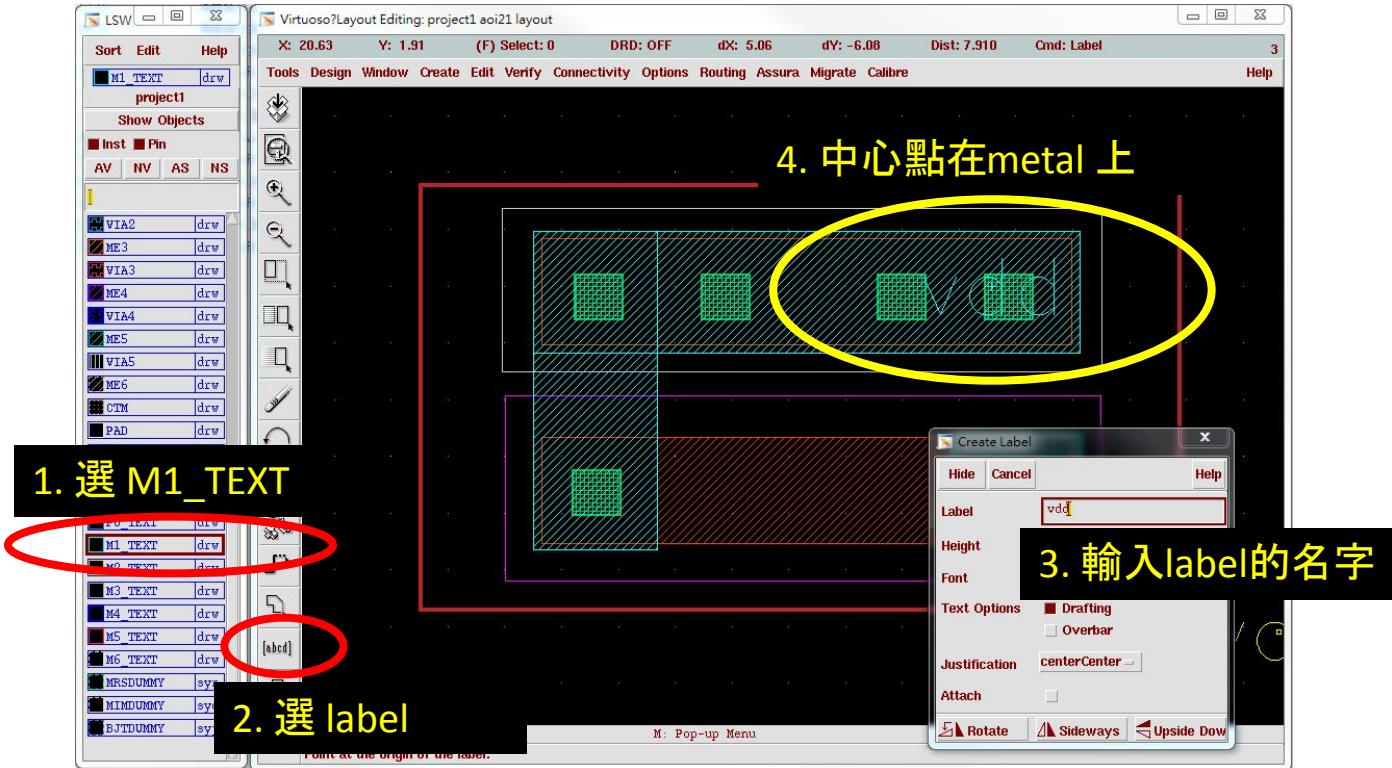
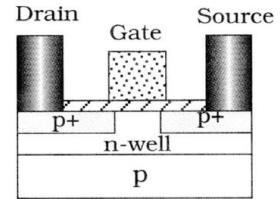


# Metal (ME1)

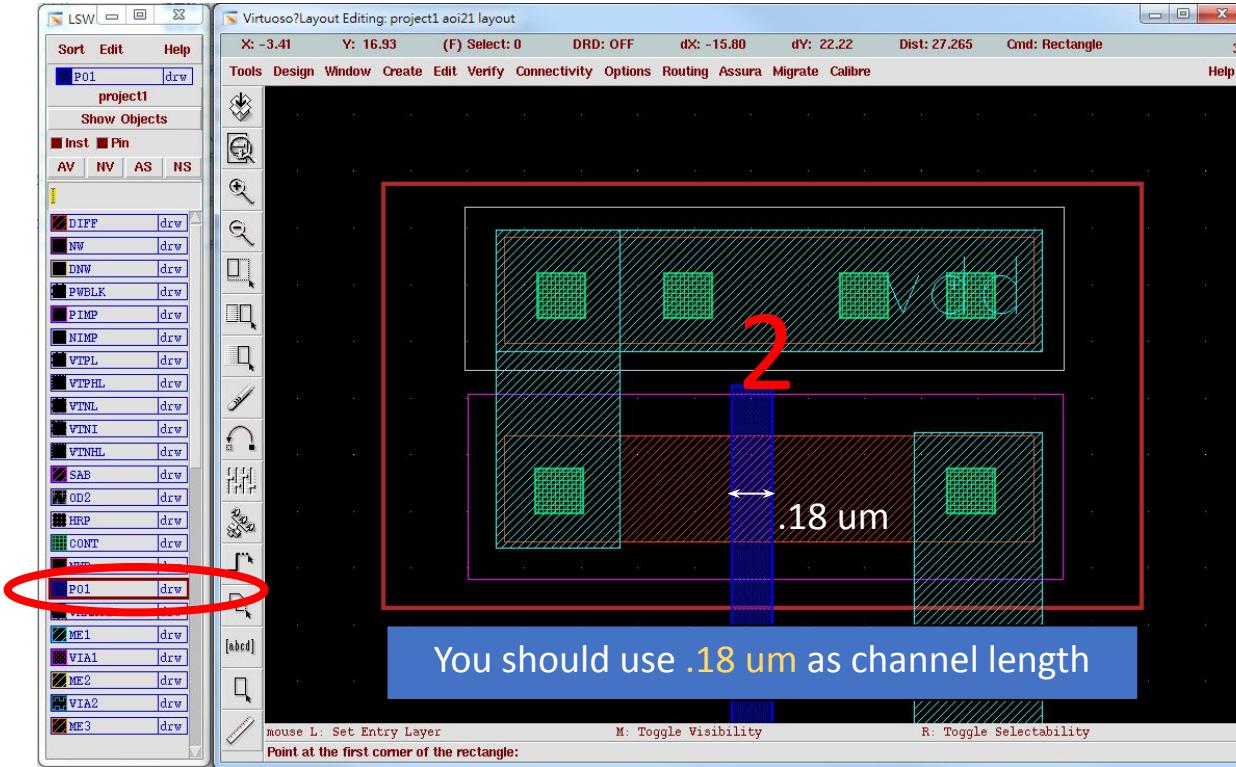
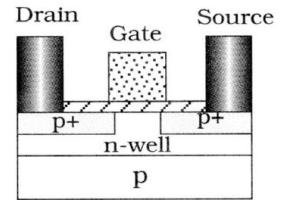


1

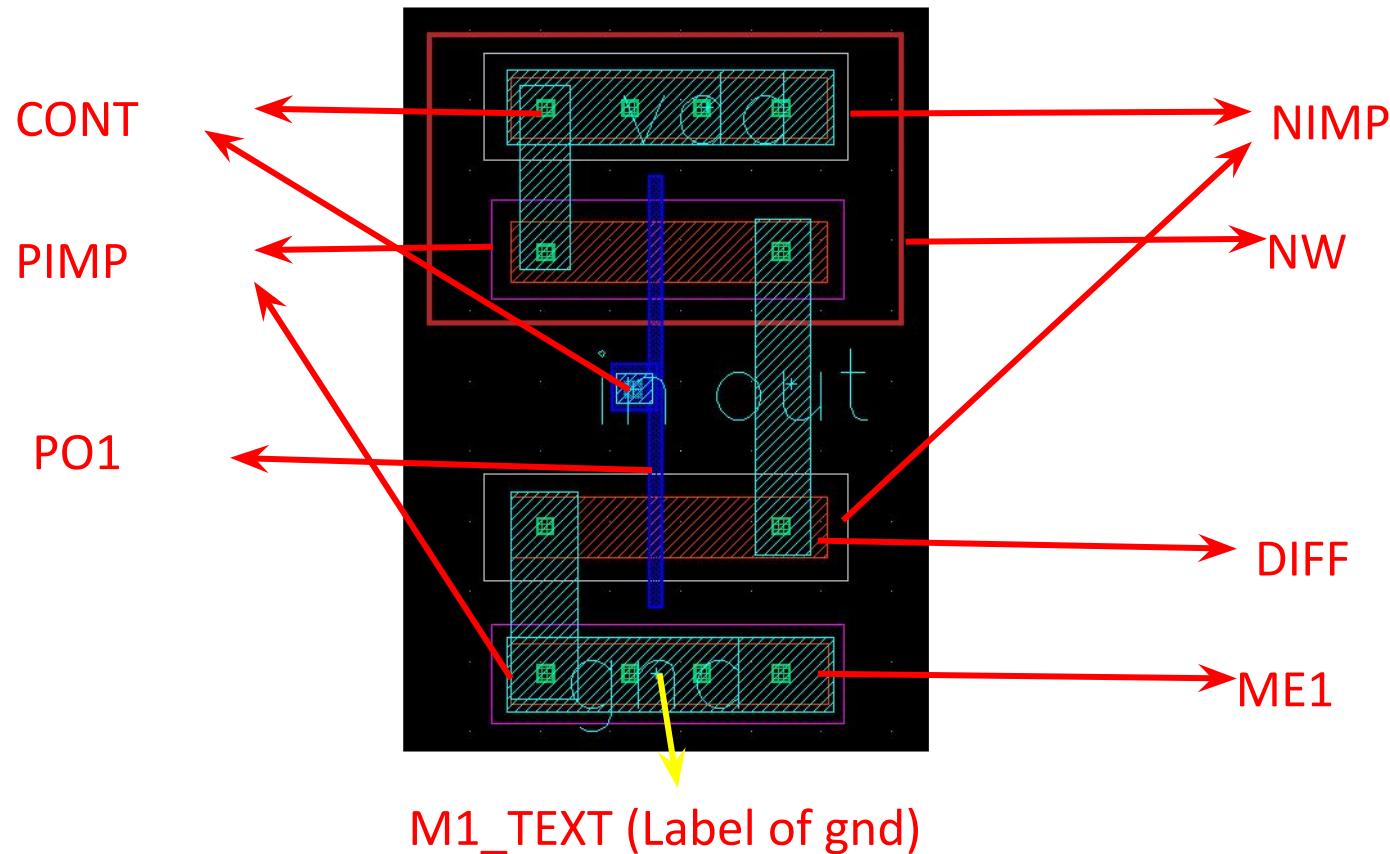
# LABEL (M1\_TEXT)



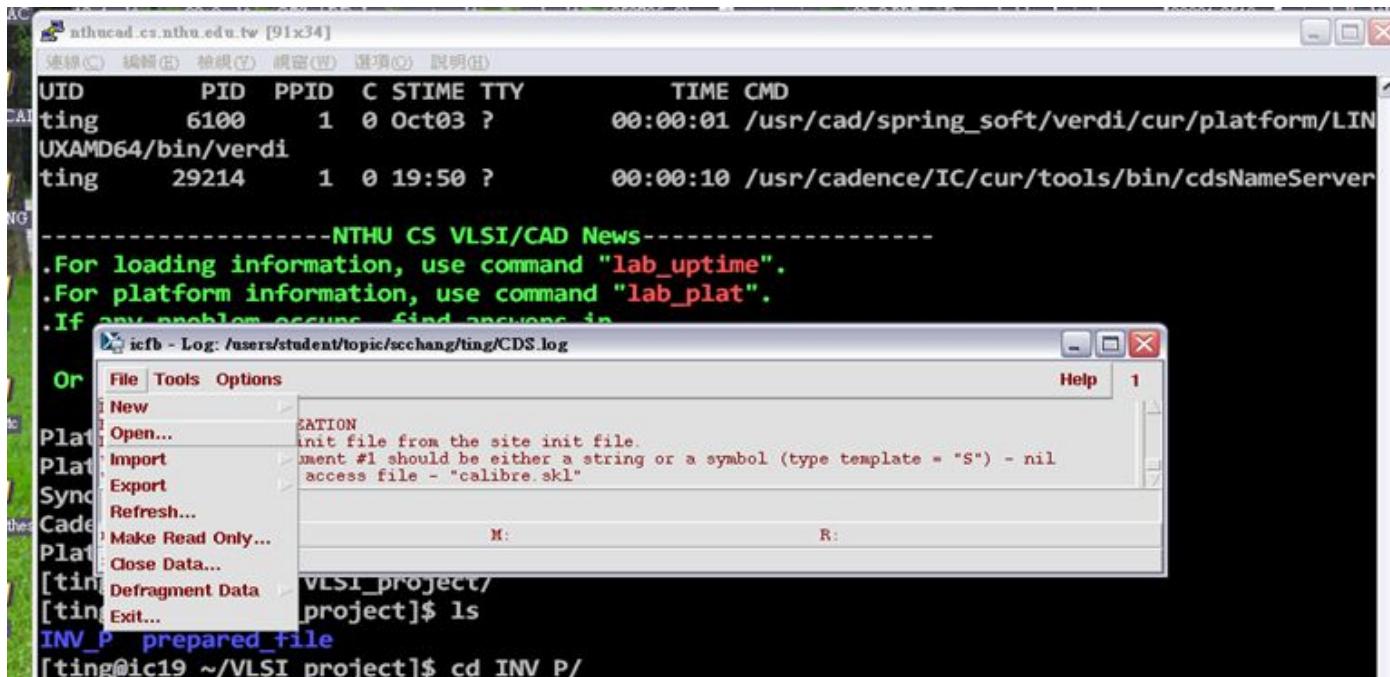
# POLY (PO1)



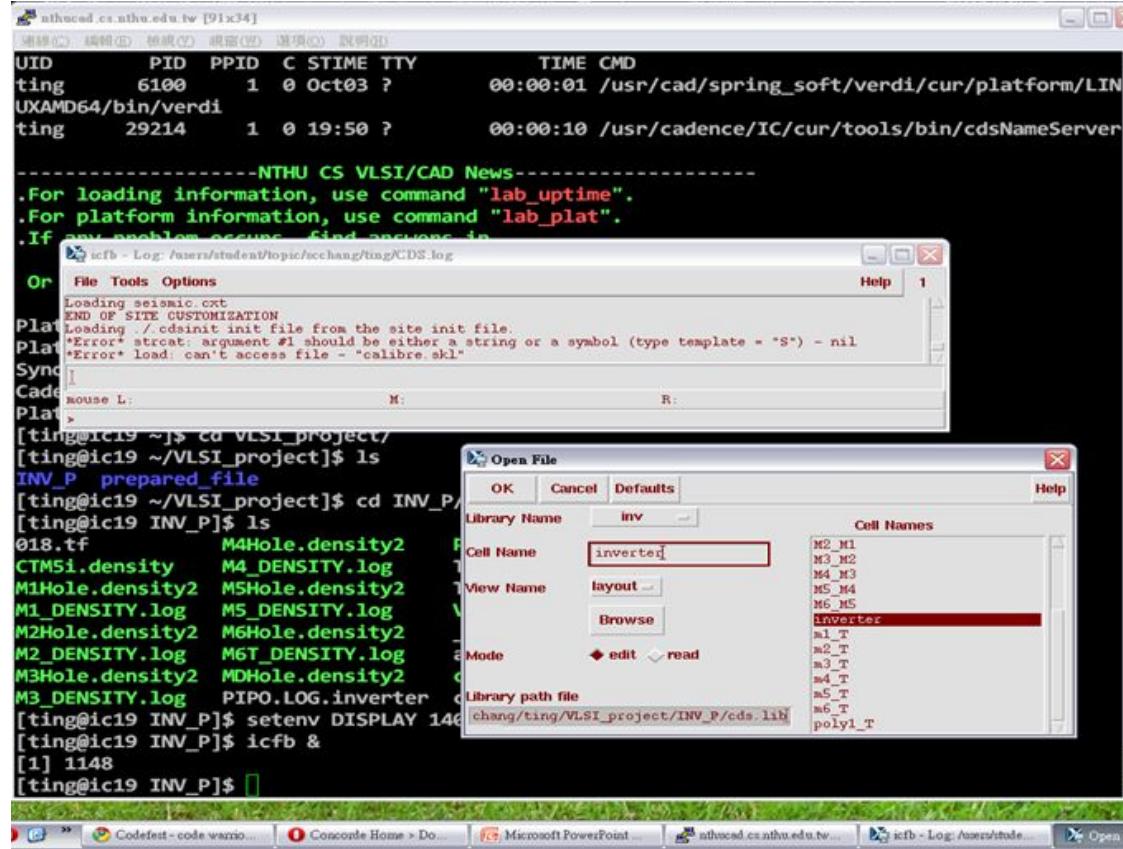
# Inverter layout



# Open Layout File Next Time



# Open Layout File Next Time



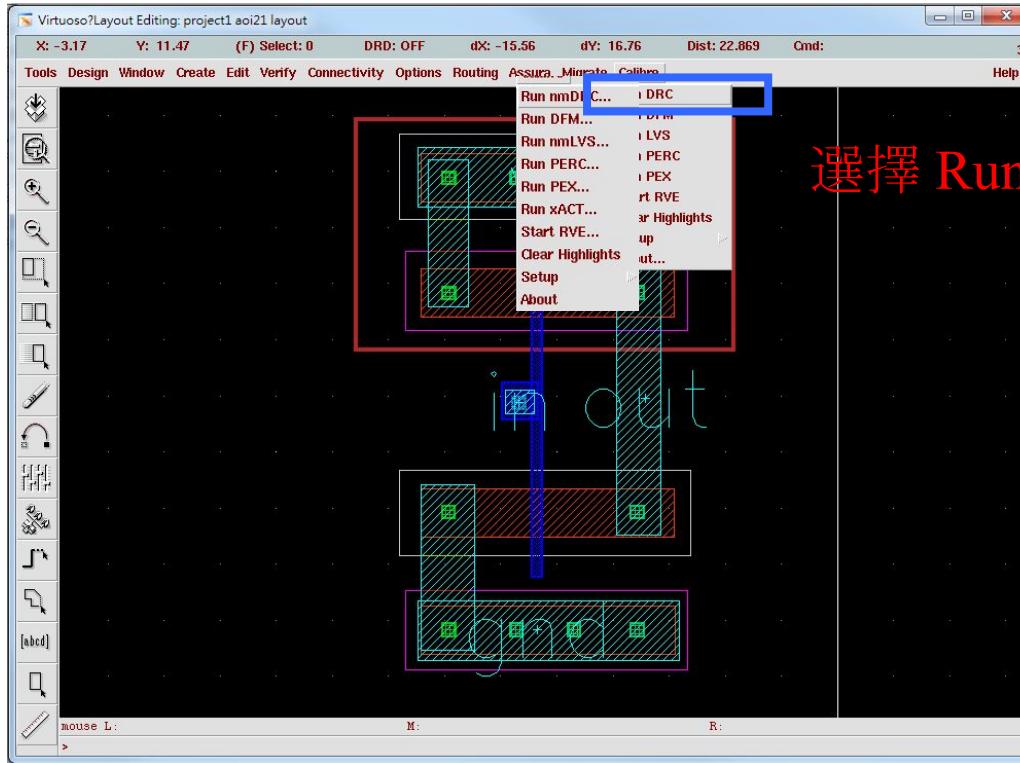
# Outline

- Environment Setup
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- Project

# DRC

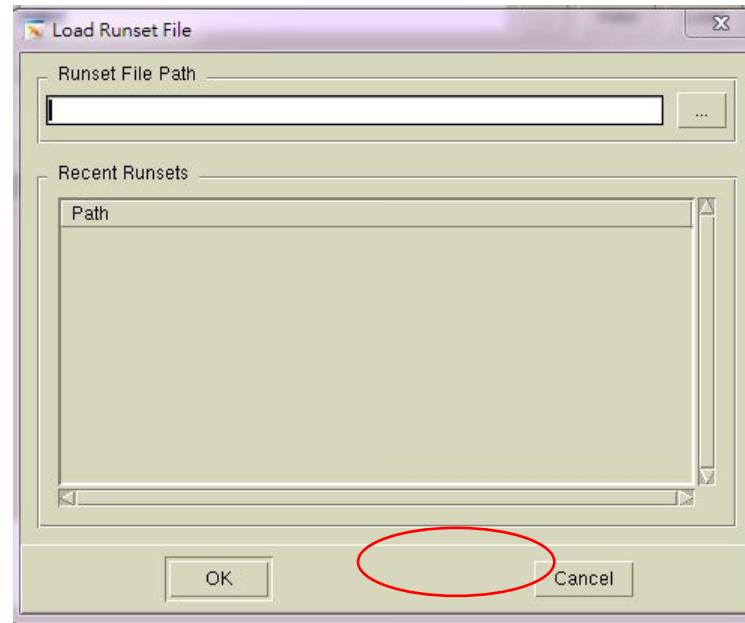
- DRC (Design Rule Check)
- A geometric constraint imposed on circuit board, semiconductor device, and integrated circuit (IC) designers to ensure their designs function properly, reliably, and can be produced with acceptable yield.

# Design Rule Check (DRC)

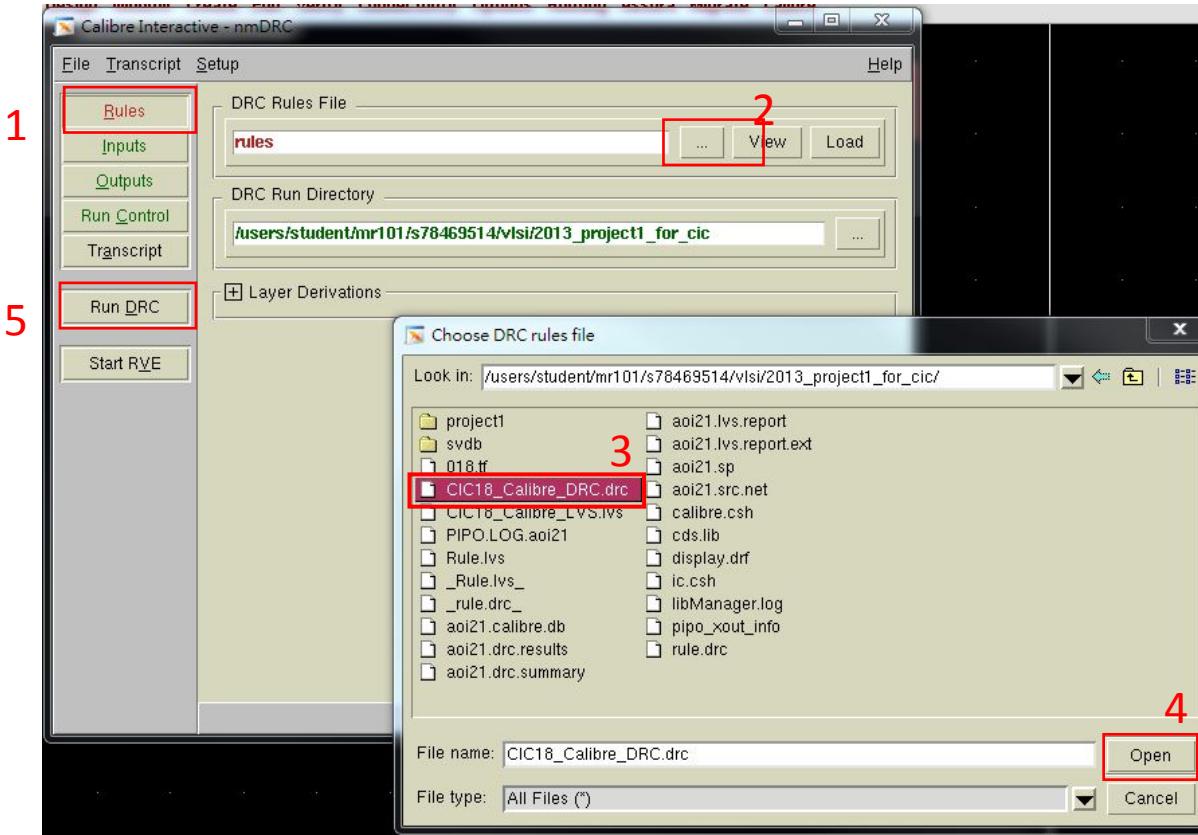


選擇 Run nmDRC

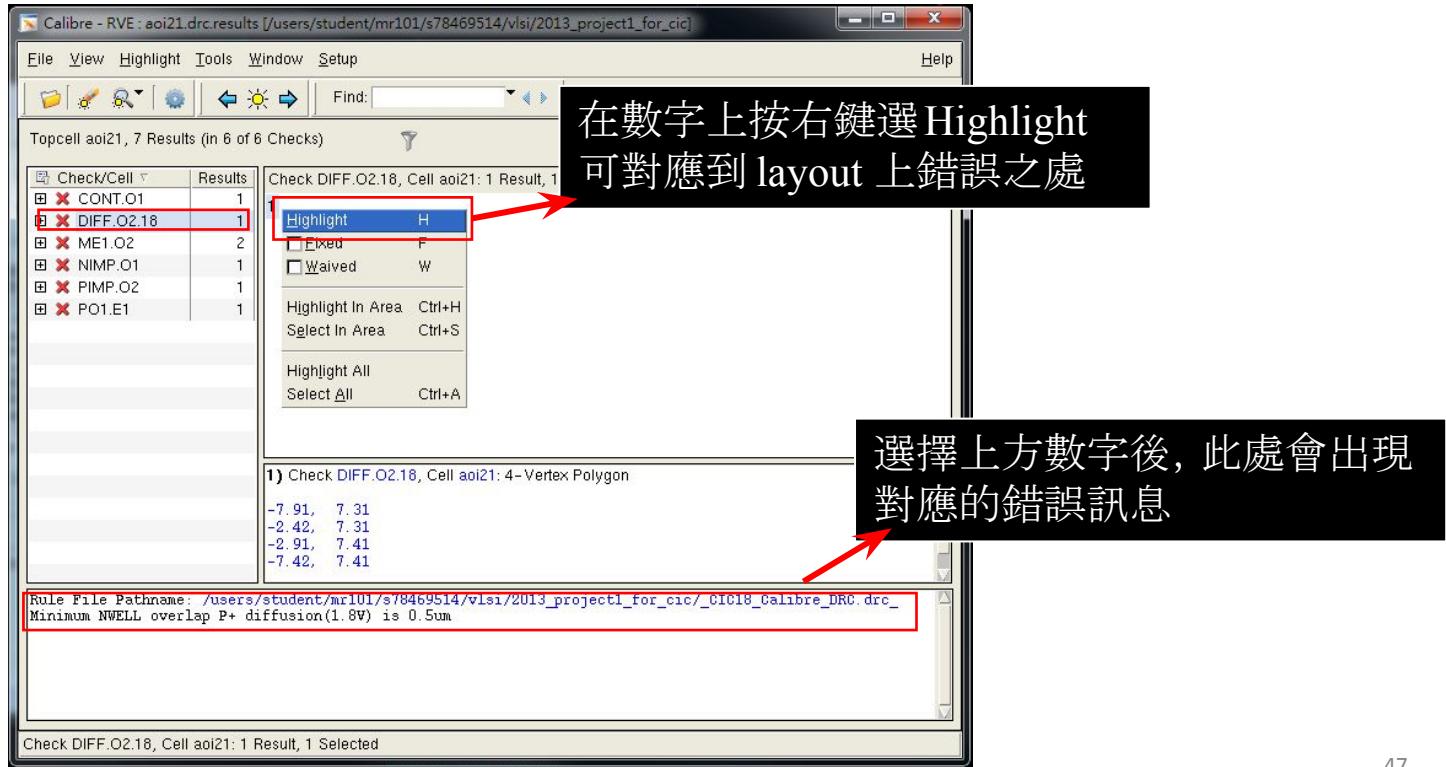
# Design Rule Check (DRC)



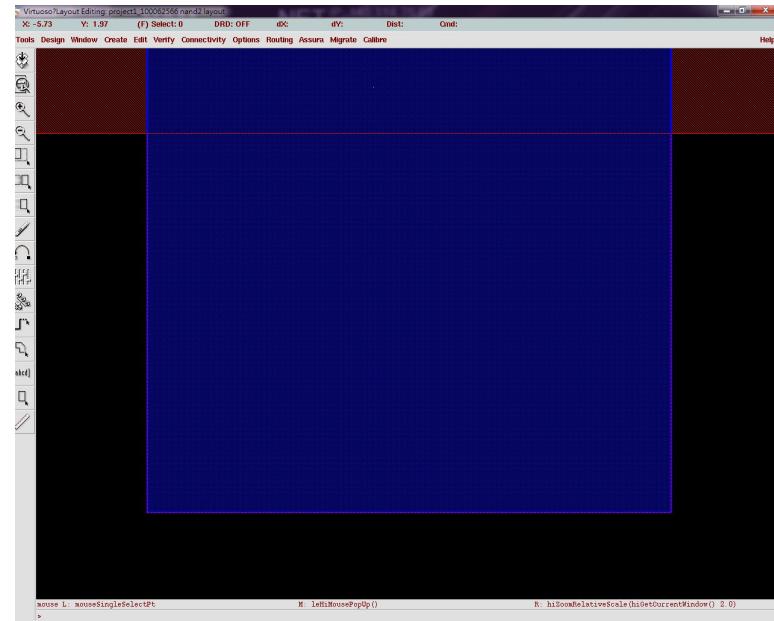
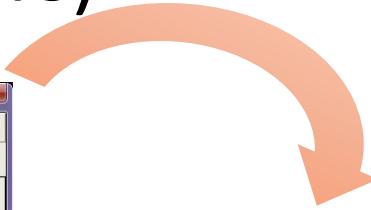
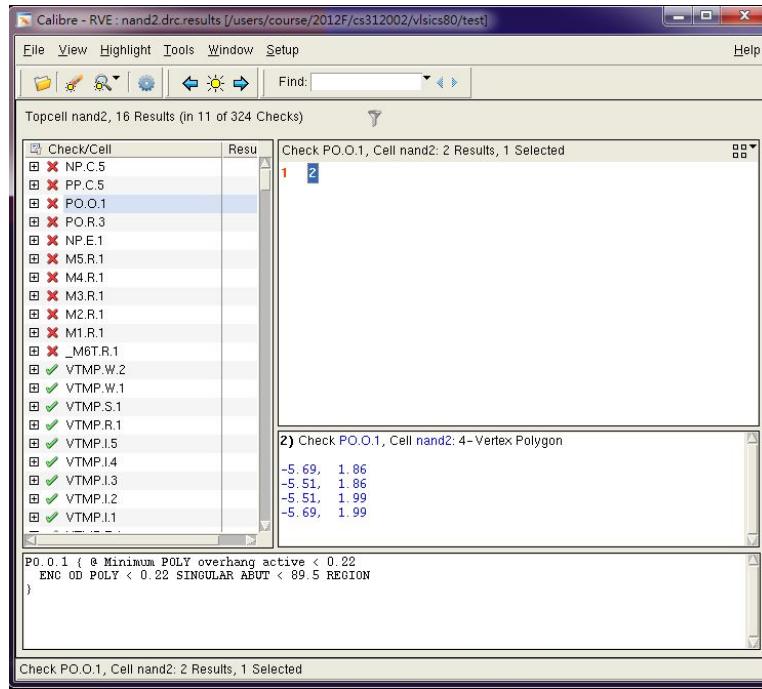
# Design Rule Check (DRC)



# Design Rule Check (DRC)



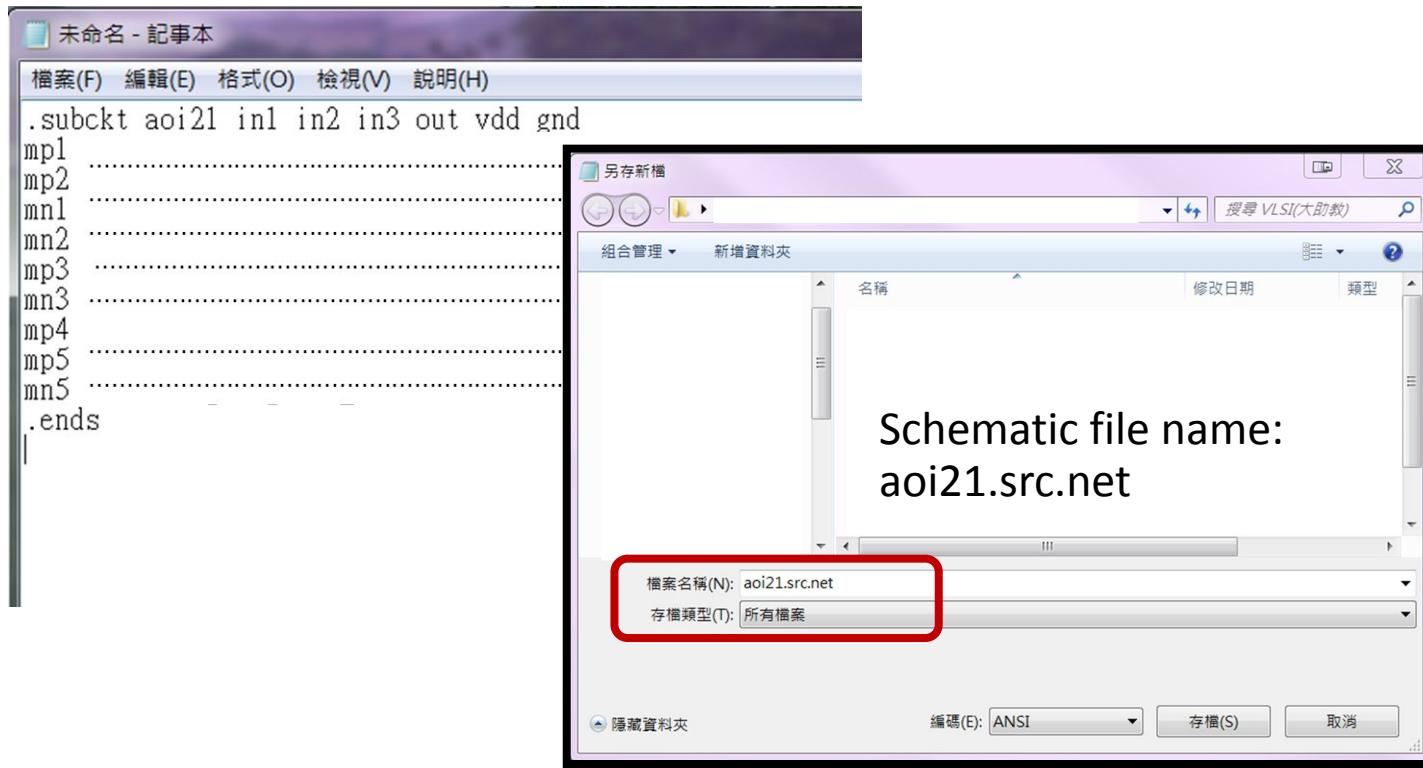
# Design Rule Check (DRC)



# LVS

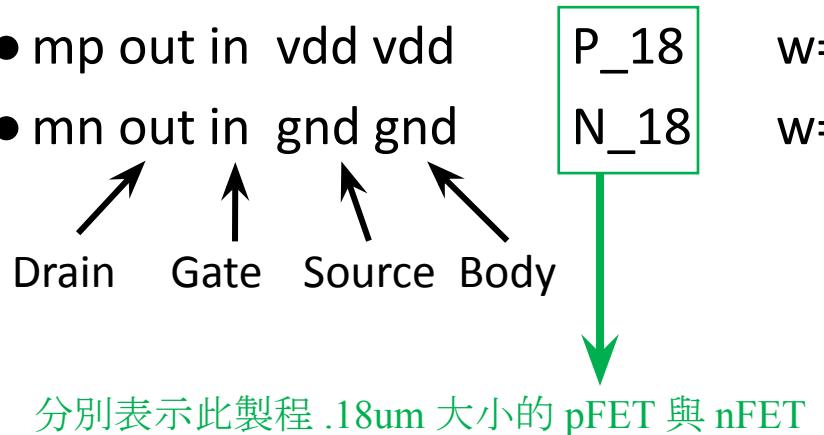
- LVS (Layout Versus Schematic)
- Verify the conductivity and functionalities between the layout and the schematic file.
- Put your schematic file **under your working directory**, **layout**
  - You can write it on Notepad and upload it afterwards
  - Schematic file name: **aoi21.src.net**

# Schematic Writing

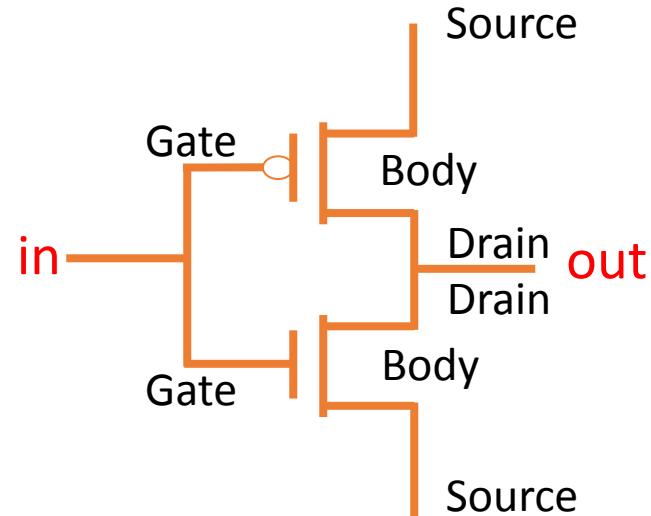


# Write LVS Schematic (1)

- mp out in vdd vdd
- mn out in gnd gnd



w=0.80u l=0.18u  
w=0.42u l=0.18u

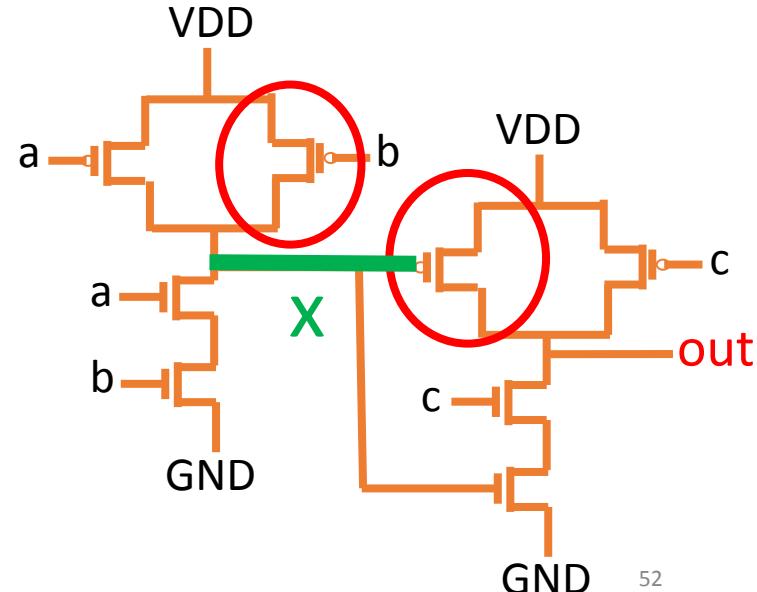


# Write LVS Schematic (2)

Please use different labels  
to differentiate the transistors

- mp1 x b vdd vdd P\_18 w=0.80u l=0.18u
- mp2 out vdd vdd P\_18 w=0.42u l=0.18u
- ....

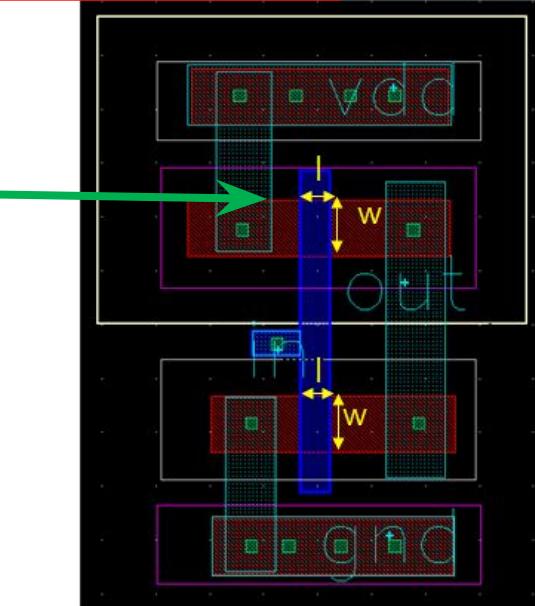
“x” can be any variable  
name as preferred.



# Write LVS Schematic (3)

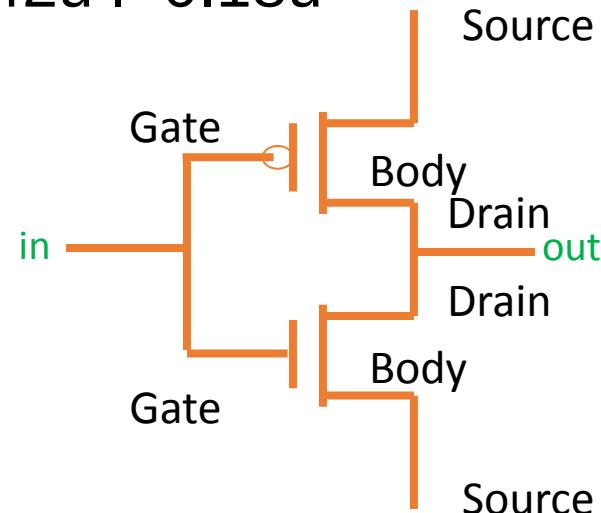
- mp out in vdd vdd P\_18       $w=0.80u \quad l=0.18u$
- mn out in gnd gnd N\_18       $w=0.42u \quad l=0.18u$

ps. 這邊  $l$  統一為  $0.18u$ , 而  $w$  則要根據自己畫的寬度去做設定。

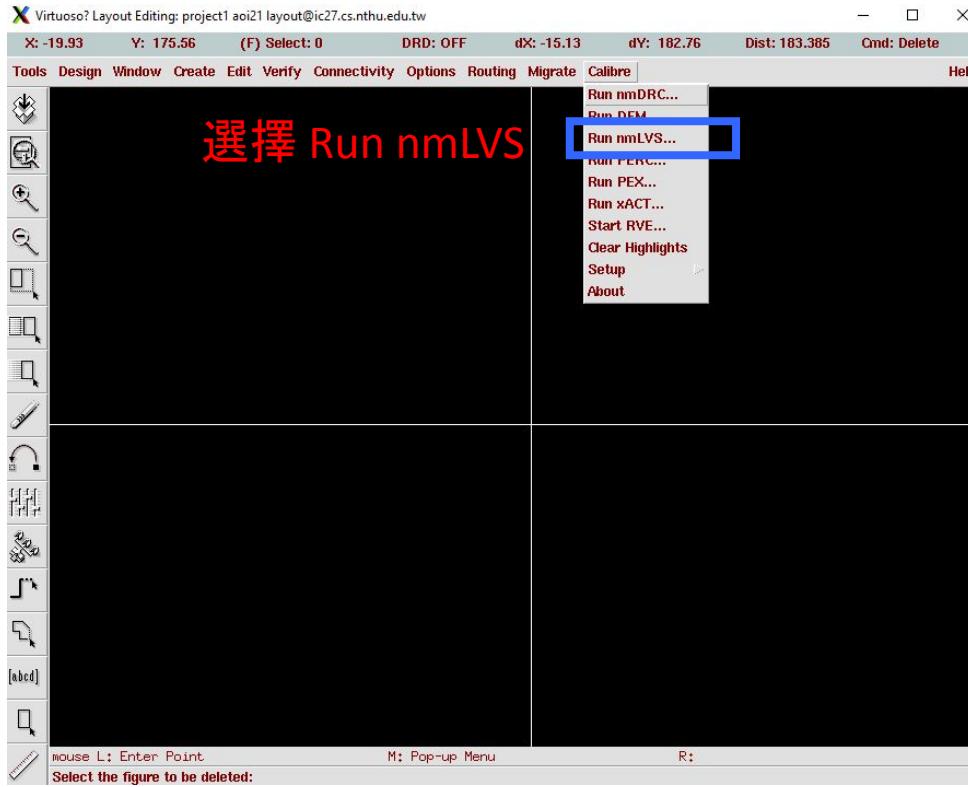


# Sample – Inverter Schematic

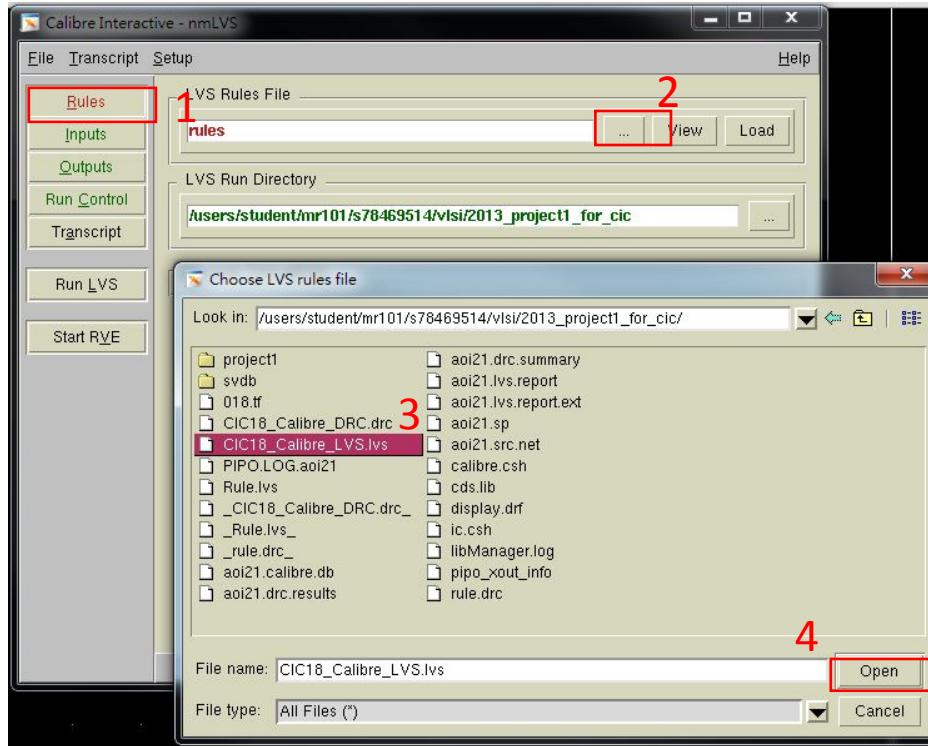
```
.subckt inverter in out vdd gnd  
mp out in vdd vdd P_18 w=0.80u l=0.18u  
mn out in gnd gnd N_18 w=0.42u l=0.18u  
.ends
```



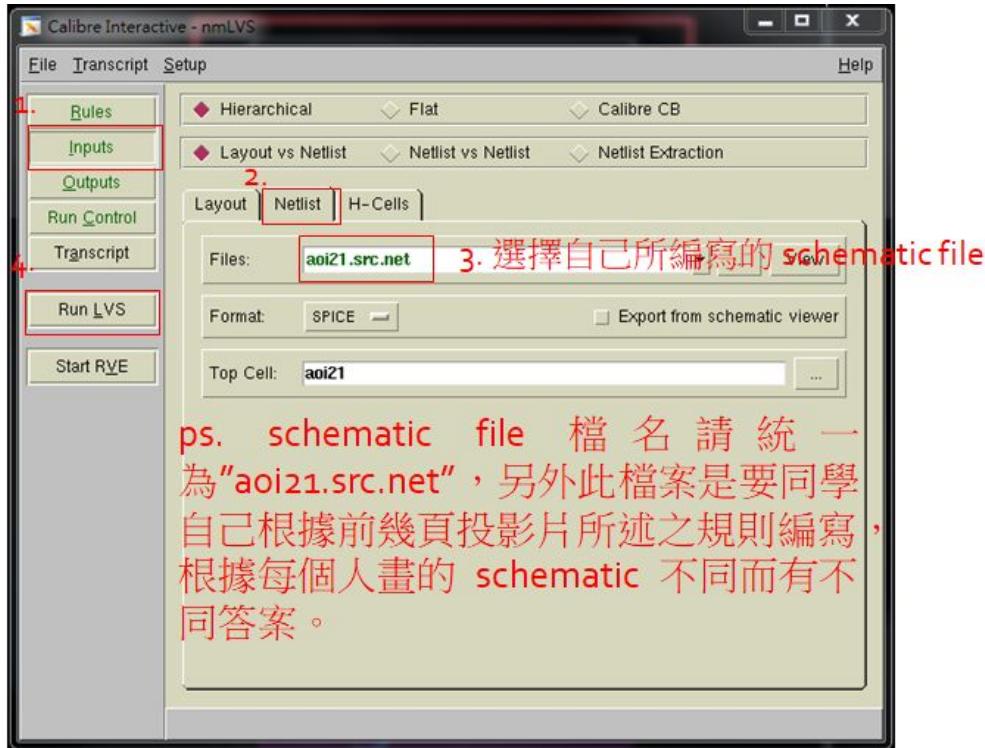
# Run LVS



# Select LVS Rule

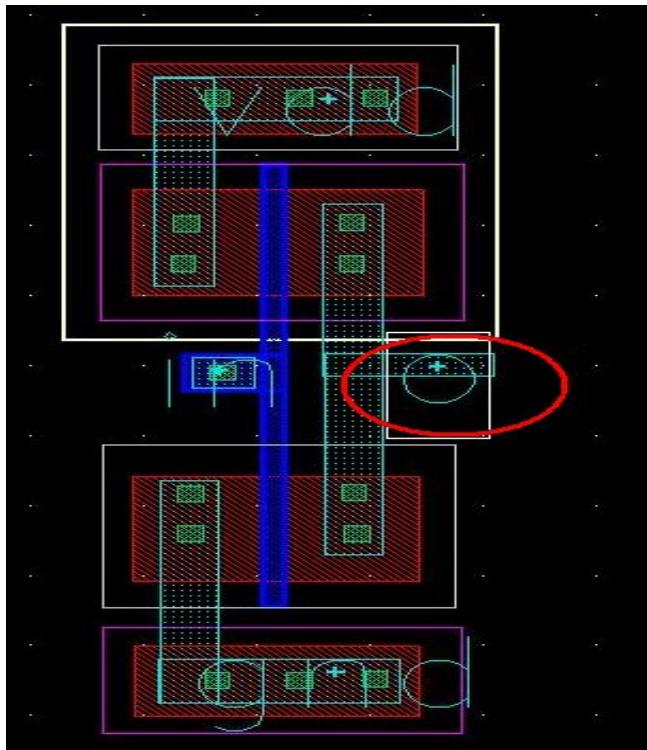


# Select LVS Schematic



# LVS Error (pin name)

\*以下範例圖片僅供參考



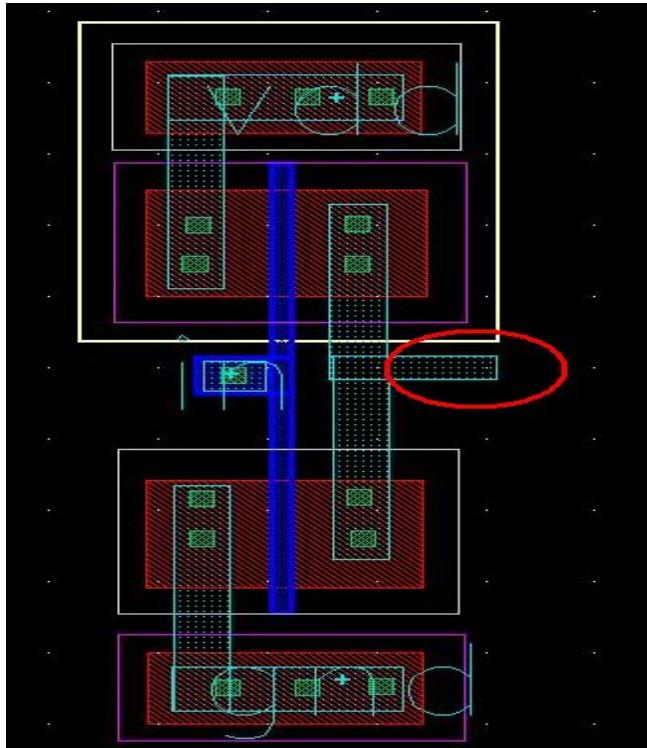
LVS Report File - inverter.lvs.report

File Edit Options Windows

\*\*\*\*\*  
\*\*\*\*\* INCORRECT OBJECTS \*\*\*\*\*  
\*\*\*\*\*  
LEGEND:  
----  
ne = Naming Error (same layout name found in source circuit, but object was matched otherwise).  
\*\*\*\*\*  
\*\*\*\*\* INCORRECT PORTS \*\*\*\*\*  
DISC# LAYOUT NAME SOURCE NAME  
\*\*\*\*\*  
0 on net: 0 OUT on net: OUT  
\*\*\*\*\*  
\*\*\*\*\* INFORMATION AND WARNINGS \*\*\*\*\*  
nthucad.cs.nthu.edu.tw [80x9]  
連線(C) 編輯(E) 檢視(V) 視窗(W) 選項(O) 說明(H)  
.subckt aoi21 in out vdd gnd  
mp1 out in vdd vdd P\_18 w=1.5u l=0.18u  
mn2 out in gnd gnd N\_18 w=1.5u l=0.18u  
.ends

# LVS Error (missing port)

\*以下範例圖片僅供參考



LVS Report File - inverter.lvs.report

File Edit Options Windows

\* = Number of objects in layout different from number in source.

\*\*\*\*\*  
\*\*\*\*\* INCORRECT OBJECTS \*\*\*\*\*  
\*\*\*\*\*

LEGEND :

ne = Naming Error (same layout name found in source circuit, but object was matched otherwise).

\*\*\*\*\*  
\*\*\*\*\* INCORRECT PORTS \*\*\*\*\*

| DISC# | LAYOUT NAME        | SOURCE NAME     |
|-------|--------------------|-----------------|
| 1     | ** missing port ** | OUT on net: OUT |

\*\*\*\*\*  
\*\*\*\*\* INFORMATION AND WARNINGS \*\*\*\*\*

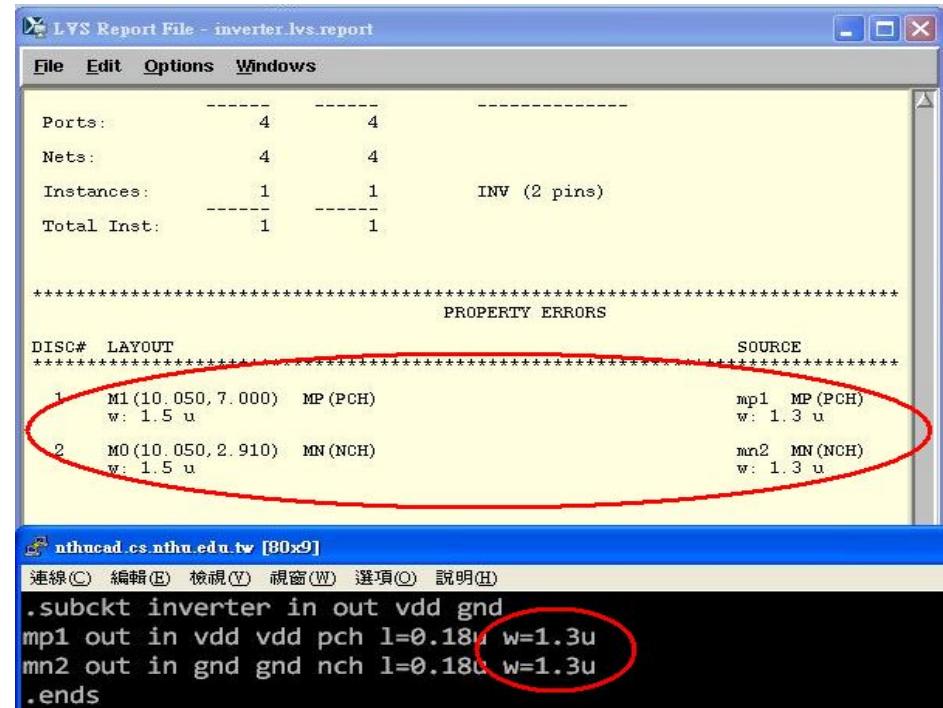
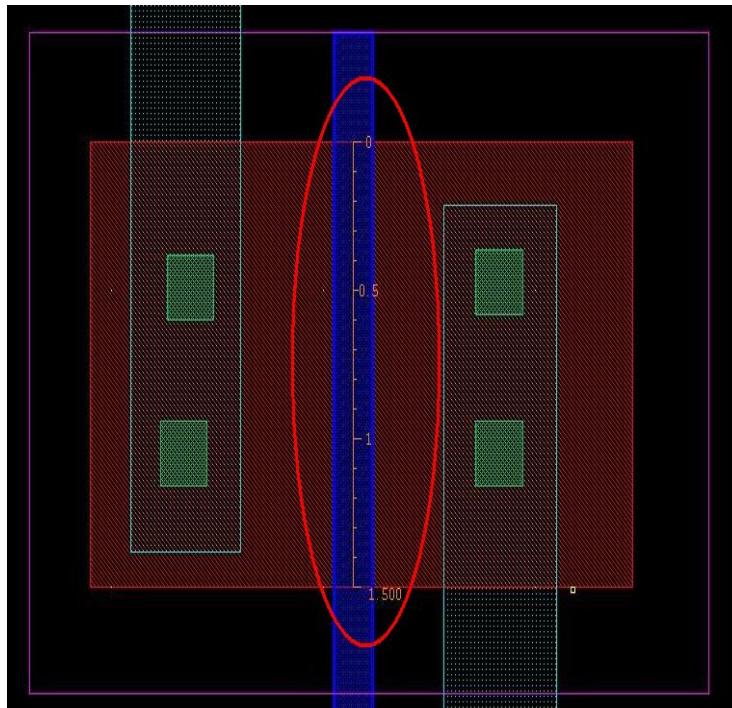
nthucad.cs.nthu.edu.tw [80x9]

連線(C) 編輯(E) 檢視(V) 視窗(W) 選項(O) 說明(H)

```
.subckt aoi21 in out vdd gnd
mp1 out in vdd vdd P_18 w=1.5u l=0.18u
mn2 out in gnd gnd N_18 w=1.5u l=0.18u
.ends
```

# LVS Error (size different)

\*以下範例圖片僅供參考



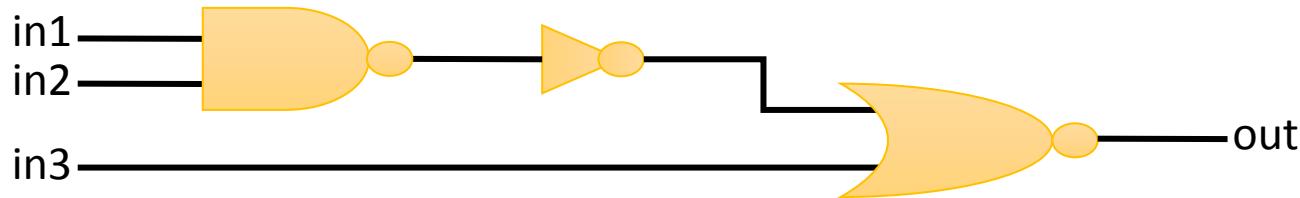
Check the width by selecting “properties”

# Outline

- Environment Setup
- Virtuoso
- Inverter
- DRC & LVS
- Project

# Project: aoi21

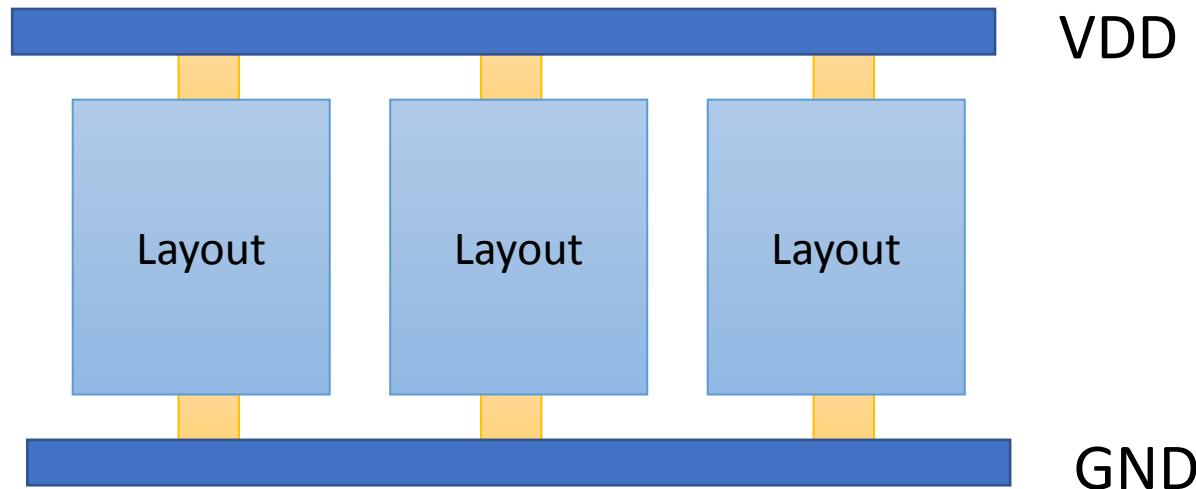
- NAND2 + Inverter + NOR2
- *Please notice that your label name should same as follows:*



1. You have to draw the layout of all these 3 gates
2. You can use metal1 only.

# Tips

- Put VDD of all gates into **one** row (so does GND)



# Report

- Your report should contain the following content, and you can add more as you wish.
  - Your name and student ID
  - FOUR screenclips:
    - Layout with rulers
    - DRC summary report
    - The message of passing LVS... ✓ [ CORRECT ] 😊
    - LVS schematic (screenclip of the text file)
  - What else did you do to enhance your layout quality?
  - What have you learned from this homework? What problem(s) have you encountered in this homework?

# Grading (1)

- Deadline: 2021/11/12 (Fri.) 23:59

- Files to upload:

1. A .pdf format report

2. A .tar.gz file includes all files in directory layout.

*You can use the following command to compress your directory on a workstation:*

```
$ tar -zcvf StudentID_project1.tar.gz <directory>
```

- Upload 1. and 2. to eeclass.

- Name the files as “StudentID\_report1.pdf” and “StudentID\_project1.tar.gz”, respectively.

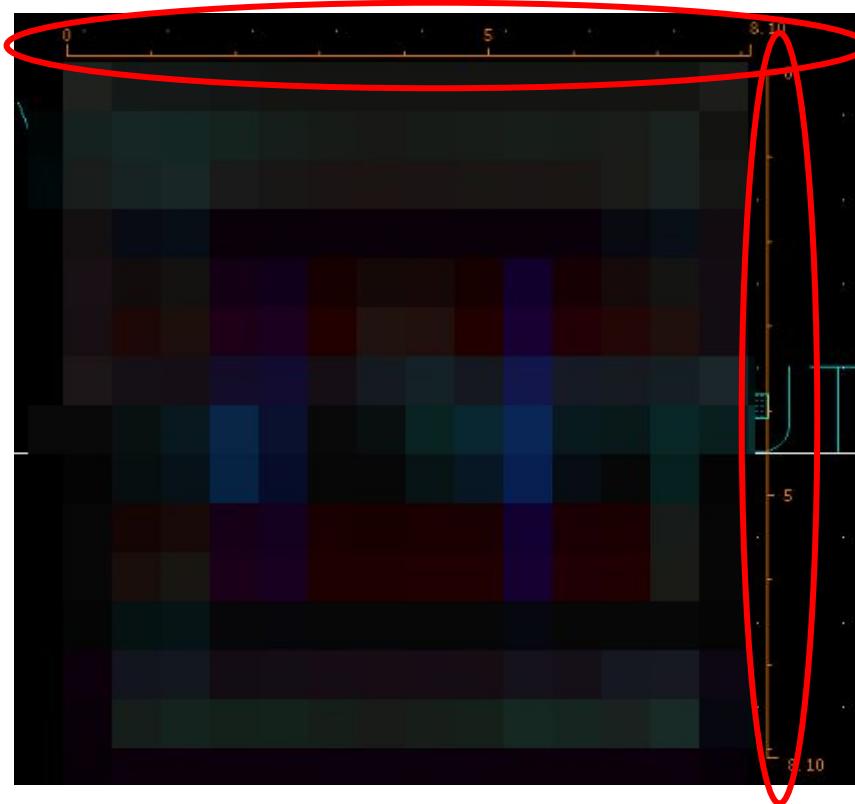
# Grading (2)

## ● Assessment

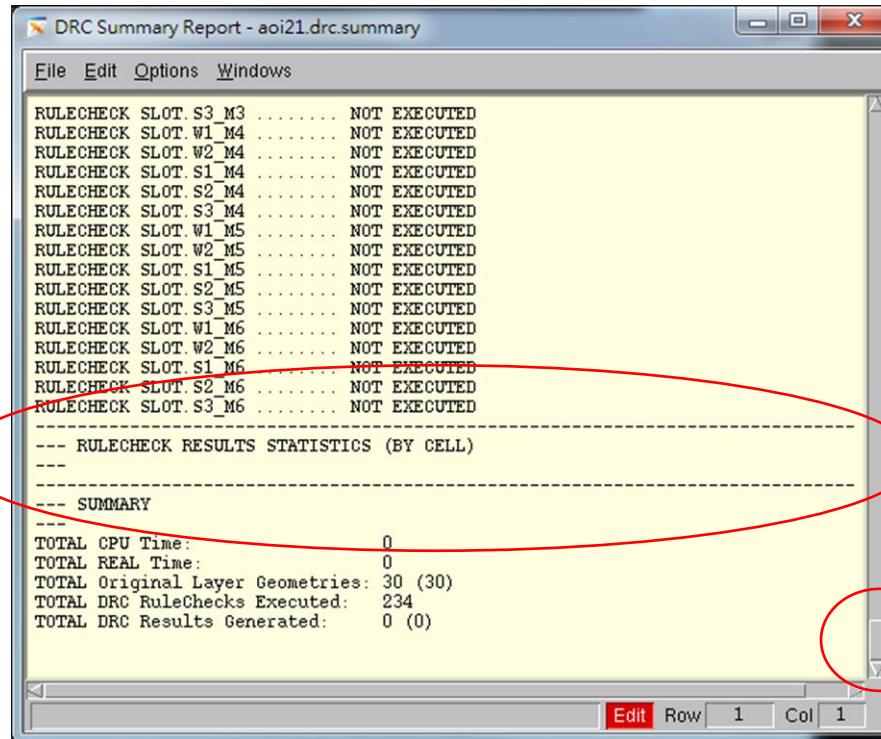
- Layout Area (以全班1/3、2/3為分界，給予三等級分數)
- DRC pass
- LVS pass
- LVS schematic
- Report
- Uploading date
  - Early Bird Bonus: Extra 10 points if uploaded before 2021/11/05 (Fri.) 23:59
  - No late submission.

# Layout with Rulers to Show Area

No Ruler:  
-10 points



# DRC Summary Report



The screenshot shows a Windows application window titled "DRC Summary Report - aoi21.drc.summary". The menu bar includes File, Edit, Options, and Windows. The main content area displays a list of rule checks and their status, followed by section headers and summary statistics.

```
File Edit Options Windows
RULECHECK SLOT.S3_M3 ..... NOT EXECUTED
RULECHECK SLOT.W1_M4 ..... NOT EXECUTED
RULECHECK SLOT.W2_M4 ..... NOT EXECUTED
RULECHECK SLOT.S1_M4 ..... NOT EXECUTED
RULECHECK SLOT.S2_M4 ..... NOT EXECUTED
RULECHECK SLOT.S3_M4 ..... NOT EXECUTED
RULECHECK SLOT.W1_M5 ..... NOT EXECUTED
RULECHECK SLOT.W2_M5 ..... NOT EXECUTED
RULECHECK SLOT.S1_M5 ..... NOT EXECUTED
RULECHECK SLOT.S2_M5 ..... NOT EXECUTED
RULECHECK SLOT.S3_M5 ..... NOT EXECUTED
RULECHECK SLOT.W1_M6 ..... NOT EXECUTED
RULECHECK SLOT.W2_M6 ..... NOT EXECUTED
RULECHECK SLOT.S1_M6 ..... NOT EXECUTED
RULECHECK SLOT.S2_M6 ..... NOT EXECUTED
RULECHECK SLOT.S3_M6 ..... NOT EXECUTED
-----
--- RULECHECK RESULTS STATISTICS (BY CELL)
---
--- SUMMARY
---
TOTAL CPU Time: 0
TOTAL REAL Time: 0
TOTAL Original Layer Geometries: 30 (30)
TOTAL DRC RuleChecks Executed: 234
TOTAL DRC Results Generated: 0 (0)
```

Bottom page

# LVS Passing Message

The screenshot shows a Windows application window titled "LVS Report File - NAND2.lvs.report". The menu bar includes "File", "Edit", "Options", and "Windows". The main content area displays the LVS report text. A red circle highlights the top right corner of the window, and a large red oval highlights the bottom left portion of the report content.

```
#####
##      C A L I B R E      S Y S T E M      ##
##      L V S      R E P O R T      ##
#####

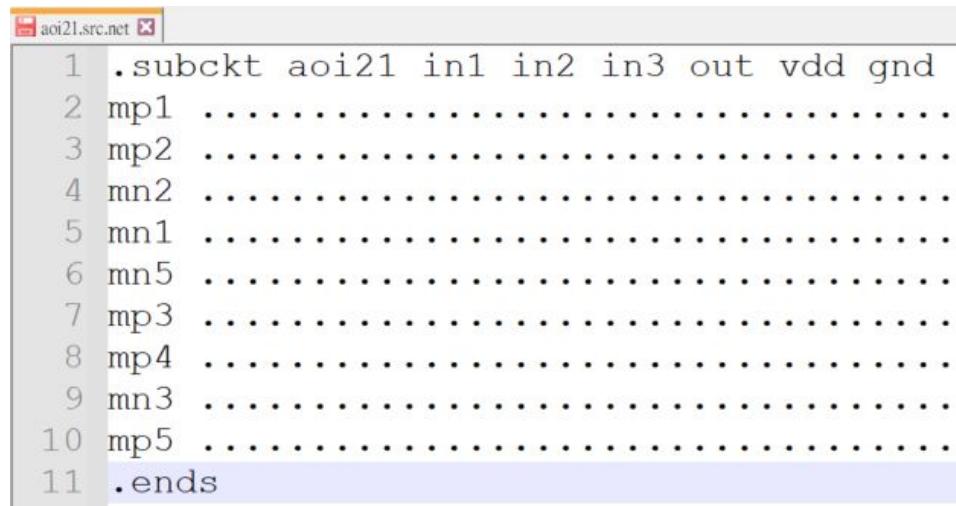
REPORT FILE NAME: NAND2.lvs.report
LAYOUT NAME: /users/student/topic/scchang/comaniac/course/VLSITA/project1/NAND2.sp ('NAND2')
SOURCE NAME: /users/student/topic/scchang/comaniac/course/VLSITA/project1/NAND2.src.net ('NAND2')
RULE FILE: /users/student/topic/scchang/comaniac/course/VLSITA/project1/_T18_Calibre_LVS_13A.13a
CREATION TIME: Tue Oct 11 10:02:36 2011
CURRENT DIRECTORY: /users/student/topic/scchang/comaniac/course/VLSITA/project1
USER NAME: comaniac
CALIBRE VERSION: v2009.2_36.21      Tue Jul 7 15:50:02 PDT 2009

OVERALL COMPARISON RESULTS

#####
# *   *   *
#   *   *
#     CORRECT   *
#   *   *
#####
|   |
```

Top page

# LVS Schematic



A screenshot of a text editor window titled "aoi21.src.net". The code inside the window is as follows:

```
1 .subckt aoi21 in1 in2 in3 out vdd gnd
2 mp1 .....
3 mp2 .....
4 mn2 .....
5 mn1 .....
6 mn5 .....
7 mp3 .....
8 mp4 .....
9 mn3 .....
10 mp5 .....
11 .ends
```

# Notice

- File Naming
  - Library name : project1
  - Cell name: aoi21
  - LVS netlist name: aoi21.src.net
- Width of every poly (channel length) must be **0.18u**, or you will get **0 point** even when passing DRC and LVS

# Notice (cont.)

- Submission after deadline → 0 point
- Plagiarism → 0 point
- Dishonest contents in the report → 0 point

# FAQ

- Q1. 為甚麼 project 1 中的參數會跟老師投影片的不一樣？
  - size 是根據 DRC 決定的，不同製程下會規定不一樣的 contact size
- Q2. 開啟 icfb 有點問題，它顯示的錯誤是 DISPLAY <not defined> ?

```
[VLSI017@ic29 ~/layout]$ *WARNING* X Window Display Initialization failure  
*WARNING* (DISPLAY "<not defined>")  
[1] Exit 255 icfb
```

- ssh 連線到 icXX 時，要加參數 -X

# Terminate the Workstation

- 一定要正常關閉 Virtuoso

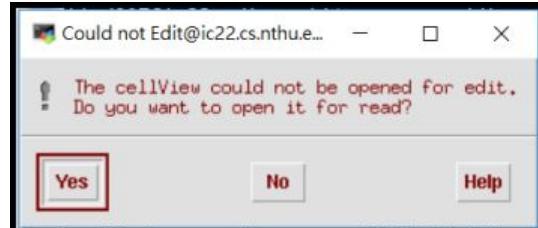
```
$ exit
```

```
$ exit
```

```
[lhsiung21@ic27 ~/layout]$ exit
logout
Connection to ic27 closed.
nthucad:~> exit
logout
```

# File lock

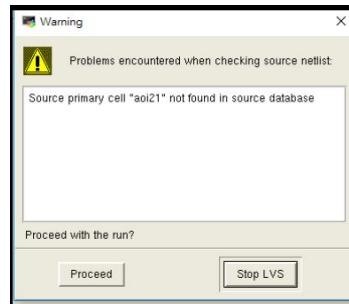
- Solution 1: 在目前使用的工作站 icXX 中打上 “`pkill virtuoso`” 關閉卡住的 process, 關閉工作站帳號後重啟再切換別的工作站
- Solution 2: 先輸入“`clsAdminTool`”, 用“`ale .`” 找到哪個被鎖住, 再用“`asre <filename>`” 把他解鎖。



```
[wshung20@ic56 ~/layout]$ *WARNING* file /users/student/mr109/wshung20/CDS.log File is already locked by some other process.
```

# LVS error

- Solution 1: Delete *aoi21.src.net* and upload again



- Solution 2: 第一行的 cell name “aoi21” 要和 Layout 的 cell name 一致

The image shows two side-by-side windows. On the left is a Notepad window titled "未命名 - 記事本" containing a Verilog-like code snippet:

```
.subckt aoi21 in1 in2 in3 out vdd gnd
mp1
mp2
mn1
```

The word "aoi21" is highlighted with a red rectangle. On the right is a file browser window showing a file named "aoi21.src.net" with a red rectangle around it. The file path is "C:\Users\...\".