

Dark Current and Noise of 100nm Thick Silicon On Sapphire CMOS Lateral PIN Photodiodes

Miriam Adlerstein Marwick*, Francisco Tejada*, Philippe Pouliquen*, Eugenio Culurciello†,
Kim Strohbehn‡, Andreas G. Andreou*

*Electrical and Computer Engineering, Johns Hopkins University, Baltimore, MD USA

†Electrical Engineering, Yale University, New Haven, CT USA

‡Johns Hopkins University Applied Physics Laboratory, Laurel, MD USA

Abstract—We report on dark current measurements from lateral, 100nm thick, PIN photodiodes fabricated in the Peregrine Semiconductor, Silicon on Sapphire (SOS) CMOS technology. We compare interdigitated photodiode geometries with edgeless structures that do not have active device regions adjacent to LOCOS. We also compare two methods for device design. One employs a polysilicon gate to block the implant in the intrinsic region of the device while the second utilizes a specific mask layer in the technology called an *SDBlock* mask. Our results suggests that the the dark current is primarily a function of the junction width. Furthermore, polysilicon gate devices have lower dark currents than *SDBlock* structures. Finally, we perform noise measurements and extract flicker noise parameters for the two methods and find that polysilicon gate structures have greater levels of flicker noise than *SDBlock* devices.

I. INTRODUCTION

Peregrine's Silicon on Sapphire (SOS) CMOS technology [1] is a type of silicon on insulator technology that is particularly suited to chip scale optoelectronic systems [2] because it employs synthetic sapphire, an optically transparent material, as its substrate. Another positive side-effect of the fully insulating substrate is the devices' inherent immunity to radiation-induced latch-up, a desirable characteristic when designing circuits and systems [3], [4] for space applications [5]. Lateral PIN photodiodes can be fabricated in this technology [6], giving incident light direct access to the active intrinsic region of the device through both the front and the back of the substrate [2], [7], [8].

The Peregrine technology gives options for leaving the channel of a MOS transistors undoped, lightly doped, or doped as a regular MOS transistor, yielding devices with three different threshold voltages. Using the first option, an intrinsic region can be formed between a p-type silicon “source” and an n-type silicon “drain”, resulting in a lateral PIN structure with a silicon thickness of only 100nm. This technique enables detection of shorter wavelengths when compared to those that construct shallow vertical silicon photodiodes in specialized processes. The advantages of lateral PIN photodiodes on a thin film SOI substrate for UV light detection are presented in [9]. The responsivity of the device to visible and IR wavelengths, along with the frequency response of PIN photodiodes in the

Peregrine SOS-CMOS technology, was reported in [6].

In this paper we experimentally study the leakage current and noise characteristics of PIN photodiodes fabricated in the Peregrine SOS-CMOS technology. The study explores how various factors in the device structure affect the leakage current and noise. We also extract flicker model parameters suitable for circuit simulation noise models.

II. TEST DEVICES

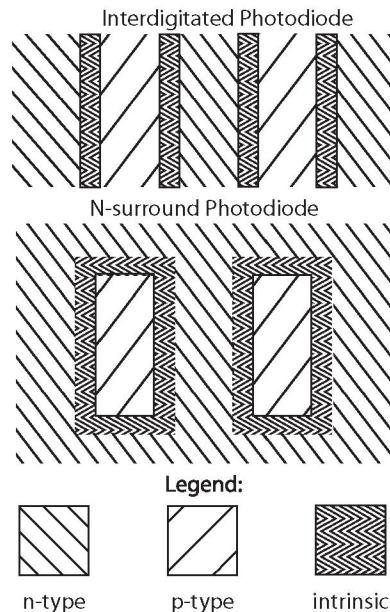


Fig. 1. Simplified sample layout geometries of PIN photodiode test structures.

The intrinsic region of the devices was formed by blocking the source/drain implant doping along a junction of abutting p- and n-type silicon using either polysilicon or the source/drain blocking mask (*SDBlock*). Three layout variations were employed to design the devices [see Figure (1)]. The first design consisted of interdigitated n-type and p-type fingers. The other two designs employed an edgeless layout formed by

completely surrounding one type of doping with the other (n-type silicon regions surrounded on all sides by p-type silicon, versus p-type regions surrounded by n-type silicon). A total of eighteen different geometries were used that had junction lengths that vary from 325 microns to 3664 microns.

The original hypothesis in this study was that the PIN photodiode with the simple interdigitated geometry would demonstrate the worst dark current characteristics, an indication that having a junction edge adjacent to the material isolating the device (LOCOS) is problematic (i.e., a poor $Si-SiO_2$ lateral interface). In this study, the length and width of the three types of devices are varied five times (either by using additional fingers to lengthen it, or by extending each finger to widen it) to identify which dimension contributes more to the dark current. The length of the intrinsic region itself was maintained at $1.2\mu m$, while the total width of the intrinsic region was determined by the width and the number of fingers (or surrounded regions).

III. DARK CURRENT MEASUREMENTS

All measurements were performed using low-noise probes to apply a positive bias to the cathode of the device while reading the current out of the anode through an electrometer (Keithley 617). The noise floor in our measurement setup was approximately 10fA. The instruments were controlled by a computer through a GPIB interface.

Figure (2) shows the dark currents of six devices of different sizes, all in this case consisting of p-type silicon fingers surrounded by n-type silicon.

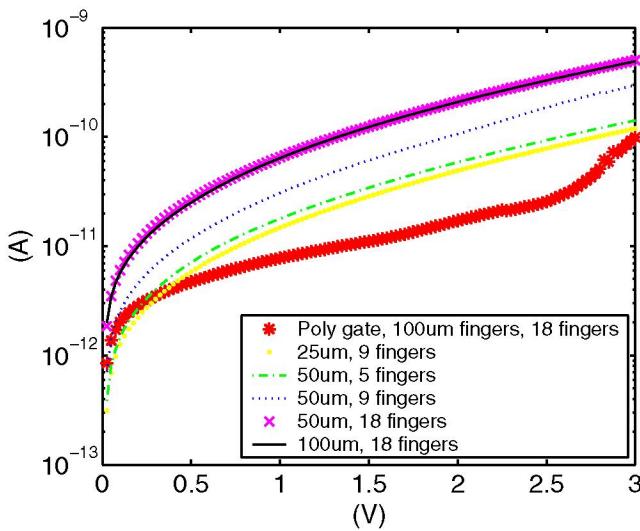


Fig. 2. Current voltage characteristics for N-surround devices of all sizes

Polysilicon gate intrinsic regions give the lowest dark current comparable to the smallest device at zero bias. At any non-zero bias, the increase in dark-current for any of the *SDBlock* diodes was significantly higher compared to the polysilicon gate type. In a typical process, the use of a polysilicon layer to fabricate the photodiodes would not be advisable as this

would limit the amount of light incident on the active region, and therefore limit the photosensitivity of the device. In SOS-CMOS, on the other hand, the option of illuminating through the backside of the die [2], [7], [8] (i.e., through the sapphire substrate), eliminates this problem and makes the poly-covered photodiodes preferable.

A comparison of the measurements from the three different device geometries, all occupying the same die area is depicted in Figure (3):

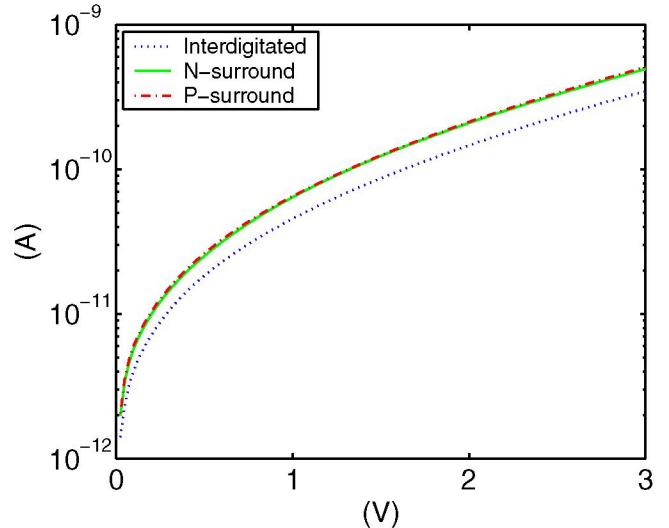


Fig. 3. Current voltage characteristics for three different structures of the same size ($100\mu m \times 50\mu m$)

The results of Figure (3), which suggests that interdigitated photodiodes have lower dark current than the edgeless structures, was highly questionable. A careful analysis of the actual intrinsic area present in each of the three geometries was performed. It was found that for two structures of equal area, the edgeless structures had a greater intrinsic area than the interdigitated devices. We therefore normalized the dark current measurements to the total width of the intrinsic area, and the normalized data is plotted in Figures 4 and 5, for *SDBlock* and polysilicon gate photodiodes respectively.

The two sets of normalized data indicate that the dark current in these PIN photodiodes is primarily determined by the total junction width, and by the quality of the oxide deposited directly on top of it, rather than by the oxide surrounding the device (LOCOS), or the sapphire-silicon interface at the bottom of the device as proposed in [10] (though the latter may still make a contribution to the total dark current.) When the polysilicon gate is used to create the intrinsic region, high quality gate oxide is deposited over the device. When the intrinsic region is formed by using the *SDBlock* mask, a lower quality field oxide is deposited over the junction.

All devices investigated in this work had an intrinsic region length of $1.2\mu m$ because the photodiodes were designed for high speed circuits and a short intrinsic region yields the highest speed. Additional test devices are fabricated to perform

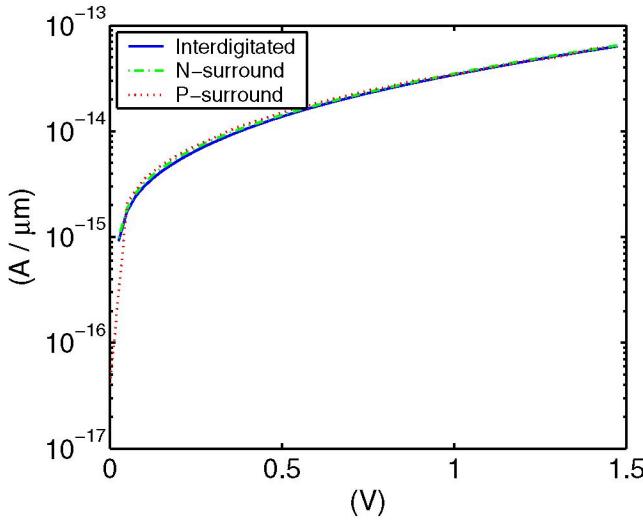


Fig. 4. Dark current normalized to junction width for *SDblock* photodiodes.

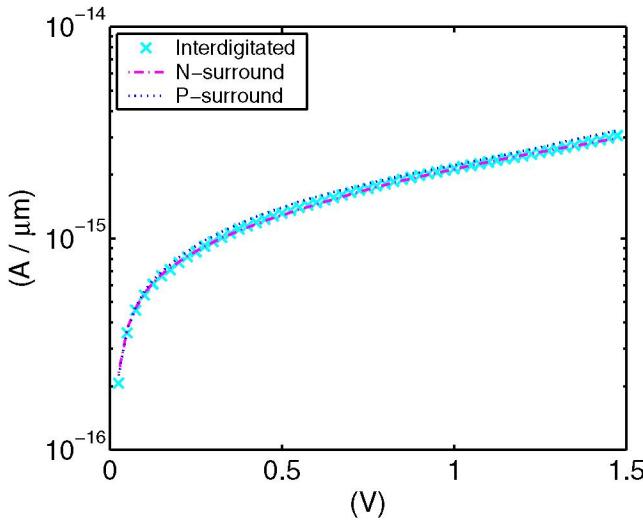


Fig. 5. Dark current normalized to junction width for polysilicon gate photodiodes

a parametric study of noise and leakage current in devices that have intrinsic regions of different lengths.

IV. PHOTODIODE NOISE MEASUREMENTS

The noise measurement setup consisted of the test circuit depicted in Figure 6. A shielded box includes all electronics, batteries and the device under test.

The use of a transconductance amplifier to measure the current [11] facilitates the automation of the noise measurements as the bias point of the device can be set through the virtual ground of the operational amplifier. The operating current of the device can be measured indirectly by measuring the voltage at the output of the amplifier and relating it to the applied bias and a calibrated feedback resistor. Coaxial connections from the shielded box are directly connected to the input

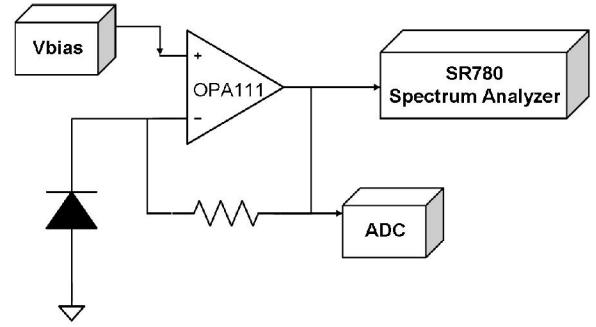


Fig. 6. Noise measurement setup

terminals of an SR780 Network Analyzer [?], that has a noise floor of $6nV/\sqrt{Hz}$. A Keithley K213 Programmable Voltage Source [12] is used to set the reference voltage (and therefore the photodiode reverse bias) and an IOTech Analog-to-Digital converter [13] is used to measure the voltage presented to the spectrum analyzer. All instruments are controlled through the GPIB interface using a computer and software written in MATLAB [14].

We first measured the noise in an $1864\mu m$ wide edgeless NSurround *SDblock* photodiode (the largest photodiode in the *SDblock* set of devices). Figure 7 shows the noise spectra for the device biased at four different voltages.

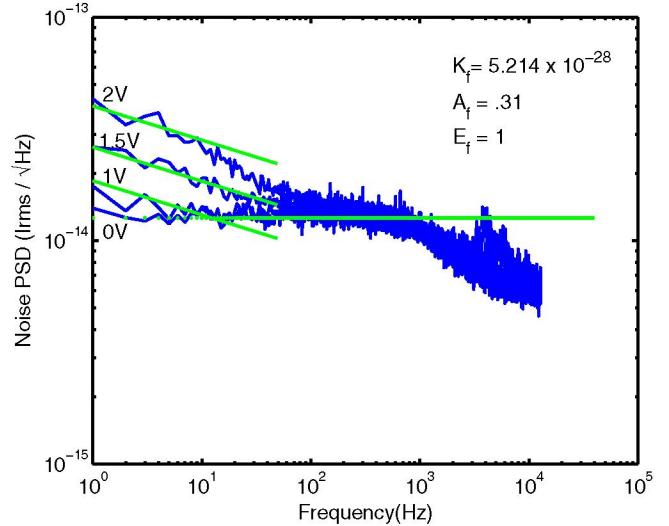


Fig. 7. Noise in an edgeless N-surround, $1864\mu m$ wide, *SDblock* photodiode under four different bias conditions. The noise model plot is superimposed to the measured noise data with extracted noise parameters in the inset.

We then measured the noise in a $3664\mu m$ wide edgeless NSurround polysilicon gate photodiode. The data for the polysilicon gate device is shown in Figure 8. A far more pronounced $1/f$ noise is evident for the range of frequencies of our instrument.

The lowest, mostly flat spectrum apparent in both cases represents the zero bias condition, in which both the flicker noise contribution and the dark current shot noise contribution

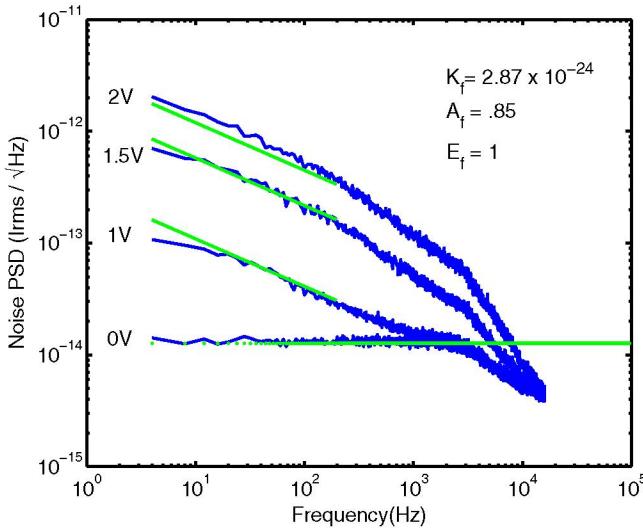


Fig. 8. Noise in an edgeless N-surround, $3664\mu\text{m}$ wide polysilicon gate photodiode under four different bias conditions. The noise model plot is superimposed to the measured noise data with extracted noise parameters in the inset.

are overshadowed by the feedback resistor's Johnson noise contribution given by:

$$S(f) = \frac{4kT}{R} \quad [I^2/\text{Hz}] \quad (1)$$

For the $100M\Omega$ thin film resistor in our setup the equivalent voltage noise is approximately $1.26\mu\text{V}/\sqrt{\text{Hz}}$, or $1.26e^{-14}A/\sqrt{\text{Hz}}$. This feedback resistor noise is also included in the plots of Figure (7) and Figure (8).

The $1/f$ component of the noise spectrum is modeled using the equation:

$$S(f) = \frac{K_f I_d^{E_f}}{C_{ox} W L f^{A_f}} \quad [I^2/\text{Hz}] \quad (2)$$

[15]

The values of the noise parameters K_f , A_f , and E_f in Equation (2) are fitted to the two sets of data, and the best fits for each set are chosen and superimposed on the data in Figure (7) and Figure (8). The model parameters used to fit the data are shown in the upper right corner of the figures.

The parameter values derived from the polysilicon photodiode's flicker noise data are similar to those reported for the flicker noise in an SOS MOSFET [16], an outcome that is not surprising given that the device structure is identical to that of an MOS device in all ways except of the complementary doping in the source and drain.

V. CONCLUSIONS

The results of measurements taken from a set of various 100nm thick PIN photodiodes fabricated in Peregrine's SOS CMOS process highlight the design tradeoffs encountered when choosing the right photodetector for a particular application. Overall, a minimum size polysilicon gate photodiode has the least dark current of any PIN device fabricated in the

process. On the other hand, the *SDBlock* designed devices have less excess noise when compared to polysilicon gate structures.

ACKNOWLEDGMENT

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