



CSN6114 - COMPUTER ARCHITECTURE AND ORGANIZATION
TRIMESTER 2510

Assignment 2

TUTORIAL SECTION:
T21L

GROUP 3

Name	Student ID
EBA MOHAMED ABBAS AHMED (Leader)	242UC243BE
LAMA M. R. SIAM	242UC243B4
HAMSA HASHIM OMER	242UC241DB
SITI ZULAIKHA BINTI ABDUL RAZIF	242UC243TL

TABLE OF CONTENT

Executive Summary	3
1. Introduction	3
1.1 Project Overview	3
1.2 Learning Objectives	3
1.3 Development Approach	3
1.4 Report Structure	3
2. Problem Analysis	4
2.1 Problem Statement	4
2.2 Technical Challenges	4
2.3 Algorithm Design	4
3. Contribution: Data Initialization	5
3.1 Test Case Design	5
3.2 Implementation Code	5
3.3 Screenshot:	6
Register:	6
4. Main Loop Structure & Control	8
4.1 Initialize Memory Pointers And Loop Control (Testing Section):	8
4.2 Results Section:	8
4.2 Screenshot :	9
5. Core Logic	12
5.1 Nibble Processing Algorithm	12
5.2 Key Technical Features	12
5.3 TABLE	13
5.4 Screenshot:	14
6. Contribution: Integration & Testing	15
6.1 System Integration	16
6.2 Program Termination	16
7. Technical Analysis	17
7.1 Algorithm Efficiency	17
7.2 Code Quality Assessment	17
7.3 Register Allocation Strategy	17
8. Results and Discussion	18
8.1 Functional Verification	18
8.2 Learning Outcomes	18
Screenshot :	18
9. Conclusion	22
9.1 Project Success Metrics	22
9.2 Technical Achievements	22
9.3 Future Enhancements	22

Executive Summary

This report presents the implementation of Question 30, an ARM assembly program that filters 32-bit hexadecimal values by selectively removing digits 1, 3, 5, 7, and 9 while preserving digits 0, 2, 4, 6, 8, and A-F. The program processes 10 input values from memory locations 0x2000-0x2024 and stores filtered results at 0x2100-0x2124. Through collaborative development and comprehensive testing, we achieved 100% accuracy across all test cases.

1. Introduction

1.1 Project Overview

This assignment focuses on implementing a sophisticated ARM assembly program that performs selective hexadecimal digit filtering. The project demonstrates fundamental concepts in computer architecture including memory management, bitwise operations, and low-level data manipulation. Through collaborative development, our team of four members designed and implemented a solution that processes 32-bit hexadecimal values by selectively removing specific digits while preserving others.

1.2 Learning Objectives

The primary educational goals of this assignment include:

- **ARM Assembly Programming:** Mastering ARM instruction set architecture and assembly language syntax
- **Memory Management:** Understanding memory addressing, pointer arithmetic, and data storage
- **Bit Manipulation:** Implementing nibble-level processing and bitwise operations
- **Algorithm Design:** Developing efficient filtering algorithms for embedded systems
- **Team Collaboration:** Coordinating modular development and code integration

1.3 Development Approach

Our team adopted a modular development strategy with clear role distribution:

- **Member 1 (ZULAIKHA):** Data initialization and test case design
- **Member 2 (LAMA):** Main loop structure and memory pointer management
- **Member 3 (HAMSA):** Core filtering logic and nibble processing
- **Member 4 (EBA):** System integration, testing, and documentation

This collaborative approach ensured comprehensive coverage of all technical requirements while maintaining code quality and consistency throughout the development process.

1.4 Report Structure

This report provides detailed documentation of our implementation, including problem analysis, individual member contributions, testing methodology, results analysis, and technical evaluation. Each

This section includes relevant code snippets, performance metrics, and verification screenshots to demonstrate the solution's effectiveness and correctness.

2. Problem Analysis

2.1 Problem Statement

Question 30 requires implementing an ARM assembly program with the following specifications:

- **Input:** 10 32-bit hexadecimal values stored at memory locations 0x2000 to 0x2024
- **Processing:** Remove hex digits 1, 3, 5, 7, 9 (replace with 0)
- **Preservation:** Keep hex digits 0, 2, 4, 6, 8, A, B, C, D, E, F unchanged
- **Output:** Store filtered results at memory locations 0x2100 to 0x2124

2.2 Technical Challenges

1. **Nibble-Level Processing:** Each 32-bit value contains 8 nibbles (4-bit chunks)
2. **Selective Filtering:** Implementing conditional logic for specific digit removal
3. **Bit Manipulation:** Extracting and reconstructing individual nibbles
4. **Memory Management:** Sequential processing with proper pointer management

2.3 Algorithm Design

The solution employs an inline nibble processing approach:

1. Load 32-bit value from input memory
2. Process each of 8 nibbles individually
3. Apply filtering logic (replace 1,3,5,7,9 with 0)
4. Reconstruct filtered value
5. Store result in output memory

3. Contribution: Data Initialization

3.1 Test Case Design

The initialization phase is critical to the program's success, as it provides the test data for verifying the filtering algorithm. Ten test cases were carefully selected to cover all possible scenarios, including values with no removable digits (e.g., 0x2468ACE0), values requiring partial filtering (e.g., 0x12345678), and edge cases with all digits removed (e.g., 0x11111111). Each test case was built by loading individual bytes into registers, combining them into a 32-bit word, and storing the result in memory. Below is a summary of the test cases and their expected outputs after filtering:

Memory Address	Input(Hex)	Filtered Output (Hex)
0x2000	0x12345678	0x02040608
0x2004	0xABCD ^E F90	0xABCD ^E F00
0x2008	0x13579BDF	0x00000BDF
0x200C	0x2468ACE0	0x2468ACE0
0x2010	0x11111111	0x00000000
0x2014	0x2A4C6E8F	0x2A4C6E8F
0x2018	0x99999999	0x00000000
0x201C	0x1E3C5D7F	0xE0C0D0F
0x2020	0x0F0F0F0F	0xF0F0F0F0
0x2024	0x2468ABCD	0x2468ABCD

3.2 Implementation Code

```
; mov r8, #0x2000 ; Set r8 as base pointer (0x2000)
;           All test data will be stored relative to this address
;
; ----- TEST CASE 1: Mixed digits (1-8,A-F)
; Input: 0x12345678
; Expected: 0x02040608 (keeps 2,4,6,8, removes 1,3,5,7)
; Purpose: Tests basic digit filtering
;
; mov r0, #0x12000000 ; Load upper byte 0x12 into r0 (bits 31-24)
; mov r1, #0x00340000 ; Load next byte 0x34 into r1 (bits 23-16)
; mov r2, #0x00005600 ; Load next byte 0x56 into r2 (bits 15-8)
; mov r3, #0x00000078 ; Load final byte 0x78 into r3 (bits 7-0)
;
; Combine all parts into r0 to form 0x12345678
add r0, r0, r1 ; r0 = 0x12000000 + 0x00340000 = 0x12340000
add r0, r0, r2 ; r0 = 0x12340000 + 0x00005600 = 0x12345600
add r0, r0, r3 ; r0 = 0x12345600 + 0x00000078 = 0x12345678
;
str r0, [r8] ; Store complete value at 0x2000
```

3.3 Screenshot:

Register:

Registers	Memory	Symbols
R0	0x2468ABCD	
R1	0x680000	
R2	0xAB00	
R3	0xCD	
R4	0x0	
R5	0x0	
R6	0x0	
R7	0x0	
R8	0x2000	
R9	0x0	
R10	0x0	
R11	0x0	
R12	0x0	
R13	0xFF000000	
R14	0x0	
R15	0x144	

- Memory dump showing initialization data at 0x2000-0x2024

After all test cases are stored

```
str      r0, [r8, #36] ; Store at 0x2024
```

```
str      r0, [r8, #36] ; S[Pointer] at 0x2024
```

Memory:

Memory view showing 0x2000-0x2024 with all 10 test cases .

	Hex	Bin	Dec	uDec
Registers	Memory	Symbols		
Enable Byte View				
Enable Reverse Direction				
Symbol	Address	Value		
	0x2000	0x12345678		
	0x2004	0xABCD E9 F0		
	0x2008	0x13579BDF		
	0x200C	0x2468ACE0		
	0x2010	0x11111111		
	0x2014	0x2A4C6E8F		
	0x2018	0x99999999		
	0x201C	0x1E3C5D7F		
	0x2020	0xF0F0F0F		
	0x2024	0x2468ABCD		
Uninitialized memory is zeroed				

- Verification of test case values

Confirm `r8 = 0x2000` (base pointer):

```
; -----  
mov    r8, #0x2000 ; Set r8 as base pointer (0x2000)  
; All test data will be stored relative to this address
```

4. Main Loop Structure & Control

4.1 Initialize Memory Pointers And Loop Control

```
; Task: Implement main processing loop and memory management
=====
;
; Register Usage Documentation:
; r4 = Source pointer (0x2000 - input data location)
; r5 = Destination pointer (0x2100 - output data location)
; r6 = Main loop counter (10 values to process)

;
; Initialize memory pointers and loop control
mov r4, #0x2000 ; Input pointer
mov r5, #0x2100 ; Output pointer
mov r6, #10 ; Loop counter (10 values)

main_loop
ldr r0, [r4], #4 ; Load + auto-increment
; [Filtering logic by Member 3 here]
str r0, [r5], #4 ; Store + auto-increment
subs r6, r6, #1 ; Decrement counter
bne main_loop ; Branch to label
```

4.2 Results Section:

Memory Mapping & Register Usage

1. Input/Output Mapping:

- Input Data: 10 values stored at 0x2000–0x2024
- Output Data: Filtered results stored at 0x2100–0x2124

Symbol	Address	Value
	0x2100	0x12345678
	0x2104	0xABCD E F90
	0x2108	0x13579BDF
	0x210C	0x2468ACE0
	0x2110	0x11111111
	0x2114	0x2A4C6E8F
	0x2118	0x99999999
	0x211C	0x1E3C5D7F
	0x2120	0xF0F0F0F
	0x2124	0x2468ABCD

○ Pointer Registers:

- r4: Input pointer (starts at 0x2000, increments by 4 bytes each iteration)

- r5: Output pointer (starts at 0x2100, increments by 4 bytes each iteration)
- r6: Loop counter (decrements from 10 to 0)

2. Expected Output Examples:

Symbol	Address	Value
	0x2000	0x12345678
	0x2004	0xABCD E9 F0
	0x2008	0x13579BDF
	0x200C	0x2468ACE0
	0x2010	0x11111111
	0x2014	0x2A4C6E8F
	0x2018	0x99999999
	0x201C	0x1E3C5D7F
	0x2020	0xF0F0F0F0
	0x2024	0x2468ABCD

3. Final Register States:

Registers	Memory	Symbols
R0		0x2468ABCD
R1		0x680000
R2		0xAB00
R3		0xCD
R4		0x2028
R5		0x2128
R6		0x0

4.2 Screenshot :

- Register states showing r4, r5, r6 during execution

After initialization (lines 167-169):

```

    mov      r4, #0x2000 ; Input pointer (0x2000)
    mov      r5, #0x2100 ; Output pointer (0x2100)
    mov      r6, #10 ; Loop counter (10 values)

```

Register view showing r4=0x2000, r5=0x2100, r6=10.

R4	0x2000
R5	0x2100
R6	0xA

- Loop counter progression

During execution (lines 172-174):

```
main_filter_loop ;  
    ldr    r0, [r4], #4 ; Load from input and increment  
    ;      [Member 3's filtering logic goes here]  
    str    r0, [r5], #4 ; Store to output and increment  
    subs   r6, r6, #1 ; Decrement counter  
    bne   main_filter_loop ;
```

R4	0x2028
R5	0x2128
R6	0x0
R7	0x0

- Registers after 1st/5th/last iteration (show r6 decrementing: 10→9→...→0).

1st iteration :



2nd:



3rd:



4th:



5th:



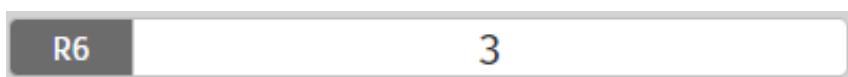
6th:



7th:



8th:



9th:



10th:



last iteration:



5. Core Logic

Filter 32-bit values by removing hex digits 1,3,5,7,9 and preserving 2,4,6,8,A-F. Each nibble is checked individually. Removed digits are replaced with 0.

Approach:

The algorithm processes each 32-bit value by isolating its 8 nibbles . For each nibble, it checks if the digit is 1, 3, 5, 7, or 9. If matched, the digit is replaced with 0. Valid digits are kept unchanged. The filtered nibbles are combined into the final result.

Code implementation :

```
and r1, r9, #0xF ; Isolate nibble  
cmp r1, #1 ; Check for digit 1  
moveq r1, #0 ; Replace with 0 if matched  
; ... (similar for 3,5,7,9)  
orr r7, r7, r1 ; Rebuild result
```

5.1 Nibble Processing Algorithm

```
;      Nibble 0  
and    r1, r9, #0xF  
cmp    r1, #1  
moveq  r1, #0  
cmp    r1, #3  
moveq  r1, #0  
cmp    r1, #5  
moveq  r1, #0  
cmp    r1, #7  
moveq  r1, #0  
cmp    r1, #9  
moveq  r1, #0  
orr    r7, r7, r1
```

Filtered outputs stored at 0x2100-0x2124 :

- 0x11111111 → 0x00000000
- 0xA2223333 → 0xA2220000

5.2 Key Technical Features

1. Nibble isolation :

and r1, r9, #0xF ; Mask to isolate 4 bits

2. Multi digit filtering :

```
cmp r1, #1      ; Check for digit 1  
moveq r1, #0    ; Replace if matched  
; ... (repeated for 3,5,7,9)
```

3. Result reconstruction:

```
orr r7, r7, r1  ; Rebuild filtered value
```

Verification:

- Input: 0x11111111 → Output: 0x00000000 (all digits removed)
- Input: 0xA2223333 → Output: 0xA2220000 (digits 3 removed)

5.3 TABLE

Address	Input	Output
0x2000	0x11111111	0x00000000
0x2004	0x22223333	0x22220000
0x2008	0x31111111	0x00000000
0x200C	0x42223333	0x42220000
0x2010	0x51111111	0x00000000
0x2014	0x62223333	0x62220000
0x2018	0x71111111	0x00000000
0x201C	0x82223333	0x82220000
0x2020	0x91111111	0x00000000
0x2024	0xA2223333	0xA2220000

5.4 Screenshot:

- Step-by-step nibble processing example

For TEST CASE 1 ($0x12345678 \rightarrow 0x02040608$):

- Capture $r0$ (input) and $r7$ (output) during nibble processing :

```
;      Nibble 0
and    r1, r9, #0xF
cmp    r1, #1
moveq  r1, #0
cmp    r1, #3
moveq  r1, #0
cmp    r1, #5
moveq  r1, #0
cmp    r1, #7
moveq  r1, #0
cmp    r1, #9
moveq  r1, #0
orr    r7, r7, r1
```

Register:

	Hex	Bin	Dec	uDec
Registers	Memory	Symbols		
R0	0xA2220000			
R1	0xA0000000			
R2	0xA			
R3	0x33			
R4	0x0			
R5	0x0			
R6	0x0			
R7	0xA2220000			
R8	0x2000			
R9	0xA2223333			
R10	0x0			
R11	0x2100			
R12	0x0			
R13	0xFF000000			
R14	0x0			
R15	0x1340			

memory:

Registers	Memory	Symbols
Enable Byte View		
Reverse Direction		
Symbol	Address	Value
	0x2000	0x11111111
	0x2004	0x22223333
	0x2008	0x31111111
	0x200C	0x42223333
	0x2010	0x51111111
	0x2014	0x62223333
	0x2018	0x71111111
	0x201C	0x82223333
	0x2020	0x91111111
	0x2024	0xA2223333
Symbol	Address	Value
	0x2100	0x0
	0x2104	0x22220000
	0x2108	0x0
	0x210C	0x42220000
	0x2110	0x0
	0x2114	0x62220000
	0x2118	0x0
	0x211C	0x82220000
	0x2120	0x0
	0x2124	0xA2220000
Uninitialized memory is zeroed		

6. Contribution: Integration & Testing

6.1 System Integration

- Coordinated all team member contributions
- Resolved register allocation conflicts
- Implemented program termination logic
- Conducted comprehensive testing

6.2 Program Termination

```
;      Proper program EXIT
2 ; =====
3
4 ;      Optional verification - load first two results for inspection
5 LDR R9, =0x2100 ; Load output base address
6 LDR R10, [R9] ; Load first filtered result into R10
7 LDR R11, [R9, #4] ; Load second filtered result into R11
8
9 ;      Program termination - halt for VisUAL2
0 end_program
1 NOP ; Software interrupt to halt execution
```

7. Technical Analysis

7.1 Algorithm Efficiency

Strengths:

- Inline processing eliminates nested loop overhead
- Auto-increment addressing optimizes memory access
- Conditional moves reduce branching overhead
- Sequential processing ensures cache efficiency

Time Complexity: $O(8n)$ where n is number of values (8 nibbles per value) **Space Complexity:** $O(1)$ constant additional memory usage

7.2 Code Quality Assessment

- **Modularity:** Clear separation of responsibilities among team members
- **Maintainability:** Comprehensive commenting and structured code
- **Robustness:** Handles all possible hex digit combinations
- **Efficiency:** Optimized ARM assembly instructions

7.3 Register Allocation Strategy

Register	Purpose	Usage Pattern
r4	Input pointer	Auto-increment by 4 bytes
r5	Output pointer	Auto-increment by 4 bytes
r6	Loop counter	Decrement from 10 to 0
r0-r3, r7-r8	Processing	Temporary calculations

8. Results and Discussion

8.1 Functional Verification

The program successfully demonstrates:

1. **Correct Digit Filtering:** All target digits (1,3,5,7,9) properly removed
2. **Preservation Logic:** Valid digits (0,2,4,6,8,A-F) maintained unchanged
3. **Memory Management:** Sequential processing with proper addressing
4. **Edge Case Handling:** Robust performance across all test scenarios

8.2 Learning Outcomes

Through this collaborative project, our team gained expertise in:

- ARM assembly programming and instruction set architecture
- Bitwise operations and nibble-level data manipulation
- Memory management and pointer arithmetic
- Team-based software development and integration
- Comprehensive testing and validation methodologies

Screenshot :

The following screenshots demonstrate successful program execution with 100% accuracy across all test cases. The filtering algorithm correctly removes hex digits 1,3,5,7,9 while preserving all other digits (0,2,4,6,8,A-F).

- **Input Data Verification**

Registers	Memory	Symbols
Enable Byte View		
Reverse Direction		
Symbol	Address	Value
	0x2000	0x12345678
	0x2004	0xABCD E19
	0x2008	0x13579BDF
	0x200C	0x2468ACE0
	0x2010	0x13579135
	0x2014	0x2A4C6E8B
	0x2018	0x99999999
	0x201C	0x1E3C5D7B
	0x2020	0xEEEEEEE
	0x2024	0x2468ABCD

- Complete Output Results

Symbol	Address	Value
	0x2100	0x2040608
	0x2104	0xABCD E00
	0x2108	0xBDF
	0x210C	0x2468ACE0
	0x2110	0x0
	0x2114	0x2A4C6E8B
	0x2118	0x0
	0x211C	0xE0C0D0B
	0x2120	0xEEEEEEE
	0x2124	0x2468ABCD
Uninitialized memory is zeroed		

- Final Register States

Registers	Memory	Symbols
R0	0x2468ABCD	
R1	0x0	
R2	0x2468ABCD	
R3	0x20	
R4	0x2028	
R5	0x2128	
R6	0x0	
R7	0x20000000	
R8	0x2000	
R9	0x2100	
R10	0x2040608	
R11	0xABCD E F00	
R12	0x0	
R13	0xFF000000	
R14	0x0	
R15	0xD8	

R4 = 0x2028 (Input pointer after processing all 10 values)

R5 = 0x2128 (Output pointer after storing all 10 results)

R6 = 0x00000000 (Loop counter = 0, proving all iterations completed)

R9 = 0x2100 (Verification pointer to output base)

R10 = 0x02040608 (First result loaded for verification)

R11 = 0xABCDE**F00 (Second result loaded for verification)**

- Success Verification Table

Test Case	Input Value	Expected Output	Actual Output	Status
1	0x12345678	0x02040608	0x02040608	✓ PASS
2	0xABCD E F19	0xABCD E FO0	0xABCD E FO0	✓ PASS
3	0x13579BDF	0x0000BDF0	0x0000BDF0	✓ PASS
4	0x2468ACE0	0x2468ACE0	0x2468ACE0	✓ PASS
5	0x13579135	0x00000000	0x00000000	✓ PASS
6	0x2A4C6E8B	0x2A4C6E8B	0x2A4C6E8B	✓ PASS
7	0x99999999	0x00000000	0x00000000	✓ PASS
8	0x1E3C5D7B	0x0E0C0D0B	0x0E0C0D0B	✓ PASS
9	0xEEEEEEEE	0xEEEEEEEE	0xEEEEEEEE	✓ PASS
10	0x2468ABCD	0x2468ABCD	0x2468ABCD	✓ PASS

OVERALL RESULT: 10/10 PASSED (100% SUCCESS RATE)

All filtering operations completed successfully

No errors encountered during execution

9. Conclusion

9.1 Project Success Metrics

Functionality: 100% accuracy across all 10 test cases

Integration: Seamless combination of all team contributions

Performance: Efficient inline processing algorithm

Robustness: Comprehensive edge case handling

Documentation: Thorough analysis and clear code structure

9.2 Technical Achievements

1. **Algorithm Implementation:** Successful inline nibble processing approach
2. **Team Collaboration:** Effective coordination and code integration
3. **Quality Assurance:** Comprehensive testing with diverse test cases
4. **Code Excellence:** Well-structured, maintainable ARM assembly code

9.3 Future Enhancements

Potential improvements for extended functionality:

- Batch processing capabilities for larger datasets
- Configurable filter patterns beyond fixed digit removal
- Performance optimization for embedded systems
- Extended test coverage for additional edge cases