MIPS CPU Architecture: Design

The overall design of the CPU prioritises intuitive codebase structure, parallel development and modularity.

Bus-interface system [*mips_cpu_bus.v*]

The bus interface is designed to function as a wrapper that hands all memory transactions and ensures the interface abides by the Intel Avalon standard. Any updates relating to memory transactions is handled in the wrapper function.

This design decision allows for the parallel development of the CPU core and the memory interface. The modular design allows the CPU to potentially support other memory interface standards like Intel Avalon as long as the wrapper meets the required interface of the CPU core.

Control Unit placement [*mips_cpu_harvard_mod.v*]

The main block, the Control Unit, is placed within the main file instead of moving it into its own file. This design decision made to aid in forming an intuitive codebase structure. The main structure of the codebase is a classification system that classifies every instruction into:

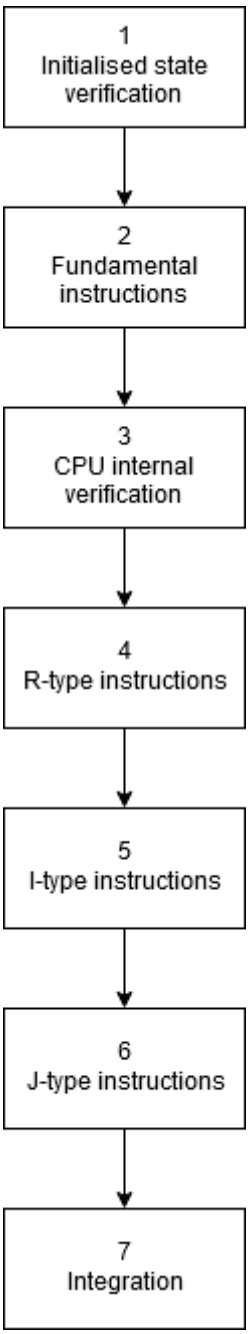
- *R-type*
- *I- and J- type*
- *Conditional branching*

Every control signal for a particular type is set within each of these blocks.

This design leverages the similarities of instructions to create an easy and readable structure by classification and sub-classifications. This continues the theme of modularity and ensures any requests made by the client can be quickly incorporated such as a new instruction. Standard commenting is used throughout the codebase to aid any future programmer hired by the client to make the changes. With the control unit incorporated into the classification system, this creates a compartmentalised design that allows easy debugging and prevents any changes from accidentally affecting other changes.

Testing and Verification: Testbench

The process of testing and verification of a given MIPS CPU is divided into 8 stages. All test files and outputs are located in the *"test"* folder of the main directory.



1. Initialised state verification:

   Verifying the MIPS CPU is behaving according to the development specifications during the start-up process. Checks completed include:
   1. During the reset stage, there are no memory transactions.
   2. First instructions executed by the CPU is in address "0xBFC0000".

   The testbench performs this stage in a special block at the beginning of the test process.

2. Fundamental instructions:

   Instructions like addition (*addiu*), jump (*jr*) and loading/storing memory content (*lw*/*sw*) are considered fundamental instructions from which testing of more complicated instructions are dependent on.

   These are loaded from the test folder *"2-Fundamental"*. Failing these instructions means other instructions have a high possibility of failing as well.

3. CPU internal verification:

   This stage of verification ensures operational aspects of the CPU follows the design specification and the general MIPS architecture. The main checks performed are:
   1. CPU fetches the next instruction from the correct address.
   2. All internal storage locations are set to 0 during a reset.
   3. Upon finishing executing instructions, the MIPS CPU halts and outputs the required data accordingly.

4. R-type, I-type and J-type instructions:

   All MIPS instructions defined in the design specification are divided into three types of instructions and each type is tested stages as defined in the test flow diagram. Respective instructions and outputs are in *"test"* folder.

7. Integration testing:

   The final stage of the testing process is to combine multiple types of instructions together and perform some simple arithmetic processes such as Fibonacci sequences.

Summaries of the functions of each of the test cases are available in each folder of the specified stage of testing stage.

Cyclone IV E 'Auto': Area and timing summary

Flow Status:	Successful - Mon Dec 14 11:50:05 2020
Quartus Prime Version:	16.0.0 Build 211 04/27/2016 SJ Lite Edition
Revision Name:	mips_cpu_bus
Top-level Entity Name:	mips_cpu_bus
Family:	Cyclone IV E
Total logic elements:	8,674 / 15,408 (56 %)
Total combinational functions:	8,092 / 15,408 (53 %)
Dedicated logic registers:	1,250 / 15,408 (8 %)
Total registers:	1250
Total pins:	138 / 344 (40 %)
Total virtual pins:	0
Total memory bits:	0 / 516,096 (0 %)
Embedded Multiplier 9-bit elements:	16 / 112 (14 %)
Total PLLs:	0 / 4 (0 %)
Device:	EP4CE15F23C6
Timing Models:	Final