DELFT UNIVERSITY OF TECHNOLOGY

SC42095 - CONTROL ENGINEERING

Orientation Control in Space

 $Emiel\ Legrand\ ^{\dagger}$

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 $^{^{\}dagger}4446100$ - e.b.legrand@student.tudelft.nl

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1 Introduction

[Intro here]

2 Continous-time PID controller

2.1 Analysis of the plant

The transfer function of the plant is

$$G(s) = \frac{s+20}{s(s^2+24s+144)} \tag{1}$$

Clearly, the system has two poles at s = -12 and one pole at the origin. There is one zero located at s = -20 (all on the real axis). A pole-zero map of the system is shown in fig. 1. From inspection of the poles and

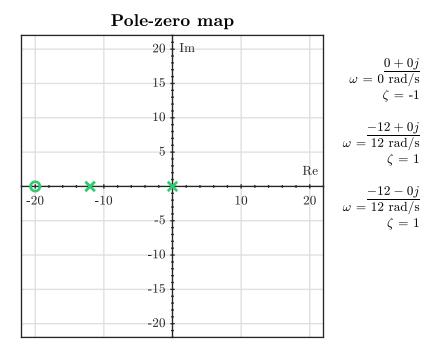


Figure 1: Pole-zero map of the continuous-time plant model. Clearly, the plant has only real, stable poles and zeros.

zeros, it can be concluded that the plant is 3^{rd} -order, minimum phase and open-loop stable. Furthermore, because of the pole at s = 0, this is a so-called Type-I system. This means that the system is able to track a step reference with perfect steady-state accuracy. Looking at the frequency response function associated with eq. (1) shown in fig. 2, a few additional remarks can be made:

- Because the system is Type-I, it approaches $j\omega = 0$ with a slope of $-20\,\mathrm{dB/dec}$.
- The stability margins of the system are ample: the phase margin is 89.1° and the gain margin infinitely large since the system never crosses (although barely) the -180°-line. The system is therefore *structurally* stable, i.e. the gain can be increased arbitrarily without causing the poles to venture into the right-half plane.
- Overall, the plant shows moderate gains around for low-frequencies and very strong attenuation of frequencies higher than those associated with the double pole at 12 rad/s.

2.2 Set-point tracking (Question 1)

First, a PID-controller has to be designed for reference-tracking. The following constraints are imposed on the design:

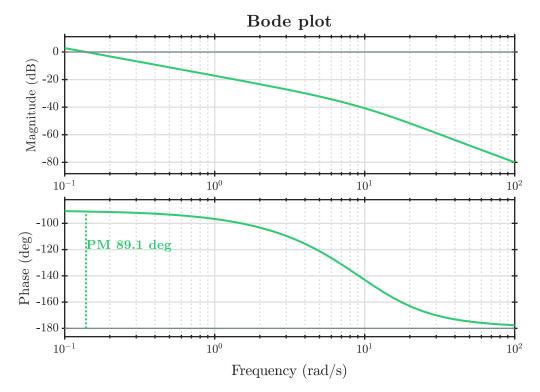


Figure 2: Bode plot of the plant. The stability margins are indicated on the plot (the phase margin is 89.1°, the gain margin is infinite).

- Minimal settling-time
- \bullet The response overshoot shall not exceed 5%
- No steady-state error

Controller structure Because the system is Type-I, integral action will not be necessary to avoid steady-state tracking errors. Although the stability margins are very generous, adequate performance may be achieved purely by proportional control. However, due to the strict overshoot requirements and the desire to reduce the settling-time to an absolute minimum, more damping will likely be required in the form of one or two D-terms, resulting in a PD(D)-type controller.

Frequency-domain requirements The formerly stated requirements are specified in the time-domain. Because the controller design will be achieved by shaping the loop transfer function, it makes sense to translate these requirements to an (approximate) frequency-domain counterpart. Because analytical results only exist for 2nd-order plants, these results will only serve as an approximate target value. Some iteration using a simulation of the closed-loop step response will be inevitable to fine-tune the controller design.

As specified by Nise [3], the following relations hold for a 2^{nd} -order plant. First of all, the relation between the bandwidth of the closed-loop system and its settling time is:

$$\omega_{BW} = \frac{4}{T_s \zeta} \sqrt{(1 - 2\zeta^2) + \sqrt{4\zeta^4 - 4\zeta^2 + 2}}$$

Hence, to minimize the settling time one preferably has a damping ration ζ close to unity and maximise the $\omega_{\rm BW}$, which in turn means that the cross-over frequency of the loop transfer function should be as large as possible. Furthermore, the overshoot of the system can be related to the damping ratio as follows:

$$\%OS = 100 \times \exp\left(-\frac{\zeta\pi}{\sqrt{1-\zeta^2}}\right)$$
 (2)

This equation suggests that for an overshoot of 5%, one should aim for $\zeta \approx 0.69$. Since ζ is still not directly visible on the loop transfer Bode plot, there also exists a relation between the damping ratio and the phase margin ϕ_m :

$$\phi_m = \tan^{-1} \left(\frac{2\zeta}{\sqrt{-2\zeta^2 + 1 + \sqrt{1 + 4\zeta^4}}} \right)$$
 (3)

Based on the required ζ , this yields a target for the phase margin of ca. 64.2°.

Loop shaping The computed target phase margin suggests to start with pure proportional control and increase K_p until the phase margin has decreased from 89.1° to 64.6°. Figure 2 hints that the new crossover frequency should then be at 4 rad/s, which means the gain can be increased by 29.9 dB. This simple step already results in a dramatic increase in the settling time from 32.7 s (no compensation) to 1.04 s.

The overshoot for this controller is only 4.7%, which is not quite limiting. As such, there is some more room to increase the gain further to 31.7, which results in a very marginal reduction of the settling time. Now, the limit of simple proportional control has been attained: in order to speed the response up even further, more damping (i.e. phase lead) must be added at the appropriate frequencies in order to observe the overshoot limit.

A realizable PD-controller has the following transfer function:

$$K_p \left(1 + \frac{sT_d}{1 + sT_d/N} \right) = K_p \frac{1 + T_d(N+1)s/N}{1 + sT_d/N} \tag{4}$$

which is essentially the same as a lead-compensator with a pole far into the left-half plane $(N \gg 1)$. The choice of N determines the second corner frequency and is dependent on the physical implementation of the system and the actuators, since it will determine noise amplification and the initial jump in the controller effort. Keviczky et al. [2] recommend this value between 4 and 6 during controller design, after which it can be retuned after testing with the physical plant. Hence, for the controller design, a value of N=5 was chosen. The choice of N places an irrevocable limit on the maximum attainable phase contribution by the PI controller, as given by the following equation¹: [4]

$$\phi_{\text{max}} = \sin^{-1} \left(\frac{N}{N+2} \right) \approx 45^{\circ} \tag{5}$$

As mentioned before, the maximum phase contribution of the lead contribution occurs at the geometric mean of the pole and zero frequencie: [4]

$$\omega_{\phi_{\text{max}}} = \frac{N}{T_d \sqrt{N+1}} \tag{6}$$

Using eqs. (5) to (6), the maximum phase contribution was placed at the highest frequency where the plant could still have the target phase margin of 64.4° (i.e. the frequency at which the plant has a phase of $180^{\circ} - 64.4^{\circ} - 45^{\circ}$). This is shown as iteration #3 in table 1. In order to obtain the desired performance, the proportional gain K_p must be adjusted accordingly. The result is iteration #4 in table 1; the settling time shows a substantial reduction of %65 to 0.39 s. Finally, the controller was tuned a little more: in order to achieve minimal settling time, the response must be well-damped as illustrated by eq. (3). The controller was therefore retuned to have a higher phase margin (70°) — from fig. 3 it is clear that this iteration has much better damping and a better settling time. At this point, the limits of the PD-controller architecture are reached, due to the limited phase contribution given by eq. (5), sufficient phase margin can only be guaranteed up to a certain frequency.

Using yet another D-term the phase contribution can be increased even more; the result is a PDD-controller:

$$K_p \left(1 + \frac{sT_{d_1}}{1 + sT_{d_1}/N} \right) \left(1 + \frac{sT_{d_2}}{1 + sT_{d_2}/N} \right) \tag{7}$$

¹The relations from Ogata [4] are based on a different parameterization of the compensator, but they are equivalent to those mentioned in this report.

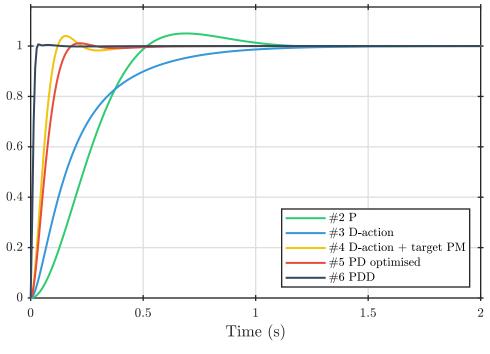


Figure 3

The idea behind the tuning process of these terms was to extend the region with sufficient phase towards higher frequencies without creating excessive 'bumps' in the phase curve to obtain an even response. To do so, one lead compensator was placed to have its $\phi_{\rm max}$ at about the same frequency as the previous one, while the other one was placed at a frequency about five times higher. The resulting phase and magnitude curves are, together with the previous iterations, displayed in fig. 4. Again, to achieve sufficient damping, the proportional gain was adjusted accordingly for a similar phase margin as iteration #5, ca. 71°. This final iteration results in a tenfold reduction of the settling time to 0.0251 s.

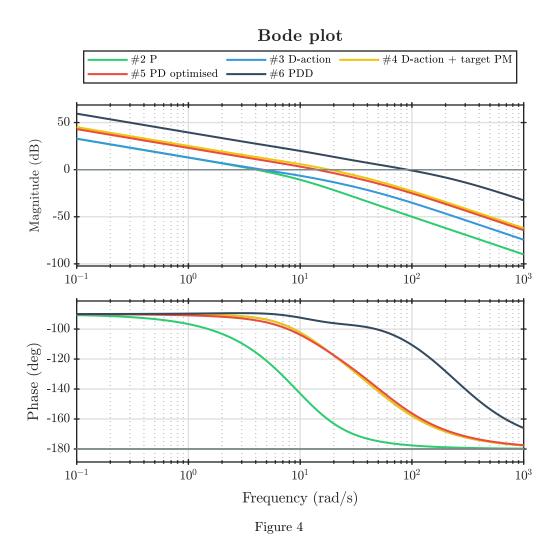
Table 1: Overview of the loop shaping process of the reference tracking controller.

#	K_p	T_{d_1}	T_{d_2}	$\phi_m \text{ (deg)}$	%OS	$T_s(s)$
0	1	0	0	89.1	0	32.7
1	31.14	0	0	64.6	4.7	1.04
2	31.71	0	0	64.2	5	1.03
3	31.71	0.112	0	86.8	0	1.08
4	130.8	0.112	0	64.7	4	0.387
5	102.4	0.102	0	70	1.1	0.233
6	675.8	0.102	0.0204	71.3	0.71	0.0267

2.3 Disturbance rejection (Question 2)

In this section, another contoller will be designed specifically for the rejection of a load disturbance q that acts on the control input in the form of a step input. The following requirements are to be fullfilled:

- Minimal amplitude of the output as a result of the disturbance.
- Minimal duration of the disturbance.



• The disturbance shall cause no offset in the response.

Controller structure The closed-loop transfer function from the load disturbance q to the output y is straightforward to determine:

$$G_q(s) = \frac{G(s)}{1 + G(s)K(s)} = G(s)S(s) \text{ with } S = \frac{1}{1 + G(s)K(s)}$$
 (8)

where S(s) is the so-called sensitivity transfer function of the closed-loop. Clearly, the sensitivity function will have the poles of the loop transfer function as zeros. Section 2.1 already mentions that the system is Type-I. Therefore, the sensitivity function must have a zero at s=0. As such, in the transfer function $G_d(s)$ the zero from S and the pole from G_d cancel. In order to meet the requirements and have no steady-state offset in the response due to the load disturbance, the final value theorem states that $\lim_{s\to 0} sG_d(s)\frac{1}{s}$. As such, $G_d(s)$ must have a zero at s=0 (which of course should not be cancelled). This can be achieved by placing an extra pole in the controller at s=0; in other words: integral action will be instrumental to eliminate steady-state offset as a result of the load disturbance. Hence, the controller will be of the type PI(DD).

Frequency-domain requirements Ideally, the transfer function from the disturbance q to the output y is no-pass (i.e. none of the frequency components in the disturbance persist to the output). Of course, this is not achievable. However, from inspection of eq. (8) it is clear that for frequencies where the loop gain

|G(s)K(s)| is high will $G_d(s)$ will show proper damping. Hence, high proportional gain and lag compensation (i.e. high gain contribution at lower frequencies) will decrease the settling time of the output after the introduction of the step load disturbance. The plant itself is low-pass with a very low crossover frequency; hence one can expected that high controller gain will be required to reject the disturbance quickly. Besides, the aforementioned requirements will likely contradict with those of the previous controller: where for the tracking case a generous phase margin reduced the settling time, higher damping in the case of disturbance rejection will jeopardise the controller's ability to amplify frequency components to a sufficient extent which in turn would mitigate the effect of the load disturbance on the output.

Loop shaping It is already known that a PI-controller structure will be inevitable to obey the imposed constraints. As such, the limits of this controller type will be explored first after which the potential extension to a PID(D) type controller can be investigated. The PI-controller has the transfer function

$$K_p\left(1 + \frac{1}{T_i s}\right) \tag{9}$$

which has a pole at s = 0 and a zero at $s = -1/T_i$. The zero determines the second corner frequency of the controller, and therefore up to which frequency the amplification occurs. Simultaneously, the PI controller will introduce a destabilising phase lag for lower frequencies, also determined by the position of this zero.

Because the proportional gain K_p does not affect the phase curve of the system, the maximum attainable phase margin (i.e. where the phase curve is maximal) is purely determined by the choice of T_i . A higher phase margin gives better damping of oscillatory respones but also means that T_i must be higher, which decreases the amplification of the lower frequencies with a deterioration of the settling time as a result (the slower frequencies will take longer to be rejected by the system). Oscillations in the response may on the other hand also slow down the time it takes for the output to return to zero, so a compromise has to be found. Figure 5 shows a comparison of three values for the phase margin: for each of these, T_i was tuned to make sure that the maximum attainable phase margin would be equal to a set value (35°, 41° and 45°), after which K_p was tuned to set the crossover frequency at the correct value. Clearly, the settling time is lowest for $\phi_m = 40$ °, so this value was used as an approximate tuning value for T_i .

It has to be noted that the two first requirements are conflicting, since both the peak amplitude and the settling time must be minimised, without a quantifiable priority of one over the other. Indeed, in fig. 5 one can see that for $\phi_m = 35^{\circ}$, the peak value is slightly lower. However, because the relative difference in the peak value is relatively low compared to the difference in settling time, $\phi_m = 40^{\circ}$ is said to show the 'better' performance.

At this point, no better performance (in terms of settling time) can be achieved by using the PI controller structure: to lower the settling time T_i must be decreased to amplify the lower frequencies to a greater extent. However, this creates two issues: firstly, the phase curve will at some point cross the -180° line, which will render the system immediately unstable: the gain will cross-over at a higher frequency. Decreasing the gain is not an option since it will yield a dramatic increase of the peak amplitude. Secondly, as illustrated by fig. 5 the smaller phase margin results in badly damped oscillatory artefacts in the response even before the point of instability is reached. Therefore, one must resort to D-action to add phase advance at these higher frequencies to keep sufficient phase margin and prevent the phase from crossing over. As in section 2.2, a realizable D-term as described by eq. (4) will be used with N = 5.

The loop shaping process for the PID controller was as the following: first, the T_d term was chosen such that the maximum phase contribution occurs at a frequency where the phase of the previous controller was about -170° . This left about 15° of excess phase (that is on top of the 'ideal' 40°), which could then be absorbed by decreasing T_i further. In the subsequent tuning process, the purpose was always to decrease T_i as much as possible while keeping sufficient phase margin and prevent the phase from crossing the -180° line. Finally, K_p was chosen to set the cross-over frequency at the peak of the phase curve. The best PID controller turned out to achieve a settling time of 700×10^{-3} s and a peak amplitude of 2.85×10^{-3} .

The final performance of the PID controller begs the question whether additional performance improvements could be made by adding additional gain with another D-term, just like in section 2.2. The tuning of this PIDD controller was straightforward: one of the lead compensator was kept at a lower frequency to keep the phase from dipping under the -180° line, while the other lead compensator was placed at a frequency



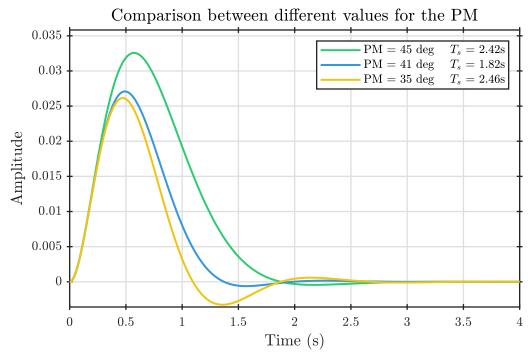


Figure 5

of about $140\,\mathrm{rad/s}$ to be able to have the desired phase margin at higher frequencies. After tuning, the resulting PIDD controller resulted in a settling time of $438.1\times10^{-3}\,\mathrm{s}$ and a peak amplitude of 71.77×10^{-6} . Although this performance is of course very nice, one can observe from fig. 7 that the result from the PIDD is not desirable as for the other controllers, in the sense that there is a large phase contribution at lower frequencies and therefore inevitably also a decrease in gain amplification. This has as the result that the speed up of the settling time is 'only' %50. The problem is that due to the impending instability, the phase contribution could not be placed at higher frequencies to make it more limiting. One could therefore wonder whether the added complexity of the PIDD controller is worth the modest advancement in performance.

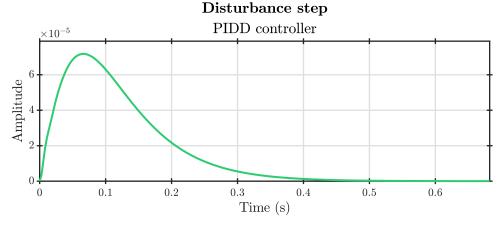


Figure 6

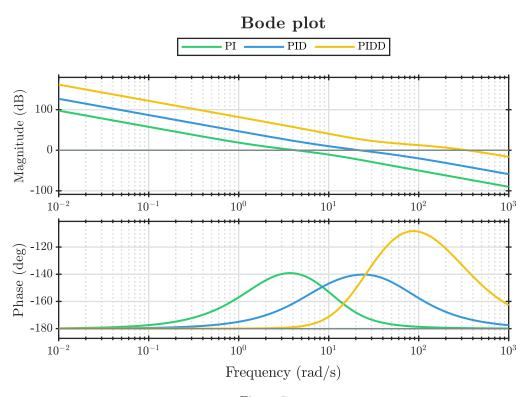


Figure 7

3 Discretisation of the problem

3.1 Discretisation of the plant (Question 3)

The transfer function of the plant (eq. (1)), has the state-space realization in the following canonical form:

$$\frac{\mathrm{d}x}{\mathrm{d}t} = \begin{pmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 0 & -144 & -24 \end{pmatrix} x + \begin{pmatrix} 0 \\ 1 \\ -4 \end{pmatrix} u$$

$$y = \begin{pmatrix} 1 & 0 & 0 \end{pmatrix} x$$
(10)

It is known that the output of the system represents the orientation of the space station. From the state space description, it is therefore clear that the first state must also be equal to this orientation. Then, from the first state-space equation it is clear that $\frac{\mathrm{d}x_1}{\mathrm{d}t} = x_2$; which means that x_2 represents the angular velocity associated with the orientation of the spacecraft. Again, $\frac{\mathrm{d}x_2}{\mathrm{d}t} = x_3 + u$. Clearly, u acts as a torque on the change in angular velocity; x_3 must therefore represent the angular acceleration. The third equation states that $\frac{\mathrm{d}x_3}{\mathrm{d}t} = -144x_2 - 24x_3 - 4u$. It is not entirely evident what this equation represents, but it introduces some coupling between the angular velocity and the angular acceleration of the system. Therefore, one might guess that this equation represent some gyroscopic effect that is present in the rotational dynamics of the system — a common way to adjust the attitude of spacecraft is by means of so-called Control Moment Gyroscopes.

Discretisation of the plant To find a discrete-time state-space representation of the plant a suitable sampling period h has to be chosen. Åström and Wittenmark [1, p. 300] provides the rule for open-loop systems that

$$\omega_c h \approx 0.15$$
 to 0.5

where ω_c is the crossover frequency of the open loop system. Based on this rule, a sampling period of $h = 1.08 \,\mathrm{s}$ was chosen; which is rather low, but so it the closed-loop uncompensated step response of the plant. Using the zero-order hold method, the resulting discrete-time state-space model is:

$$x(k+1) = \Phi x(k) + \Gamma u(k) \qquad y(k) = Cx(k) + Du(k)$$

$$\Phi = \begin{pmatrix} 1 & 0 & 0 \\ 0.166663739616237 & 0.000032777038157 & -0.000365153653910 \\ 0.006944216826124 & 0.000002535789263 & -0.000028081904161 \end{pmatrix}$$

$$\Gamma = \begin{pmatrix} 1.080177590517217 \\ 0.159196525309621 \\ 0.006343846186812 \end{pmatrix} \quad C = \begin{pmatrix} 0 & 1 & -4 \end{pmatrix} \quad D = 0$$

$$(11)$$

3.2 Discretisation of the controllers (Question 4)

Now, both the controllers from sections 2.2 and 2.3 and the plant are discretised separately, after which a closed loop response simulation is performed. Again, another rule of thumb is used from Åström and Wittenmark [1, p. 317] for PID-type controllers:

$$\frac{hN}{T_d} \approx 0.2 \text{ to } 0.6$$

Of course, the controller designs were of type PIDD so some care had to be taken when using this method.

Tracking controller The tracking controller was discretised using the Tustin approximation while the plant was discretised using the zero-order hold method (both with identical sampling period). The sampling period was computed using the aforementioned rule with the largest of the two T_d 's. The resulting sampling

time was increased slightly more to obtain also a reasonable number of samples per rise time. The sampling time used was $h = 1.4 \times 10^{-3}$ s. The resulting simulation is shown in fig. 8; the discretised controller shows comparable performance with slightly higher overshoot and settling time.

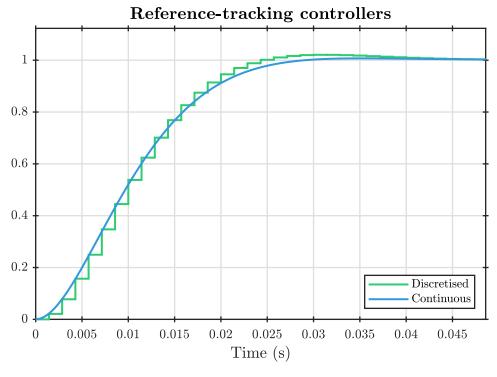


Figure 8

Disturbance rejection controller

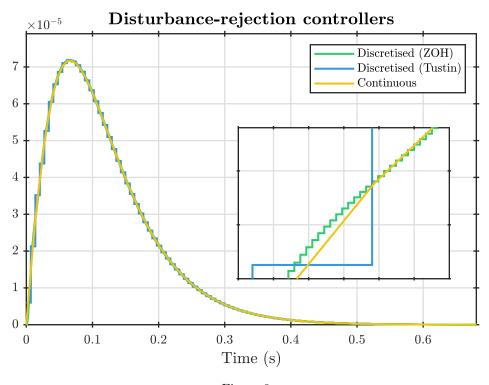


Figure 9

4 State-space approach for controller design

- 5 Taking into account actuator limits
- 6 Steady-state errors

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