

Advanced digital integrated circuits

ECE 212

VLSI DESIGN

Prof.Dr. Hossam Ahmed
The University of Minoufiya
Faculty of Electronic Engineering

Lecture (2)-MOSFET Fabrications for IC

Prof.DR. Hossam Ahmed

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Digital Integrated Circuit Technology and Design

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Course Administration

❑ Instructors: Prof Dr.Hossam Ahmed
Sure Days in the faculty

TA: Eng.

Office Hrs 10. to10.30 AM Wednesday

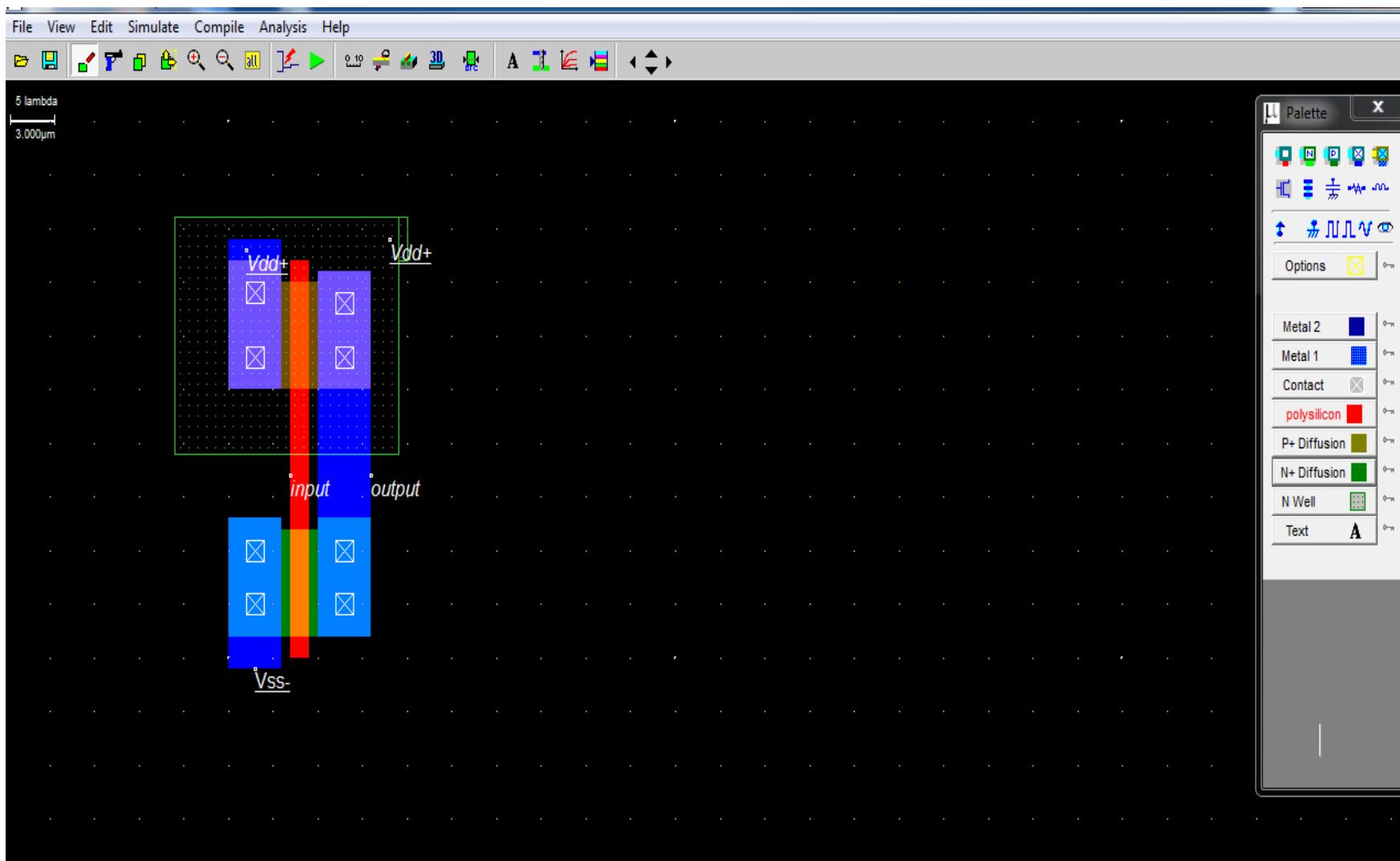
Lecture hours 12.00 to1.30 PM Sunday 1st group

Lecture hours 12.00 to1.30 PM Wednesday 2nd group

❑ Labs Microwind 3.5 Lite

❑ URL: www.Electronic.menofia.edu.eg

VLSI Lab



Degrees

- One mid term Exam. 10 degree
- Final Exam. 70 degree
- absence 10 degree
- ~ 5 homework's + several quizzes: 10 degree
 - One week to complete homework's (due on **monday**). Received at the lecture end of monday.
 - Late homework's: **25%** off if turned in one class late, no credit if later
 - Show your work on the homework! Thought process is more important than final answer → partial credit given.
 - Short quizzes will be unannounced, during class period (no makeup's!)

❑Homework

- ❑Here is a first pass at the homeworks. I may add or drop questions; I'm posting them at the start of the next lecture so you can have some idea of what's coming up. Your solutions should include the reasoning as well as the numerical result.
- ❑6(six) Homework for all the year.
- ❑Start from 2nd week of Study year 12/02/2012

Textbook and References

□Required Books:

Digital Integrated Circuit Technology and Design

By:Hossam Ahmed.

Other useful References Books:

- Digital Integrated Circuits: A Design Perspective* by Jan Rabaey, A. Chandrakasan, B. Nikolic, Prentice Hall [Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic](#)
- CMOS VLSI Design A circuit and systems perspective (4th Edition)*, Neil Weste, David Harris, Addison Wesley
- Fundamental of semiconductor fabrication, Gar.S.May,Simon M. SZE, Willy
- CMOS Digital Integrated Circuits Analysis and design, Sung-Mo Kang, Yusuf Leblebici, 3rd Edition, McGraw Hill
- Analog VLSI: Circuits and Principles, Shih-Chii Liu et al., The MIT Press

Related Web sites for this course of study

<http://www.eelab.usyd.edu.au/elec5402/>

<http://www.cmosvlsi.com>

<http://bwrc.eecs.berkeley.edu/IcBook>

1-MOSFET Fabrications for IC

The Si Planer Technology

- A planar technology is required the availability of an **adequate** set of technology steps that allows the device realization from the top!

- 1) Wafer
- 2) Oxidation
- 3) Masking and lithography
- 4) Etching
- 5) Doping by thermal or Ion Implantation Diffusion
- 6) Metallization
- 7) Testing
- 8) Packaging

1-MOSFET Fabrications for IC The Si Planer Technology

1. Wafer

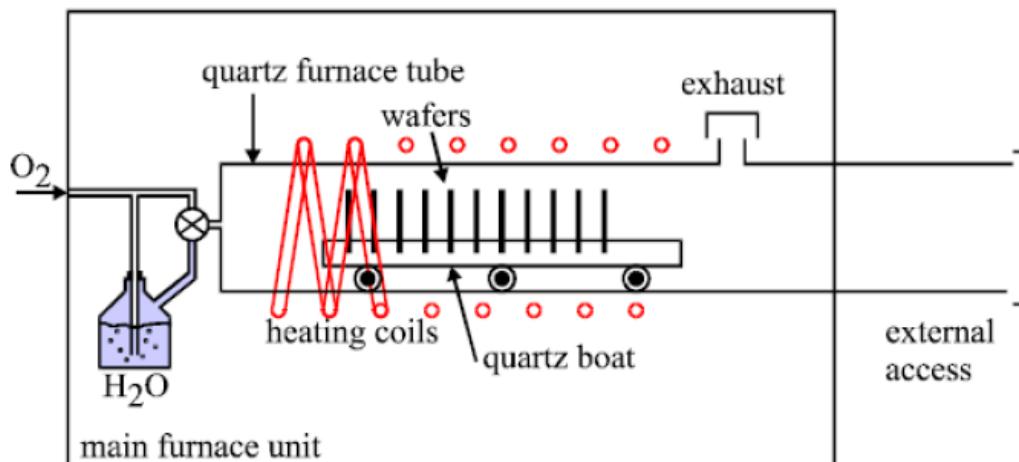
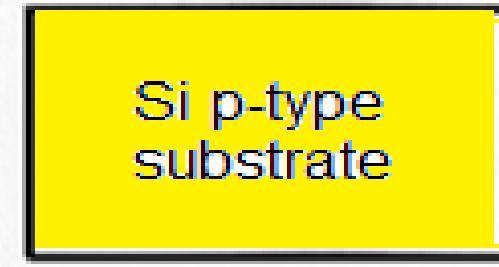
We start by the wafer which has
Prepared in the previous step

has face as a mirror with a blue-sky

color. We can cut it to cross sections called **dies** to obtain a p-type
substrate.

1. Oxidation

Realized by two method:

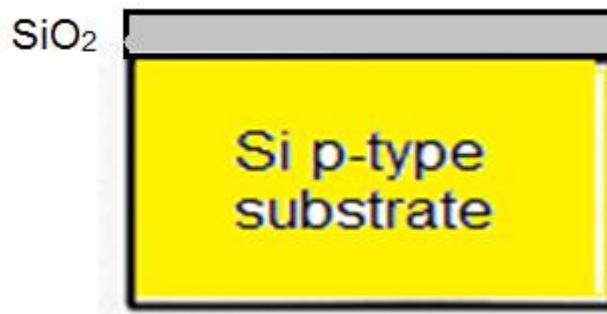


1. Wet oxidation

The silicon wafer placed into an atmosphere of water vapor (H_2O)



Give 700 nm oxide thickness in 0.65 hours at (1200°C), give poor oxide quality field oxide thickness.



2. Dry oxidation

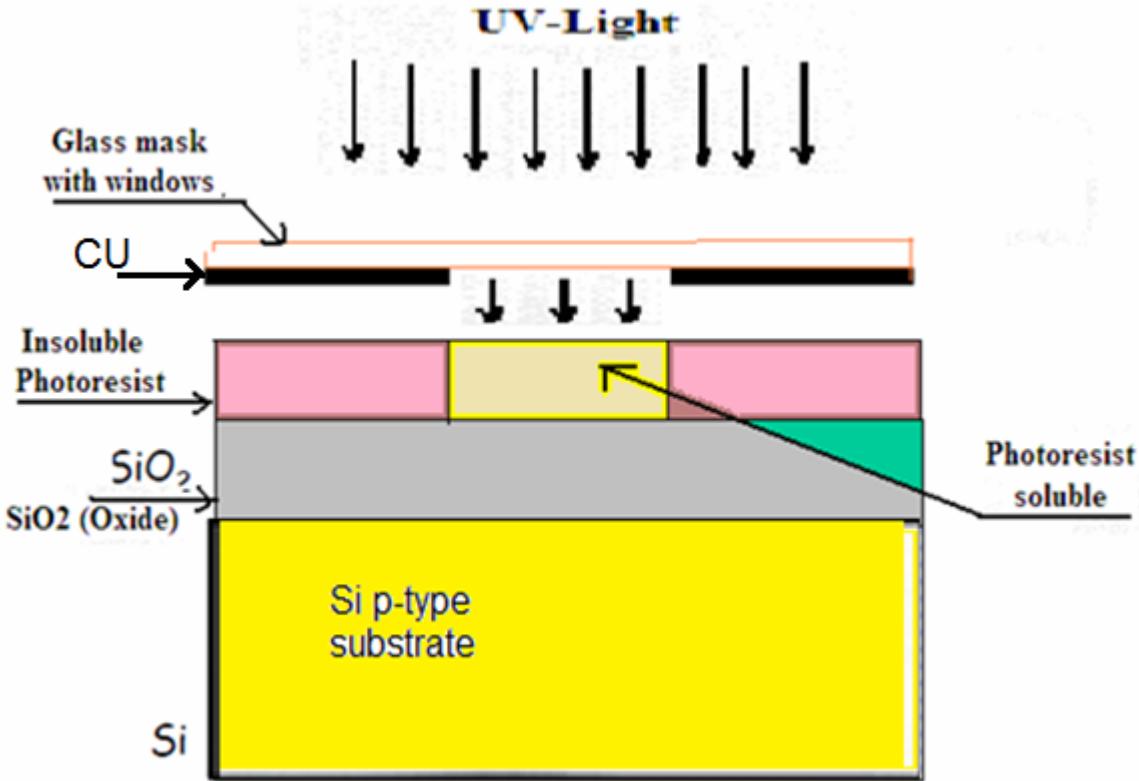
The Si wafer react with the ambient oxygen



Give a 700 nm oxide thickness in 10 hours (at 1200°C) , it has a good oxide quality.

3. Photolithography:

Positive photoresist



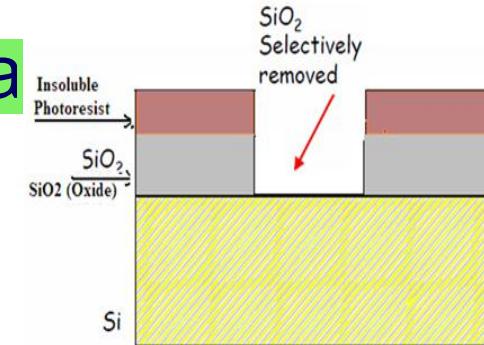
Negative Photo Resist (PR): A negative PR is hardened against the developer by the UV (Ultra Violet) radiation.

Positive Photo Resist (PR): A positive PR is the opposite, its hardened is removed by the UV (Ultra Violet) radiation

4. Etching :

1. Wet etching

Wet etching uses an acid, to remove a target material



2. Dry etching

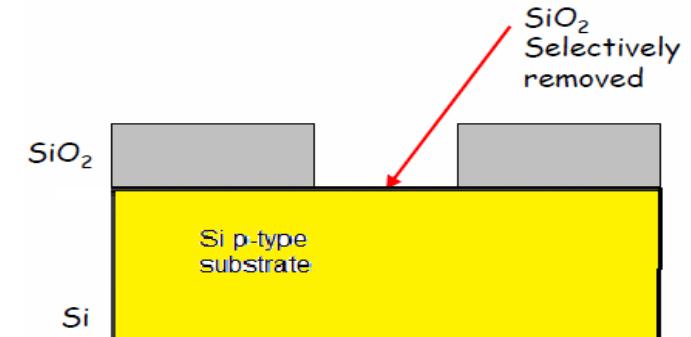
Dry etching uses gas instead of chemical etchants.

Etching the Oxide

When we put an oxide layer on a wafer and then **Etching** the oxide in the opens window by a **chemical acid** and then wash by **water** the bulk substrate.

Stripping

And then stripping the **insoluble photoresist**



5. Doping Types:

1. Epitaxy
2. Diffusion
3. Ion implantation

1. Epitaxy:

In this process a thin layer of single crystal semiconductor (nm to um) is grown on an already existing crystalline substrate

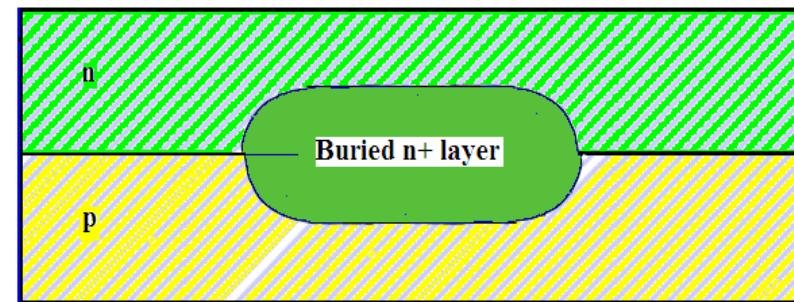
How to Create a buried n+ layer:

To create a buried n+ layer.

Growth an epitaxial of

few microns thick layer on the surface of substrate.

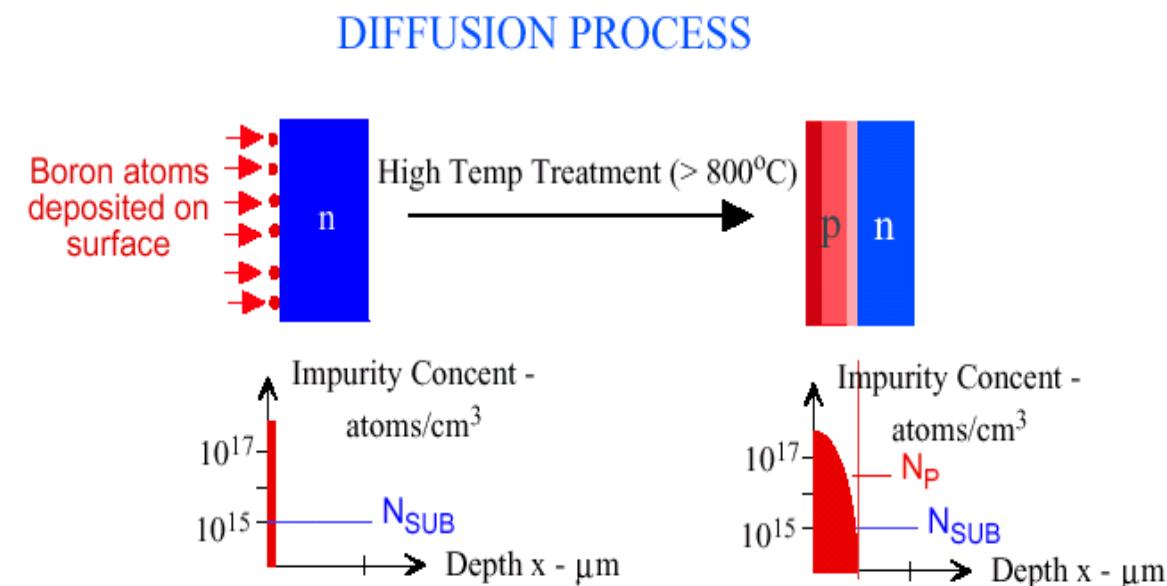
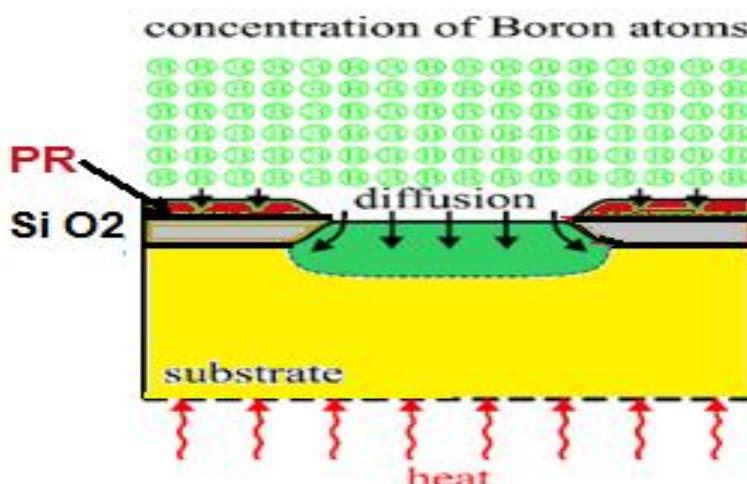
Use Epitaxial to create a buried n+ layer formed by suitable masking and diffusion.



2. Diffusion:

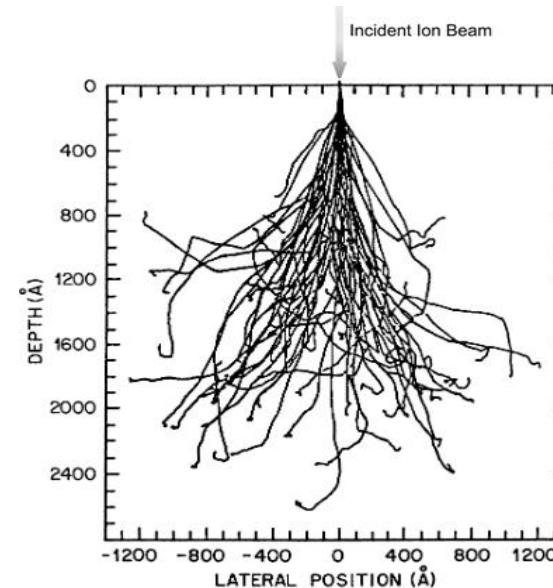
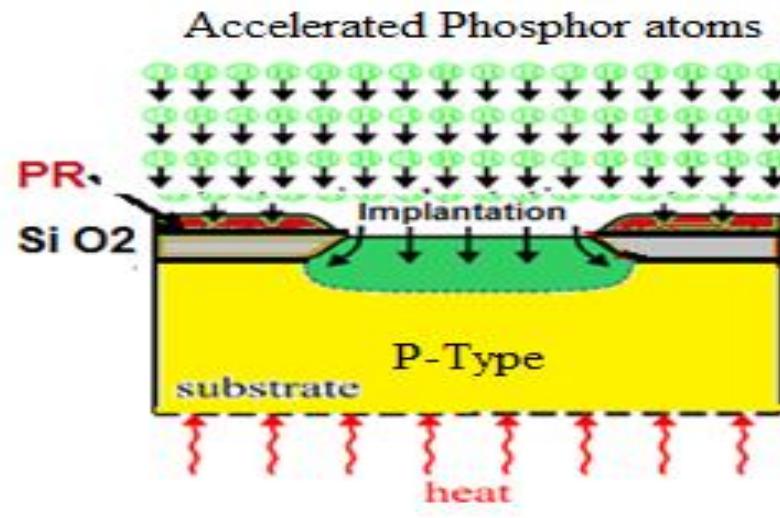
Thermal Diffusion

- p and n regions created by adding dopants into the wafer.
- Then the wafers heated at a temperature of about 1500-2200°F.
- The dopant passed through the wafers
- then drive in by heating

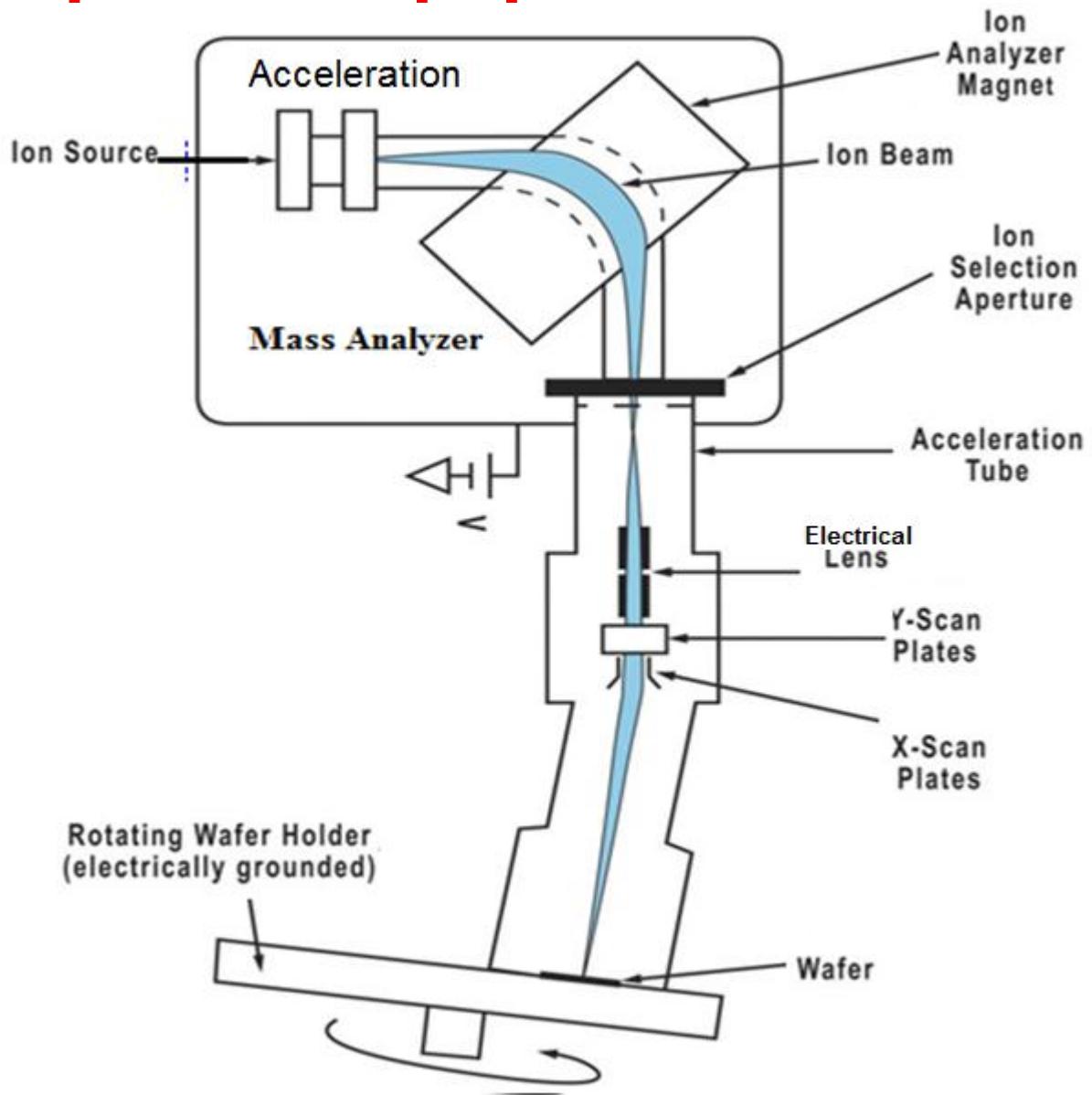


3. Ion implantation:

- First accelerated beam of high-energy dopant gas such as *phosphor ions* or *boron ions*, “shot” into the wafer surface.
- The depth of the penetration depends on the energy of the beam and orientation of crystal.
- An *annealing* (heating) step is necessary to *reorder* the crystal structure damaged by implant and *remove mechanical stresses*.



Implanter Equipment:



6. Metallization:

Metallization is a process of adding a layer of metal on the surface of wafer.

- **Aluminum:** A thin layer of aluminum deposited over the whole wafer.
Aluminum selected because it is a:
 - good conductor,
 - good mechanical bond with silicon,
 - forms low resistance contact.

7. Testing:

After the wafer has been processed and the final metallization pattern defined, it is placed in a holder under a microscope

8. Packaging:

Packaging is used to connect the IC to the outside world

The Si Planer Technology

We shall study four methods of planer Fabrication technology

1. Fabrication of Bipolar Junction Transistor (BJT) Planer Process
2. MOS Transistor fabrication Process
3. Self-Aligned Poly-Silicon Gate nMOS Transistor
4. CMOS Well fabrication Process
 - a)N-well CMOS
 - b)P-well CMOS
 - c)Twin Tube

1- Bipolar Junction Transistor (BJT) Planer Fabrication

1- Wafer

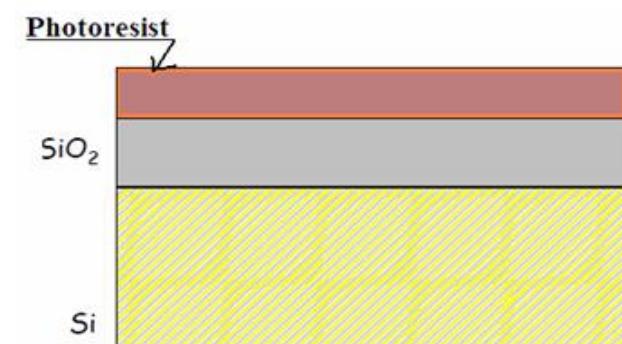
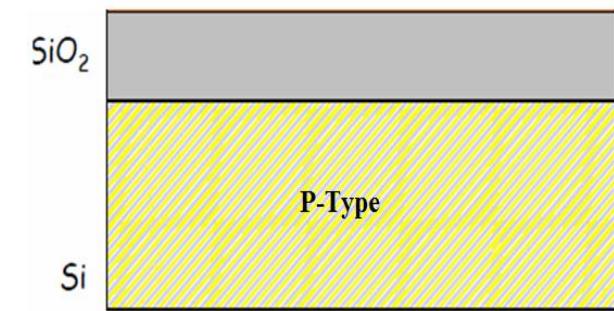
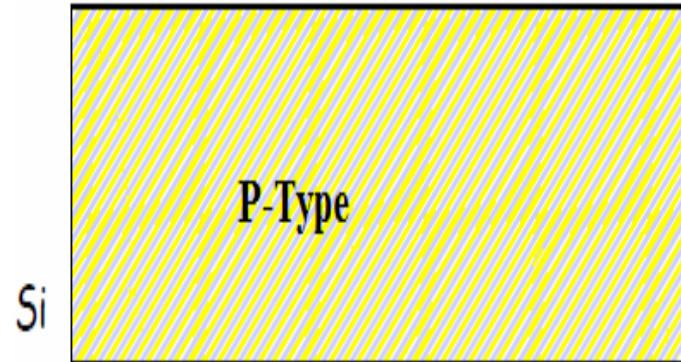
We start by the wafer which has Prepared in the previous step has face as a mirror with a blue sky color. We can cut it to cross sections called dies to obtain a p-type substrate

2-Oxidation

Silicon substrate with a thermal oxide layer on top

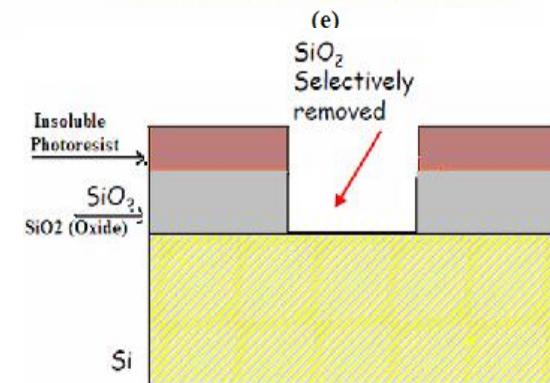
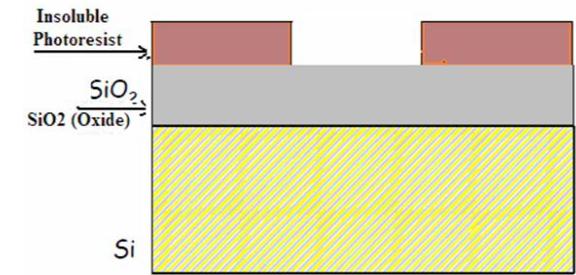
3) Photo lithography

- First the entire oxide surface is covered with a layer of positive photoresist

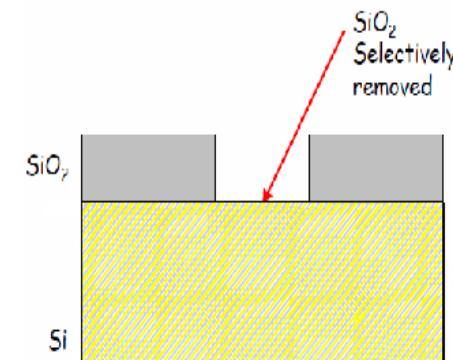


1- Bipolar Junction Transistor (BJT) Planer Fabrication

Exposed to UV and remove the soluble photoresist



Etching the oxide in the opens window



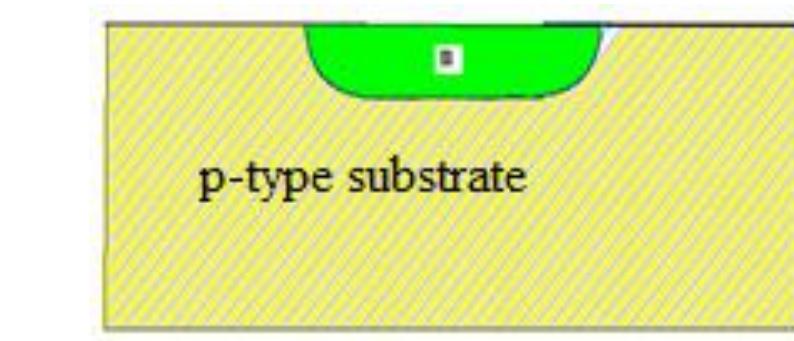
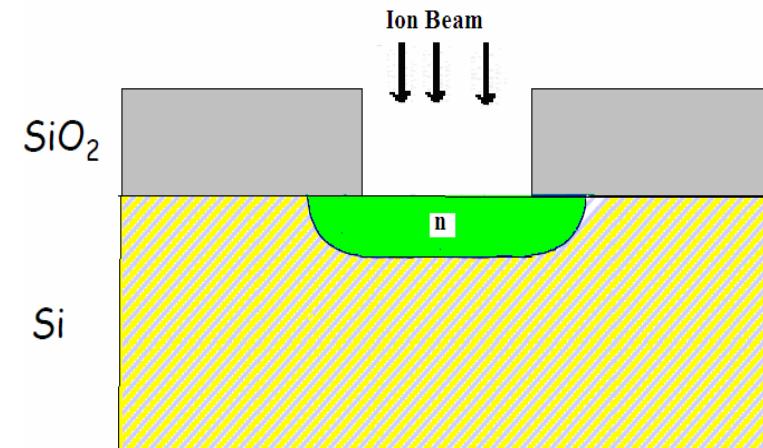
-Stripping ينزع the insoluble photoresist

1- Bipolar Junction Transistor (BJT) Planer Fabrication

4. In ion implantation

Dopants are introduced as ions into the material.

After introducing dopant, then thermal treatment to the dopant atoms will diffuse significantly only into the Si

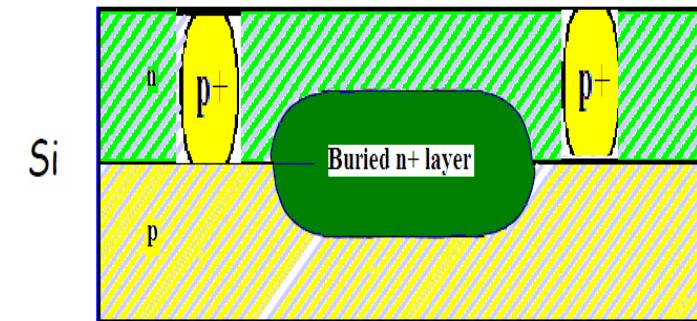


-After Ion implantation diffusion, we remove the rest of the oxide layer

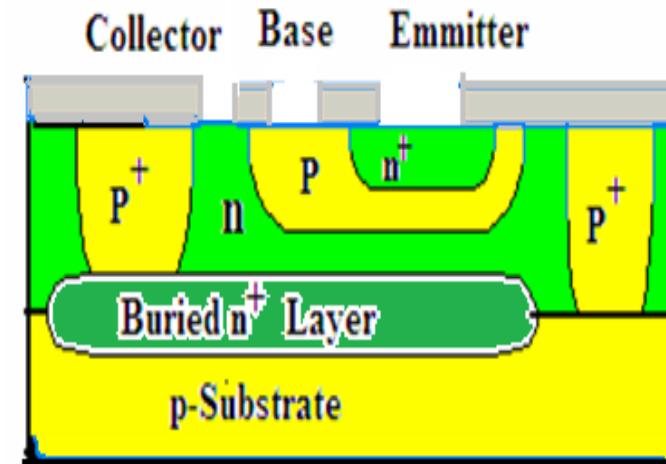
1- Bipolar Junction Transistor (BJT) Planer Fabrication

5. Epitaxial to create a buried n+ layer

-Protected diode by diffused a p+ region.

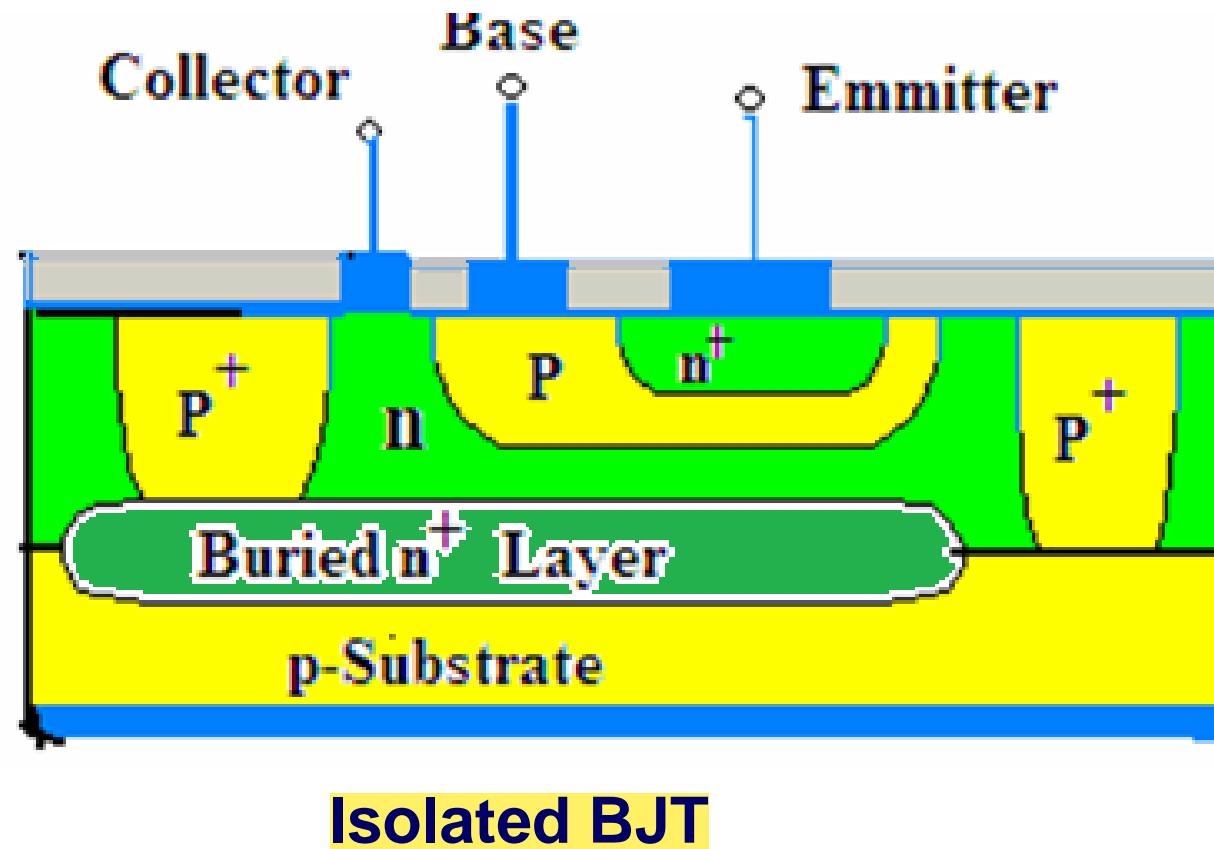


-Continue fabricate the base by 2nd mask and emitter by 3rd mask.



1- Bipolar Junction Transistor (BJT) Planer Fabrication

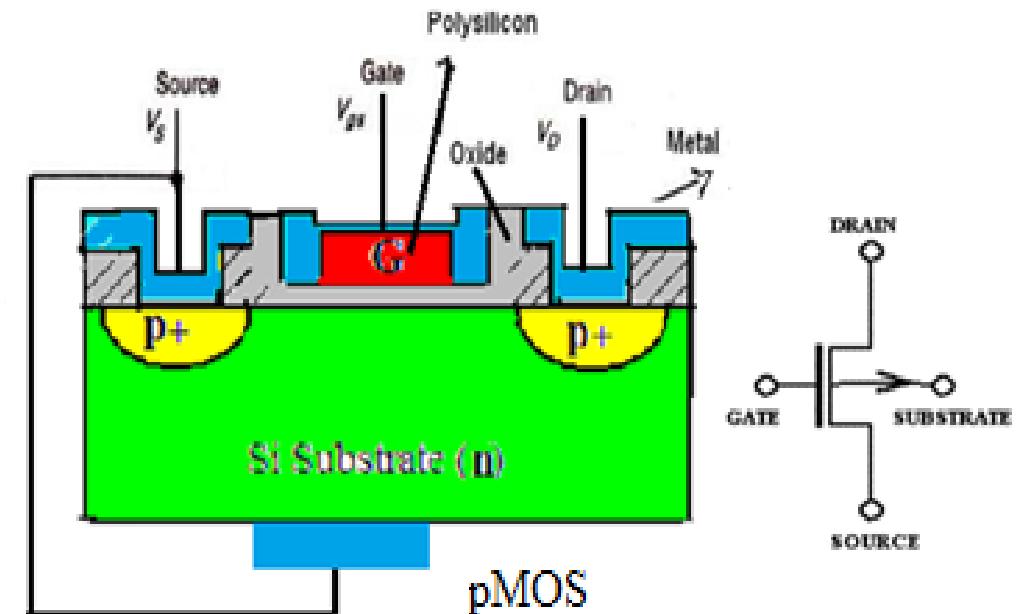
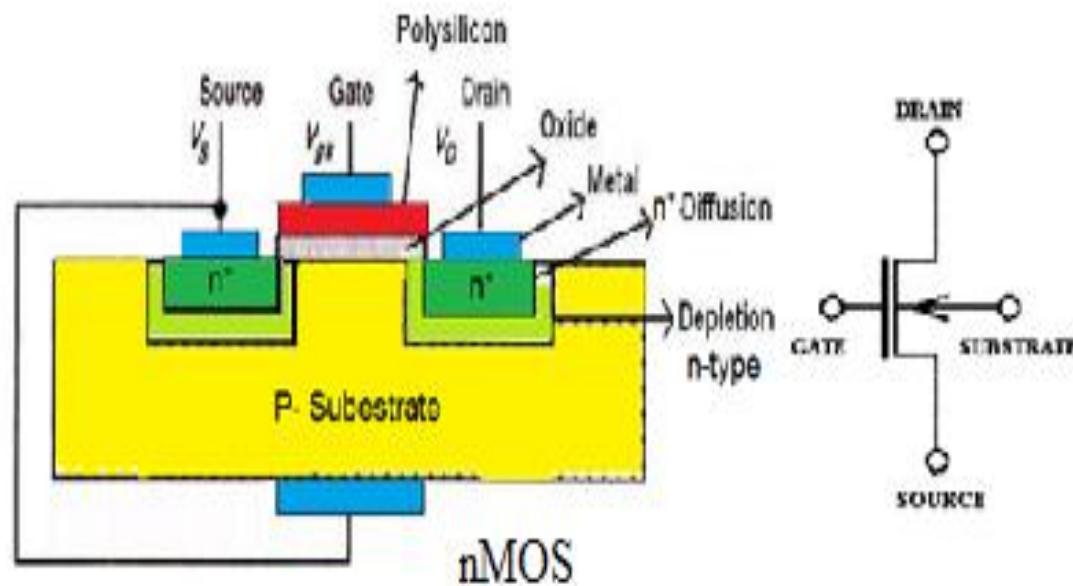
6. Metallization



2-MOS fabrication Process: Planer Technology

CMOS technology provides two types of transistors an n-type transistor (nMOS) and a p-type transistor (pMOS).

Cross-sections and symbols of these transistors are shown in Figure. The n+ and p+ regions indicate heavily doped n- or p-type silicon.



2-MOS fabrication Process: Planer Technology

- Each transistor has **conducting gate**, an **insulating layer** of silicon dioxide (SiO_2 , also known as glass), and the **silicon wafer** called the substrate/body/bulk.
- Even though the gate has formed from polycrystalline silicon (polysilicon), the name is still metal.
- An nMOS transistor built with a p-type body and has regions of **n-type** semiconductor adjacent to the gate called the **source and drain**. They are physically equivalent and they can be interchangeable. The body typically grounded.
- A pMOS transistor is just the opposite, consisting of **p-type source and drain regions** with an **n-type body**.

2- The six steps of nMOS fabrication Process

Transistor was fabricated with a simplified planer process which started with a (100) n-type silicon wafer with a resistivity 10-20 ohm-cm

Si substrate (P)

1. Field Oxide

We started by n-type substrate and first step is growth of a half-micron layer of thermal oxide, called "field oxide".

Si substrate (P)

2-The six steps of nMOS fabrication Process

2. Lithography Source and drain

Once this field oxide is grown, the next step is to opening windows by lithography.

So in this window we do the source and drain opening

3. Ion implantation

Ion implantation n-diffusion Source and drain lateral increase, which is more and more if source region is deeper

Si substrate (P)

Si substrate (P)

2-The six steps of nMOS fabrication Process

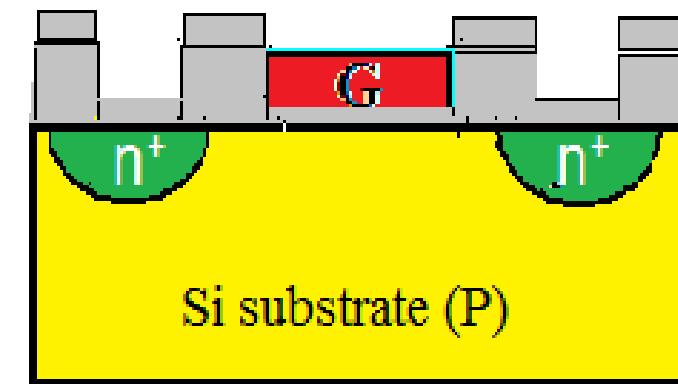
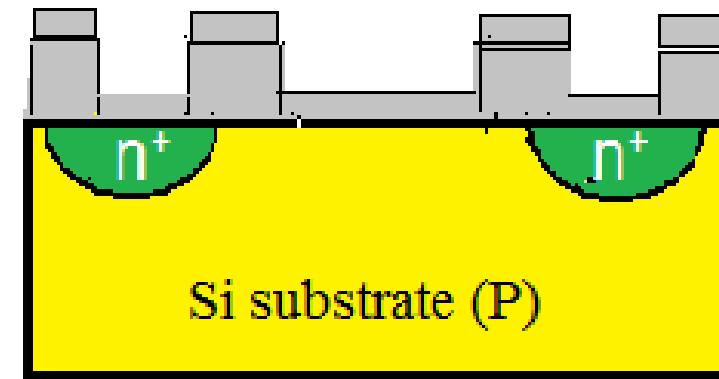
4. Gate thin Oxide

After this step is over there is another step to put thin oxide on S & D and gate.

We make gate Thin oxidation 0.81 mm to 1 mm is the technique of oxide with its mask thin oxide. (Thick oxide is about 200mm).

5. Polysilicon gate

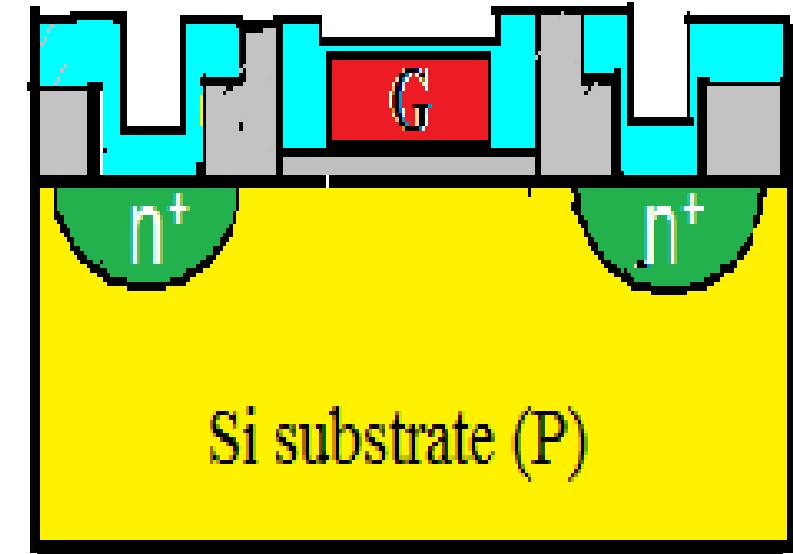
Polysilicon lithography for gate



2- The six steps of nMOS fabrication Process

6. Metal contact

Mask Lithography for poly gate.
We need to put the metal gate G
and then open the thin oxide in S &
D regions to connect them to outside
by a metal contact.



Polysilicon Gate contact as shown in figure (a). the three masks shown in figure (b).

