Ebrahim Hussain

ebrahimhussain@gmail.com - ebrahimwebsite.github.io

SKILLS

Software Python, Java, C, Verilog (Vivado and ModelSim), CAD (Onshape)

Hardware Arduino, RPi, FPGA, Digital and Analog Logic

Practical Soldering, Oscilloscope Usage and Lab Techniques, PCB Design (EasyEDA)

PROJECT EXPERIENCE

8-Bit Computer

2020-2021

An improved model of Ben Eater's 8-Bit CPU, capable of computing simple arithmetic such as the Fibonacci sequence. Received Senior Bronze Divisional at the 2021 Vancouver Science Fair (Provincial Level)

- Soldered logic chips to create registers, program counter, RAM, and clock modules.
- Designed and assembled a new program counter interface to implement jumps and conditional program execution.
- Developed a new PCB layout and FPGA substitute for interchangeable RAM to double available program memory.
- \bullet Improved instruction-retrieving opcode by 40% (on average) by adding a specialized instruction bus.
- Implemented infrastructure for writing to 16x2 LCD character displays.

Wireless Energy Transfer

2022

Applied relevant course theory into practice to create an efficient and low-power wireless energy transmitter using commonly available components.

- Created a low power DC to AC inverter without specialized components such as comparators, transformers, or excess transistors.
- Invented a self-recharging RLC oscillator by deriving a system of complex differential equations.
- Conducted circuit analysis with oscilloscopes and lab techniques to model and optimize circuit behaviour in relation to E&M theory.

Basys3 Frequency Generator

2020

Used a Basys-3 FPGA to create a precise and reliable clock module, capable of providing stable square wave frequencies up to 50 MHz.

- Created a clock divider interfaced with buttons to change the square wave frequency.
- Developed a scalable BCD to display the output frequency on a 4 digit 7 segment display.
- Implemented a manual, de-bounced clock mode triggered by button presses.
- Enhanced debugging features by implementing a clock bus to restrict access to certain clock-input logic on large projects.

EDUCATION