AHCAL test beam 2012 SPS

TDC calibration and data analysis

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- The AHCAL setup in 2012
- Status of SPS 2012 analysis
- MC digitalization
- TDC pedestal shift

AHCAL prototype 2012

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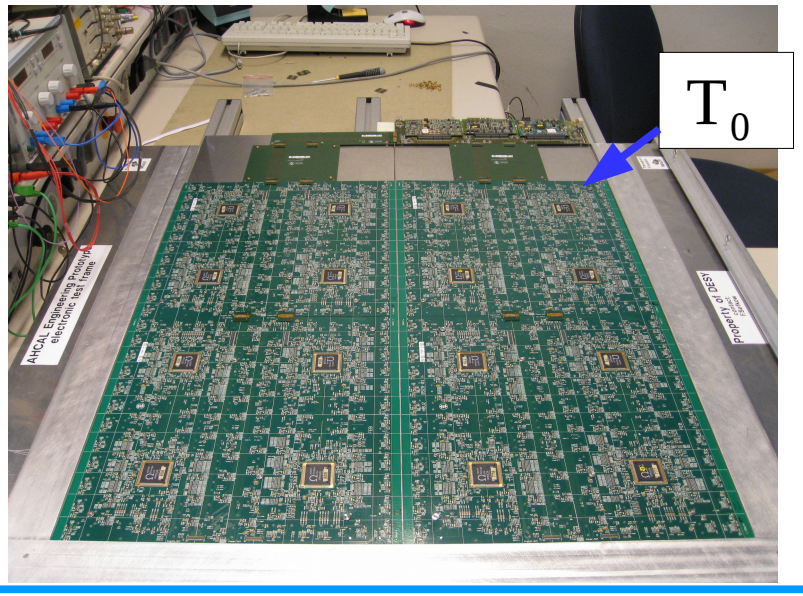
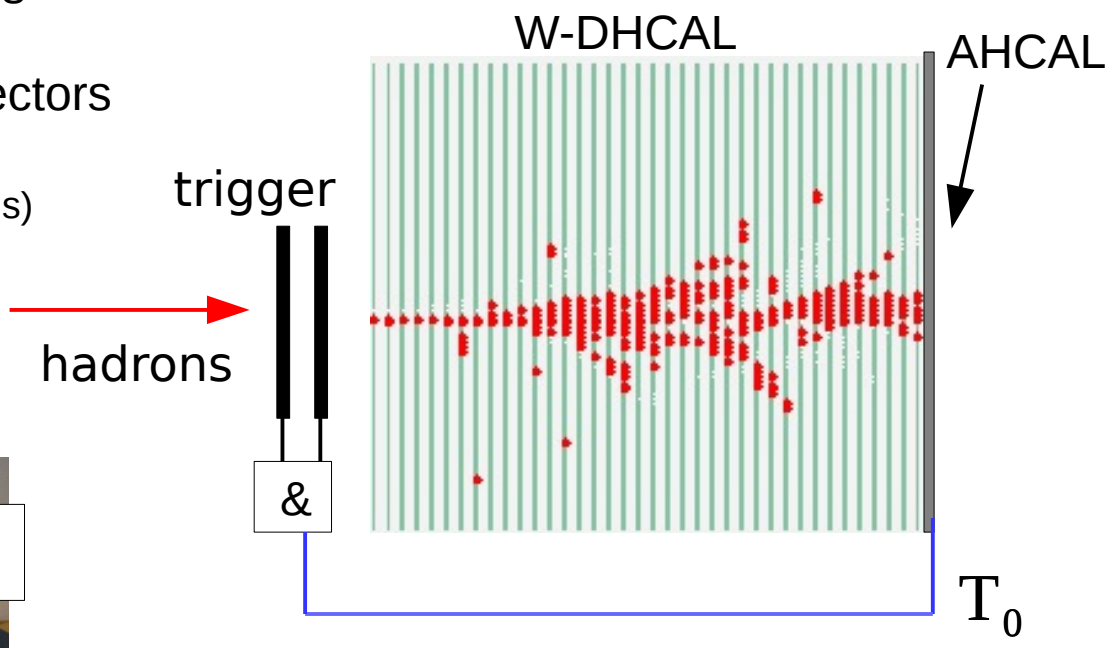
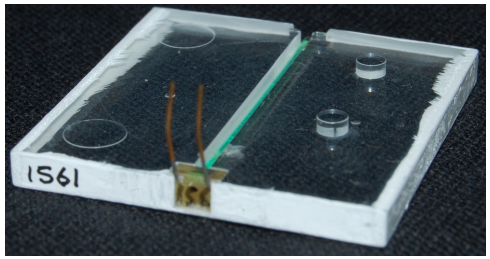
4D calorimetry provides precise and high resolution time stamping for
- Detailed investigation of hadronic showers and their simulation
- Improved event separation for future detectors

SPS 2012 (50 GeV 180 GeV Pions, 180 GeV Muons)
- One layer behind W-DHCAL prototype
- 4 HBU (ITEP tiles) with **576** channels
- Trigger as normal channel:







2012: ITEP tile

The readout chip - Spiroc2b

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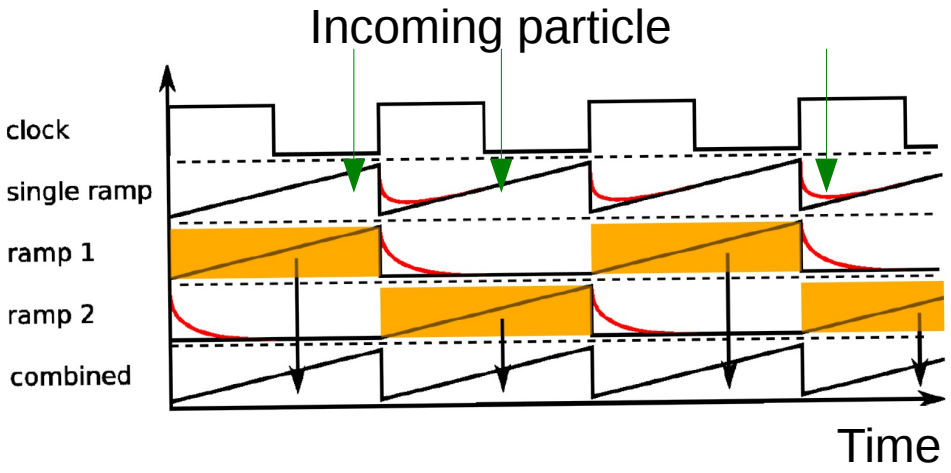
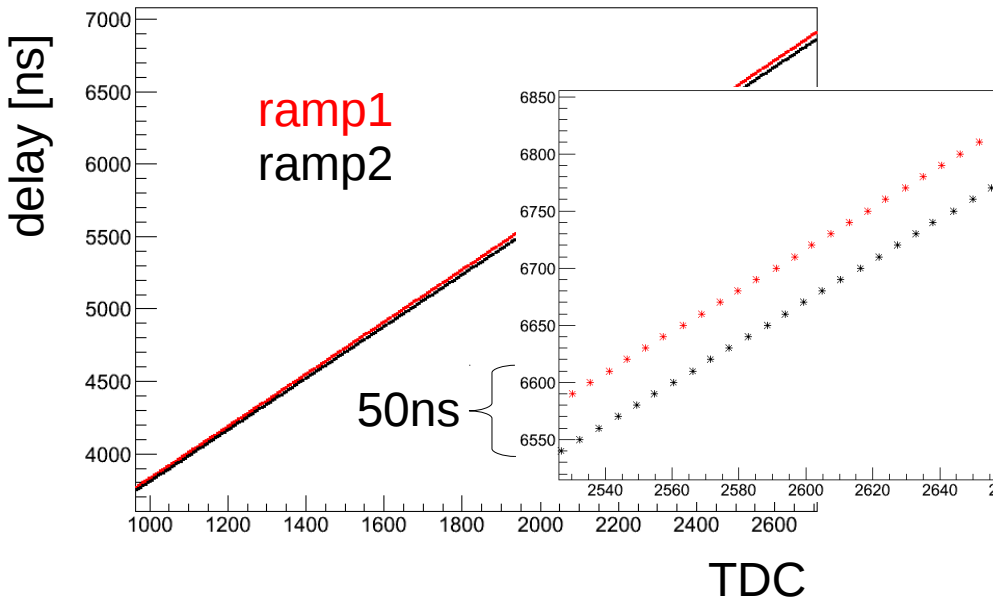
Time measurement:
- Analogue ADC samples two voltage ramps
  → needs calibration of analogue components

The Spoiroc2b:

- 16 analogue memory cells per channel
- Designed to run in sync with accelerator (ILC)
- 4 µs ramp with 4096 TDC bins
  → ~ 1.6 ns bin





TDC schematics

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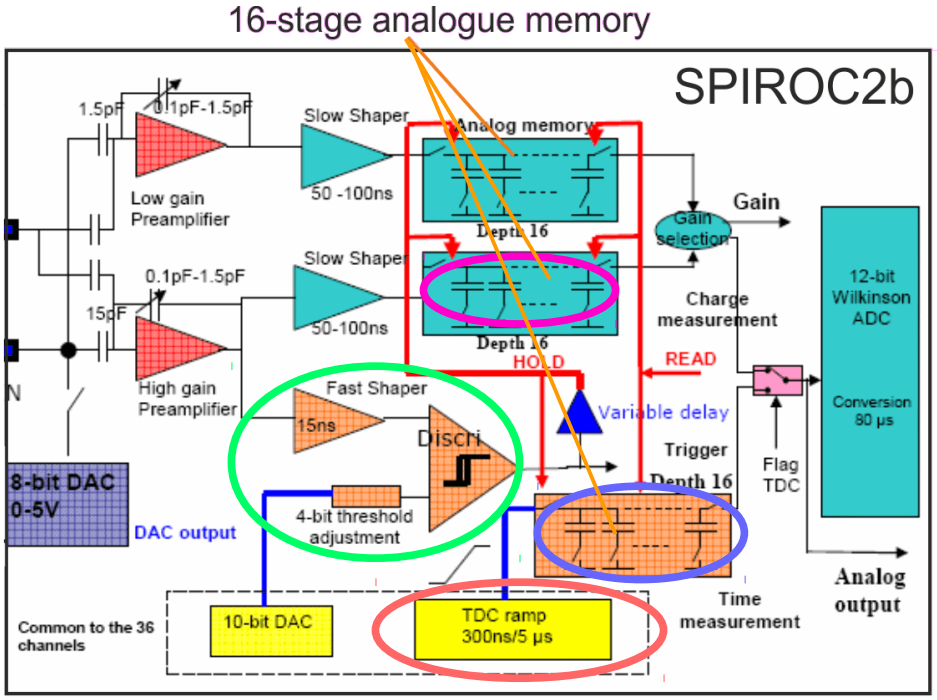
Self triggered r/o chip:

- Signal from fast shaper over threshold
- ADC values from slow shaper stored

  → analogue memory: 16 different pedestals

- TDC ramps is sampled and stored

  → analogue memory: 16 different pedestals



$$t[ns] = f_{ramp}(A^{TDC}) + K_{mem} + Ts(A^{ADC} - P^{ADC})$$

A^{TDC} = TDC signal amplitude
A^{ADC} = ADC signal amplitude
f_{ramp} = Ramp function$_{(Chip,Cycle)}$: 32
K_{mem} = Memory cell offset$_{(Chip,Channel,Cell)}$: 9216
Ts = Time slew correction : 1
P^{ADC} = ADC pedestal$_{(Chip,Channel,Cell)}$: 9216

TDC calibration

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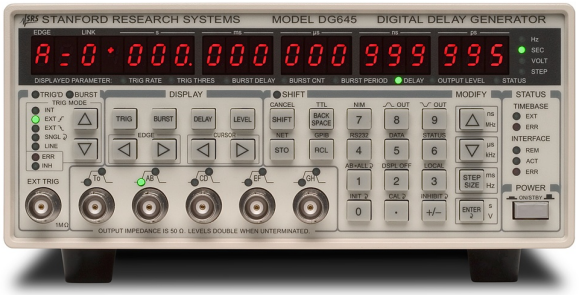
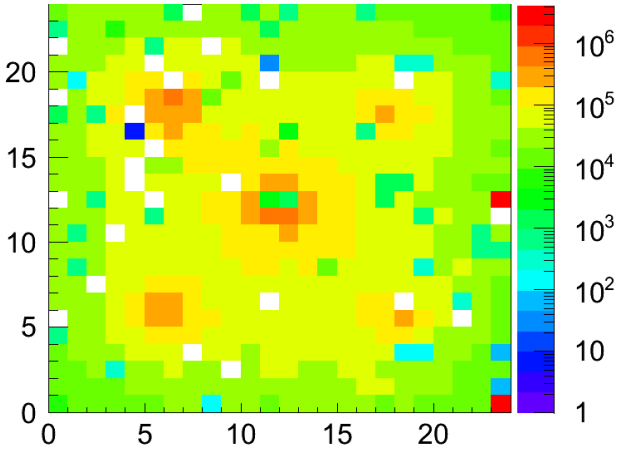
Charge injection **in the lab** with pulse generator (16 chips, 1 channel each)



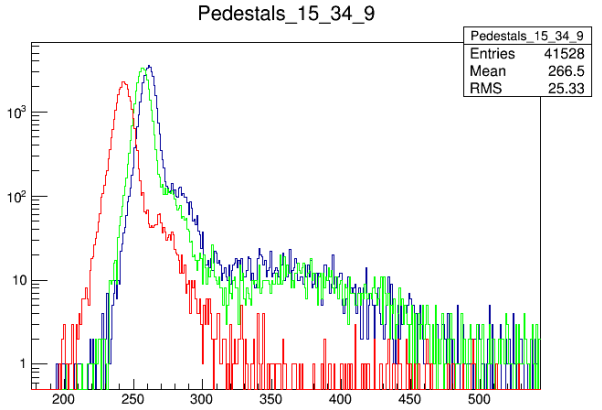
1

DESY II electron test beam:
Al absorber 33cm distance
→ prompt EM showers



2

SPS + DESY II test beam:
Time slew
pedestals
(HitBit=0 in run data)



3

$$t\,[ns] = f_{ramp}\left(A^{TDC}\right) + K_{mem} + Ts\left(A^{ADC} - P^{ADC}\right)$$

1 Voltage ramp calibration

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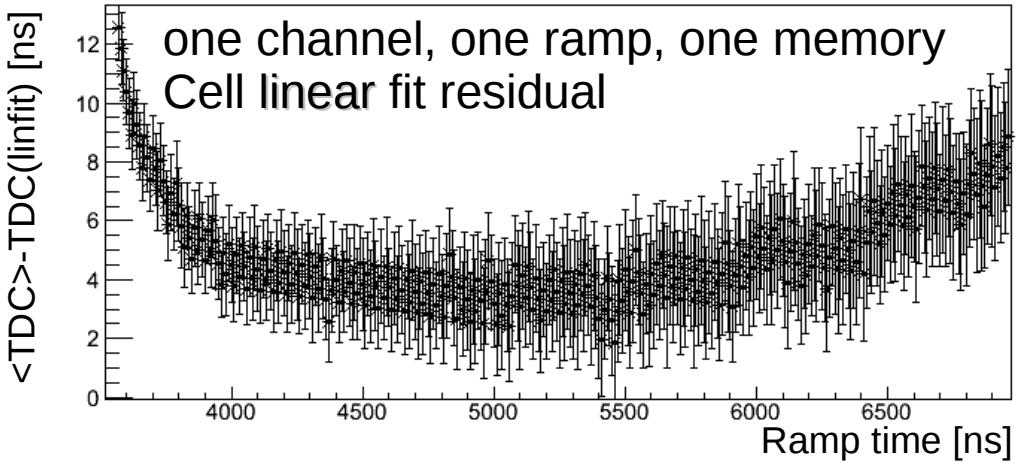
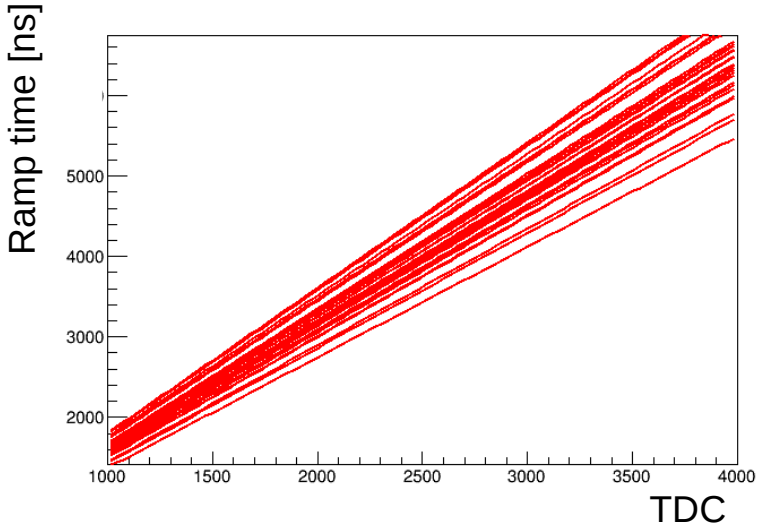
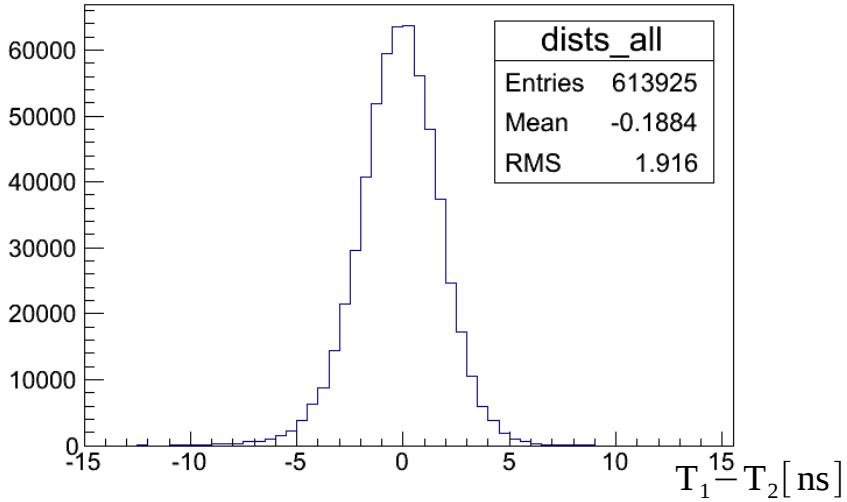
Charge injection **in the lab**
Two ramps per chip:

- Ramps are not linear
  → must be defined for every chip (look up table)







Difference between two triggered channels

→ 2ns : best achievable RMS with electronics only!

3 Time slew

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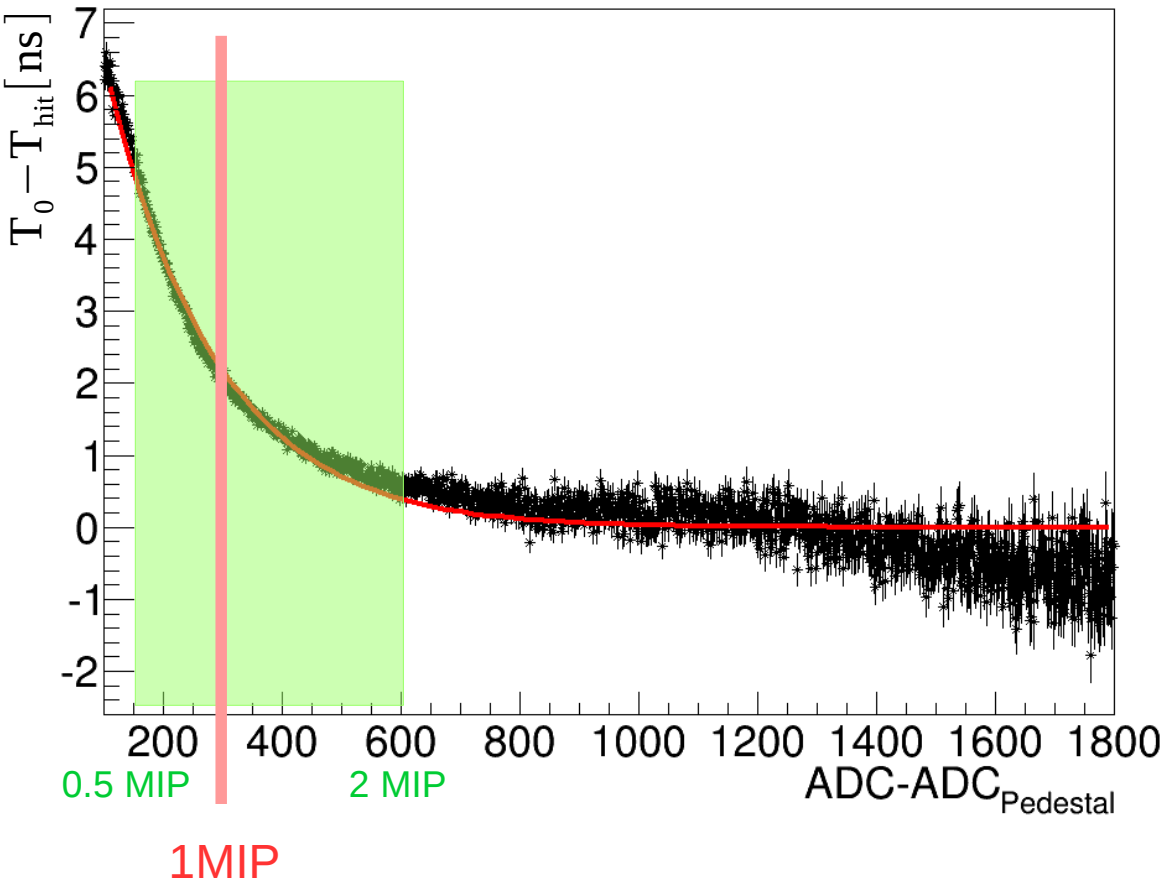
- **Test beam** inter run ADC pedestals P^{ADC}
- Fitted with simple exp function
- Assumed to be identical for all channels and memory cells



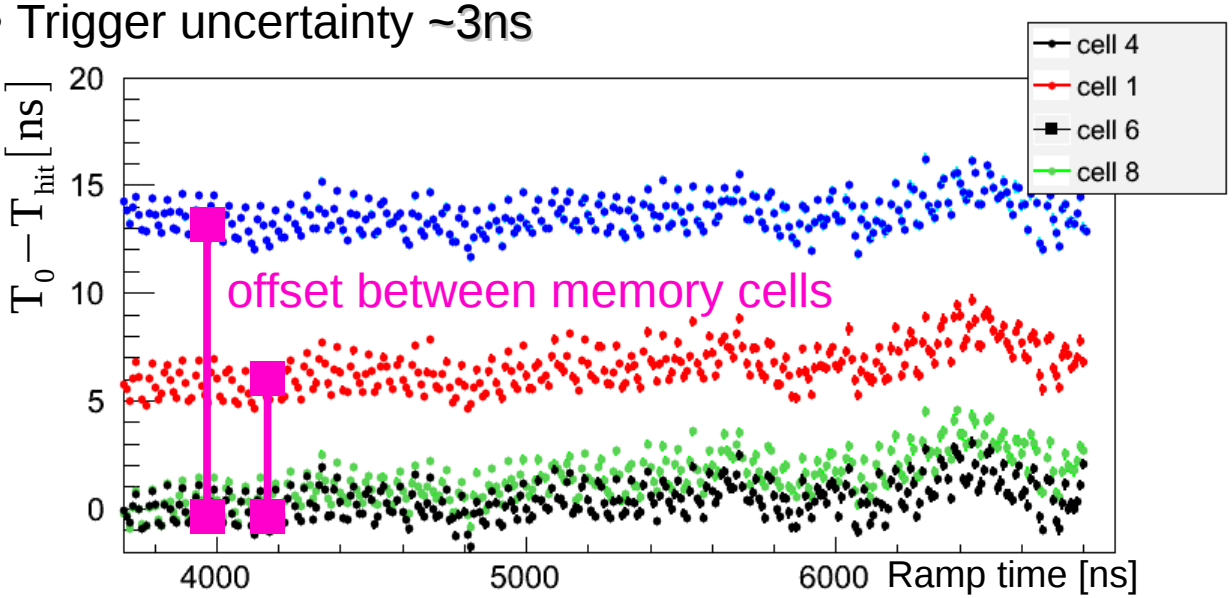
- Up to 5 ns correction for signals < 2 MIP
- High ADC signals need further investigation

2 Memory cell offset

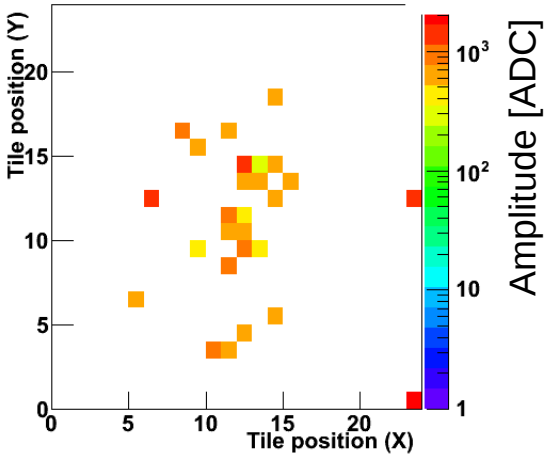
→ Table top measurement (charge injection) not practicable for a big number of channels (576 channels)

Electron test beam @ DESY II:

- High rate (kHz) / millions of events
- Instantaneous EM showers (Al target) with multiple hits
- Different beam positions to cover all chips
- Trigger uncertainty ~3ns



EM shower event:



Data driven digitization

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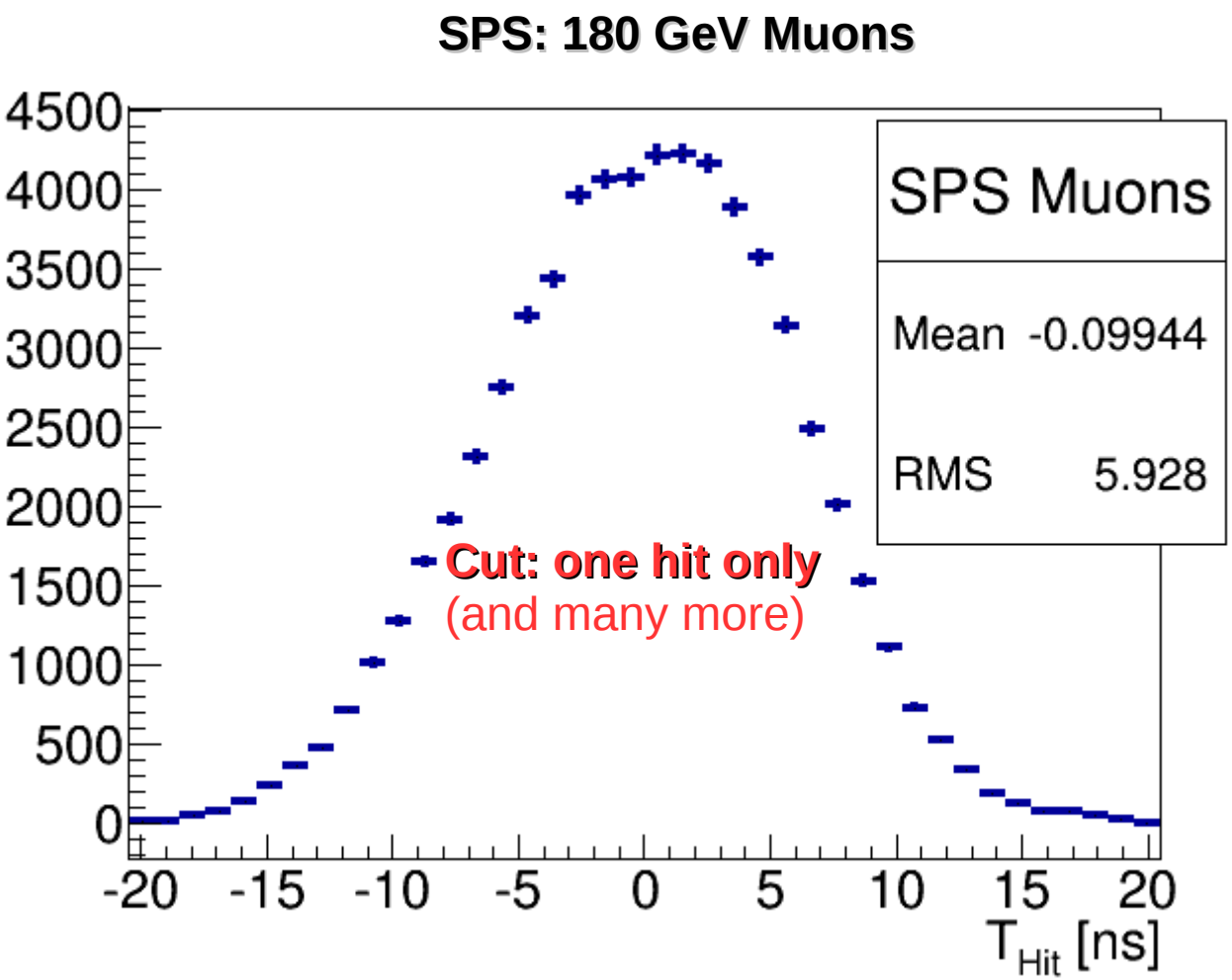
Implement digitization in MC
G4 QGSP BERT HP

- ADC calibration
  → rough chip-wise
- Correct error estimation for trigger thresholds
  → smear 0.5 MIP cut in simulation
- Time resolution
  → smear simulation by 6 ns
- Noise description
  → 1 µs tail in data (SiPM noise)



→ **6 ns RMS** with DESY TDC calibration

MIP calibration

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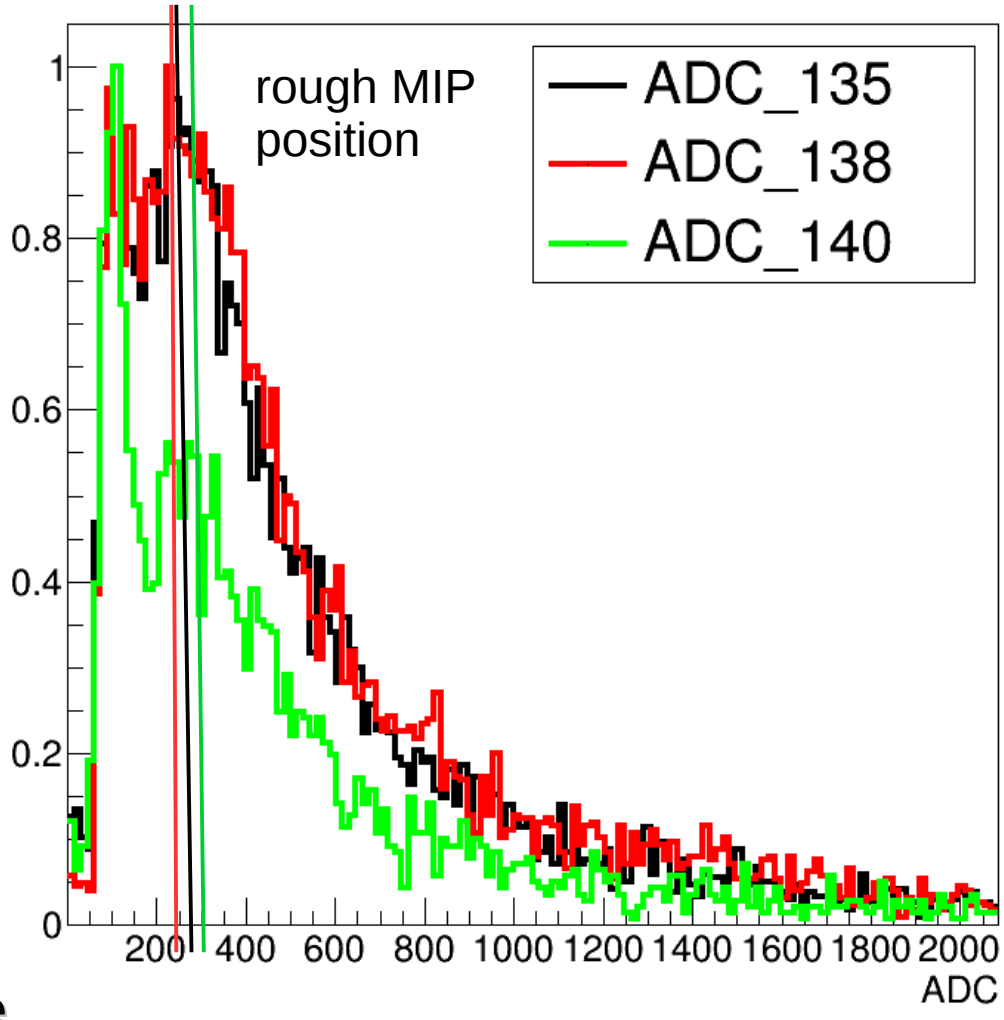
Energy scale is equalized for ITEP tiles :

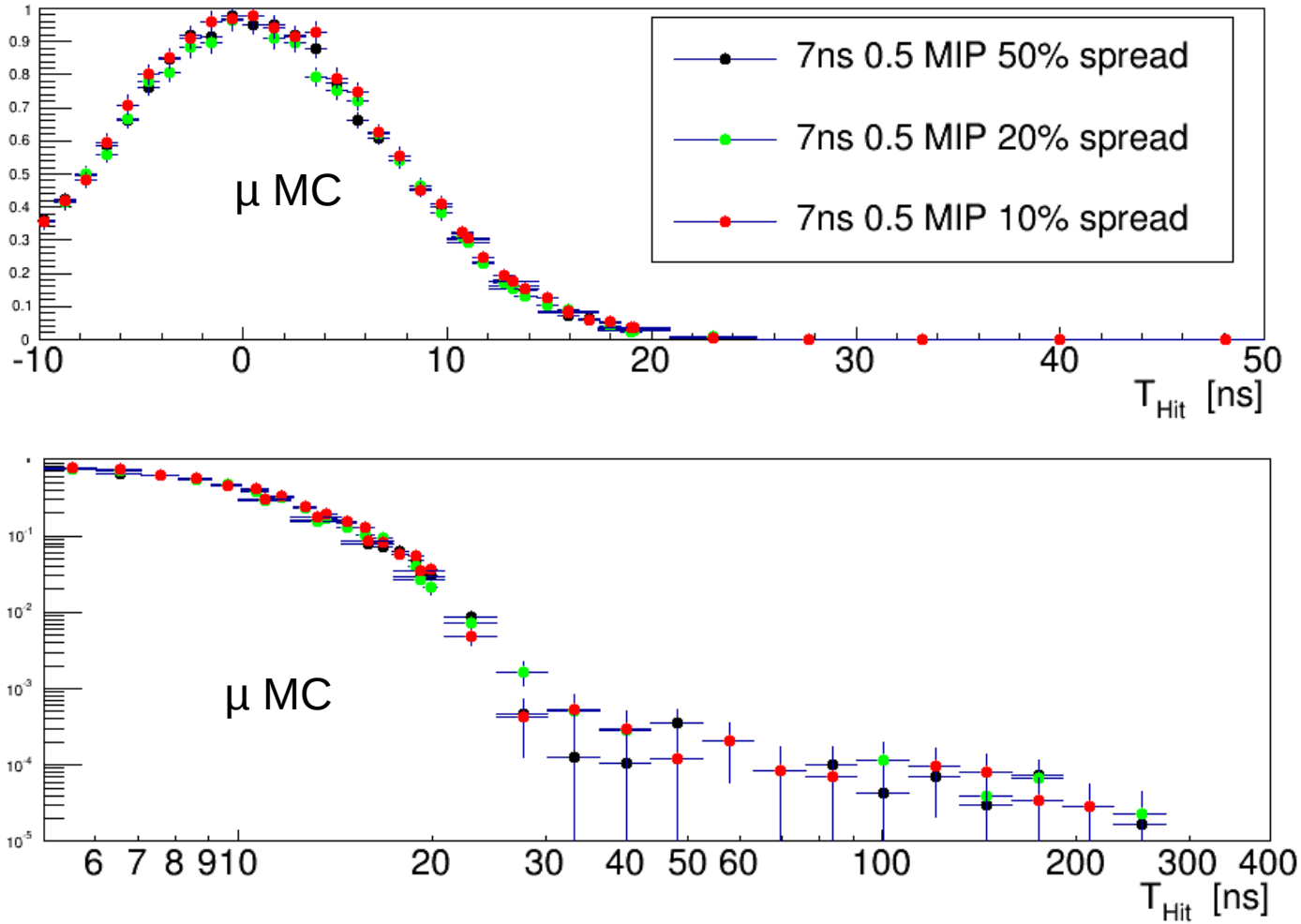
- Response equalized via bias voltage
- ADC scale equalized via pre amplifiers



→ **Chip wise calibration feasible**

Impact of rough MIP calibration

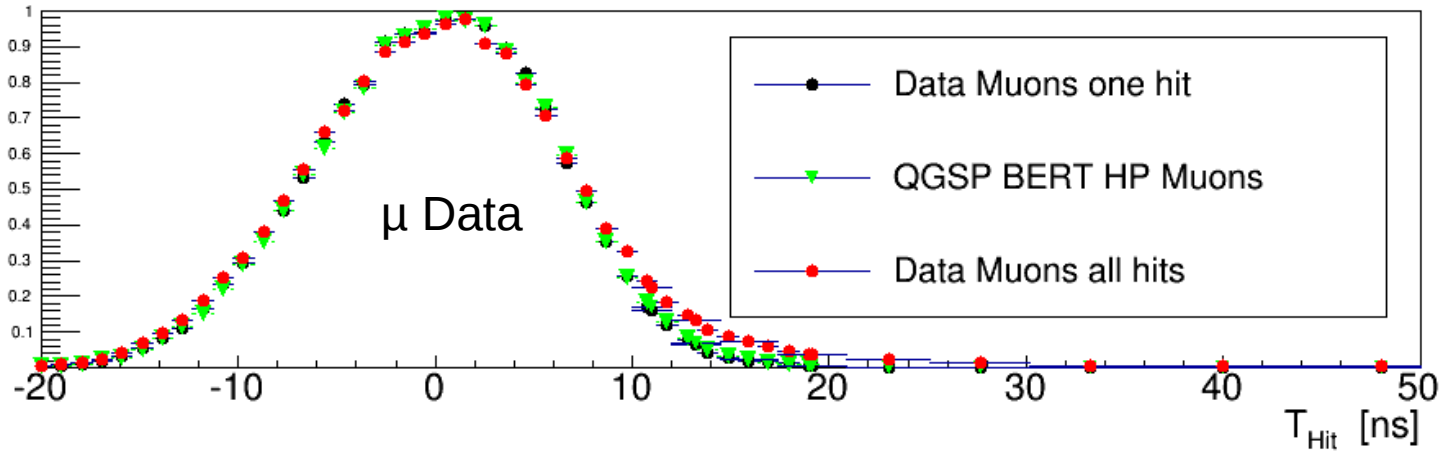
- MIP threshold in MC is varied by 10 - 50 % of 0.5 MIP



→ **Mean calibration and rough 0.5 MIP threshold is sufficient**

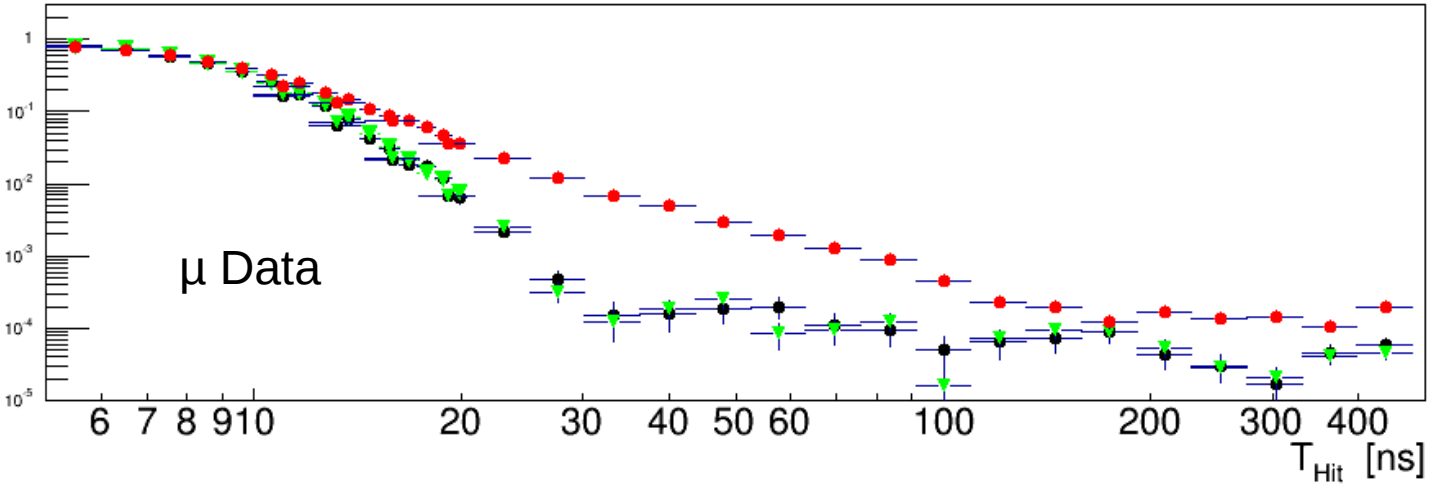
Muons: Data / MC Comparison

- Proper understanding of Muon data necessary



- For one hit only comparison looks good

- More than one hit: excess of late events (20 – 100 ns)
  → Not noise (correlated)
  → Not physics



→ **detector effect, needs to be properly understood**

TDC pedestal shift

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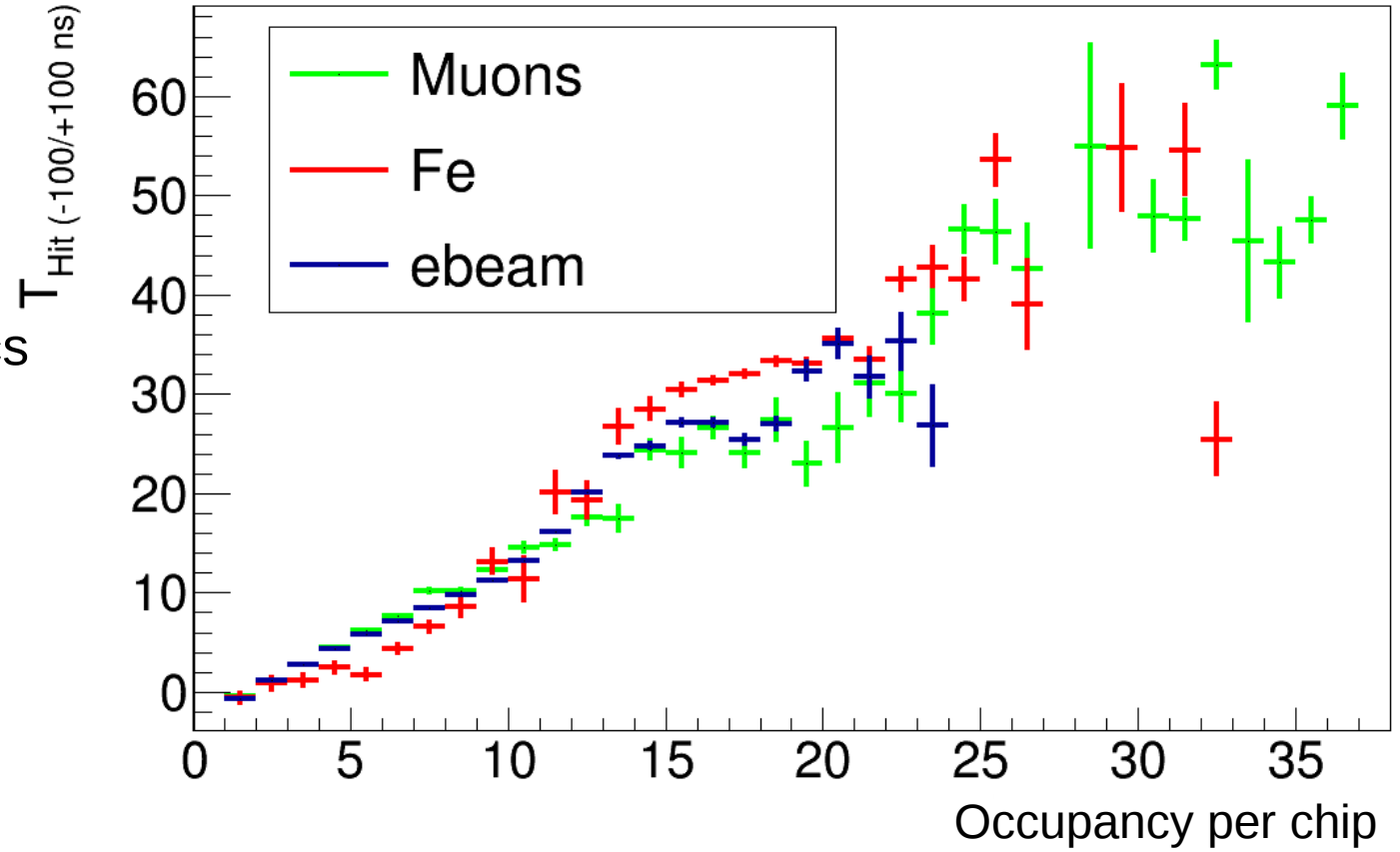
New correction step required

- Clearly electronics effect
- Common for all runs with instantaneous physics

Fe: DESY II, 2 X_0 iron

ebeam: DESY II, 7 X_0 Al

Muons: 180 GeV SPS



MC: not more than 10 hits with physics

TDC pedestal shift correction

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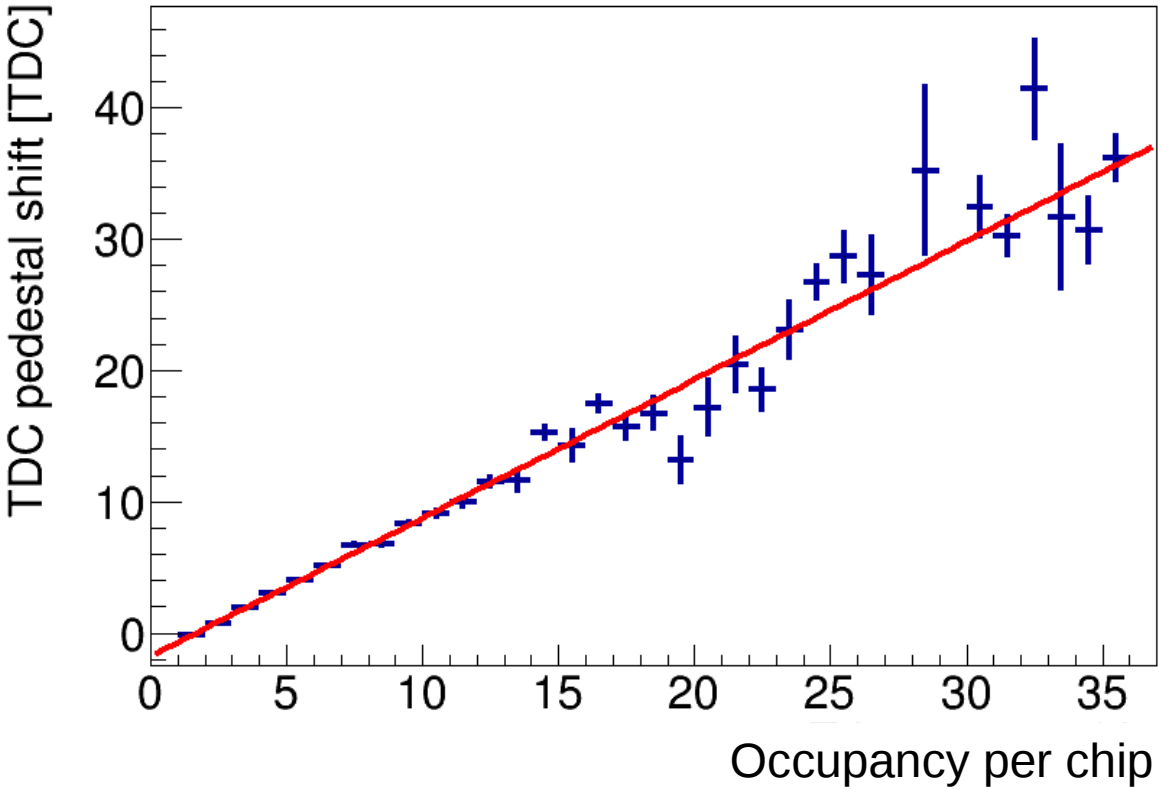
Method for correction:
For every hits extract A^{TDC}_{ped} for $T_{Hit}=0$
versus **HitBits per chip**
Linear fit used for correction

$A^{TDC}=\text{TDC signal amplitude}$
$A^{ADC}=\text{ADC signal amplitude}$
$f_{ramp}=\text{Ramp function}_{(\text{Chip},\text{Cycle})}:32$
$K_{mem}=\text{Memory cell offset}_{(\text{Chip},\text{Channel},\text{Cell})}:9216$
$Ts=\text{Time slew correction}:1$
$P^{ADC}=\text{ADC pedestal}_{(\text{Chip},\text{Channel},\text{Cell})}:9216$
$n=\text{triggers per chip}$
$A^{TDC}_{Pedestal}=\text{TDC pedestal correction}$



$$t[ns]=f_{ramp}\left(A^{TDC}-A^{TDC}_{Pedestal}(n)\right)+K_{mem}+Ts\left(A^{ADC}-P^{ADC}\right)$$

TDC pedestal shift correction

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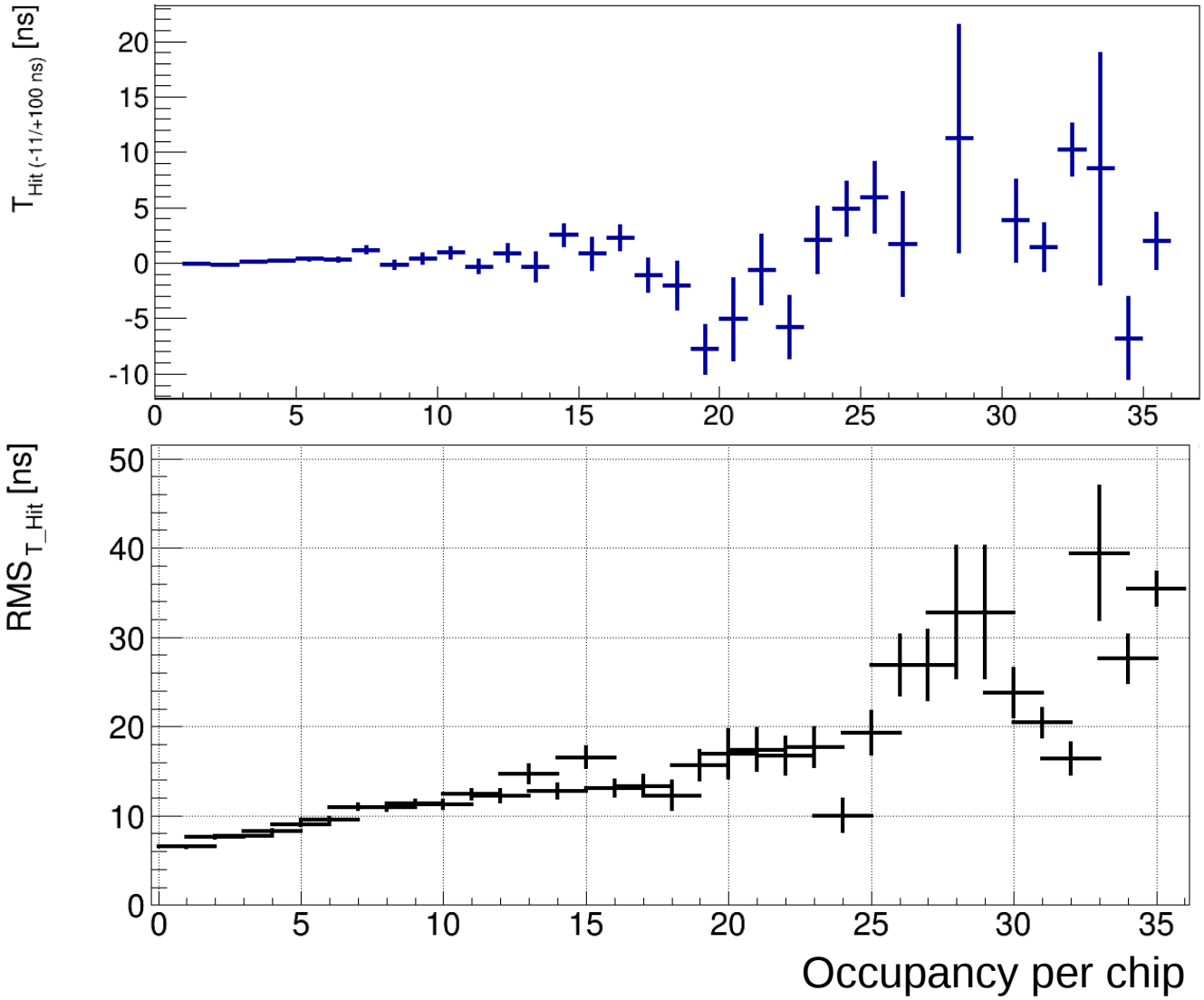
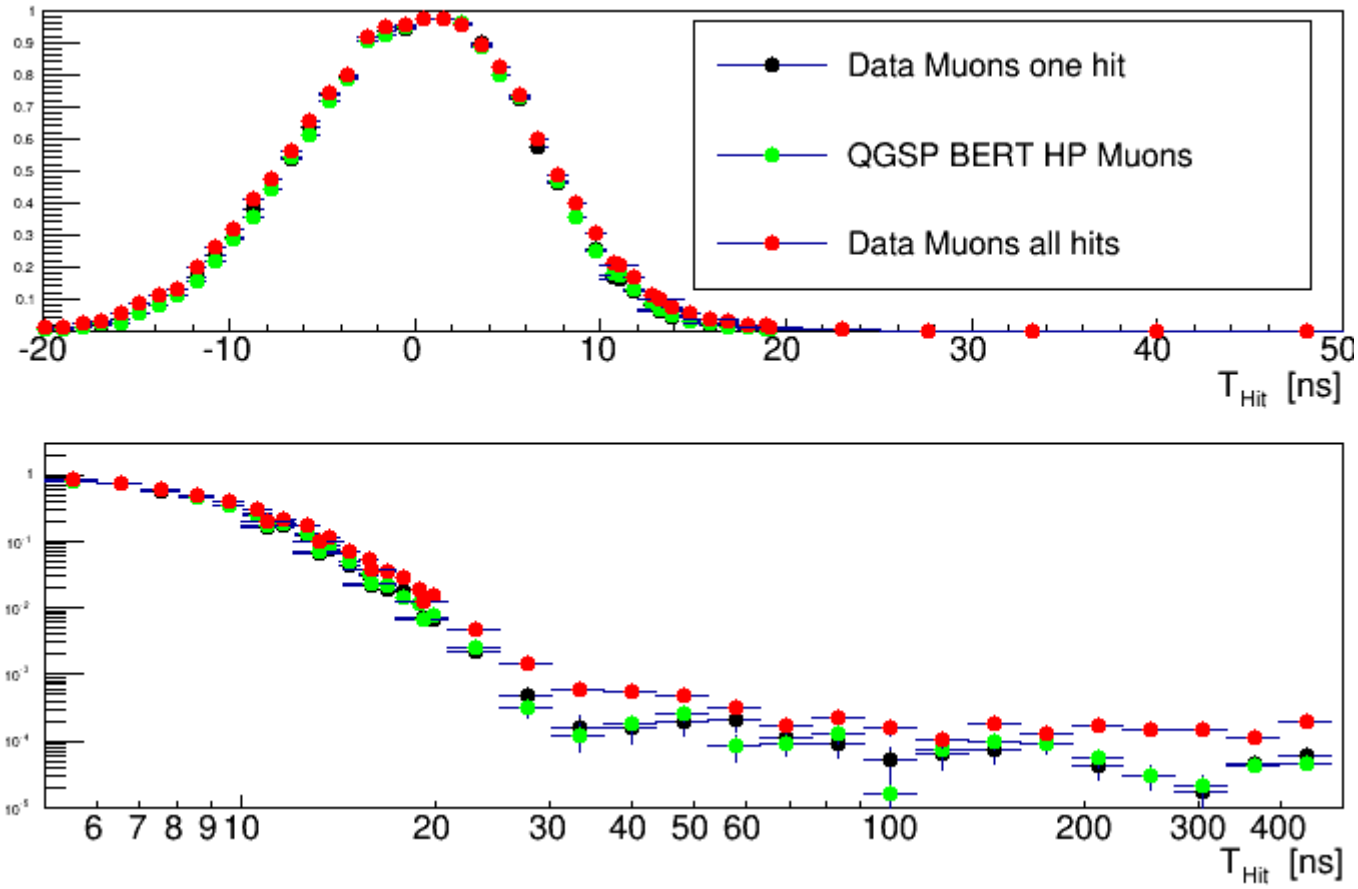
After correction

- Pedestal shift corrected

- Time resolution (RMS)
- worsens with occupancy



SPS Muons



→ **TDC pedestal shift correction improves data/ MC comparison**

Summary

- Successful data taking in 2012 with one layer prototype

TDC calibration
- Promising results from first layer
  - → Electronics resolution ~2ns
  - → Time resolution on physics ~7ns

Data / MC comparison
- Proper understanding of Muon data necessary
- New feature: TDC shift depending on chip occupancy
- Time resolution increases from 6 ns to 40 ns depending on chip occupancy