

PROJECT 01

ECE 317

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1 Overview

The purpose of this lab is to understand the fundamental usage of PECS and determine how variations in switching frequency, clocks, and pulse width modulator affect various parts of electric circuits.

2 Circuit 1

2.1 Circuit Diagram

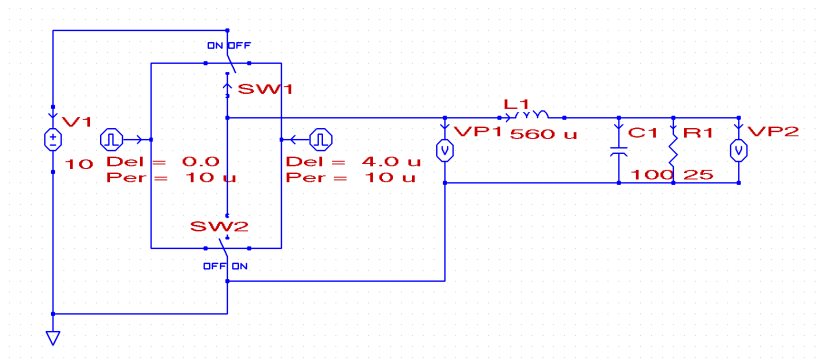


Figure 1: Circuit

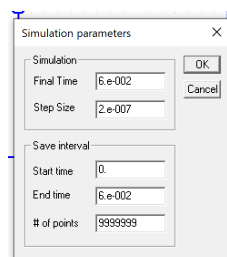


Figure 2: Simulation Parameters

2.2 Output

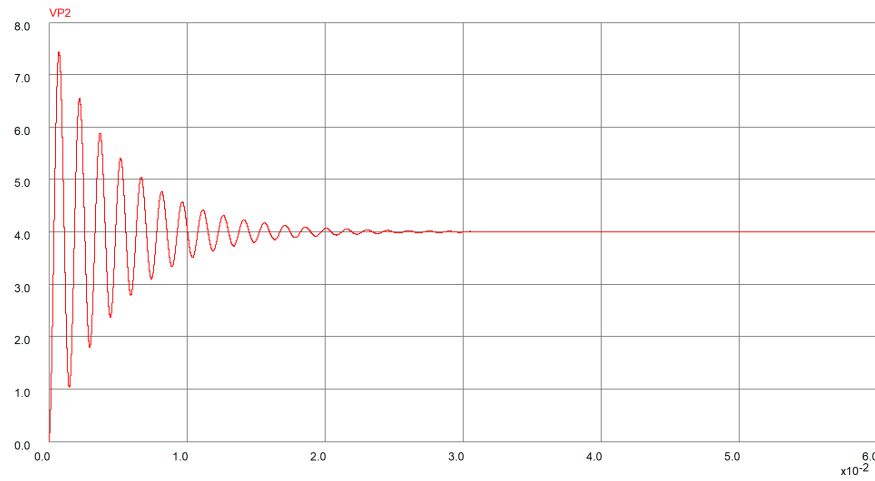


Figure 3: Full waveform

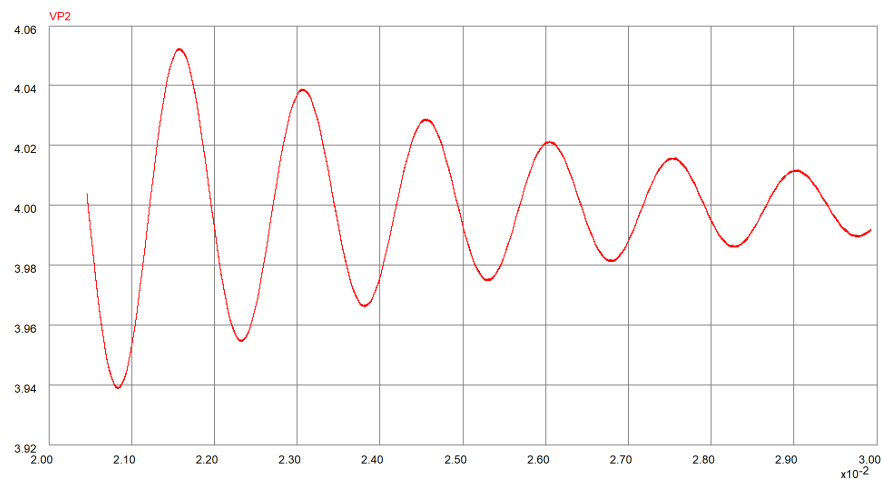


Figure 4: Zoomed waveform

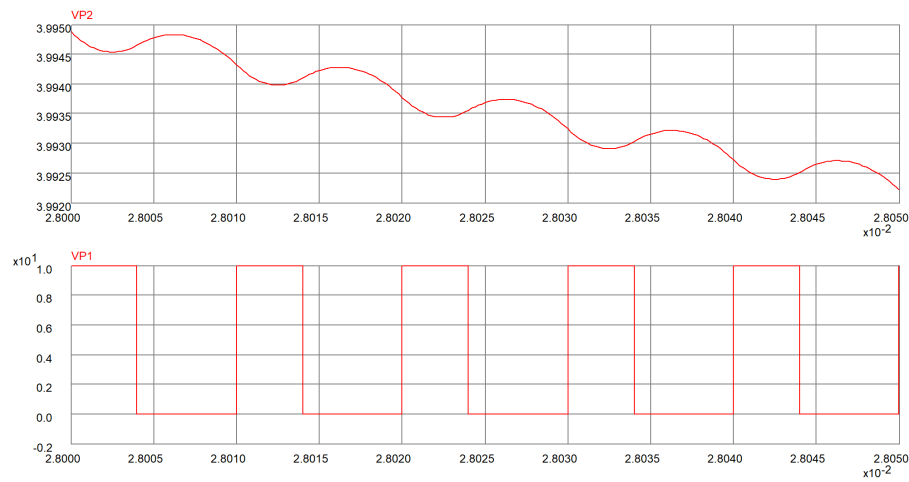


Figure 5: Comparative waveform

2.3 Analysis

Peak Amplitude	Period	Pulse Width	Duty Ratio
$10v$	$10\mu s$	$4\mu s$	0.4

Table 1: Circuit 1 calculations

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Question

Taking the above plots into consideration, explain why you would expect to get the steady state value you found above?

Answer

$$V_{SS} = V_{peak} \cdot \text{Duty Ratio} \quad (1)$$

It is expected to get the steady state above as the peak voltage is $10v$ and the duty ratio is 0.4.

3 Circuit 2

3.1 Circuit Diagram

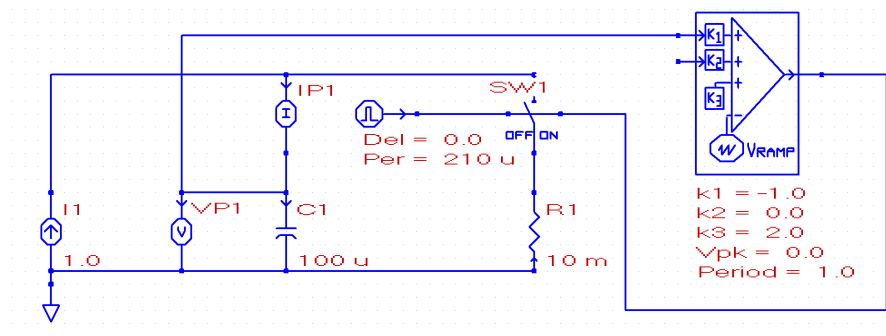


Figure 6: Sawtooth wave circuit

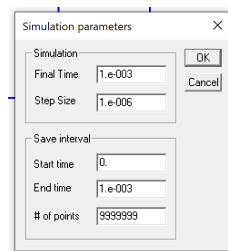


Figure 7: Simulation Parameters

3.2 Output

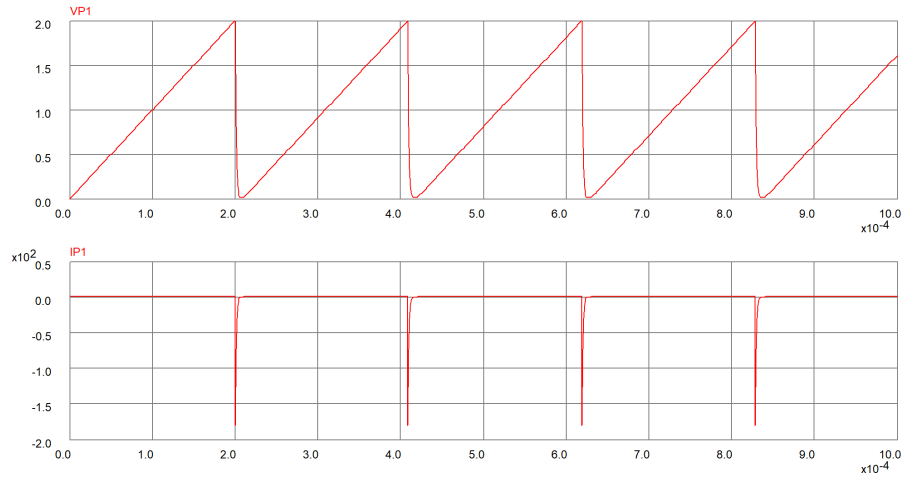


Figure 8: Comparative waveform

3.3 Analysis

Peak Amplitude	Period
$2v$	$200\mu s$

Table 2: Circuit 2 calculations

Question

Given that $K_1 = -1$, what other factors in the circuit determines the peak amplitude and why?

Answer

$$\text{Steady State} = \text{Peak Amplitude} \cdot \text{Duty Ratio} \quad (2)$$

It is expected to get the steady state above as the peak voltage is $10v$ and the duty ratio is 0.4.

4 Circuit 3

4.1 Circuit Diagram

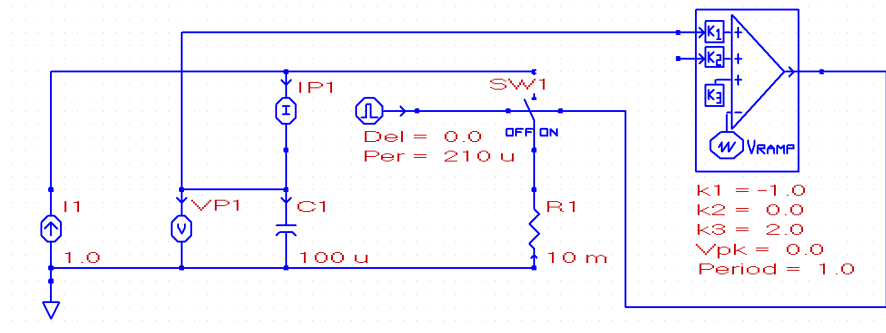


Figure 9: Circuit (adjusted)

4.2 Analysis

	Switching Frequency	Duty Ratio	Peak-to-peak Input Voltage to Filter	Steady State Average Output Voltage	Peak-to-peak Output Voltage Ripple
Circuit 1	100kHz	0.4	10v	4v	5.4mV
Circuit 3	40kHz	0.5	10v	5v	3.5mV

Table 3: Comparative omnibus

Question

Explain the differences seen in the peak-to-peak ripple voltage values between Circuit 3 and Circuit 1. Are they in line with your expectations? Why?

Answer

$$K_1(V_{P1}) + K_3 < 0 \quad (3)$$

The ripple is smaller in circuit 3 because the capacitor is being charged and discharged more frequently. This results in a smaller ripple voltage as seen in the above plots.