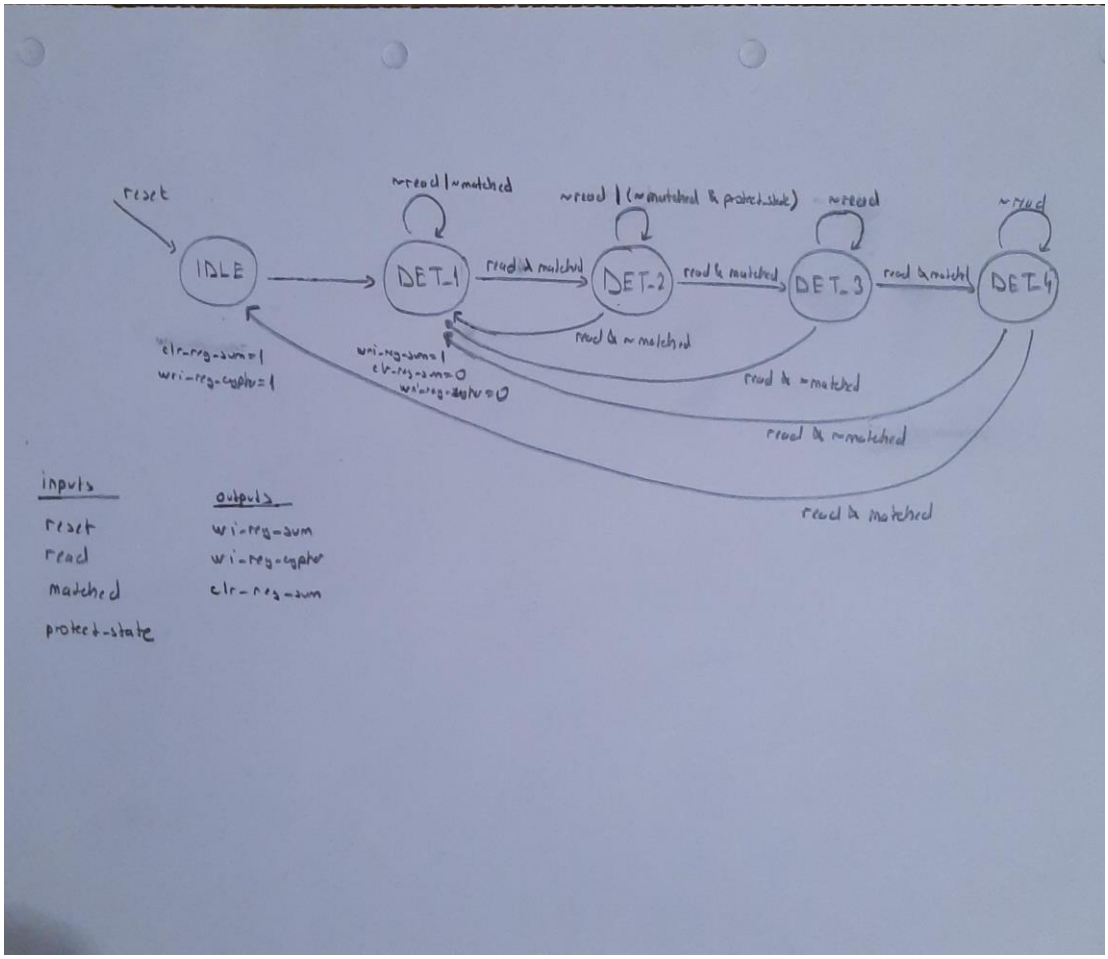
GTU Department of Computer Engineering
CSE 331/503 - Fall 2022
Bonus Assignment Report

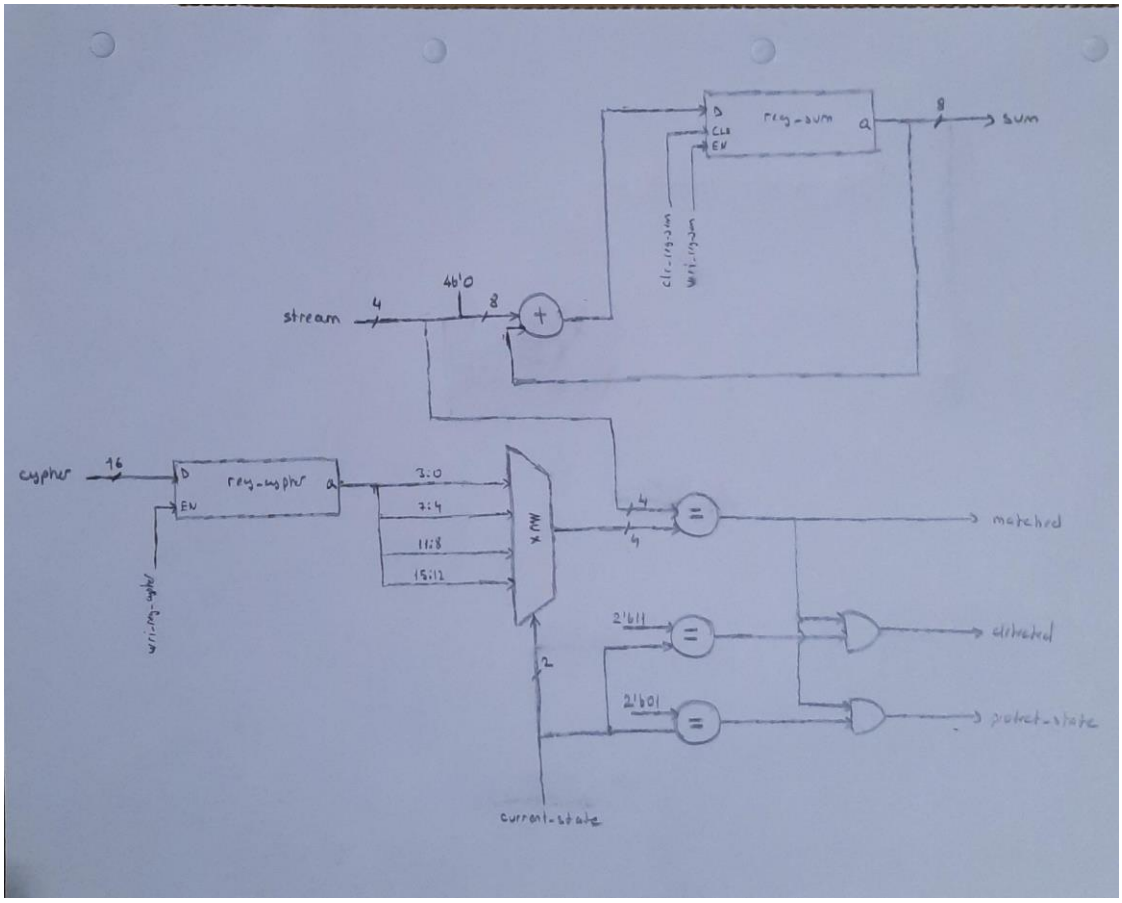
Emirkan Burak Yılmaz
1901042659

1. FSM



- There are 5 stages. First state, IDLE is the reset state that the reg_cypher takes the value of 16-bit cypher and reg_sum initialized with 0. After the reset state, the following states start with DET are for the detecting the cypher. If the read signal is low than the current state is protected, if it's high then there are two cases. First case, input stream and the related part of cypher are same (indicated with input signal matched) then continue with the next state. Second case, they are different. For that reason, turn back to DET_1 and start at the beginning of the cypher.
- For state DET_2, the input signal protect_state is becomes high when the state is DET_2 and the current input is same as the first part of the cypher. If protect_state is high and matched is low, then stay in the current state. With this way the detector can continue with state DET_2 since the coming input matched with the DET_1 state. If this does not add, then the detector cannot detect first input hazard and lose one state.
- For state DET_4, if the input stream is matched on read, then return the state IDLE for the reset. If it is not matched, then turn back the state DET_1.

2. Datapath Design



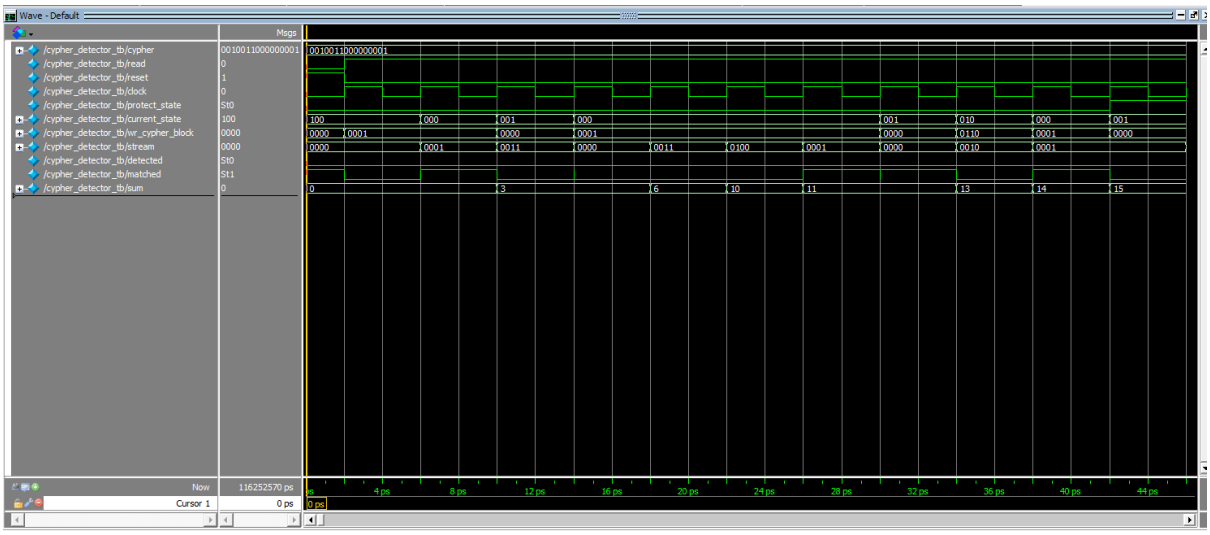
- The datapath controlled with the input signals generated by control unit which are wri_reg_cypher, wri_reg_sum, clr_reg_sum and the current_state. They are basically write and clear signals for the registers reg_sum and reg_cypher.
- The part of 16bit cypher is selected according to the input signal current_state by the multiplexer, and it's compared with the input stream. If they are same than the output signal matched becomes high.
- For detecting the cypher, if the current_state is DET_4 (2'b11) and stream is matched, then the output detected becomes high.
- The given input stream is summed and written to reg_sum if the input signal wri_reg_sum is high.
- For detecting first input hazard the output signal protect_state becomes high when the current_state is DET_2 (2'b01) and input stream matched with the part of the cypher.

3. Simulation and Tests

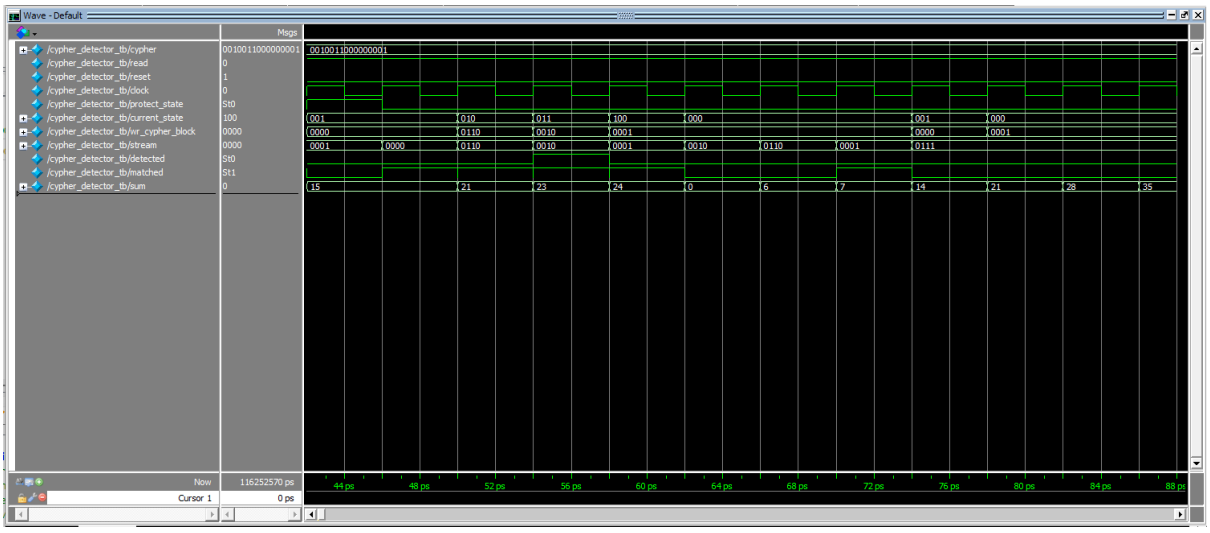
TEST CASE (Given in the PDF)
Cypher: 0010 0110 0000 0001 (Cypher is 2-6-0-1)
4-bit inputs: 0000-0001-0011-0000-0011-0100-0001-0000-0010-0001-0001-0000-0110-0010

The first output detected will become 1 after the last four numbers are observed.
The second output sum will be 24, i.e. 0001 1000.

(I also add additional output signals to better visualize and prove my solution)



- wr_cypher_block and stream are compared and if they are same, matched becomes high. And for the matching cases the current_state changes to next state. (3'b000 is DET_1 and 3'b011 is DET_4).
- As an example matching and change of states can be seen between 26ps and 34ps.



- The cypher is detected at 54ps and then sum becomes 24. After detection, current_state becomes IDLE (3'b100) for reset state. Sum initialized with 0 and and then same detection process started at the beginning at state DET_1 (3'b000).