CSE 331/503

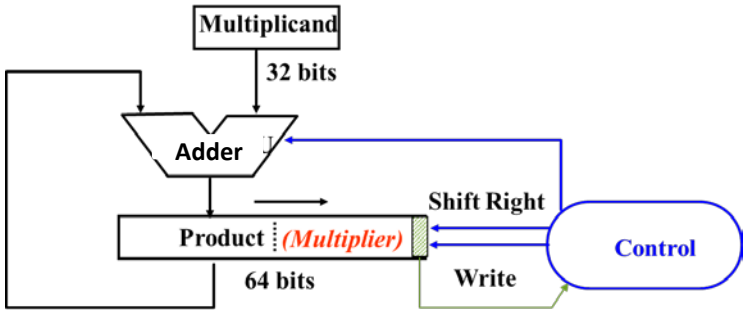
Computer Organization

Homework 2 – ALU with Multiplication Design

Due Date 08/12/2022 Thursday 23:59

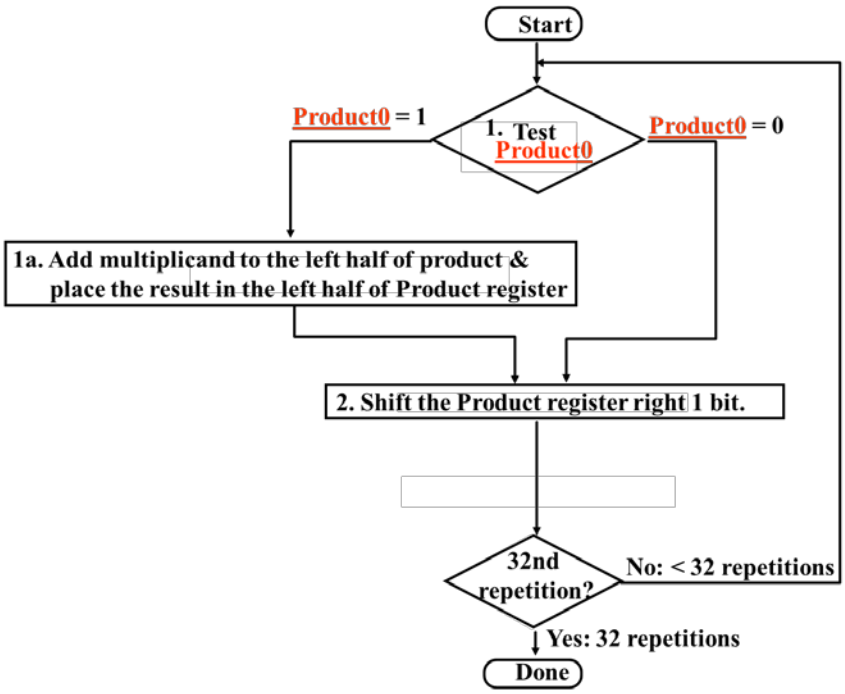
In this assignment you will design an ALU that is capable of unsigned multiplication using Quartus and Verilog HDL.

1. mult32.v Module (70pts)



Your design will have three modules: adder.v, control.v and datapath.v. You will combine them in a mult32.v file to have the 32 bit multiplier.

Your Control Unit (control.v) will implement the below ASM. Design that using Behavioral Verilog. Structural Verilog is not permitted:

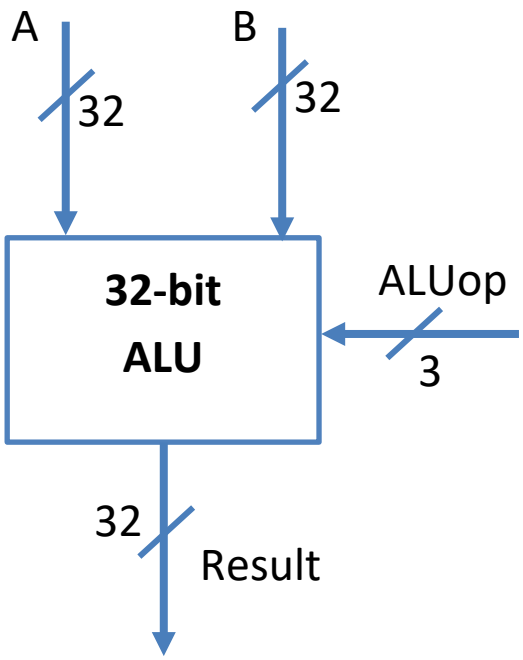


2. alu32.v Module (50pts)

Your ALU will be able to perform addition, subtraction, multiplication, AND, OR, XOR, NOR and Set Less Than operations.

Therefore the alu32.v will use mult32.v module inside.

ALUop	Operation
000	ADD
001	SUB
010	MULT
011	XOR
100	AND
101	OR
110	SLT
111	NOR



- Write a report showing and explaining all Verilog files, including your schematics.
- You can only use structural Verilog. Behavioral Verilog is not permitted other than Multiplier.
- No other operations are permitted. And you cannot change ALUop decisions.
- Perform simulations and check for accuracy. Not working designs will not get above 30pts. If the mistake is small it is your responsibility to find and correct it.
- Cheating results in -100 even from outer resources if not mentioned in the report.
- Use only one adder in your design used by multiplier and adder and subtractor.
- Attend the PS explaining the homework and further constraints will be explained there. So PS attendance is a MUST.

"The punishment of desire is the agony of unfulfillment"