MIPS32

32-bit Single Cycle MIPS Processor

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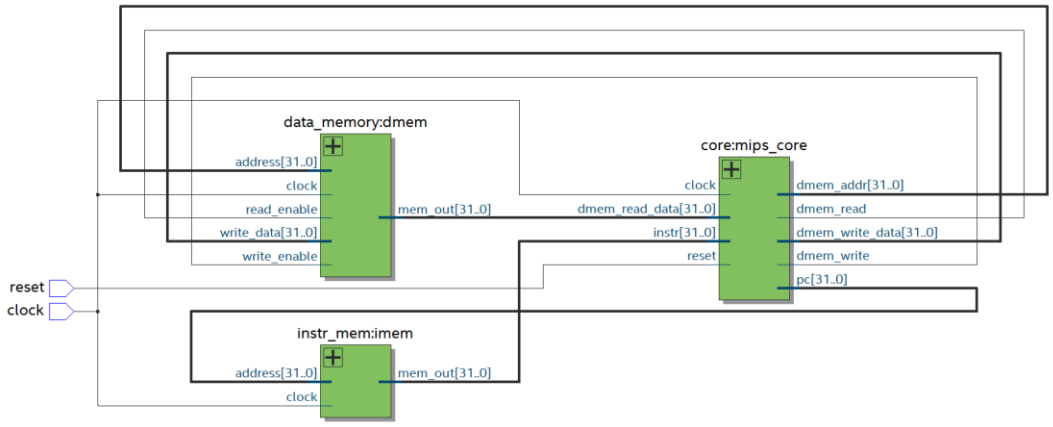
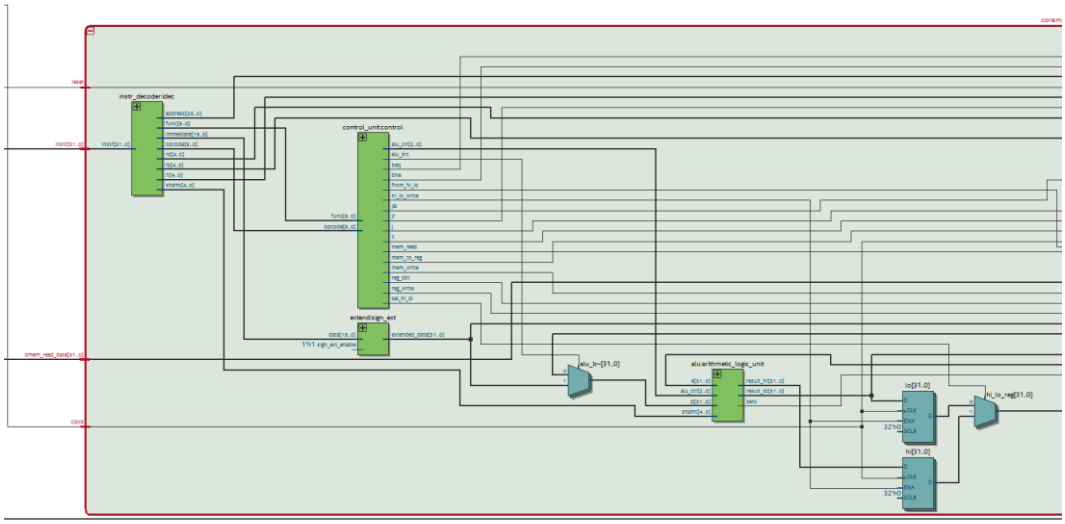
1. **mips32:** Consist of instruction memory, data memory and core.

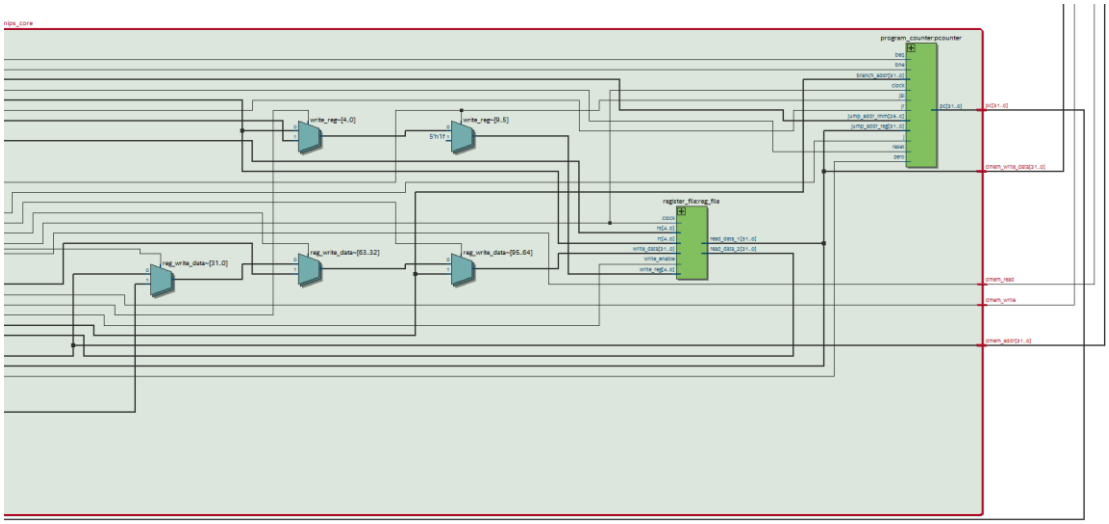


Supported instructions are given below.

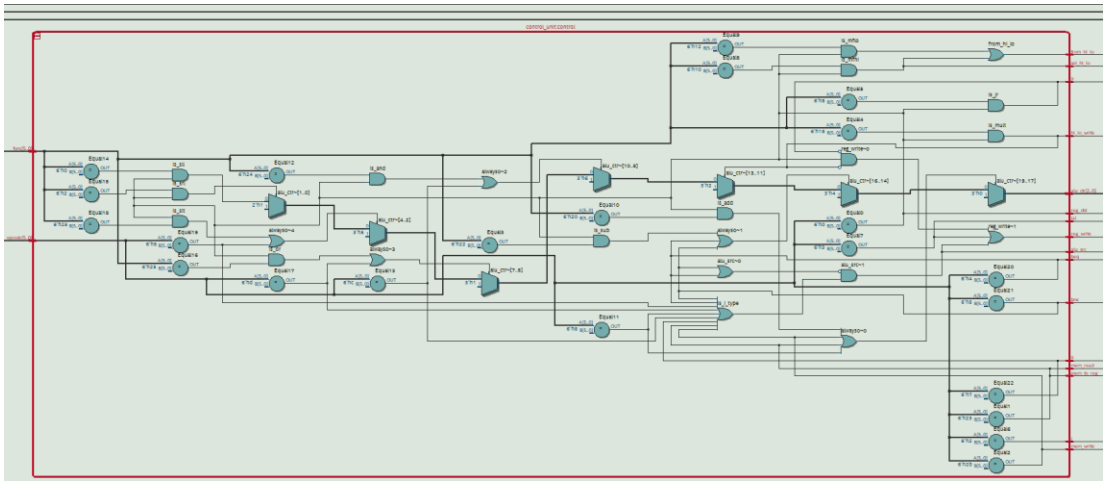
Instruction	Instruction Type
add	R
sub	R
mult	R
or	R
and	R
slt	R
jr	R
mfhi	R
mflo	R
addi	I
ori	I
andi	I
slti	I
lw	I
li	I
sw	I
beq	I
bne	I
j	J
jal	J

2. **core:** Contains register file, ALU and multiplexers for control signals.





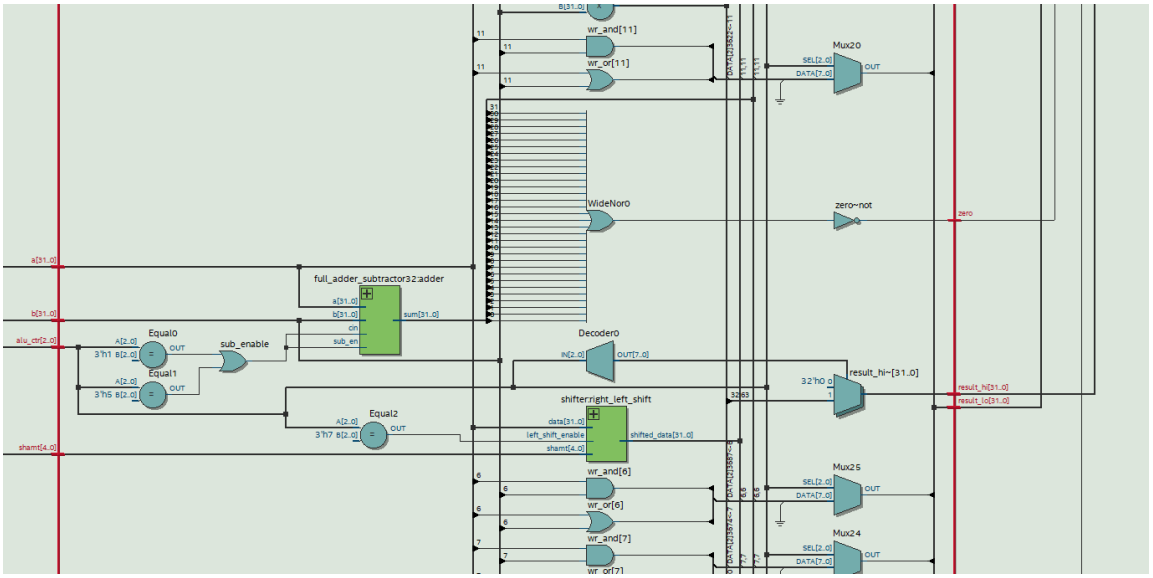
3. **control_unit:** Produces control signals according to opcode and function field of the instruction.



The following table explains the control signals with their meaning.

Signal	Meaning
reg_dst	Selects rt (0) or rd (1) register for write register address
beq	beq instruction
bne	bne instruction
j	j instruction
jr	jr instruction
jal	Selects $ra for destination register
li	Selects extended immediate value for destination register
hi_lo_write	Write the multiplication result into hi and lo registers
from_hi_lo	Selects the hi or lo register content for destination register
sel_hi_lo	Selects register hi (1) or lo (0) content for destination register
reg_write	Enables write for register file
alu_ctr	Selects ALU operation
alu_src	Select extended immediate value (1) or rt register content (0)
mem_read	Enables read for data memory
mem_write	Enables write for data memory
mem_to_reg	Select the data comes from memory for destination register

4. **alu:** Provides arithmetic and logical operations and desired operation is selected by the control signal alu_ctr.



alu_ctr	Operation
000	ADD
001	SUB
010	MULT
011	AND
100	OR
101	SLT
110	SRL
111	SLL

instruction	ALU Operation
add, addi	ADD
sub	SUB
mult	MULT
and	AND
or	OR
sll	SLL
srl	SRL
mflo	X
mfhi	X
li	X
lw	ADD
sw	ADD
beq, bne	SUB
slt, slti	SUB
j, jr, jal	X