28.14 Timer Output Module (TOM)

28.14.1 Overview

The Timer Output Module (TOM) offers up to 16 independent channels (index x) to generate simple PWM signals at each output pin *TOM[i]_CH[x]_OUT*.

Additionally, at TOM output *TOM[i]_CH15_OUT* a pulse count modulated signal can be generated.

The architecture of the TOM sub-module is depicted in **Figure 47**.

Indices and their range as used inside this chapter are:

y=0,1

z=0…7

The following design variables are used inside this chapter. Please refer to AURIX device specific appendix for correct value.

cCTO: TOM channel count; number of channels per instance - 1.

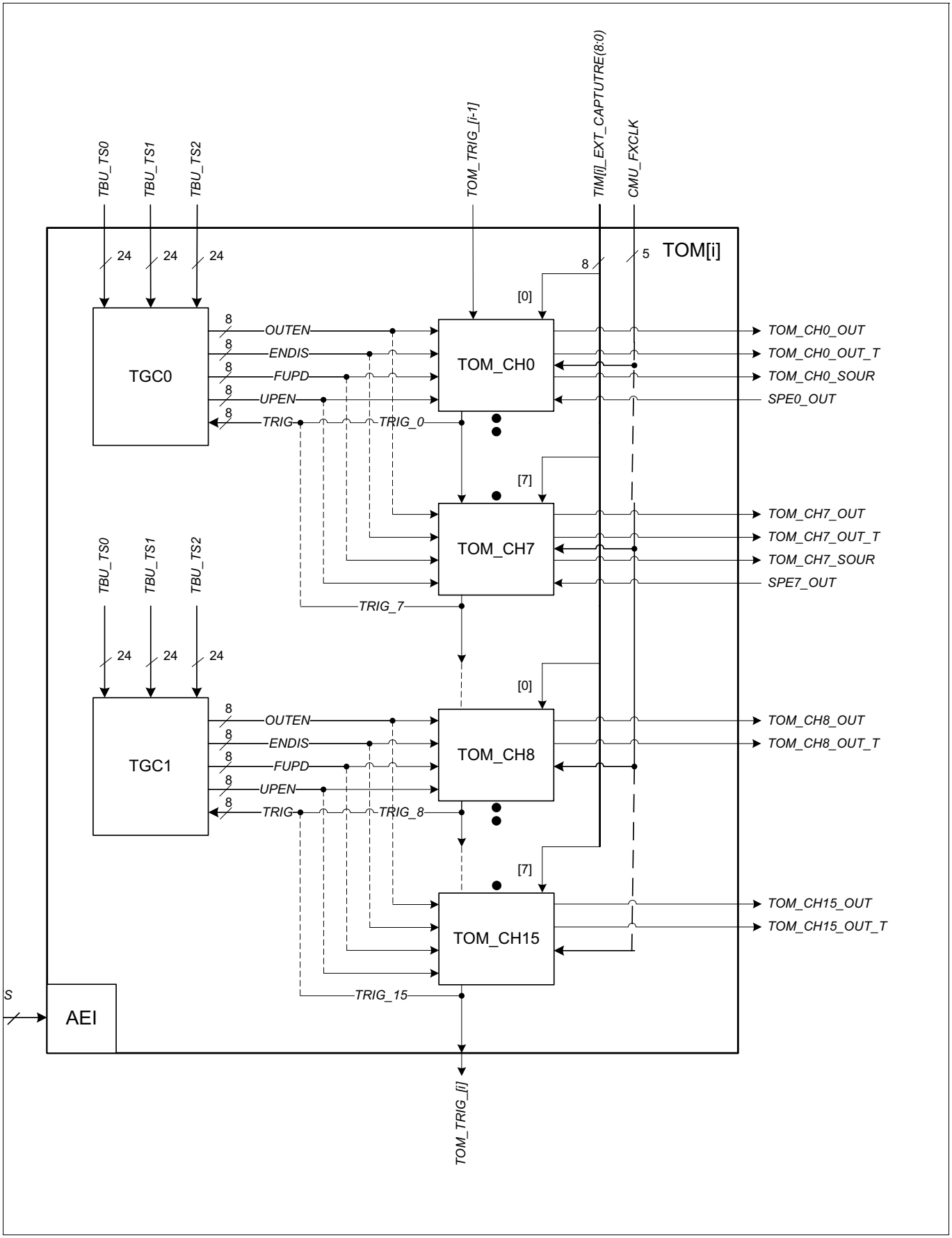


Figure 47 TOM block diagram

The two sub-modules TGC0 and TGC1 are global channel control units that control the enabling/disabling of the channels and their outputs as well as the update of their period and duty cycle register.

The module TOM receives two (three) timestamp values *TBU_TS0*, *TBU_TS1* (and *TBU_TS2*) in order to realize synchronized output behavior on behalf of a common time base.

The 5 dedicated clock line inputs *CMU_FXCLK* are providing divided clocks that can be selected to clock the output pins.

The trigger signal *TOM_TRIG_[i-1]* of TOM instance i comes from the preceding instance i-1, the trigger *TOM_TRIG_[i]* is routed to succeeding instance i+1.Note, TOM0 is connected to its own output *TOM_TRIG_0*, i.e. the last channel of TOM instance 0 can trigger the first channel of TOM instance 0 (this path is registered, which means delayed by one SYS_CLK period).

28.14.2 TOM Global Channel Control (TGC0, TGC1)

28.14.2.1 Overview

There exist two global channel control units (TGC0 and TGC1) to drive a number of individual TOM channels synchronously by external or internal events.

Each TGC[y] can drive up to eight TOM channels where TGC0 controls TOM channels 0 to 7 and TGC1 controls TOM channels 8 to 15.

The TOM sub-module supports four different kinds of signaling mechanisms:

- Global enable/disable mechanism for each TOM channel with control register **TOM[i]_TGC[y]_ENDIS_CTRL** and status register **TOM[i]_TGC[y]_ENDIS_STAT**
- Global output enable mechanism for each TOM channel with control register **TOM[i]_TGC[y]_OUTEN_CTRL** and status register **TOM[i]_TGC[y]_OUTEN_STAT**
- Global force update mechanism for each TOM channel with control register **TOM[i]_TGC[y]_FUPD_CTRL**
- Update enable of the register **CM0**, **CM1** and **CLK_SRC** for each TOM channel with the control bit field **UPEN_CTRL[z]** of **TOM[i]_TGC[y]_GLB_CTRL**

28.14.2.2 TGC Sub-unit

Each of the first three individual mechanisms (enable/disable of the channel, output enable and force update) can be driven by three different trigger sources. The three trigger sources are:

- the host CPU (bit **HOST_TRIG** of register **TOM[i]_TGC[y]_GLB_CTRL**)
- the TBU time stamp (signal *TBU_TS0, TBU_TS1, TBU_TS2* if available)
- the internal trigger signal *TRIG* (bunch of trigger signals *TRIG_[x]* which can be either the trigger *TRIG_CCU0* of channel x, the trigger of preceding channel x-1 (i.e. signal *TRIG_[x-1]*) or the external trigger *TIM_EXT_CAPTURE(t)* of assigned TIM channel t.

The first way is to trigger the control mechanism by a direct register write access via host CPU (bit **HOST_TRIG** of register **TOM[i]_TGC[y]_GLB_CTRL**).

The second way is provided by a compare match trigger on behalf of a specified time base coming from the module TBU (selected by bits **TBU_SEL**) and the time stamp compare value defined in the bit field **ACT_TB** of register **TOM[i]_TGC[y]_ACT_TB**.Note, a signed compare of **ACT_TB** and selected *TBU_TS*[*x*] with x=0,1,2 is performed.

The third possibility is the input *TRIG* (bunch of trigger signals *TRIG_[x]*) coming from the TOM channels 0 to 7 / 8 to 15.

The corresponding trigger signal *TRIG_[x]* coming from channel [x] can be masked by the register **TOM[i]_TGC[y]_INT_TRIG**.

To enable or disable each individual TOM channel, the register **TOM[i]_TGC[y]_ENDIS_CTRL** and/or **TOM[i]_TGC[y]_ENDIS_STAT** have to be used.

The register **TOM[i]_TGC[y]_ENDIS_STAT** controls directly the signal *ENDIS*. A write access to this register is possible.

The register **TOM[i]_TGC[y]_ENDIS_CTRL** is a shadow register that overwrites the value of register **TOM[i]_TGC[y]_ENDIS_STAT** if one of the three trigger conditions matches.

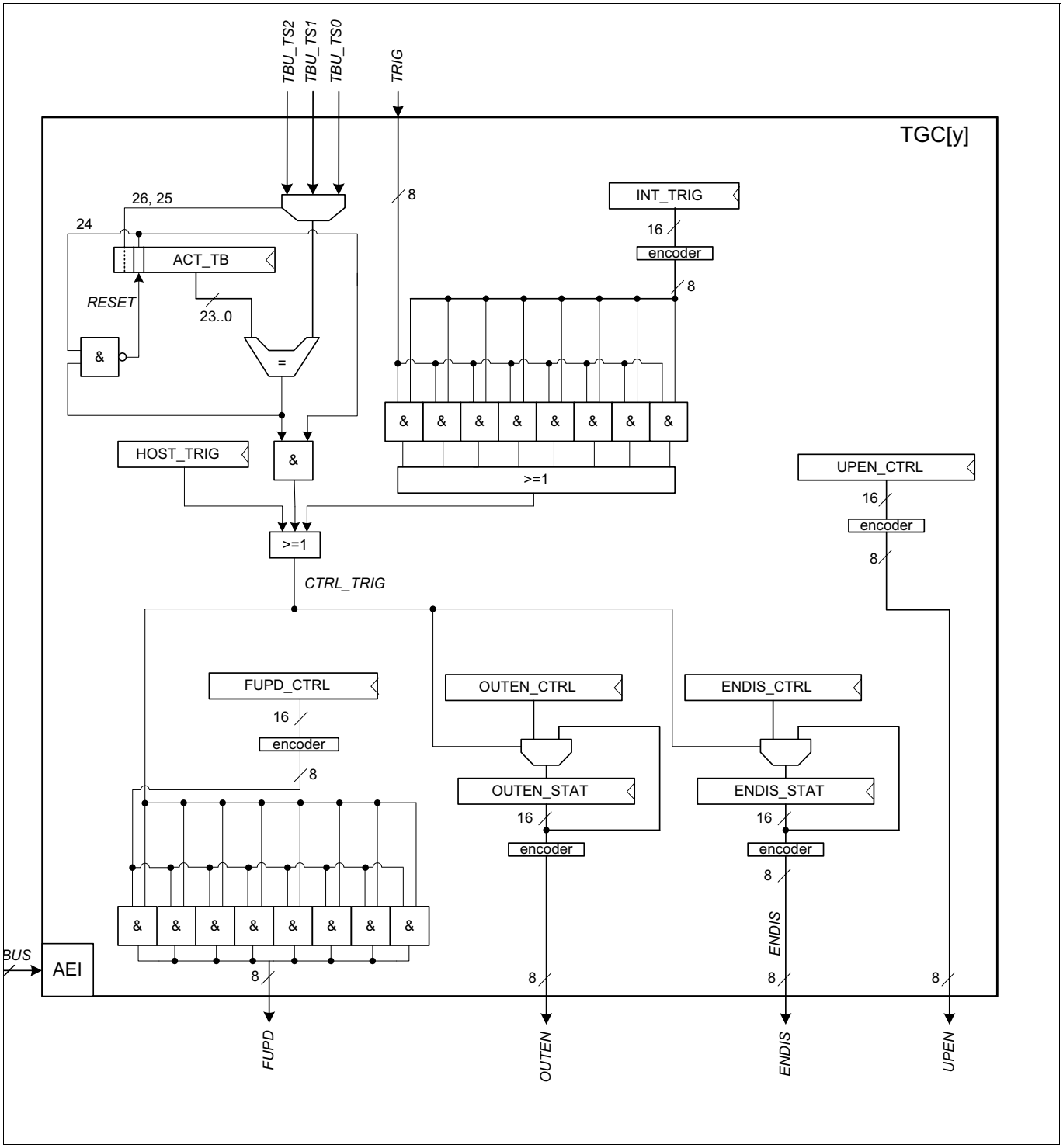


Figure 48 TOM Global channel control mechanism

The output of the individual TOM channels can be controlled using the register **TOM[i]_TGC[y]_OUTEN_CTRL** and **TOM[i]_TGC[y]_OUTEN_STAT**.

The register **TOM[i]_TGC[y]_OUTEN_STAT** controls directly the signal *OUTEN*. A write access to this register is possible.

The register **TOM[i]_TGC[y]_OUTEN_CTRL** is a shadow register that overwrites the value of register **TOM[i]_TGC[y]_OUTEN_STAT** if one of the three trigger conditions matches.

If a TOM channel is disabled by the register **TOM[i]_TGC[y]_OUTEN_STAT**, the actual value of the channel output at *TOM_CH[x]_OUT* is defined by the signal level bit (**SL**) defined in the channel control register **TOM[i]_CH[x]_CTRL**.If the output is enabled, the output at *TOM_CH[x]_OUT* depends on value of flip-flop **SOUR**.

The register **TOM[i]_TGC[y]_FUPD_CTRL** defines which of the TOM channels receive a *FORCE_UPDATE* event if the trigger signal *CTRL_TRIG* is raised.

Note: The force update request is stored and executed synchronized to the selected CMU_FXCLK.

The register bits **UPEN_CTRL[z]** defines for which TOM channel the update of the working register **CM0**, **CM1** and **CLK_SRC** by the corresponding shadow register **SR0**, **SR1** and **CLK_SRC_SR** is enabled. If update is enabled, the register **CM0**, **CM1** and **CLK_SRC** will be updated on reset of counter register **CN0** (see **Figure 49** and **Figure 50**). An exception is the configuration of SR0_TRIG=1 which enable the trigger generation defined by **SR0**. Then **CM0** is not updated with **SR0**.

28.14.3 TOM Channel

Each individual TOM channel comprises a Counter Compare Unit 0 (CCU0) which contains the counter register **CN0** and the period register **CM0**, a Counter Compare Unit 1 (CCU1) which contains the duty cycle register **CM1** and the Signal Output Generation Unit (SOU) which contains the output register **SOUR**. The architecture is depicted in **Figure 49** for channels 0 to 7 and in **Figure 50** for channels 8 to 15.

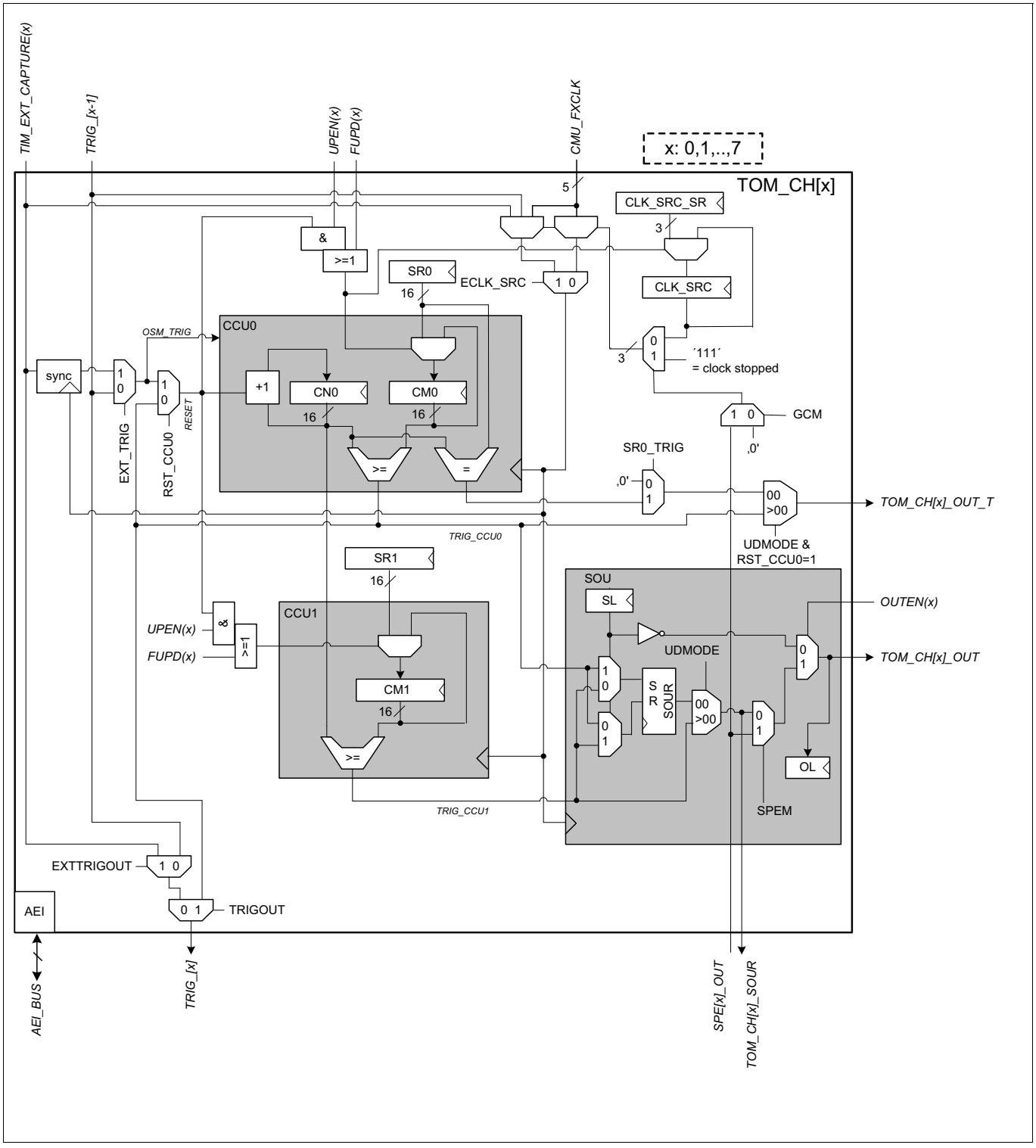


Figure 49 TOM Channel 0…7 architecture

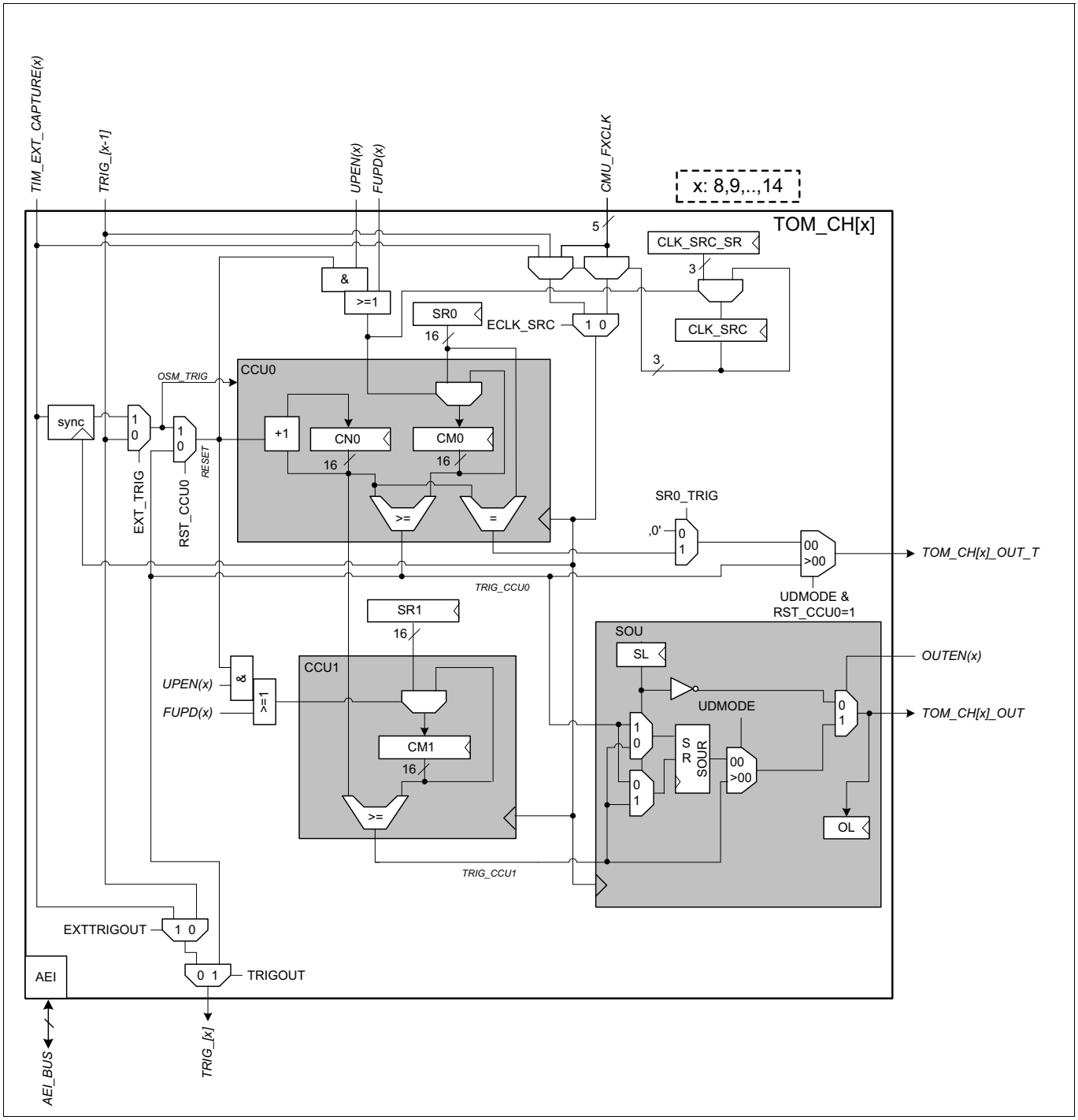


Figure 50 TOM Channel 8...14 architecture

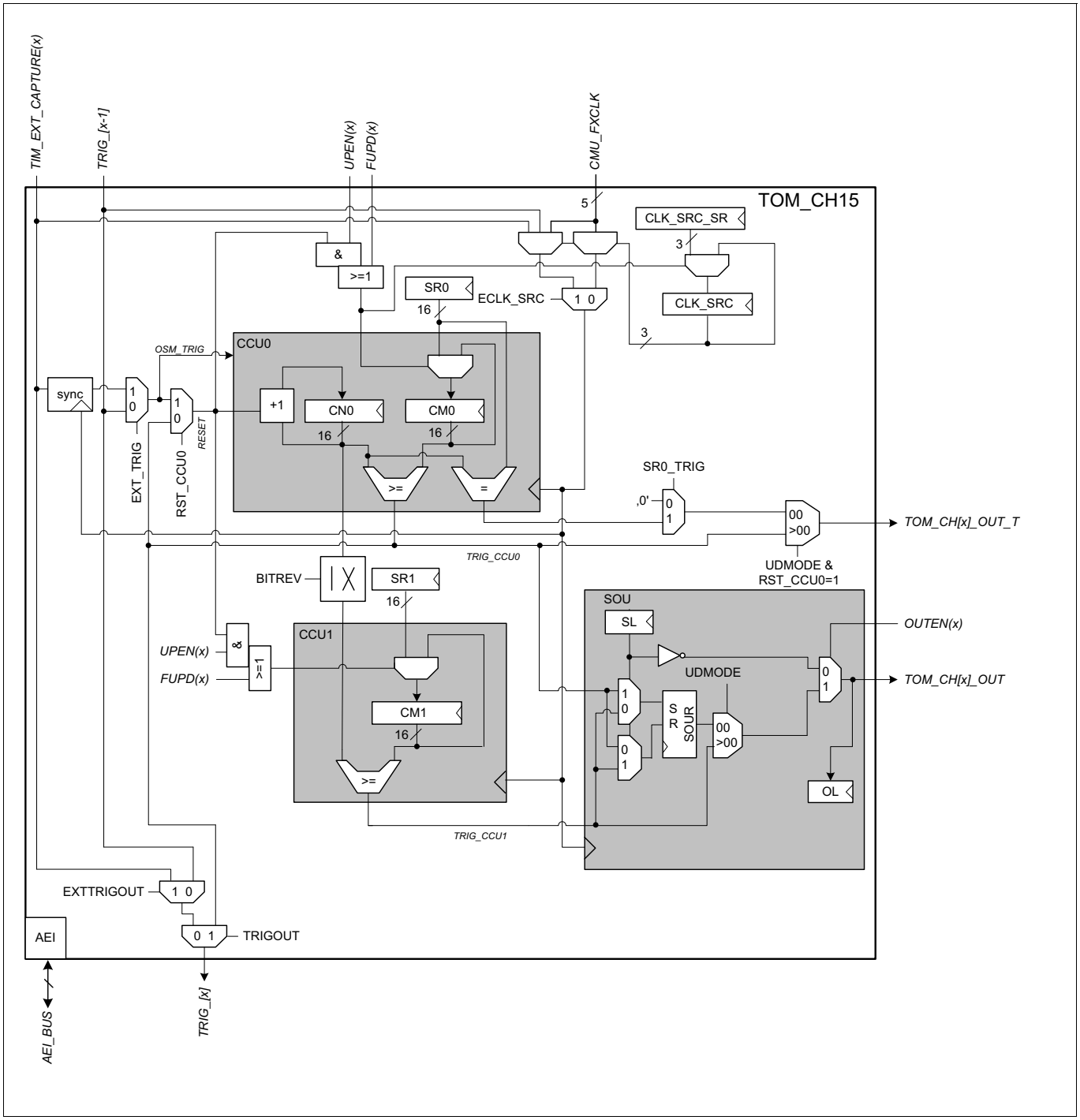


Figure 51 TOM Channel 15 architecture

The CCU0 contains a counter **CN0** which is clocked with one of the selected input frequencies (*CMU_FXCLK*) provided from outside of the sub-module.

Depending on configuration bits RST_CCU0 of register **TOM[i]_CH[x]_CTRL** the counter register **CN0** can be reset either when the counter value is equal to the compare value **CM0** (i.e. CN0 counts only 0 to CM0-1 and is then reset to 0) or when signaled by the TOM[i] trigger signal *TRIG_[x-1]* of the preceding channel [x-1] (which can also be the last channel of preceding instance TOM[i-1]) or the trigger signal *TIM_EXT_CAPTURE(x)* of the assigned TIM channel [x].

Note: As an exception, the input *TRIG_[0]* of instance TOM0 is triggered by its own last channel cCTO via signal *TRIG_[cCTO]*.

When the counter register **CN0** is greater or equal than the value **CM0** (in fact CM0-1) the sub-unit CCU0 triggers the SOU sub-unit and the succeeding TOM sub-module channel (signal *TRIG_CCU0*).

In the sub-unit CCU1 the counter register **CN0** is compared with the value of register **CM1**. If **CN0** is greater or equal than **CM1** the sub-unit CCU1 triggers the SOU sub-unit (signal *TRIG_CCU1*).

If counter register **CN0** of channel x is reset by its own CCU0 unit (i.e. the compare match of **CN0**>=**CM0**-1 configured by RST_CCU0=0), following statements are valid:

- **CN0** counts from 0 to **CM0**-1 and is then reset to 0.
- When CN0 is reset from CM0 to 0, an edge to SL is generated
- When CN0 is incrementing and reaches CN0 > CM1, an edge to !SL is generated.
- if **CM0**=0 or **CM0**=1, the counter **CN0** is constant 0.
- if **CM1**=0, the output is !SL = 0% duty cycle
- if **CM1** >= **CM0** and **CM0**>1, the output is SL = 100% duty cycle

If the counter register **CN0** of channel x is reset by the trigger signal coming from another channel or the assigned TIM module (configured by RST_CCU0=1), following statements are valid:

- **CN0** counts from 0 to MAX-1 and is then reset to 0 by trigger signal
- **CM0** defines the edge to SL value, **CM1** defines the edge to !SL value.
- if **CM0**=**CM1**, the output switches to SL if **CN0**=**CM0**=**CM1** (**CM0** has higher priority)
- if **CM0**=0 and **CM1**=MAX, the output is SL = 100% duty cycle
- if **CM0** > MAX, the output is !SL = 0% duty cycle, independent of **CM1**.

The hardware ensures that for both 0% and 100% duty cycle no glitch occurs at the output of the TOM channel.

The SOU sub-unit is responsible for output signal generation. On a trigger *TRIG_CCU0* from sub-unit CCU0 or *TRIG_CCU1* from sub-unit CCU1 an SR flip-flop of sub-unit SOU is either set or reset. If it is set or reset depends on the configuration bit **SL** of the control register **TOM[i]_CH[x]_CTRL**. The initial signal output level for the channel is the reverse value of the bit **SL**.

Figure 54 clarifies the PWM output behavior with respect to the **SL** bit definition. The output level on the TOM channel output pin *TOM[i]_CH[x]_OUT* is captured in bit **OL** of register **TOM[i]_CH[x]_STAT**.

28.14.3.1 Duty cycle, Period and Clock Frequency Update Mechanisms

The two action register **CM0** and **CM1** can be reloaded with the content of the shadow register **SR0** and **SR1**. The register **CLK_SRC** that determines the clock frequency of the counter register **CN0** can be reloaded with its shadow register **CLK_SRC_SR** (bit field in register **TOM[i]_CH[x]_CTRL**).

The update of the register **CM0**, **CM1** and **CLK_SRC** with the content of its shadow register is done when the reset of the counter register **CN0** is requested (via signal *RESET*). This reset of **CN0** is done if the comparison of **CN0** greater or equal than **CM0** is true or when the reset is triggered by another TOM channel [x-1] via the signal *TRIG_[x-1]* or when signaled via the signal *TIM_EXT_CAPTURE(x)* of the assigned TIM channel [x].

With the update of the register **CLK_SRC** at the end of a period a new counter **CN0** clock frequency can easily be adjusted.

In case of RST_CCU0=1 and update enabled by UPEN_CTRL[z] the register CM0, CM1 and CLK_SRC will be updated when CN0 is reset.

An update of duty cycle, period and counter **CN0** clock frequency becoming effective synchronously with start of a new period can easily be reached by performing following steps:

1. disable the update of the action register with the content of the corresponding shadow register by setting the channel specific configuration bit **UPEN_CTRL[z]** of register **TOM[i]_TGC[y]_GLB_CTRL** to '0'.
2. write new desired values to **SR0**, **SR1**, **CLK_SRC_SR**

3. enable update of the action register by setting the channel specific configuration bit **UPEN_CTRL[z]** of register **TOM[i]_TGC[y]_GLB_CTRL** to '1'.

28.14.3.1.1 Synchronous Update Of Duty Cycle Only

A synchronous update of only the duty cycle can be done by simply writing the desired new value to register **SR1** without preceding disable of the update mechanism (as described in the chapter above). The new duty cycle is then applied in the period following the period where the update of register **SR1** was done.

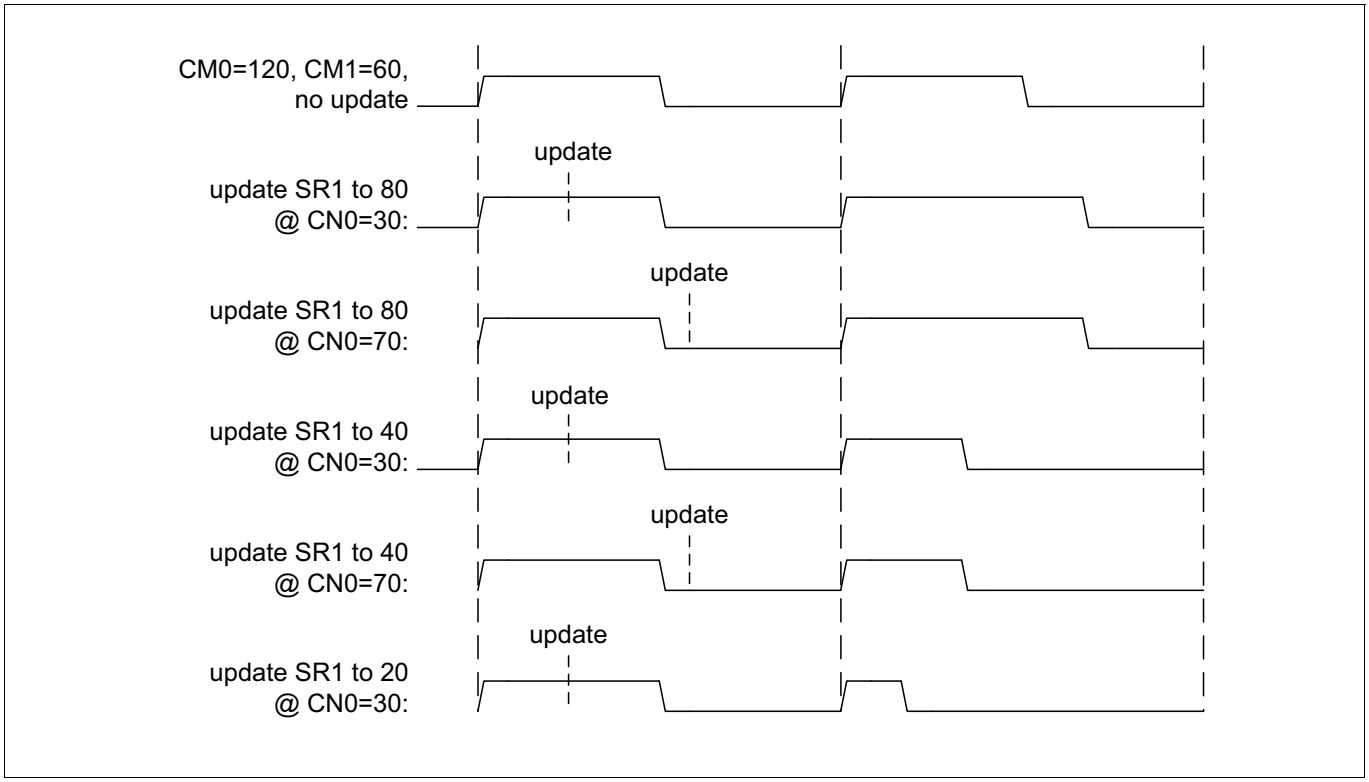


Figure 52 Synchronous update of duty cycle

28.14.3.1.2 Asynchronous Update Of Duty Cycle Only

If the update of the duty cycle should be performed independent of the start of a new period (asynchronous), the desired new value can be written directly to register **CM1**. In this case it is recommended to additionally either disable the synchronous update mechanism as a whole (i.e. clearing bits **UPEN_CTRL[z]** of corresponding channel [x] in register **TOM[i]_TGX[y]_GLB_CTRL**) or updating **SR1** with the same value as **CM1** before writing to **CM1**.

Depending on the point of time of the update of **CM1** in relation to the actual value of **CN0** and **CM1**, the new duty cycle is applied in the current period or the following period (see **Figure 53**). In any case the creation of glitches are avoided. The new duty cycle may jitter from update to update by a maximum of one period (given by **CM0**). However, the period remains unchanged.

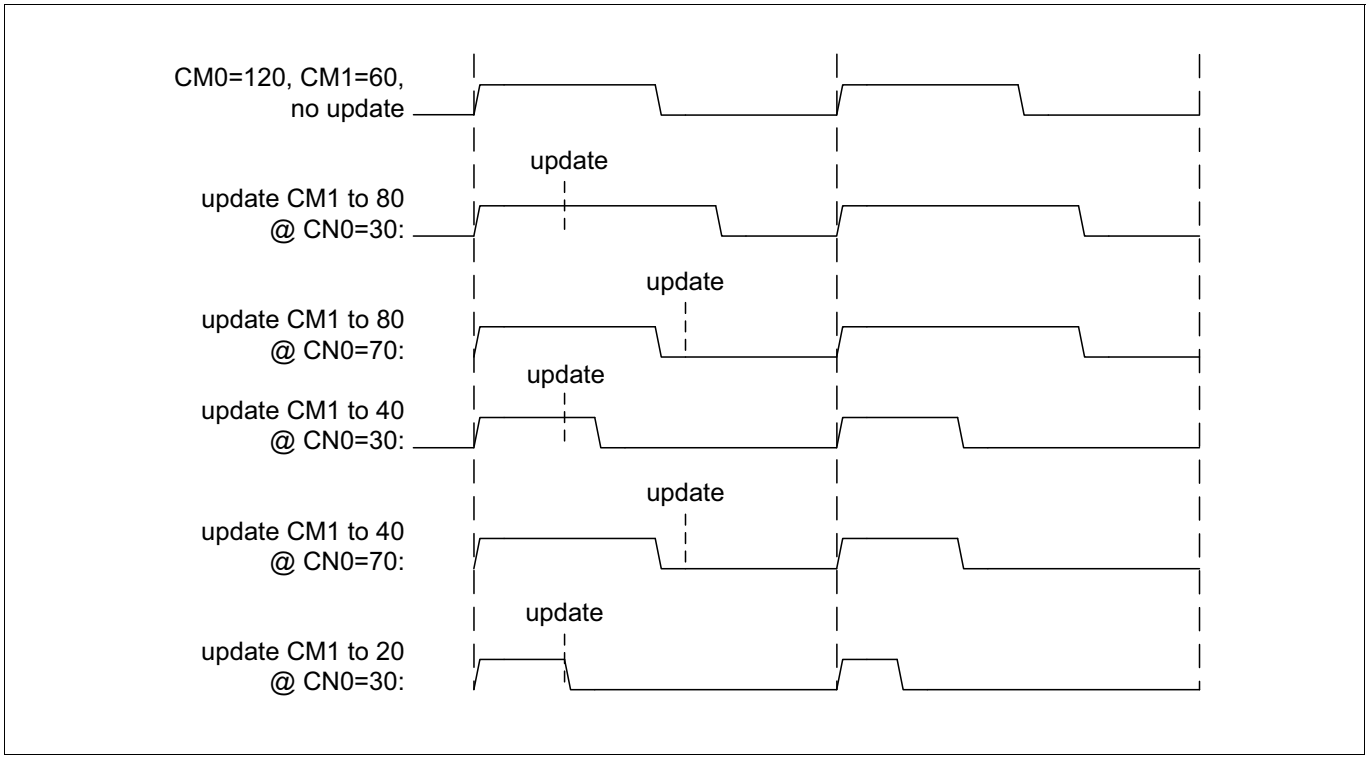


Figure 53 Asynchronous update of duty cycle

28.14.3.2 Continuous Counting Up Mode

In continuous mode the TOM channel starts incrementing the counter register **CN0** once it is enabled by setting the corresponding bits in register **TOM[i]_TGC[y]_ENDIS_STAT** (refer to **Section 28.14.2.2** for details of enabling a TOM channel).

The signal level of the generated output signal can be configured with the configuration bit **SL** of the channel configuration register **TOM[i]_CH[x]_CTRL**.

If the counter **CN0** is reset from **CM0** back to zero, the first edge of a period is generated at *TOM[i]_CH[x]_OUT*.

The second edge of the period is generated if **CN0** has reached **CM1**.

Every time the counter **CN0** has reached the value of **CM0** it is reset back to zero and proceeds with incrementing.

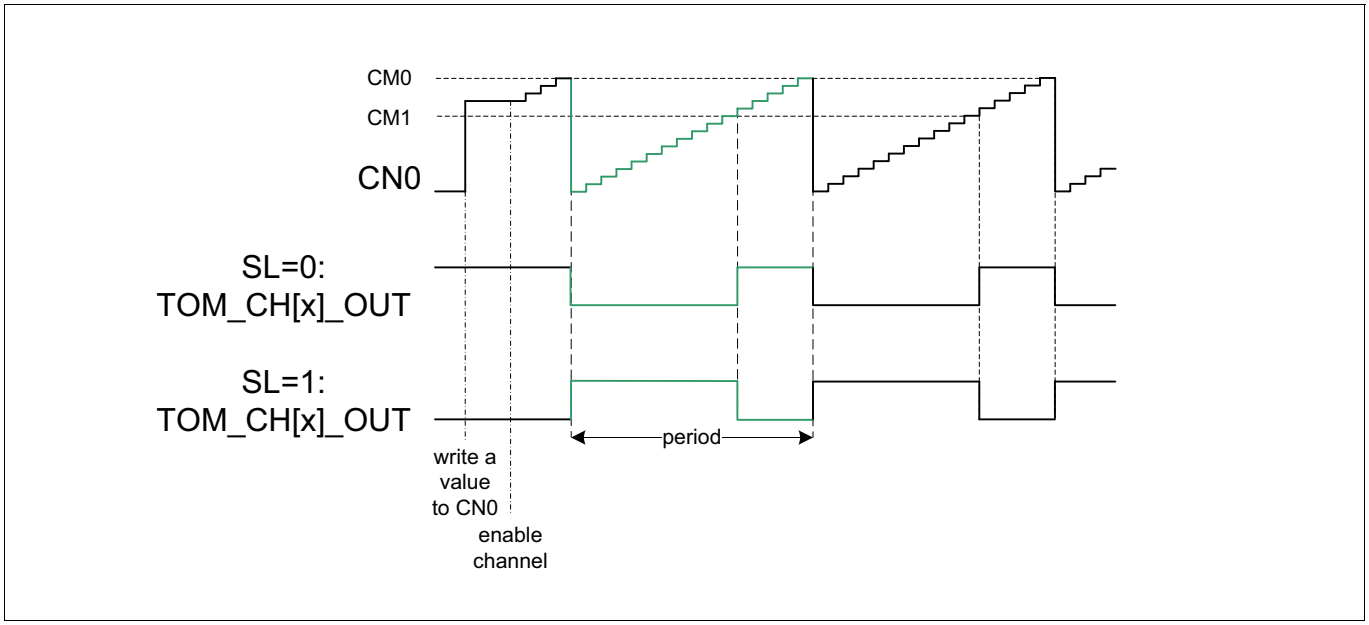


Figure 54 PWM Output with respect to configuration bit SL in continuous mode

28.14.3.3 Continuous Counting Up-Down Mode

In continuous mode, if **CN0** counts up and down (UDMODE != 0b00), depending on configuration bits RST_CCU0 of register **TOM[i]_CH[x]_CTRL** the counter register **CN0** changes direction either when the counter value is equal to the compare value **CM0,** has counted down to 0 or when triggered by the TOM[i] trigger signal *TRIG_[x-1]* of the preceding channel [x-1] (which can also be the last channel of preceding instance TOM[i-1]) or the trigger signal *TIM_EXT_CAPTURE(x)* of the assigned TIM channel [x].

In this case, if UPEN_CTRL[x]=1, also the working register **CM0**, **CM1** and **CLK_SRC** are updated depending on UDMODE.

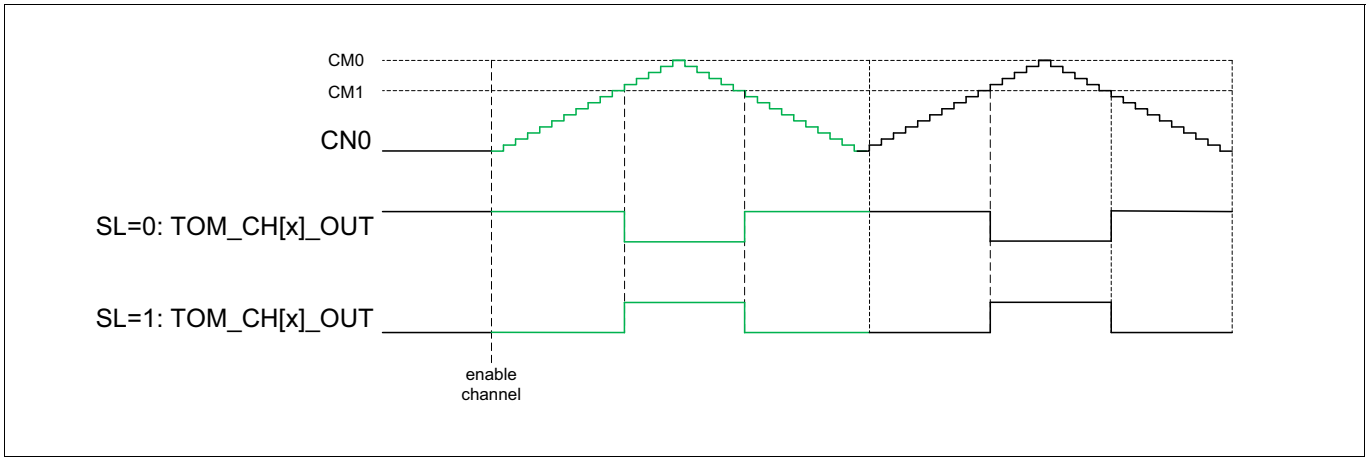


Figure 55 PWM Output behavior with respect to the SL bit in the ATOM[i]_CH[x]_CTRL register if UDMODE != 0b00

The clock of the counter register **CN0** can be one of the CMU clocks CMU_FXCLKx.The clock for **CN0** is defined by CLK_SRC_SR value in register **TOM[i]_CH[x]_CTRL.**The duration of a period in multiples of selected **CN0** counter clock ticks is defined by the **CM0** configuration value (i.e. **CM0** defines half of period in up-down mode).**CM1** defines the duty cycle value in clock ticks of selected **CN0** counter clock **CM0** defines half of duty cycle in up-down mode).

If counter register **CN0** of channel x is reset by its own CCU0 unit (i.e. the compare match of **CN0**>=**CM0** configured by RST_CCU0=0), following statements are valid:

- **CN0** counts continuously first up from 0 to **CM0**-1 and then down to 0.
- if **CN0** >= **CM1**, the output is set to SL
- if **CM1**=0, the output is SL (i.e. 100% duty cycle)
- if **CM1**>= **CM0**, the output is !SL (i.e. 0% duty cycle)
- On output *TOM[i]_CHx]_OUT* a PWM signal is generated. The period is defined by **CM0**, the duty cycle is defined by **CM1**.

This behavior is depicted in **Figure 55**.

If the counter register **CN0** of channel x is reset by the trigger signal coming from another channel or the assigned TIM module (configured by RST_CCU0=1), following statements are valid:

- **CN0** counts continuously first up. On a trigger signal the counter switches to count down mode. If <**CN0** has reached 0, it switches to count up mode.
- if **CN0** >= **CM1**, the output is set to SL
- if **CM1**=0, the output is SL (i.e. 100% duty cycle)
- if **CM1** >= **CM0**, the output is !SL (i.e. 0% duty cycle)
- On output **TOM[i]_CHx]_OUT** a PWM signal is generated. The period is defined by the CCU0 trigger of triggering channel, the duty cycle is defined by **CM1**.
- On output **TOM[i]_CHx]_OUT** a PWM signal is generated. The period is defined by the CCU0 trigger of triggering channel, the duty cycle is defined by **CM0**.

This behavior is depicted in figure **Figure 56**.

Note that in case of up-down counter mode and RST_CCU0=1 it is recommended that:

- the triggering channel and the triggered channel are both running in up-down mode,
- the time between two trigger signals is equal to the time needed for CN0 of triggered to count back to 0 and again up to the same upper value.

The second recommendation can be reached by synchronizing the start of triggering channel and triggered channel,i.e. let both channels start with CN0 value 0. Note that if there is a synchronization register in the trigger chain (indicated by value TOM_TRIG_CHAIN in register CCM[i]_HW_CONF), the additional delay of the trigger by one clock period has to be taken into account by starting at triggering channel with a CN0 value 1 (+1 compared to CN0 of triggered channel).

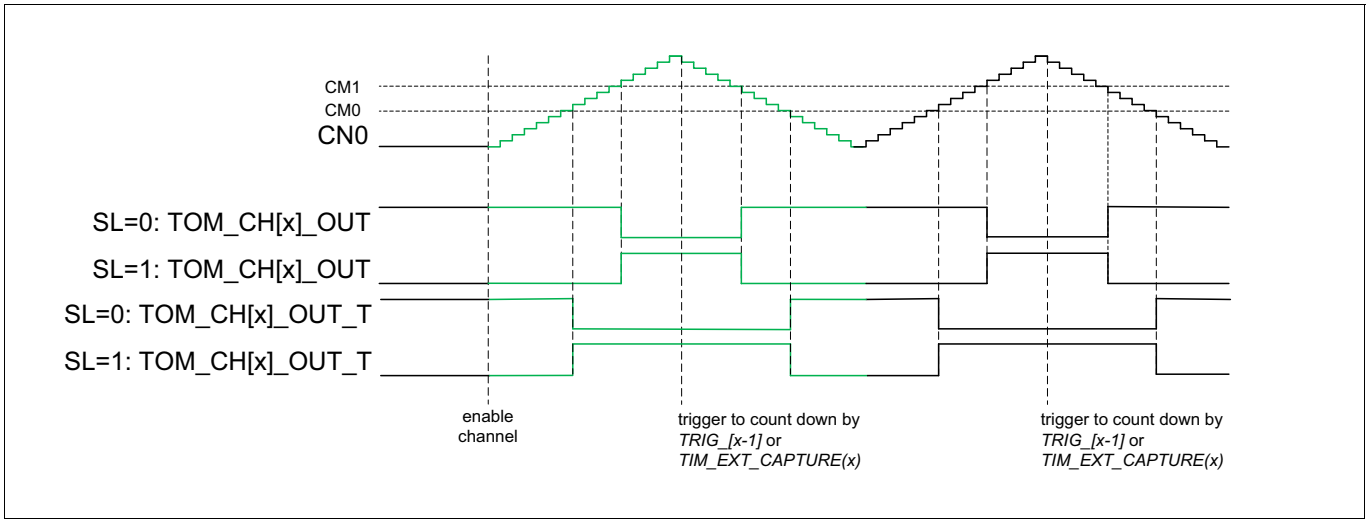


Figure 56 PWM Output behavior in case of RST_CCU0=1 and UDMODE != 0b00

28.14.3.4 One-shot Counting Up Mode

In one-shot mode, the TOM channel generates one pulse with a signal level specified by the configuration bit **SL** in the channel [x] configuration register **TOM[i]_CH[x]_CTRL**.

First the channel has to be enabled by setting the corresponding **TOM[i]_TGC[y]_ENDIS_STAT** value and the one-shot mode has to be enabled by setting bit **OSM** in register **TOM[i]_CH[x]_CTRL**.

In one-shot mode the counter **CN0** will not be incremented once the channel is enabled.

A write access to the register **CN0** triggers the start of pulse generation (i.e. the increment of the counter register **CN0**).

If SPE mode of TOM[i] channel 2 is enabled (set bit **SPEM** of register **TOM[i]_CH2_CTRL**), also the trigger signal *SPE[i]_NIPD* can trigger the reset of register **CN0** to zero and a start of the pulse generation.

The new value of **CN0** determines the start delay of the first edge. The delay time of the first edge is given by (**CM0-CN0**) multiplied with period defined by current value of **CLK_SRC**.

If the counter **CN0** is reset from **CM0** back to zero, the first edge at *TOM[i]_CH[x]_OUT* is generated.

To avoid an update of **CMx** register with content of **SRx** register at this point in time, the automatic update should be disabled by setting UPEN_CTRL[x] = 00 (in register **TOM[i]_TGC[y]_GLB_CTRL**)

The second edge is generated if **CN0** is greater or equal than **CM1** (i.e. **CN0** was incremented until it has reached **CM1** or **CN0** is greater than **CM1** after an update of **CM1**).

If the counter **CN0** has reached the value of **CM0** a second time, the counter stops.

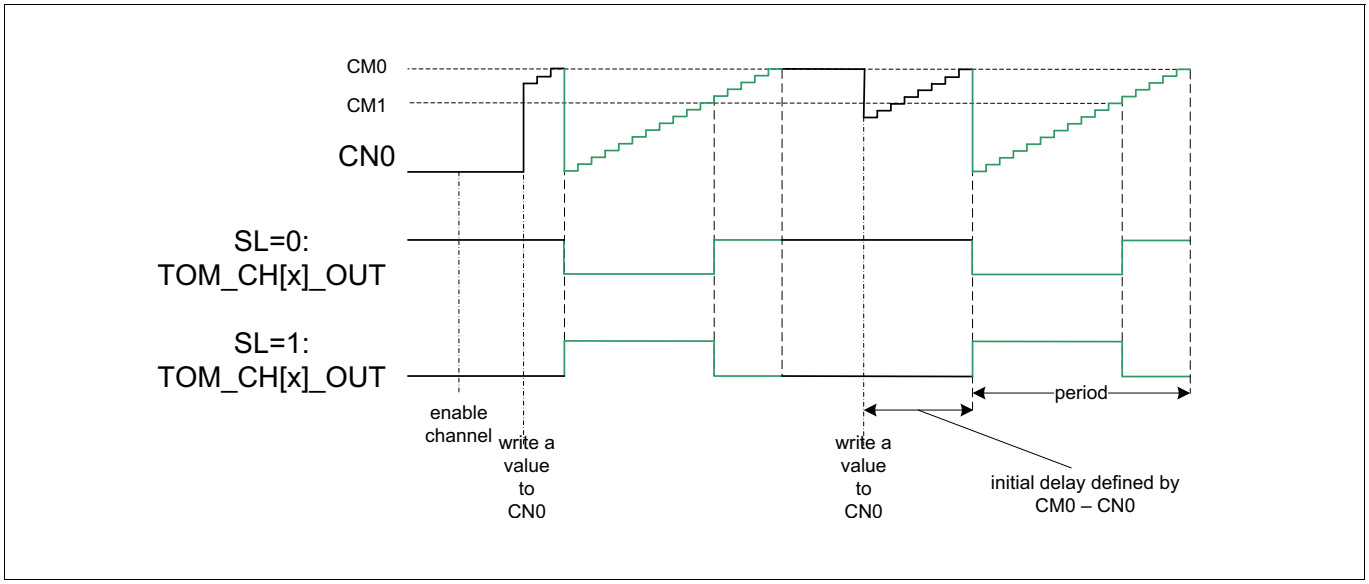


Figure 57 PWM Output with respect to configuration bit SL in one-shot mode: trigger by writing to CN0

Further output of single periods can be started by a write access to register CN0.

If CN0 is already incrementing (i.e. started by writing to CN0 a value CN0start < CM0), the affect of a second write access to CN0 depends on the phase of CN0:

phase 1: update of CN0 before CN0 reaches first time CM0

phase 2: update of CN0 after CN0 has reached first time CM0 but is less than CM1

phase 3: update of CN0 after CN0 has reached first time CM0 and CN0 is greater than or equal CM1

In phase 1: writing to counter CN0 a value CN0new < CM0 leads to a shift of first edge (generated if CN0 reaches CM0 first time) by the time CM0-CN0new.

In phase 2: writing to incrementing counter CN0 a value CN0new < CM1 while CN0old is below CM1 leads to a lengthening of the pulse. The counter CN0 stops if it reaches CM0.

In phase 3: Writing to incrementing counter CN0 a value CN0new while CN0old is already greater than or equal CM1 leads to an immediate restart of a single pulse generation inclusive the initial delay defined by CM0 - CN0new.

If a channel is configured to one-shot mode and configuration bit OSM_TRIG is set to 1, the trigger signal *OSM_TRIG* (i.e. *TRIG_[x-1]* or *TIM_EXT_CAPTURE(x)*) triggers start of one pulse generation.

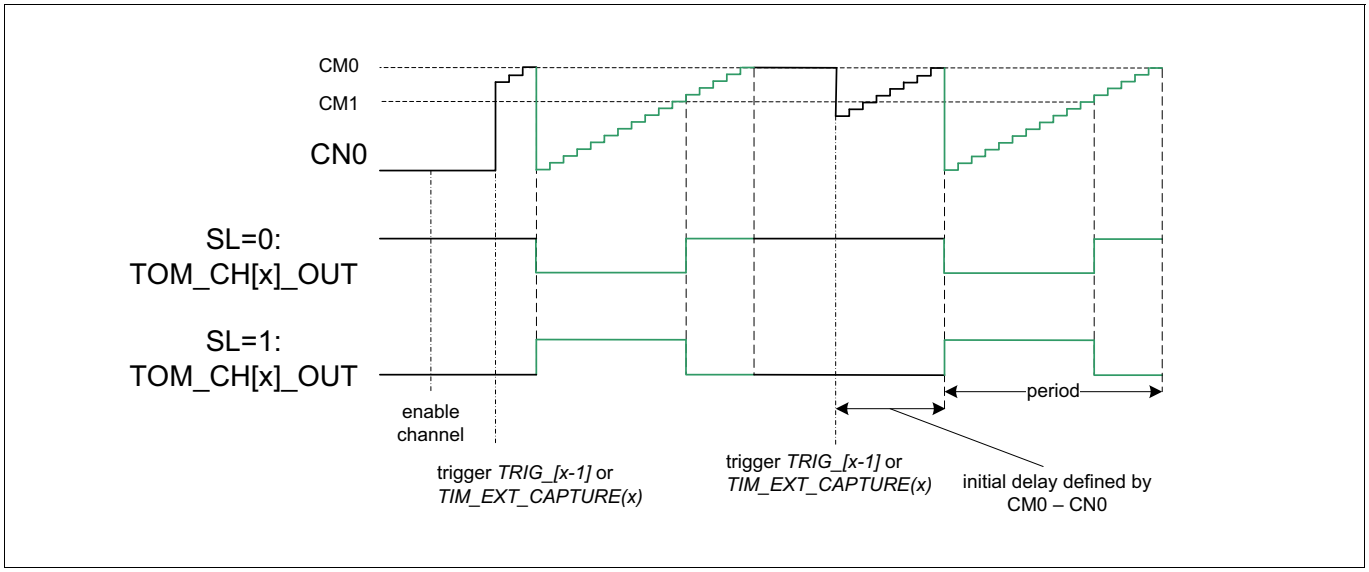


Figure 58 PWM Output with respect to configuration bit SL in one-shot mode: trigger by TRIG_[x-1] or TIM_EXT_CAPTURE(x)

28.14.3.5 One-shot Counting Up-Down Mode

The TOM channel can operate in one-shot counting up-down mode when the bit OSM = 1 and the UDMODE != 0b00. One-shot mode means that a single pulse with the pulse level defined in bit SL is generated on the output line.

First the channel has to be enabled by setting the corresponding **ENDIS_STAT** value.

In One-shot mode the counter **CN0** will not be incremented once the channel is enabled.

A write access to the register **CN0** triggers the start of pulse generation (i.e. the increment of the counter register **CN0**).

To avoid an update of **CMx** register with content of **SRx** register at this point in time, the automatic update should be disabled by setting UPEN_CTRL[x] = 0b00 (in register **TOM[i]_CH[x]_CTRL**)

If the counter **CN0** is greater or equal than **CM1**, the output *TOM[i]_CH[x]_OUT* is set to SL value.

If the counter **CN0** is less than **CM1**, the output *TOM[i]_CH[x]_OUT* is set to !SL value.

If the counter **CN0** has reached the value 0 (by counting down), it stops.

The new value of **CN0** determines the start delay of the first edge. The delay time of the first edge is given by (**CM1-CN0**) multiplied with period defined by current value of **CLK_SRC**.

Figure 59 depicts the pulse generation in one-shot mode.

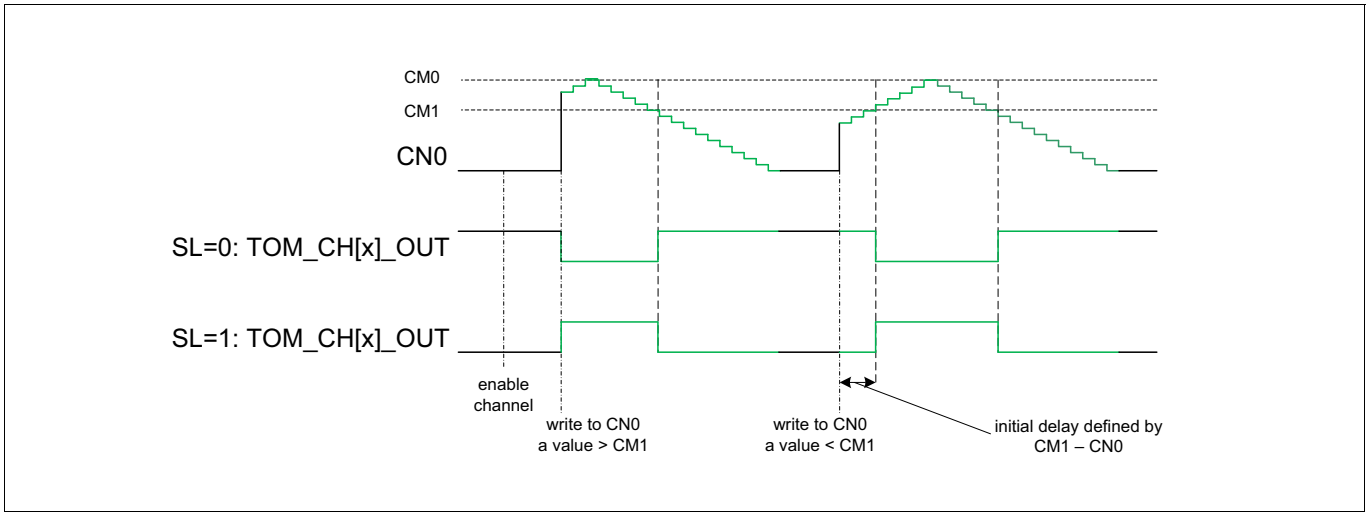


Figure 59 PWM Output with respect to configuration bit SL in one-shot counting up-down mode and UDMODE != 0b00: trigger by writing to CN0

Further output of single pulses can be started by writing to register **CN0**.

If a channel is configured to one-shot counting up-down mode and configuration bit OSM_TRIG is set to 1, the trigger signal *OSM_TRIG* (i.e. *TRIG_[x-1]* or *TIM_EXT_CAPTURE(x)*) triggers start of one pulse generation.

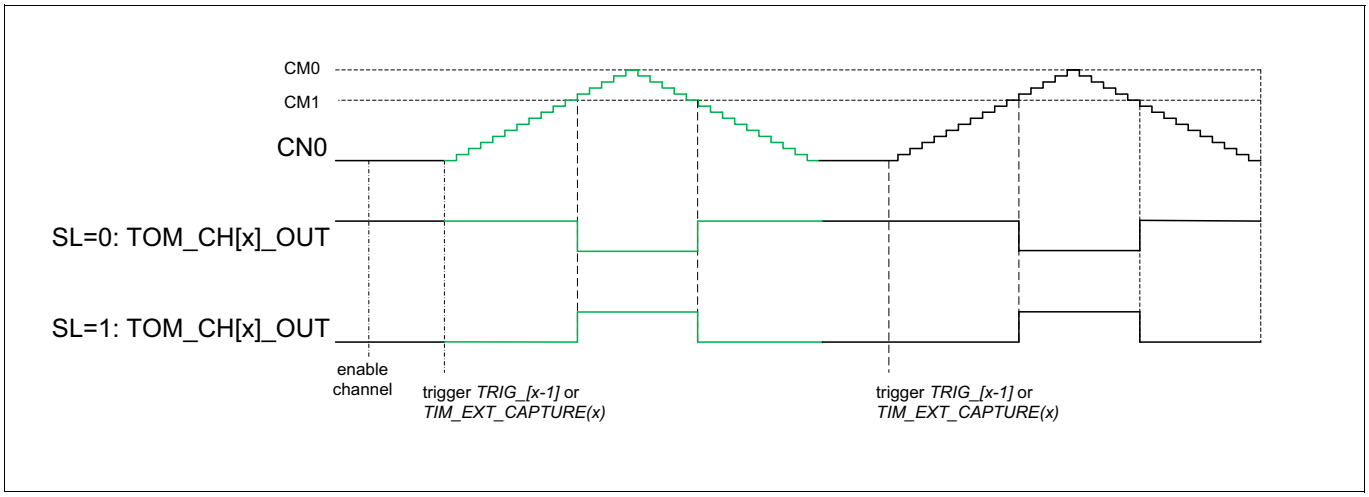


Figure 60 PWM Output with respect to configuration bit SL in one-shot counting up-down mode and UDMODE != 0b00: trigger by TRIG_[x-1] or TIM_EXT_CAPTURE(x)

28.14.3.6 Pulse Count Modulation Mode

At the output *TOM[i]_CH15_OUT* a pulse count modulated signal can be generated instead of the simple PWM output signal.

Figure **Figure 51** outlines the circuit for Pulse Count Modulation.

The PCM mode is enabled by setting bit **BITREV** to 1.

With the configuration bit **BITREV**=1 a bit-reversing of the counter output **CN0** is configured. In this case the bits LSB and MSB are swapped, the bits LSB+1 and MSB-1 are swapped, the bits LSB+2 and MSB-2 are swapped and so on.

The effect of bit-reversing of the **CN0** register value is shown in the following **Figure 61**.

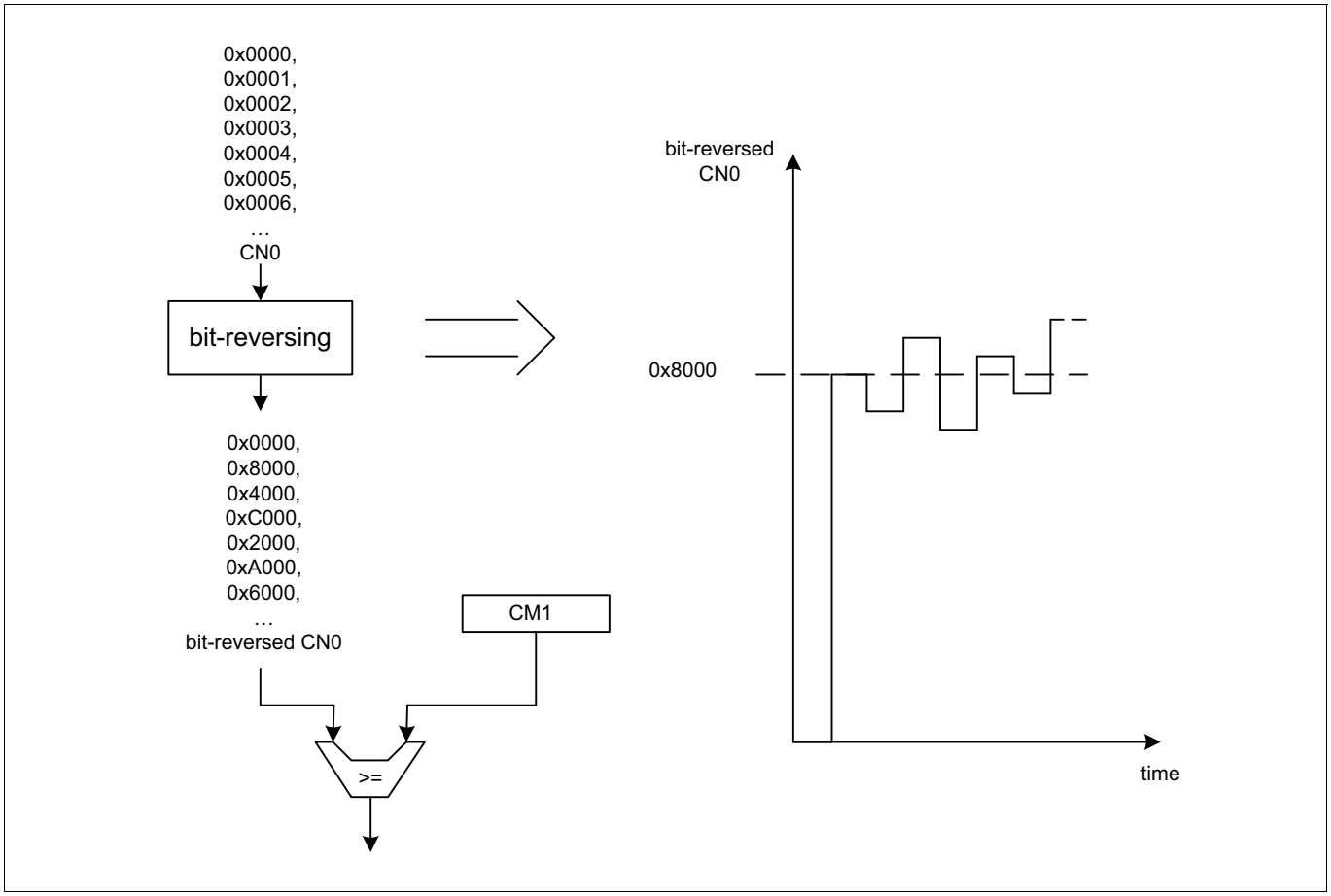


Figure 61 Bit reversing of counter CN0 output

In the PCM mode the counter register **CN0** is incremented by every clock tick depending on configured CMU clock (*CMU_FXCLK*).

The output of counter register **CN0** is first bit-reversed and then compared with the configured register value **CM1**.

If the bit-reversed value of register **CN0** is greater than **CM1**, the SR flip-flop of sub-module SOU is set (depending on configuration register **SL**) otherwise the SR flip-flop is reset. This generates at the output *TOM[i]_CH15_OUT* a pulse count modulated signal.

In PCM mode the **CM0** register - in which the period is defined - normally has to be set to its maximum value 0xFFFF.

To reduce time period of updating duty cycle value in **CM1** register, it is additionally possible to setup period value in **CM0** register to smaller values than maximum value as described before.

Possible values for **CM0** register are each even numbered values to the power of 2 e.g. 0x8000, 0x4000, 0x2000 ….

In this case the duty cycle has to be configured in the following manner.

Depending on how much the period in CM0 register is decreased - means shifted right starting from 0x10000 - the duty cycle in CM1 register has to be shifted left (= rotated: shift MSB back into LSB) with same value, e.g.

period CM0 = 0x0100 -> shifted 8 bits right from 0x10000

--> so duty cycle has to be shifted left 8 bit:

e.g. 50% duty cycle = 0x00080 -> shift 8 bits left -> CM1 = 0x8000

More examples:

period CM0	-->	duty cycle	-->	no shift	-->	CM1
0xFFFF	-->	0x8000	-->	no shift	-->	0x8000
0x8000	-->	0x4000	-->	shift 1 bit left	-->	0x8000
0x4000	-->	0x1000	-->	shift 2 bits left	-->	0x4000
0x2000	-->	0x0FFF	-->	shift 3 bits left	-->	0x7FF8
0x1000	-->	0x0333	-->	shift 4 bits left	-->	0x3330
0x0800	-->	0x0055	-->	shift 5 bits left	-->	0x0AA0
…						
0x0020	-->	0x0008	-->	shift 19 bits left	-->	0x4000
0x0010	-->	0x0005	-->	shift 20 bits left	-->	0x5000
…						

Note: In this mode the interrupt CCU1TC (see register **TOM[i]_CH[x]_IRQ_NOTIFY**) is set every time if bit reverse value of **CN0** is greater or equal than **CM1** which may be multiple times during one period. Therefore, from application point of view it is not useful to enable this interrupt.

28.14.3.7 Trigger Generation

For applications with constant PWM period defined by CM0, it is not necessary to update regularly the **CM0** register with **SR0** register. For these applications the **SR0** register can be used to define an additional output signal and interrupt trigger event.

If bit SR0_TRIG in register **TOM[i]_CH[x]_CTRL** is set, the register **SR0** is no longer used as a shadow register for register **CM0**. Instead, **SR0** is compared against **CN0** and if both are equal, a pulse of signal level '1' is generated at the output *TOM[i]_CH[x]_OUT_T*.The bit SR0_TRIG should only be set if bit RST_CCU0 of this channel is 0.

If bit SR0_TRIG is set the interrupt notify flag CCU1TC is no longer set on a compare match of **CM1** and **CN0**. Instead, the CCU1TC interrupt notify flag is set in case of a compare equal match of **SR0** and **CN0**.

With configuration bit TRIG_PULSE one can select if the output *TOM[i]_CH[x]_OUT_T* is high as long as CN0=SR0 (TRIG_PULSE=0) or if there will be only one pulse of length one SYS_CLK period when CN0 becomes SR0 (TRIG_PULSE=1).

The TOM output signal routing to DTM or GTM top level is described in subchapter “DTM connections on GTM-IP top level”

28.14.4 TOM BLDC Support

The TOM sub-module offers in combination with the SPE sub-module a BLDC support. To drive a BLDC engine TOM channels 0 to 7 can be used.

The BLDC support can be configured by setting the **SPEM** bit inside the **TOM[i]_CH[z]_CTRL** register. When this bit is set the TOM channel output is controlled through the SPE_OUT(z) signal coming from the SPE sub-module (see **Figure 49**). Please refer to chapter “Sensor Pattern Evaluation” for a detailed description of the SPE sub-module.

The TOM[i]_CH2,6,7,8 or 9 can be used together with the SPE module to trigger a delayed update of the **SPE_OUT_CTRL** register (i.e. commutation delay) after new input pattern detected by SPE (signaled by *SPE[i]_NIPD*). This feature is configured on TOM[i]_CH2,6,7,8 or 9 by setting SPE_TRIG=1 and OSM=1. With this configuration the TOM channel i generates one single PWM pulse on trigger by signal *SPE_NIPD*.

For details please refer to chapter of SPE sub-module description.

28.14.5 TOM Gated Counter Mode

Each TOM - SPE module combination provides also the feature of a gated counter mode. This is reached by using the *FSOI* input of a TIM module to gate the clock of a CCU0 sub-module.

To configure this mode, registers of module SPE should be set as following:

- the SPE should be enabled (bit **SPE_EN** = 1),
- all three TIM inputs should be disabled **SIE0** = **SIE1** = **SIE2** = 0),
- **SPE[i]_OUT_CTRL** should be set to 00005555h (set **SPE_OUT()** to '0'),
- mode FSOM should be enabled (**FSOM**=1),
- set in bit field **FSOL** bit c if channel c of module TOM is chosen for gated counter mode
- Additionally in module TOM
  - mode should be disabled (**SPEM**=0) and
  - the gated counter mode should be enabled (**GCM**=1)

As a result of this configuration, the counter **CN0** in sub-module CCU0 of TOM channel c counts as long as input *FSOI* is '0'.

28.14.6 TOM Interrupt signals

Table 48 TOM Interrupt signals

Signal	Description
TOM_CCU0TCx_IRQ	CCU0 Trigger condition interrupt for channel x
TOM_CCU1TCx_IRQ	CCU1 Trigger condition interrupt for channel x

28.14.7 TOM Configuration Register Overview

Table 49 TOM Configuration Register Overview

Register name	Description	see Page
TOM[i]_TGC[y]_GLB_CTRL	TOMi TGC y global control register	221
TOM[i]_TGC[y]_ENDIS_CTRL	TOMi TGC y enable/disable control register	222
TOM[i]_TGC[y]_ENDIS_STAT	TOMi TGC y enable/disable status register	223
TOM[i]_TGC[y]_ACT_TB	TOMi TGC y action time base register	224
TOM[i]_TGC[y]_OUTEN_CTRL	TOMi TGC y output enable control register	225
TOM[i]_TGC[y]_OUTEN_STAT	TOMi TGC y output enable status register	226
TOM[i]_TGC[y]_FUPD_CTRL	TOMi TGC y force update control register	226
TOM[i]_TGC[y]_INT_TRIG	TOMi TGC y internal trigger control register	227
TOM[i]_CH[x]_CTRL	TOMi channel x control register	228
TOM[i]_CH[x]_CN0	TOMi channel x CCU0 counter register	232
TOM[i]_CH[x]_CM0	TOMi channel x CCU0 compare register	233
TOM[i]_CH[x]_SR0	TOMi channel x CCU0 compare shadow register	233
TOM[i]_CH[x]_CM1	TOMi channel x CCU1 compare register	234
TOM[i]_CH[x]_SR1	TOMi channel x CCU1 compare shadow register	234
TOM[i]_CH[x]_STAT	TOMi channel x status register	235
TOM[i]_CH[x]_IRQ_NOTIFY	TOMi channel x interrupt notification register	235
TOM[i]_CH[x]_IRQ_EN	TOMi channel x interrupt enable register	236
TOM[i]_CH[x]_IRQ_FORCINT	TOMi channel x force interrupt register	237
TOM[i]_CH[x]_IRQ_MODE	TOMi channel x interrupt mode register	237

28.14.8 TOM Configuration Register Description

28.14.8.1 Register TOM[i]_TGC[y]_GLB_CTRL

TOMi TGC0 Global Control Register

TOMi_TGC0_GLB_CTRL (i=0-5)
TOMi TGC0 Global Control Register **(008030_H+i*800_H)** **Application Reset Value: 0000 0000_H**
TOMi_TGC1_GLB_CTRL (i=0-5)
TOMi TGC1 Global Control Register **(008230_H+i*800_H)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UPEN_CTRL7		UPEN_CTRL6		UPEN_CTRL5		UPEN_CTRL4		UPEN_CTRL3		UPEN_CTRL2		UPEN_CTRL1		UPEN_CTRL0	
rw		rw		rw		rw		rw		rw		rw		rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RST_CH7	RST_CH6	RST_CH5	RST_CH4	RST_CH3	RST_CH2	RST_CH1	RST_CH0	0							HOST_TRIG
w	w	w	w	w	w	w	w	r							w

Field	Bits	Type	Description
HOST_TRIG	0	w	**Trigger request signal (see TGC0, TGC1) to update the register ENDIS_STAT and OUTEN_STAT** This flag is reset automatically after triggering the update. 0_B No trigger request 1_B Set trigger request
RST_CHx (x=0-7)	x+8	w	**Software reset of channel x** This bit is cleared automatically after write by CPU. The channel register are set to their reset values and channel x operation is stopped immediately. The SR flip-flop SOUR is set to '1'. 0_B No action 1_B Reset channel x
UPEN_CTRLx (x=0-7)	2*x+17:2*x +16	rw	**TOM channel x enable update of register CM0, CM1 and CLK_SRC from SR0, SR1 and CLK_SRC_SR** Write / Read : 00_B Don’t care, bits 1:0 will not be changed / update disabled 01_B Disable update / -- 10_B Enable update / -- 11_B Don’t care, bits 1:0 will not be changed / update enabled
0	7:1	r	**Reserved** Read as zero, shall be written as zero.

28.14.8.2 Register TOM[i]_TGC[y]_ENDIS_CTRL

TOMi TGC0 Enable/Disable Control Register

TOMi_TGC0_ENDIS_CTRL (i=0-5)
TOMi TGC0 Enable/Disable Control Register(008070_H+i*800_H) **Application Reset Value: 0000 0000_H**
TOMi_TGC1_ENDIS_CTRL (i=0-5)
TOMi TGC1 Enable/Disable Control Register(008270_H+i*800_H) **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENDIS_CTRL7		ENDIS_CTRL6		ENDIS_CTRL5		ENDIS_CTRL4		ENDIS_CTRL3		ENDIS_CTRL2		ENDIS_CTRL1		ENDIS_CTRL0	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
ENDIS_CTRLx (x=0-7)	2*x+1:2*x	rw	**TOM channel x enable/disable update value** If FREEZE = 0: If a TOM channel is disabled, the counter CN0 is stopped and the output register of SOU unit is set to the inverse value of control bit SL. On an enable event, the counter CN0 starts counting from its current value. If FREEZE = 1: If a TOM channel is disabled, the counter CN0 is stopped. On an enable event, the counter CN0 starts counting from its current value. Write of following double bit values is possible: If the output is disabled (OUTEN[0]=0), the TOM channel 0 output TOM[i]_CH0_OUT is the inverted value of bit SL. 00_B Don't care, bits 1:0 of register ENDIS_STAT will not be changed on an update trigger 01_B Disable channel on an update trigger 10_B Enable channel on an update trigger 11_B Don't change bits 1:0 of this register
0	31:16	r	**Reserved** Read as zero, shall be written as zero.

28.14.8.3 Register TOM[i]_TGC[y]_ENDIS_STAT

TOMi TGC0 Enable/Disable Status Register

TOMi_TGC0_ENDIS_STAT (i=0-5)
TOMi TGC0 Enable/Disable Status Register (008074_H+i*800_H) **Application Reset Value: 0000 0000_H**
TOMi_TGC1_ENDIS_STAT (i=0-5)
TOMi TGC1 Enable/Disable Status Register (008274_H+i*800_H) **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

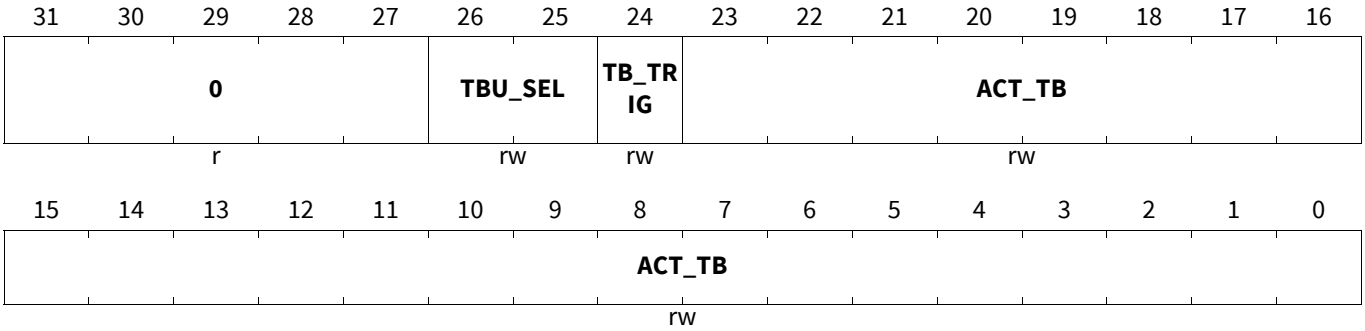
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENDIS_STAT7		ENDIS_STAT6		ENDIS_STAT5		ENDIS_STAT4		ENDIS_STAT3		ENDIS_STAT2		ENDIS_STAT1		ENDIS_STAT0	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
ENDIS_STATx (x=0-7)	2*x+1:2*x	rw	**TOM channel x enable/disable update value** If FREEZE = 0: If a TOM channel is disabled, the counter CN0 is stopped and the output register of SOU unit is set to the inverse value of control bit SL. On an enable event, the counter CN0 starts counting from its current value. If FREEZE = 1: If a TOM channel is disabled, the counter CN0 is stopped. On an enable event, the counter CN0 starts counting from its current value. Write of following double bit values is possible: 00_B Don't care, bits 1:0 will not be changed / channel disabled 01_B Disable channel / -- 10_B Enable channel / -- 11_B Don't care, bits 1:0 will not be changed / channel enabled
0	31:16	r	**Reserved** Read as zero, shall be written as zero.

28.14.8.4 Register TOM[i]_TGC[y]_ACT_TB

TOMi TGC0 Action Time Base Register

TOMi_TGC0_ACT_TB (i=0-5)
TOMi TGC0 Action Time Base Register **(008034_H+i*800_H)** **Application Reset Value: 0000 0000_H**
TOMi_TGC1_ACT_TB (i=0-5)
TOMi TGC1 Action Time Base Register **(008234_H+i*800_H)** **Application Reset Value: 0000 0000_H**



Field	Bits	Type	Description
ACT_TB	23:0	rw	**Time base value** Specifies the signed compare value with selected signal TBU_TS[x], x=0..2 If selected TBU_TS[x] value is in the interval [**ACT_TB** - 007FFFFFh, **ACT_TB**], the event is in the past, and the trigger is generated immediately. Otherwise, the event is in the future, and the trigger is generated if selected TBU_TS[x] is equal to **ACT_TB**.
TB_TRIG	24	rw	**Set trigger request** This flag is reset automatically if the selected time base unit (*TBU_TS0* or *TBU_TS1* or *TBU_TS2,* if present) has reached the value ACT_TB and the update of the register was triggered. 0_B No trigger request 1_B Set trigger request
TBU_SEL	26:25	rw	**Selection of time base used for comparison** The bit combination 0b10 is only applicable if the TBU of the device contains three time base channels. Otherwise, this bit combination is also reserved. Please refer to GTM Architecture block diagram on page 3 to determine the number of channels for TBU of this device. 00_B TBU_TS0 selected 01_B TBU_TS1 selected 10_B TBU_TS2 selected 11_B Same as 0b00
0	31:27	r	**Reserved** Read as zero, shall be written as zero.

28.14.8.5 Register TOM[i]_TGC[y]_OUTEN_CTRL

TOMi TGC0 Output Enable Control Register

TOMi_TGC0_OUTEN_CTRL (i=0-5)
TOMi TGC0 Output Enable Control Register(008078_H+i*800_H) **Application Reset Value: 0000 0000_H**
TOMi_TGC1_OUTEN_CTRL (i=0-5)
TOMi TGC1 Output Enable Control Register(008278_H+i*800_H) **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTEN_CTRL 7		OUTEN_CTRL 6		OUTEN_CTRL 5		OUTEN_CTRL 4		OUTEN_CTRL 3		OUTEN_CTRL 2		OUTEN_CTRL 1		OUTEN_CTRL 0	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
OUTEN_CTRL x (x=0-7)	2*x+1:2*x	rw	**Output TOM[i]_CHx_OUT enable/disable update value** Write of following double bit values is possible: If the channel is disabled (ENDIS[0]=0) or the output is disabled (OUTEN[0]=0), the TOM channel 0 output *TOM[i]_CH0_OUT* is the inverted value of bit SL. 00_B Don't care, bits 1:0 of register OUTEN_STAT will not be changed on an update trigger 01_B Disable channel output on an update trigger 10_B Enable channel output on an update trigger 11_B Don't change bits 1:0 of this register
0	31:16	r	**Reserved** Read as zero, shall be written as zero.

28.14.8.6 Register TOM[i]_TGC[y]_OUTEN_STAT

TOMi TGC0 Output Enable Status Register

TOMi_TGC0_OUTEN_STAT (i=0-5)
TOMi TGC0 Output Enable Status Register (00807C$_H$+i*800$_H$) **Application Reset Value: 0000 0000$_H$**
TOMi_TGC1_OUTEN_STAT (i=0-5)
TOMi TGC1 Output Enable Status Register (00827C$_H$+i*800$_H$) **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTEN_STAT7		OUTEN_STAT6		OUTEN_STAT5		OUTEN_STAT4		OUTEN_STAT3		OUTEN_STAT2		OUTEN_STAT1		OUTEN_STAT0	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
OUTEN_STATx (x=0-7)	2*x+1:2*x	rw	**Control/status of output TOM[i]_CHx_OUT** Write of following double bit values is possible: 00_B Don't care, bits 1:0 will not be changed / output disabled 01_B Disable output / -- 10_B Enable output / -- 11_B Don't care, bits 1:0 will not be changed / output enabled
0	31:16	r	**Reserved** Read as zero, shall be written as zero

28.14.8.7 Register TOM[i]_TGC[y]_FUPD_CTRL

TOMi TGC0 Force Update Control Register

TOMi_TGC0_FUPD_CTRL (i=0-5)
TOMi TGC0 Force Update Control Register (008038$_H$+i*800$_H$) **Application Reset Value: 0000 0000$_H$**
TOMi_TGC1_FUPD_CTRL (i=0-5)
TOMi TGC1 Force Update Control Register (008238$_H$+i*800$_H$) **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSTCN0_CH7		RSTCN0_CH6		RSTCN0_CH5		RSTCN0_CH4		RSTCN0_CH3		RSTCN0_CH2		RSTCN0_CH1		RSTCN0_CH0	
rw		rw		rw		rw		rw		rw		rw		rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FUPD_CTRL7		FUPD_CTRL6		FUPD_CTRL5		FUPD_CTRL4		FUPD_CTRL3		FUPD_CTRL2		FUPD_CTRL1		FUPD_CTRL0	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
FUPD_CTRLx (x=0-7)	2*x+1:2*x	rw	**Force update of TOM channel x operation registers** If enabled, force update of register CM0, CM1 and CLK_SRC triggered by HOST_TRIG, ACT_TB compare match, or internal trigger. Write / Read: The force update request is stored and executed synchronized to the selected FXCLK. 00_B Don't care, bits 1:0 will not be changed / force update disabled 01_B Disable force update / -- 10_B Enable force update / -- 11_B Don't care, bits 1:0 will not be changed / force update enabled
RSTCN0_CHx (x=0-7)	2*x+17:2*x +16	rw	**Reset CN0 of channel x on force update event** If enabled, reset CN0 triggered by HOST_TRIG, ACT_TB compare match, or internal trigger. Write / Read: 00_B Don't care, bits 1:0 will not be changed / CN0 is not reset on forced update 01_B Do not reset CN0 on forced update / -- 10_B Reset CN0 on forced update / -- 11_B Don't care, bits 1:0 will not be changed / CN0 is reset on forced update

28.14.8.8 Register TOM[i]_TGC[y]_INT_TRIG

TOMi TGC0 Internal Trigger Control Register

TOMi_TGC0_INT_TRIG (i=0-5)
TOMi TGC0 Internal Trigger Control Register($00803C_H$+i*800_H) **Application Reset Value: 0000 0000_H**
TOMi_TGC1_INT_TRIG (i=0-5)
TOMi TGC1 Internal Trigger Control Register($00823C_H$+i*800_H) **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_TRIG7		INT_TRIG6		INT_TRIG5		INT_TRIG4		INT_TRIG3		INT_TRIG2		INT_TRIG1		INT_TRIG0	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
INT_TRIGx (x=0-7)	2*x+1:2*x	rw	**Select input signal TRIG_x as a trigger source** Write / Read: 00_B Don't care, bits 1:0 will not be changed / internal trigger from channel 0 (TRIG_0) not used 01_B Do not use internal trigger from channel 0 (TRIG_0) / -- 10_B Use internal trigger from channel 0 (TRIG_0) / -- 11_B Don't care, bits 1:0 will not be changed / internal trigger from channel 0 (TRIG_0) used
0	31:16	r	**Reserved** Read as zero, shall be written as zero.

28.14.8.9 Register TOM[i]_CH[x]_CTRL

TOMi Channel x Control Register

TOMi_CHx_CTRL (i=0-5;x=0-15)

TOMi Channel x Control Register **(008000_H+i*800_H+x*40_H)** **Application Reset Value: 0000 0800_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FREEZE	**0**	**GCM**	**SPEM**	**BITREV**	**OSM**	**SPE_TRIG**	**TRIGOUT**	**EXTTRIGOUT**	**EXT_TRIG**	**OSM_TRIG**	**RST_CCU0**	**UDMODE**		**TRIG_PULSE**	**0**
rw	r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw		rw	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECLK_SRC	**CLK_SRC_SR**			**SL**	**0**			**SR0_TRIG**	**0**						
rw	rw			rw	r			rw	r						

Field	Bits	Type	Description
SR0_TRIG	7	rw	**SR0 is used to generate a trigger on output TOM[i]_CH[x]_OUT_T if equal to CN0** *Note: This bit should only be set if RST_CCU0 of this channel is 0.* 0_B SR0 is used as a shadow register for register CM0. 1_B SR0 is not used as a shadow register for register CM0. SR0 is compared with CN0 and if both are equal, a trigger pulse is generated at output TOM[i]_CH[x]_OUT_T.
SL	11	rw	**Signal level for duty cycle** If the output is disabled, the output TOM_OUT[x] is set to the inverse value of SL. Reset value depends on the hardware configuration chosen by silicon vendor. 0_B Low signal level 1_B High signal level

Field	Bits	Type	Description
CLK_SRC_SR	14:12	rw	**Clock source select for channel** The register CLK_SRC is updated with the value of CLK_SRC_SR together with the update of register CM0 and CM1. The input of the FX clock divider depends on the value of FXCLK_SEL (see CMU). *Note: This register is a shadow register for the register CLK_SRC. Thus, if the CMU_CLK source for PWM generation should be changed during operation, the old CMU_CLK has to operate until the update of the ATOM channels internal CLK_SRC register by the CLK_SRC_SR content is done either by an end of a period or a forced update.* *Note: If clock of channel is stopped (i.e. ECLK_SRC=0 and CLK_SRC=101_B/110_B/111_B), the channel can only be restarted by resetting CLK_SRC_SR to a value of 000_B to 100_B and forcing an update via the force update mechanism.* If ECLK_SRC=0 / ECLK_SRC=1: 000_B CMU_FXCLK (0) selected / CMU_FXCLK (0) selected 001_B CMU_FXCLK (1) selected / CMU_FXCLK (1) selected 010_B CMU_FXCLK (2) selected / CMU_FXCLK (2) selected 011_B CMU_FXCLK (3) selected / CMU_FXCLK (3) selected 100_B CMU_FXCLK (4) selected / CMU_FXCLK (4) selected 101_B Clock of channel stopped / TRIG[x-1] selected 110_B Clock of channel stopped / TIM_EXT_CAPTURE[x] selected 111_B Clock of channel stopped / reserved
ECLK_SRC	15	rw	**Extend CLK_SRC** 0_B CLK_SRC_SR set 1 selected (see bit CLK_SRC_SR) 1_B CLK_SRC_SR set 2 selected (see bit CLK_SRC_SR)
TRIG_PULSE	17	rw	**Trigger output pulse length of one SYS_CLK period** 0_B Output on TOM[i]_OUT[x]_T is 1 as long as CN0=SR0 (if SR=_TRIG=1) 1_B Output on TOM[i]_OUT[x]_T is 1 for only one SYS_CLK period if CN0=SR0 (if SR=_TRIG=1)
UDMODE	19:18	rw	**Up-down counter mode** 00_B Up-down counter mode disabled: CN0 counts always up 01_B Up-down counter mode enabled: CN0 counts up and down, CM0, CM1 are updated if CN0 reaches 0 (i.e. changes from down to up) 10_B Up-down counter mode enabled: CN0 counts up and down, CM0, CM1 are updated if CN0 reaches CM0 (i.e. changes from up to down) 11_B Up-down counter mode enabled: CN0 counts up and down, CM0, CM1 are updated if CN0 reaches 0 or CM0 (i.e. changes direction)

Field	Bits	Type	Description
RST_CCU0	20	rw	**Reset source of CCU0** *Note: On TOM channel 2, SPEM=1 has special meaning. If SPEM = 1, the signal SPE_NIPD triggers the reset of CN0 independent of RST_CN0.* *Note: This bit should only be set if bit OSM=0 (i.e. in continuous mode).* 0_B Reset counter register CN0 to 0 on matching comparison CM0 1_B Reset counter register CN0 to 0 on trigger TRIG_[x-1] or TIM_EXT_CAPTURE(x).
OSM_TRIG	21	rw	**Enable trigger of one-shot pulse by trigger signal OSM_TRIG** *Note: This bit should only be set if bit OSM=1 and bit RST_CCU0=0.* 0_B Signal OSM_TRIG cannot trigger start of single pulse generation 1_B Signal OSM_TRIG can trigger start of single pulse generation (only if bit OSM = 1)
EXT_TRIG	22	rw	**Select TIM_EXT_CAPTURE(x) as trigger signal** 0_B Signal TRIG_[x-1] is selected as trigger to reset CN0 or to start single pulse generation 1_B Signal TIM_EXT_CAPTURE(x) is selected
EXTTRIGOUT	23	rw	**TIM_EXT_CAPTURE(x) as potential output signal TRIG_[x]** 0_B Signal TRIG_[x-1] is selected as output on TRIG_[x] (if TRIGOUT=0) 1_B Signal TIM_EXT_CAPTURE(x) is selected as output on TRIG_[x] (if TRIGOUT=0)
TRIGOUT	24	rw	**Trigger output selection (output signal TRIG_[x]) of module TOM_CH[x]** 0_B TRIG_[x] is TRIG_[x-1] or TIM _EXT_CAPTURE(x) 1_B TRIG_[x] is TRIG_CCU0

Field	Bits	Type	Description
SPE_TRIG	25	rw	**SPE trigger to reset CN0** For TOM channel 2, 6 and 7, this bit defines, in combination with bit SPEM, the source of output pin TOM[i]_CH[x]_OUT, and if CN0 can be reset by TOM input signal SPE[i]_NIPD. *Note: For TOM channel 8 and 9, this bit defines only if CN0 reset is defined by input signal SPE[i]_NIPD or by configuration of RST_CCU0. The output TOM[i]_CH[x]_OUT is not affected. The configuration bit SPEM is not available for these channels, and thus assumed to be 0.* *Note: If a configuration of SPEM | SPE_TRIG = 0 | 1 or 1 | 0 is chosen (i.e. CN0 is reset by signal SPE[i]_NIPD), the one-shot mode in corresponding TOM channel should also be enabled by setting bit OSM=1 to generate one PWM pulse in case of trigger SPE[i]_NIPD.* *Note: In SPE module, one of the trigger signals TOM[i]_CH2_TRIG_CCU1, TOM[i]_CH6_TRIG_CCU1, TOM[i]_CH7_TRIG_CCU1, TOM[i]_CH8_TRIG_CCU1, or TOM[i]_CH9_TRIG_CCU1 can be used to trigger the update of register SPE[i]_OUT_CTRL.* If SPEM=0 / SPEM=1: 0_B TOM[i]_CH[x]_OUT defined by TOM[i] channel x SOUR register, CN0 reset is defined by configuration of bit RST_CCU0 / TOM[i]_CH[x]_OUT is defined by SPE[i]_OUT[x], CN0 is reset by signal SPE[i]_NIPD 1_B TOM[i]_CH[x]_OUT defined by TOM[i] channel x SOUR register, CN0 is reset by signal SPE[i]_NIPD / TOM[i]_CH[x]_OUT is defined by SPE[i]_OUT[x], CN0 reset is defined by configuration of bit RST_CCU0
OSM	26	rw	**One-shot mode** In this mode, the counter CN0 counts for only one period. The length of period is defined by CM0. A write access to the register CN0 triggers the start of counting. 0_B One-shot mode disabled 1_B One-shot mode enabled
BITREV	27	rw	**Bit-reversing of output of counter register CN0** *Note: This bit enables the PCM mode of channel 15.*

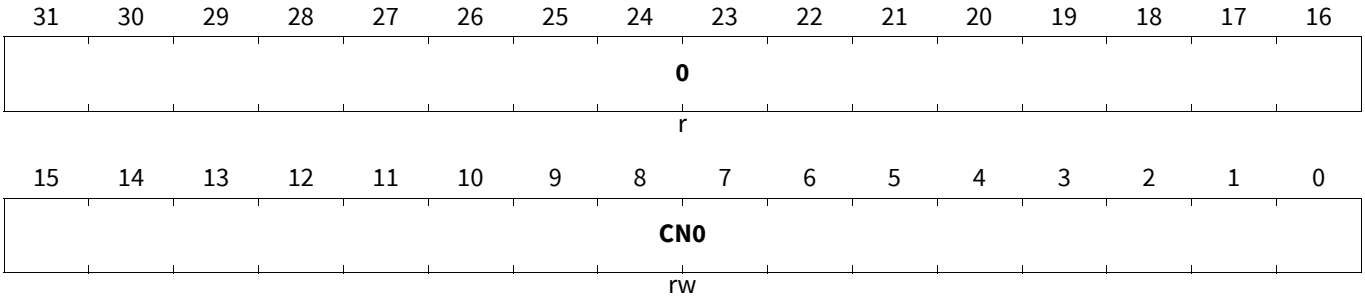
Field	Bits	Type	Description
SPEM	28	rw	**SPE output mode enable for channel** *Note: The SPE output mode is only implemented for TOM instances connected to an SPE module, and only for TOM channels 0 to 7.* *Note: For TOM channel 2, 6 and 7, this bit defines, in combination with bit SPE_TRIG, the source of output pin TOM[i]_CH[x]_OUT, and if CN0 can be reset by TOM input signal SPE[i]_NIPD.* 0_B SPE output mode disabled: TOM[i]_CH[x]_OUT defined by TOM[i] channel x SOUR register 1_B SPE output mode enabled: TOM[i]_CH[x]_OUT is defined by SPE[i]_OUT[x]
GCM	29	rw	**Gated Counter Mode enable** The Gated Counter mode is only available for TOM instances connected to an SPE module, and only for channels 0 to 7. 0_B Gated Counter mode disabled 1_B Gated Counter mode enabled
FREEZE	31	rw	**FREEZE** 0_B A channel disable/enable may change internal register and output register 1_B A channel enable/disable does not change an internal or output register, but stops counter CN0
0	6:0, 10:8, 16, 30	r	**Reserved** Read as zero, shall be written as zero.

28.14.8.10Register TOM[i]_CH[x]_CN0

TOMi Channel x CCU0 Counter Register

TOMi_CHx_CN0 (i=0-5;x=0-15)

TOMi Channel x CCU0 Counter Register (008014_H+i*800_H+x*40_H) **Application Reset Value: $0000\ 0000_H$**



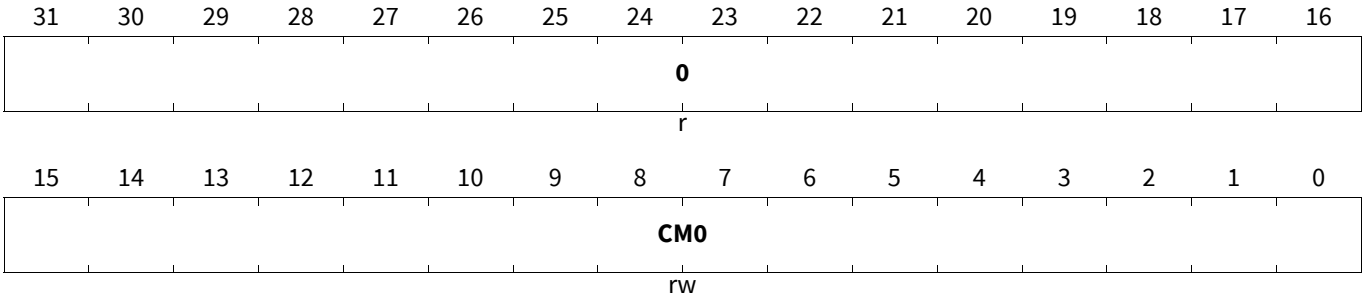
Field	Bits	Type	Description
CN0	15:0	rw	**TOM CCU0 counter register** This counter is stopped if the TOM channel is disabled and not reset on an enable event of TOM channel.

Field	Bits	Type	Description
0	31:16	r	**Reserved** Read as zero, shall be written as zero

28.14.8.11Register TOM[i]_CH[x]_CM0

TOMi Channel x CCU0 Compare Register

TOMi_CHx_CM0 (i=0-5;x=0-15)
TOMi Channel x CCU0 Compare Register($00800C_H$+i*800_H+x*40_H) **Application Reset Value: 0000 0000_H**

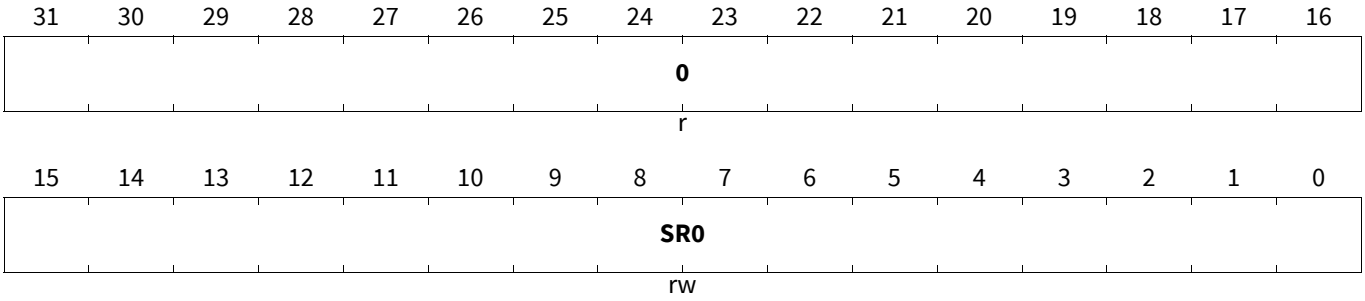


Field	Bits	Type	Description
CM0	15:0	rw	**TOM CCU0 compare register** Setting CM0 < CM1 configures a duty cycle of 100%.
0	31:16	r	**Reserved** Read as zero, shall be written as zero

28.14.8.12Register TOM[i]_CH[x]_SR0

TOMi Channel x CCU0 Compare Shadow Register

TOMi_CHx_SR0 (i=0-5;x=0-15)
TOMi Channel x CCU0 Compare Shadow Register(008004_H+i*800_H+x*40_H) **Application Reset Value: 0000 0000_H**



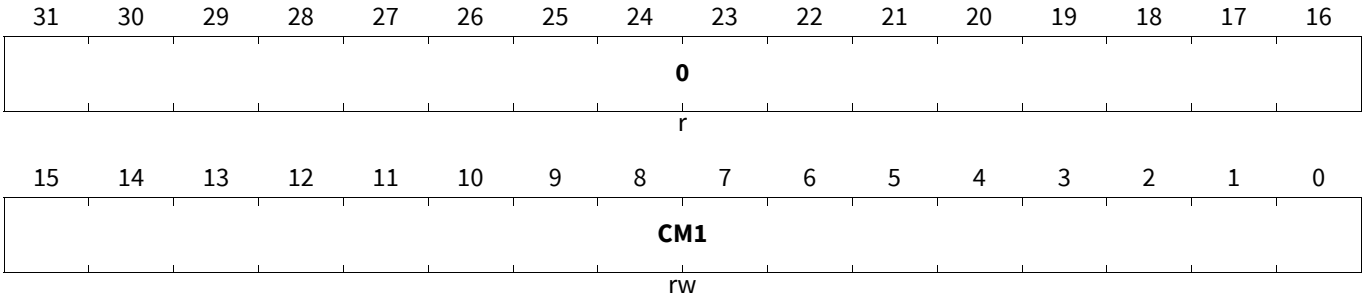
Field	Bits	Type	Description
SR0	15:0	rw	**TOM channel x shadow register SR0 for update of compare register CM0**

Field	Bits	Type	Description
0	31:16	r	**Reserved** Read as zero, shall be written as zero.

28.14.8.13Register TOM[i]_CH[x]_CM1

TOMi Channel x CCU1 Compare Register

TOMi_CHx_CM1 (i=0-5;x=0-15)
TOMi Channel x CCU1 Compare Register(008010_H+i*800_H+x*40_H) **Application Reset Value: 0000 0000_H**

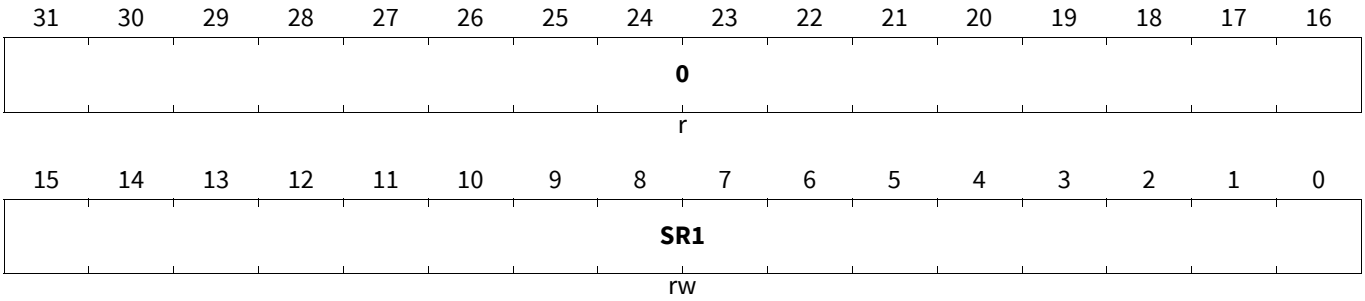


Field	Bits	Type	Description
CM1	15:0	rw	**TOM CCU1 compare register** Setting CM1 = 0 configures a duty cycle of 0%, independent of the configured value of CM0.
0	31:16	r	**Reserved** Read as zero, shall be written as zero

28.14.8.14Register TOM[i]_CH[x]_SR1

TOMi Channel x CCU1 Compare Shadow Register

TOMi_CHx_SR1 (i=0-5;x=0-15)
TOMi Channel x CCU1 Compare Shadow Register(008008_H+i*800_H+x*40_H) **Application Reset Value: 0000 0000_H**



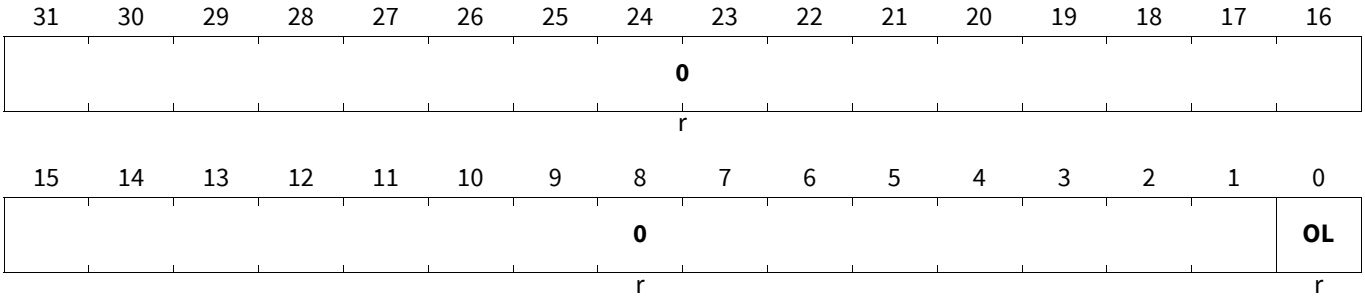
Field	Bits	Type	Description
SR1	15:0	rw	**TOM channel x shadow register SR1 for update of compare register CM1**

Field	Bits	Type	Description
0	31:16	r	**Reserved** Read as zero, shall be written as zero

28.14.8.15Register TOM[i]_CH[x]_STAT

TOMi Channel x Status Register

TOMi_CHx_STAT (i=0-5;x=0-15)
TOMi Channel x Status Register **(008018_H+i*800_H+x*40_H)** **Application Reset Value: 0000 0000_H**

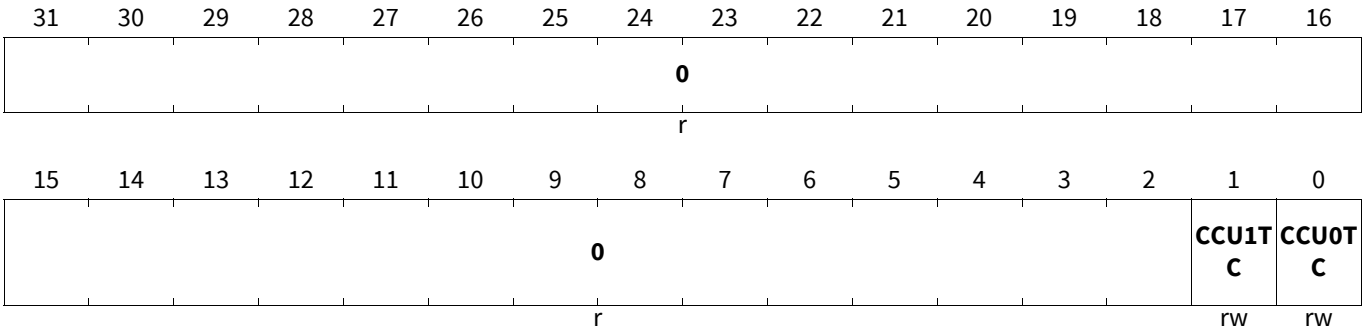


Field	Bits	Type	Description
OL	0	r	**Output level of output TOM_OUT(x)** Reset value is the inverted value of SL bit, which depends on the hardware configuration chosen by silicon vendor.
0	31:1	r	**Reserved** Read as zero, shall be written as zero

28.14.8.16Register TOM[i]_CH[x]_IRQ_NOTIFY

TOMi Channel x Interrupt Notification Register

TOMi_CHx_IRQ_NOTIFY (i=0-5;x=0-15)
TOMi Channel x Interrupt Notification Register($00801C_H$+i*800_H+x*40_H) **Application Reset Value: 0000 0000_H**



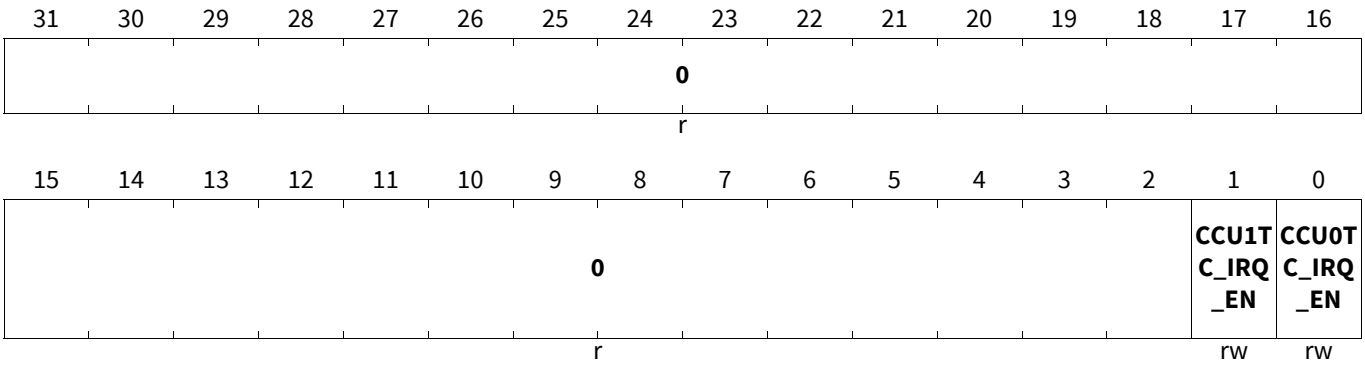
Field	Bits	Type	Description
CCU0TC	0	rw	**CCU0 Trigger condition interrupt for channel x** The notification of the interrupt is only triggered one time after reaching the condition CN0 >= CM0. To enable re-trigger of the notification, first the condition CN0 < CM1 has to be reached. *Note: This bit will be cleared on a CPU write access of value 1. A read access leaves the bit unchanged.* 0_B No interrupt occurred 1_B The condition CN0 >= CM0 was detected
CCU1TC	1	rw	**CCU1 Trigger condition interrupt for channel x** The notification of the interrupt is only triggered one time after reaching the condition CN0 >= CM1. To enable re-trigger of the notification, first the condition CN0 < CM1 has to be reached. *Note: This bit will be cleared on a CPU write access of value 1. A read access leaves the bit unchanged.* 0_B No interrupt occurred 1_B The condition CN0 >= CM1 was detected (if SR0_TRIG=0) / the condition SR0=CN0 was detected (if SR0_TRIG=1)
0	31:2	r	**Reserved** Read as zero, shall be written as zero.

28.14.8.17Register TOM[i]_CH[x]_IRQ_EN

TOMi Channel x Interrupt Enable Register

TOMi_CHx_IRQ_EN (i=0-5;x=0-15)

TOMi Channel x Interrupt Enable Register(008020_H+i*800_H+x*40_H) **Application Reset Value: 0000 0000_H**



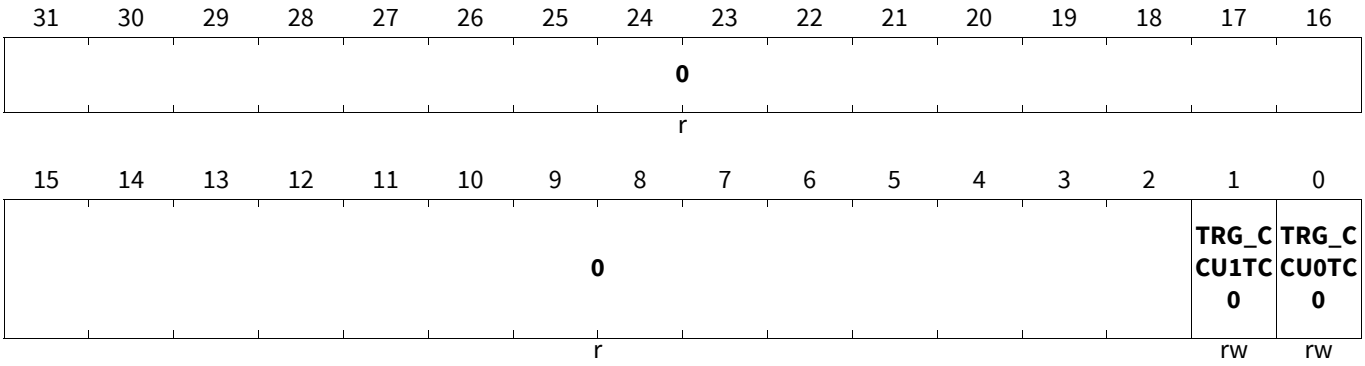
Field	Bits	Type	Description
CCU0TC_IRQ_EN	0	rw	**TOM_CCU0TC_IRQ interrupt enable** 0_B Disable interrupt, interrupt is not visible outside GTM 1_B Enable interrupt, interrupt is visible outside GTM
CCU1TC_IRQ_EN	1	rw	**TOM_CCU1TC_IRQ interrupt enable** Coding see bit 0.
0	31:2	r	**Reserved** Read as zero, shall be written as zero.

28.14.8.18Register TOM[i]_CH[x]_IRQ_FORCINT

TOMi Channel x Force Interrupt Register

TOMi_CHx_IRQ_FORCINT (i=0-5;x=0-15)

TOMi Channel x Force Interrupt Register(008024_H+i*800_H+x*40_H) **Application Reset Value: 0000 0000_H**



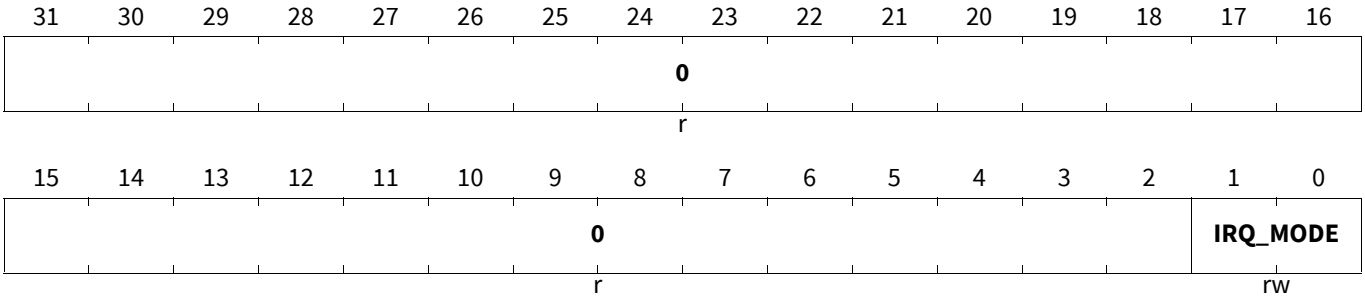
Field	Bits	Type	Description
TRG_CCU0TC0	0	rw	**Trigger TOM_CCU0TC0_IRQ interrupt by software** This bit is cleared automatically after write. This bit is write protected by bit RF_PROT of register GTM_CTRL 0_B No interrupt triggering 1_B Assert CCU0TC0_IRQ interrupt for one clock cycle
TRG_CCU1TC0	1	rw	**Trigger TOM_CCU1TC0_IRQ interrupt by software** This bit is cleared automatically after write. This bit is write protected by bit RF_PROT of register GTM_CTRL. 0_B No interrupt triggering 1_B Assert CCU1TC0_IRQ interrupt for one clock cycle
0	31:2	r	**Reserved** Read as zero, shall be written as zero.

28.14.8.19Register TOM[i]_CH[x]_IRQ_MODE

TOMi Channel x Interrupt Mode Register

TOMi_CHx_IRQ_MODE (i=0-5;x=0-15)

TOMi Channel x Interrupt Mode Register(008028_H+i*800_H+x*40_H) **Application Reset Value: 0000 0000_H**



Field	Bits	Type	Description
IRQ_MODE	1:0	rw	**IRQ mode selection** The interrupt modes are described in **Section 28.4.5**. 00_B Level mode 01_B Pulse mode 10_B Pulse-Notify mode 11_B Single-Pulse mode
0	31:2	r	**Reserved** Read as zero, shall be written as zero