28.9 FIFO to ARU Unit (F2A)

28.9.1 Overview

The F2A is the interface between the ARU and the FIFO sub-module. Since the data width of the ARU (ARU word) is 53 bit (two 24 bit values and five control bits) and the data width of the FIFO is only 29 bit, the F2A has to distribute the data from and to the FIFO channels in a configurable manner.

The data transfer between FIFO and ARU is organized with eight different streams that are connected to the eight different channels of the corresponding FIFO module. A stream represents a data flow from/to ARU to/from the FIFO via the F2A.

The general definition of 'channels' and 'streams' in the ARU context is done in the subparagraph “ARU routing concept”.

Each FIFO channel can act as a write stream (data flow from FIFO to ARU) or as a read stream (data flow from ARU to FIFO).

Within these streams the F2A can transmit/receive the lower, the upper or both 24 bit values of the ARU together with the ARU control bits according to the configured transfer modes as described in **Section 28.9.2**.

Each stream can be enabled/disabled separately within the register **F2A[i]_ENABLE**. If a stream will be disabled, the stream data which are stored inside the F2A will be deleted. This is necessary to ensure, that no old data are transferred after enabling a stream.

28.9.2 Transfer modes

The F2A unit provides several transfer modes to map 29 bit data of the FIFO from/to 53 bit data of the ARU. E.g. it is configurable that the 24 bit FIFO data is written to the lower ARU data entry (means bits 0 to 23) or to the higher 24 bit ARU data entry (means bits 24 to 47). Bits 24 to 28 of the FIFO data entry (the five control bits) are written/read in both cases to/from bits 48 to 52 of the ARU entry.

When both values of the ARU have to be stored in the FIFO the values are stored behind each other inside the FIFO if the FIFO is not full.

If there is only space for one 24 bit data word plus the five control bits, the F2A transfers one part of the 53 bits first and then waits for transferring the second part before new data is requested from the ARU.

When two values from the FIFO have to be written to one ARU location the words have to be located behind each other inside the FIFO.

The transfer to ARU is only established when both parts could be read out of the FIFO otherwise if only one 29 bit word was provided by the FIFO the F2A waits until the second part is available before the data is made available at the ARU.

Figure 25 shows the data ordering of the FIFO when both ARU values must be transferred between ARU and FIFO.

When reading from the ARU the F2A first writes the lower word to the FIFO.

In case of writing to the ARU the F2A reads the lower word first from the FIFO, thus the lower word must be written first to the FIFO through the AFD interface.

Please note, that the five control bits (bits 48 to 52 of the ARU data word) are duplicated as bit 24 to 28 of both FIFO words in case of reading from ARU.

In the case of writing to the ARU, bits 24 to 28 of the last written FIFO word (the higher ARU word) are copied to bits 48 to 52 of the corresponding ARU location.

The transfer modes can be configured with the **TMODE** bits of registers **F2A[i]_CH[x]_STR_CFG**.

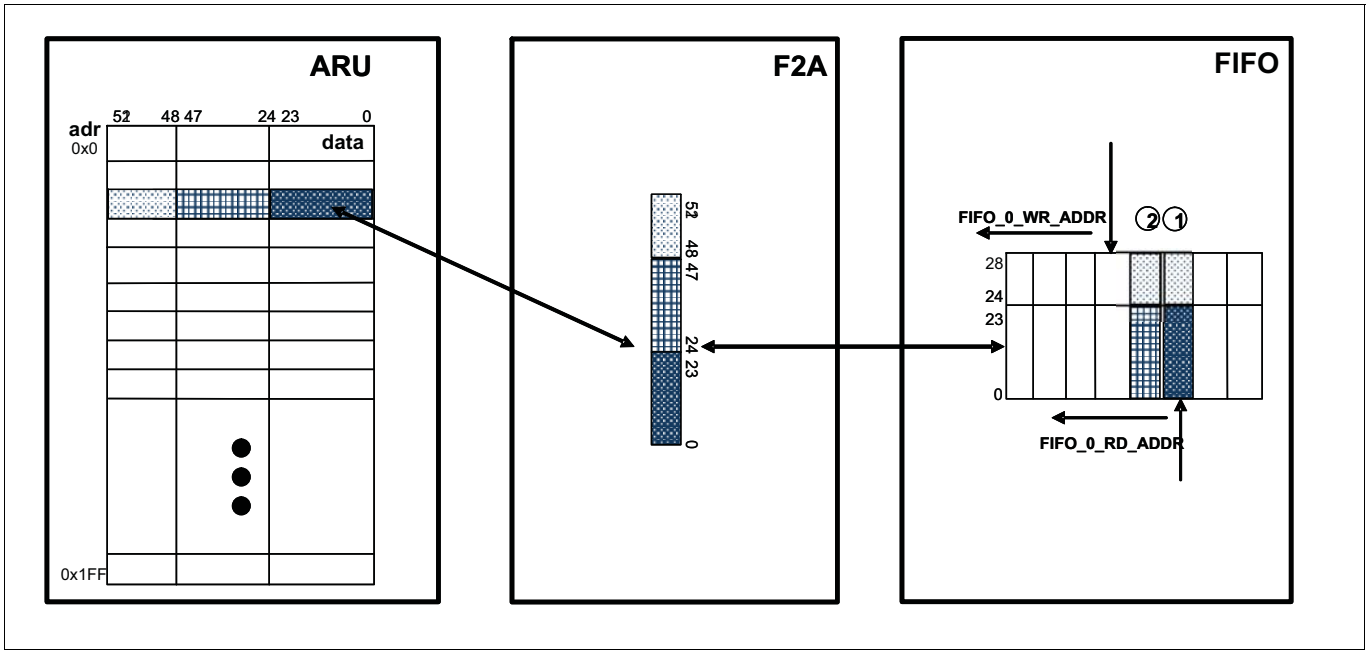


Figure 25 Data transfer of both ARU words between ARU and FIFO

28.9.3 Internal buffer mode

It is possible to use a FIFO channel as a buffer which is accessed only internally from ARU side. To do this, a read and a write stream of the F2A to one FIFO channel are needed. Therefore it is possible to reconfigure the upper 4 F2A streams 4…7 to the lower 4 FIFO channels 0…3 in the following manner:

- F2A stream 4 (+ F2A stream 0) -> FIFO channel 0
- F2A stream 5 (+ F2A stream 1) -> FIFO channel 1
- F2A stream 6 (+ F2A stream 2) -> FIFO channel 2
- F2A stream 7 (+ F2A stream 3) -> FIFO channel 3

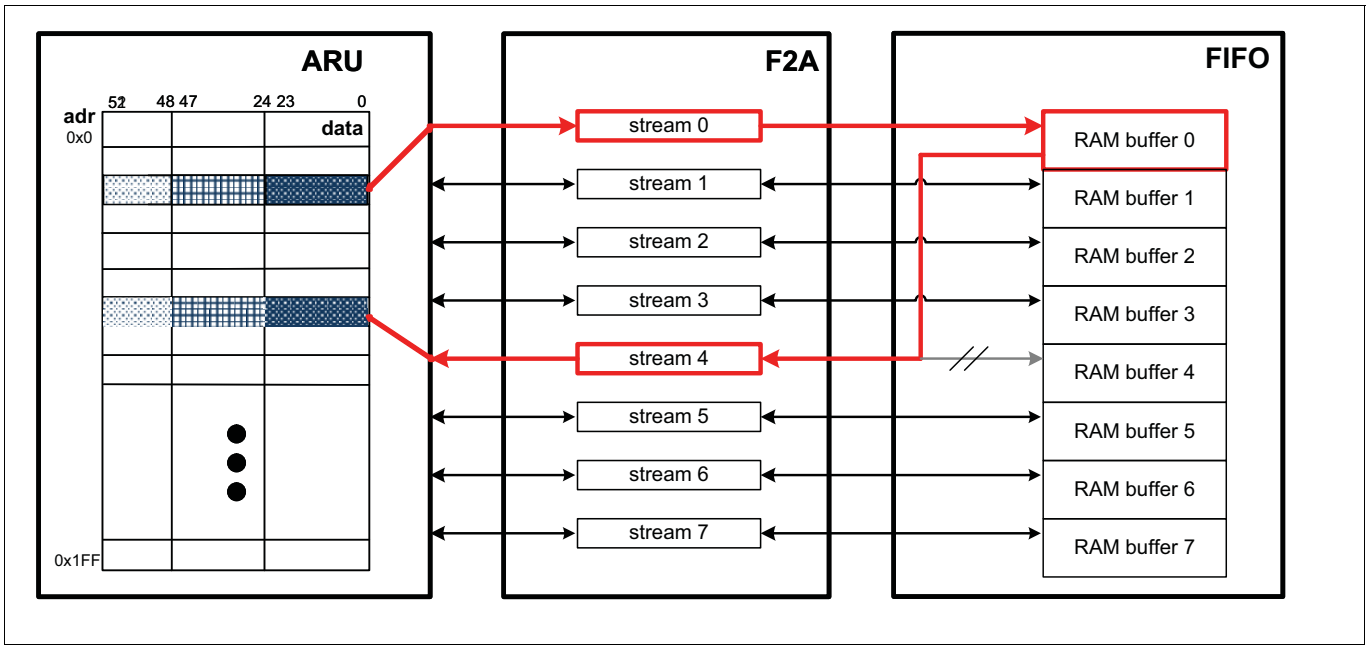


Figure 26 Re-configuration of F2A stream 4 to FIFO channel 0

The configuration of each 4 upper F2A streams can be done separately for each stream in the configuration register **F2A[i]_CTRL**.

Note that the corresponding upper FIFO channel (4…7) cannot be used in this configuration.

28.9.4 F2A Configuration Register Overview

Table 24 F2A Configuration Register Overview

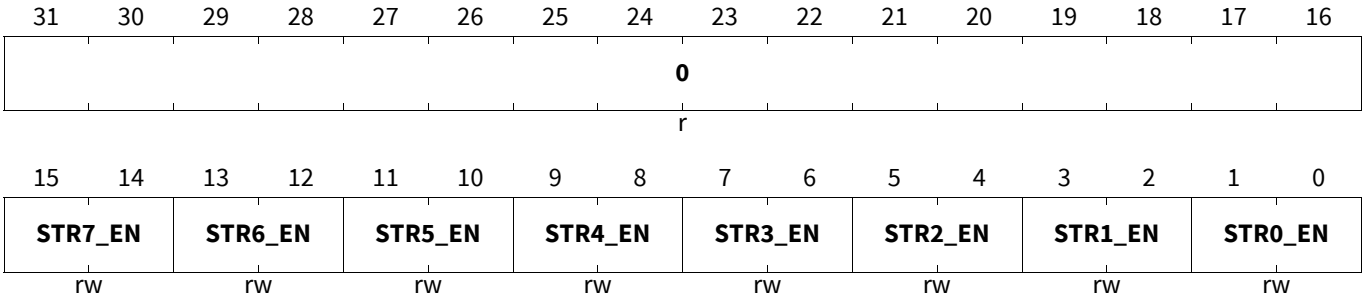
Register name	Description	see Page
F2A[i]_ENABLE	F2Ai stream activation register	99
F2A[i]_CH[z]_ARU_RD_FIFO	F2Ai channel z read address register	99
F2A[i]_CH[z]_STR_CFG	F2Ai stream z configuration register	100
F2A[i]_CTRL	F2Ai stream control register	101

28.9.5 F2A Configuration Register description

28.9.5.1 Register F2A[i]_ENABLE

F2Ai Stream Activation Register

F2Ai_ENABLE (i=0-2)
F2Ai Stream Activation Register **(018040_H+i*4000_H)** **Application Reset Value: 0000 0000_H**

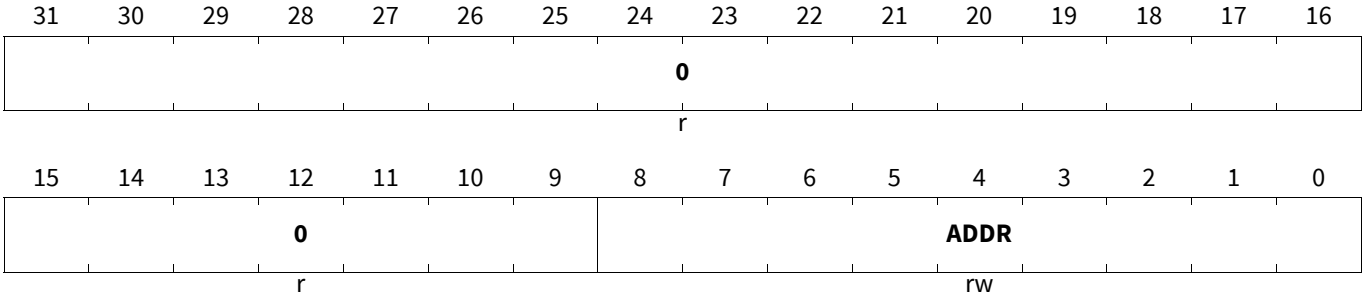


Field	Bits	Type	Description
STRx_EN (x=0-7)	2*x+1:2*x	rw	**Enable/disable stream x** Write of following double bit values is possible: 00_B Write: Don't care, bits 1:0 will not be changed / Read: Stream disabled 01_B Stream 0 is disabled and internal states are reset 10_B Stream 0 is enabled 11_B Write: Don't care, bits 1:0 will not be changed / Read: Stream enabled
0	31:16	r	**Reserved** Read as zero, shall be written as zero.

28.9.5.2 Register F2A[i]_CH[z]_ARU_RD_FIFO

F2Ai Stream z Read Address Register

F2Ai_CHz_ARU_RD_FIFO (i=0-2;z=0-7)
F2Ai Stream z Read Address Register **(018000_H+i*4000_H+z*4)** **Application Reset Value: 0000 $01FE_H$**



Field	Bits	Type	Description
ADDR	8:0	rw	**ARU Read address** This bit field is only writable if channel is disabled.
0	31:9	r	**Reserved** Read as zero, shall be written as zero

28.9.5.3 Register F2A[i]_CH[z]_STR_CFG

F2Ai Stream z Configuration Register

Note: The write protected bits of register **F2A_CH[z]_STR_CFG** are only writable if the corresponding enable bit STRx_EN of register **F2A_ENABLE** is cleared.

F2Ai_CHz_STR_CFG (i=0-2;z=0-7)
F2Ai Stream z Configuration Register **(018020_H+i*4000_H+z*4)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0													DIR	TMODE	
r													rw	rw	

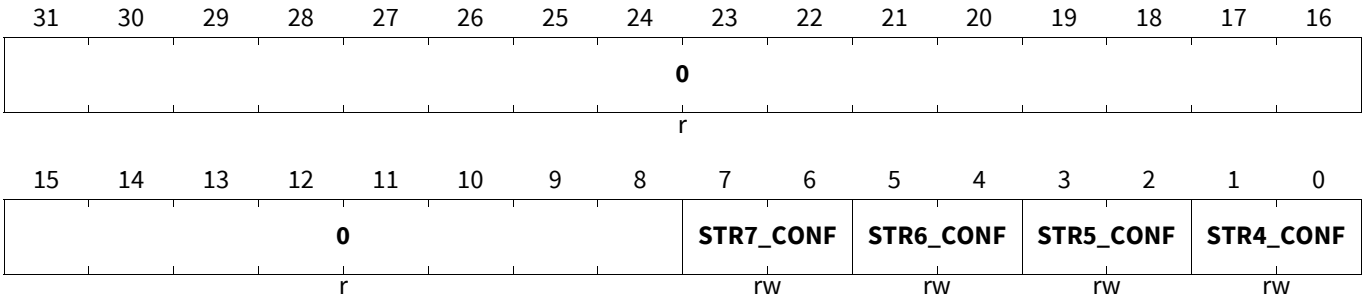
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0															
r															

Field	Bits	Type	Description
TMODE	17:16	rw	**Transfer mode for 53 bit ARU data from/to FIFO** 00_B Transfer low word (ARU bits 23:0) from/to FIFO 01_B Transfer high word (ARU bits 47:24) from/to FIFO 10_B Transfer both words from/to FIFO 11_B Reserved
DIR	18	rw	**Data transfer direction** 0_B Transport from ARU to FIFO 1_B Transport from FIFO to ARU
0	15:0, 31:19	r	**Reserved** Read as zero, shall be written as zero

28.9.5.4 Register F2A[i]_CTRL

F2Ai Stream Control Register

F2Ai_CTRL (i=0-2)
F2Ai Stream Control Register **(018044_H+i*4000_H)** **Application Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
STR4_CONF	1:0	rw	**Reconfiguration of stream 4 to FIFO channel 0** Write of following double bit values is possible: The write protected bits of register **F2A[i]_CTRL** are only writable if the corresponding enable bit STR0_EN and STR4_EN of register **F2A_ENABLE** is cleared. 00_B Write: don't care, bits 1:0 will not be changed / Read: Stream 4 is mapped to FIFO buffer 4 01_B Stream 4 is mapped to FIFO buffer 4 10_B Stream 4 is mapped to FIFO buffer 0 11_B Write: don't care, bits 1:0 will not be changed / Read: Stream 4 is mapped to FIFO buffer 0
STR5_CONF	3:2	rw	**Reconfiguration of stream 5 to FIFO channel 1** Write of following double bit values is possible: The write protected bits of register **F2A[i]_CTRL** are only writable if the corresponding enable bit STR1_EN and STR5_EN of register **F2A_ENABLE** is cleared. 00_B Write: don't care, bits 1:0 will not be changed / Read: Stream 5 is mapped to FIFO buffer 5 01_B Stream 5 is mapped to FIFO buffer 5 10_B Stream 5 is mapped to FIFO buffer 1 11_B Write: don't care, bits 1:0 will not be changed / Read: Stream 5 is mapped to FIFO buffer 1