33.12 Resolver Support

Resolver applications determine the rotation angle by evaluating the signals from two orthogonally placed coils. These coils are excited by the magnetic field of a third coil.
Several features are available to support these applications by offering the almost complete interface hardware (except for power stages) and by preprocessing the input data (rectification, integration) to optimize evaluation by higher level software algorithms.

33.12.1 Resolver System Overview

The EDSADC can read the two return signals using two input channels and can also generate the excitation sine signal (carrier). It also provides synchronization logic to compensate the delay between the generated carrier signal and the received position signals. The integrator stage converts the carrier-based return signals to position-based values (carrier cancellation).

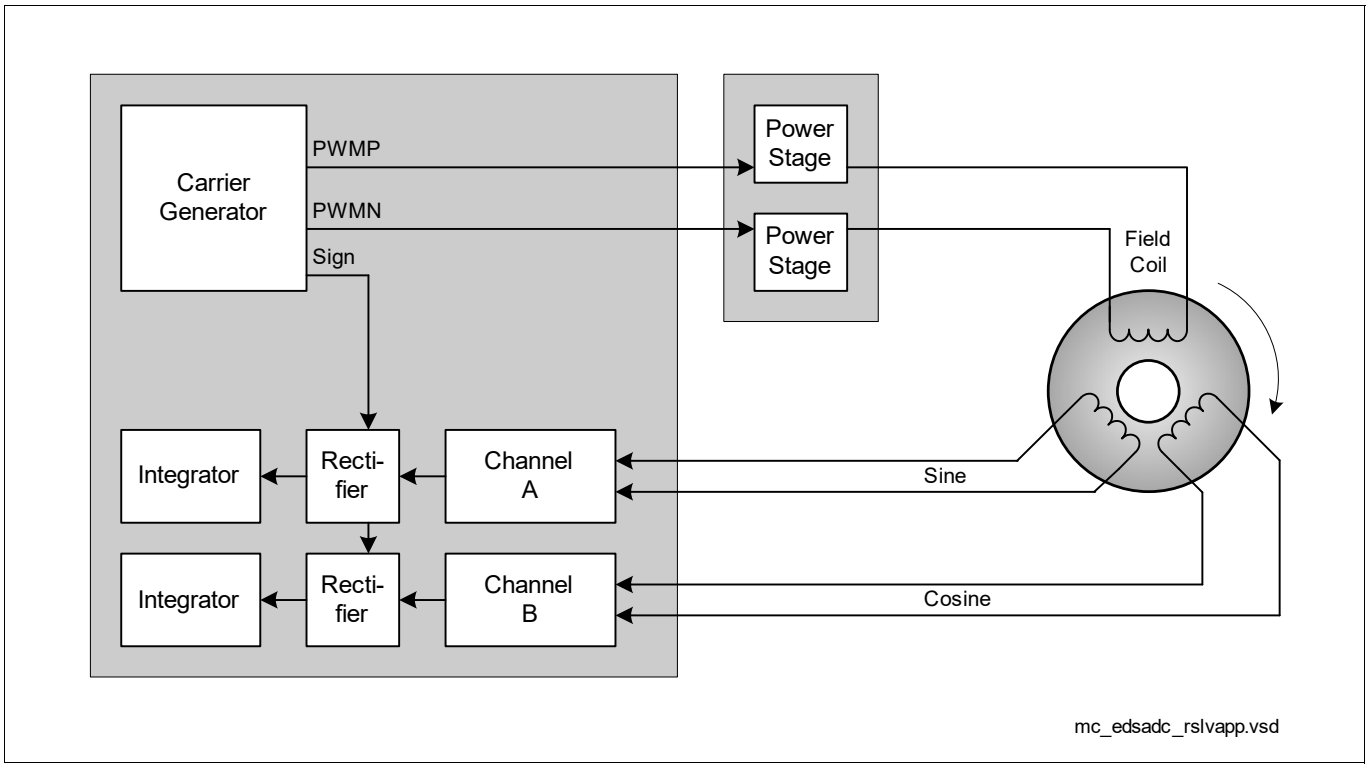

Figure 320 Resolver Application

33.12.2 Carrier Signal Generation

The carrier signal generator (CG) is supplied with the module clock signal and outputs a PWM signal that induces a sine signal in the excitation coil of the resolver. Alternatively, it can generate PWM patterns that resemble triangle or square signals (see **Figure 322**). The polarity of the carrier signal can be selected.

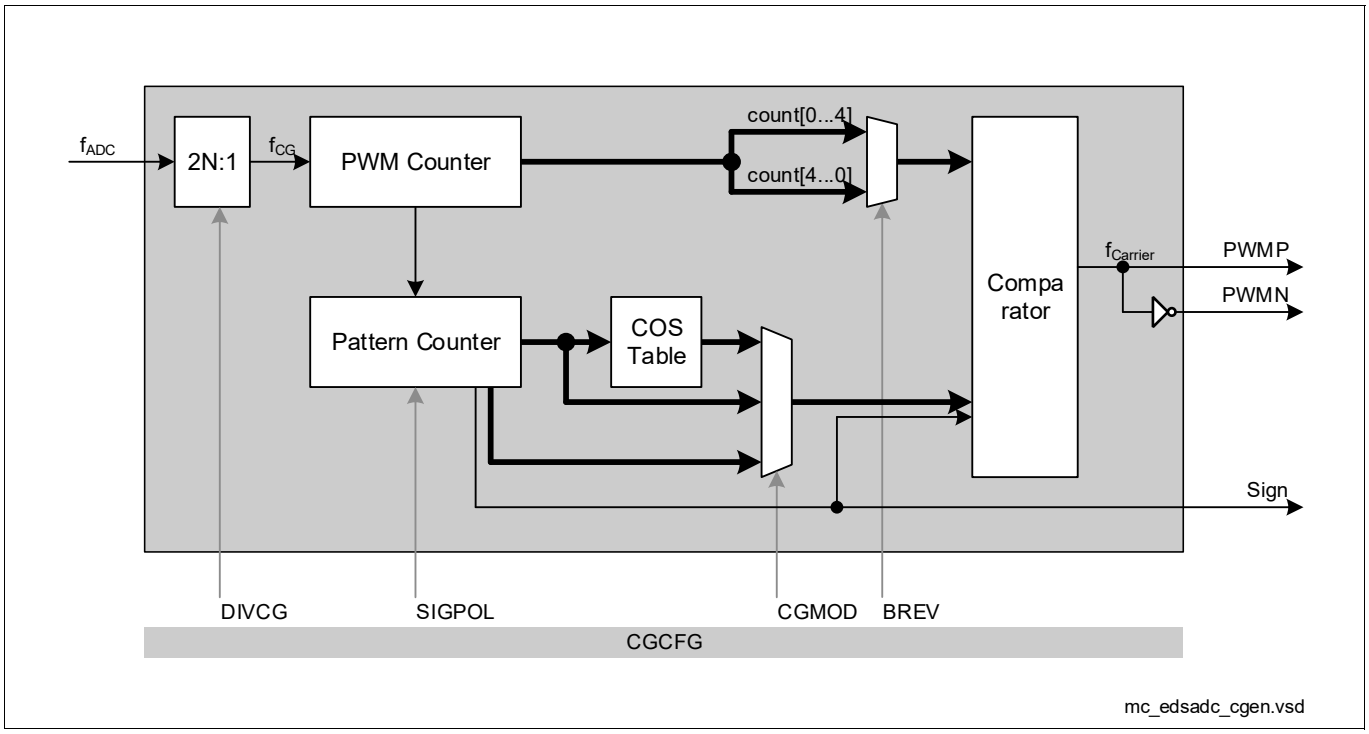

Figure 321 Carrier Generator Block Diagram

A carrier signal period consists of 32 steps. Each step equals a PWM period of 32 cycles.

Bit-reverse generation mode increases the frequency spectrum to yield a smoother induced sine signal. This is done by distributing the 0 and 1 bits over the 32 cycles of a PWM period.

The generated pattern is actually a cosine signal, i.e. it starts at the maximum output value. This is advantageous if the output pin is pulled high before the carrier signal is generated. In case of a pull-down the inverted output signal should be selected.

Note: All configurations become effective, when the carrier generator is started.

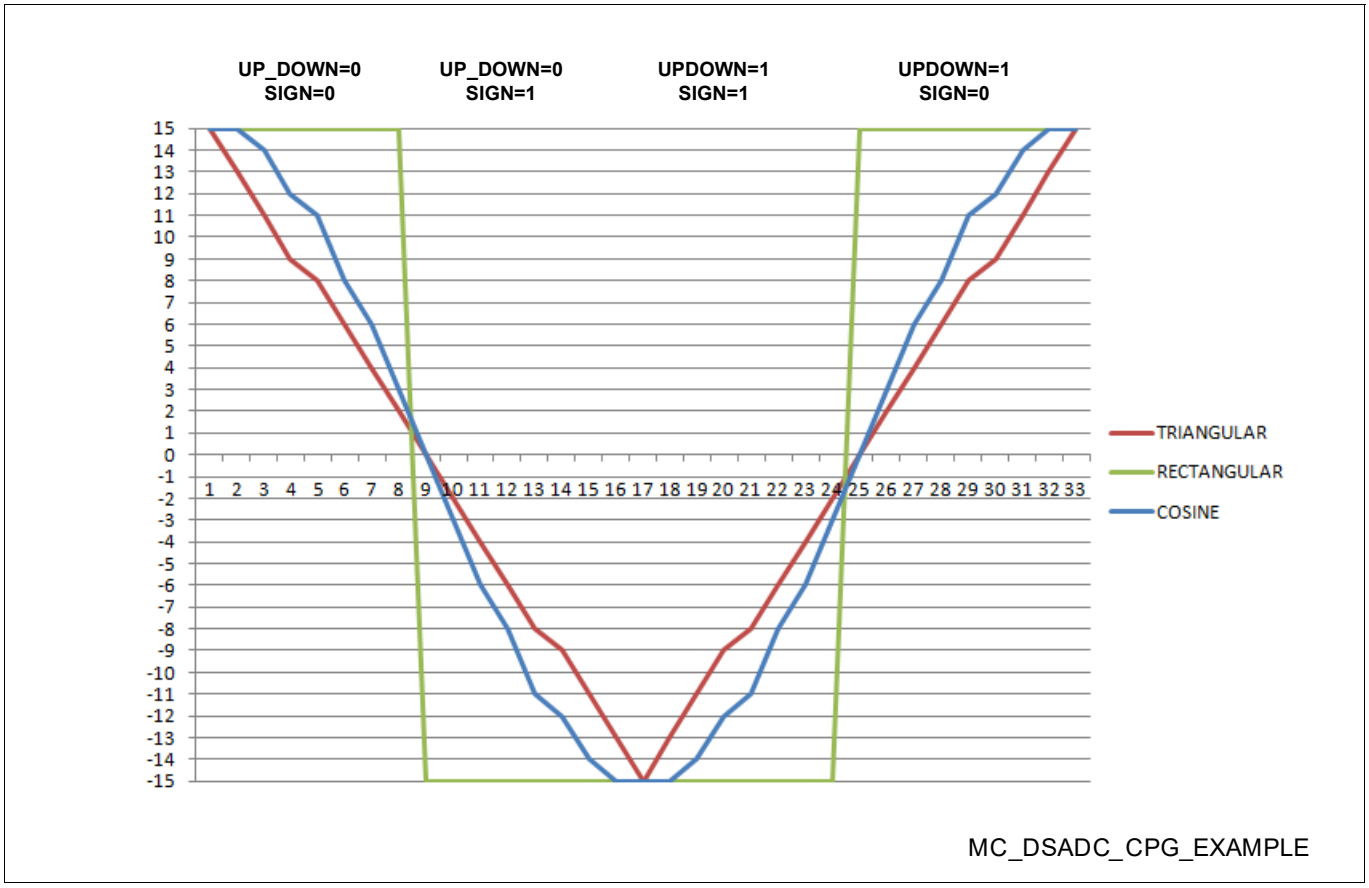

Figure 322 Example Pattern/Waveform Outputs

Carrier Generator Configuration Register

Note: The current position within a carrier signal period is indicated by bitfields STEPD, STEPS and STEPCOUNT.

CGCFG

Carrier Generator Configuration Register (00A0$_H$) Application Reset Value: 0710 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	SGNCG	STEPD	STEPS	0	STEPCOUNT			0			BITCOUNT				
r	rh	rh	rh	r	rh			r			rh				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RUN	0							DIVCG				SIGPOL	BREV	CGMOD	
rh	r							rw				rw	rw	rw	

Field	Bits	Type	Description
CGMOD	1:0	rw	**Carrier Generator Operating Mode** Stopping the carrier generator (CGMOD = 00_B) terminates the PWM output after completion of the current period (indicated by bit RUN = 0). 00_B Stopped 01_B Square wave 10_B Triangle 11_B Sine wave
BREV	2	rw	**Bit-Reverse PWM Generation** 0_B Normal mode 1_B Bit-reverse mode
SIGPOL	3	rw	**Signal Polarity** 0_B Normal: carrier signal begins with +1 1_B Inverted: carrier signal begins with -1
DIVCG	7:4	rw	**Divider Factor for the PWM Pattern Signal Generator** Defines the input frequency of the carrier signal generator, derived from the selected internal clock source: $f_{CG} = f_{ADC}$ / CGP. *Note: The frequency of the carrier signal itself is f_{CG} / 1024.* 0_H CGP = 2 … F_H CGP = 32
RUN	15	rh	**Run Indicator** 0_B Stopped (cleared at the end of a period) 1_B Running
BITCOUNT	20:16	rh	**Bit Counter** Counts the 32 cycles generated for each step
STEPCOUNT	26:24	rh	**Step Counter** Counts the 8 steps generated for each quadrant of the carrier signal period
STEPS	28	rh	**Step Counter Sign** Indicates the sign of the step counter value 0_B Step counter value is positive 1_B Step counter value is negative
STEPD	29	rh	**Step Counter Direction** 0_B Step counter is counting down 1_B Step counter is counting up
SGNCG	30	rh	**Sign Signal from Carrier Generator** 0_B Positive values 1_B Negative values
0	14:8, 23:21, 27, 31	r	**Reserved, write 0, read as 0**

33.12.3 Return Signal Synchronization

In a resolver, the received return signals are induced by the carrier signal and their amplitudes are modulated with the sine and cosine magnitudes corresponding to the current resolver position. These amplitudes are determined by integrating the return signals over a carrier signal period.

To properly integrate their magnitude, the return signals must be rectified. For this purpose the carrier generator provides the sign information of the generated carrier signal (SGNCG in register **CGCFG**).

Alternatively, an external carrier signal generator can be used. If this generator delivers a sign signal, this can be input to a pin and is then used as external carrier sign signal. If no sign signal is available, the carrier signal itself can be converted by another input channel (SSCH in register **RECTCFGx (x=0-13)**) and its sign signal is then used as alternate carrier sign signal.

The rectification of the received signals must be delayed to compensate the round trip delay through the system (driver, resolver coils, cables, etc.). For the rectification, the received values are multiplied with the delayed carrier sign signal (SGND in register **RECTCFGx (x=0-13)**). This synchronization is done for each channel separately, to achieve the maximum possible amplitudes for each signal.

Note: The rectification unit is part of the integrator stage. Therefore, it is only active while the integrator is active.

The delay is realized with the sign delay counter SDCOUNT. SDCOUNT is cleared and started upon a falling edge of the carrier's sign signal (SGNCS), i.e. at the begin of the positive halfwave of the carrier signal. After counting SDPOS results from the filter chain, also the rectification signal (SGND) is cleared, indicating positive values from now on. After counting SDNEG values, the rectification signal is set, indicating negative values (see also **Figure 323**).

The compare values SDPOS and SDNEG are stored by the application software. SDPOS is the delay value that accounts for the resolver signal's round trip delay. This delay is constantly measured by capturing the current counter value into bitfield SDCAP when the first positive result (after negative results) is received in the respective channel. Software can read these value and compute a delay value e.g. by averaging a series of measured values to compensate noise. The delay for the negative halfwave (SGND = 0) is determined by adding the duration of a carrier signal halfwave. This value is written to bitfield SDNEG.

A new captured value is indicated by setting the flag SDCVAL. This flag is cleared when reading register CGSYNCx.

Capturing a new value can trigger a service request. The alternate service request line is used for this purpose. This alternate request source is selected by bitfield SRGA in register **FCFGMx (x=0-13)**.

Note: When the filter chain is initialized, bitfields SGND, SDCVAL, SDCAP and SDCOUNT are cleared.

Carrier Generator Synchronization Reg. x

CGSYNCx (x=0-13)

Carrier Generator Synchronization Reg. x (01A0$_H$+x*100$_H$) Application Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SDNEG								SDPOS							
rw								rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDCAP								SDCOUNT							
rh								rh							

Field	Bits	Type	Description
SDCOUNT	7:0	rh	**Sign Delay Counter** Counts the result values from the filter chain to delay the carrier sign signal
SDCAP	15:8	rh	**Sign Delay Capture Value** Indicates the result values counted between the begin of the positive halfwave of the carrier signal and the first received positive value.
SDPOS	23:16	rw	**Sign Delay Value for Positive Halfwave** Defines the content of SDCOUNT to generate a negative delayed sign signal (SGND).
SDNEG	31:24	rw	**Sign Delay Value for Negative Halfwave** Defines the content of SDCOUNT to generate a positive delayed sign signal (SGND).

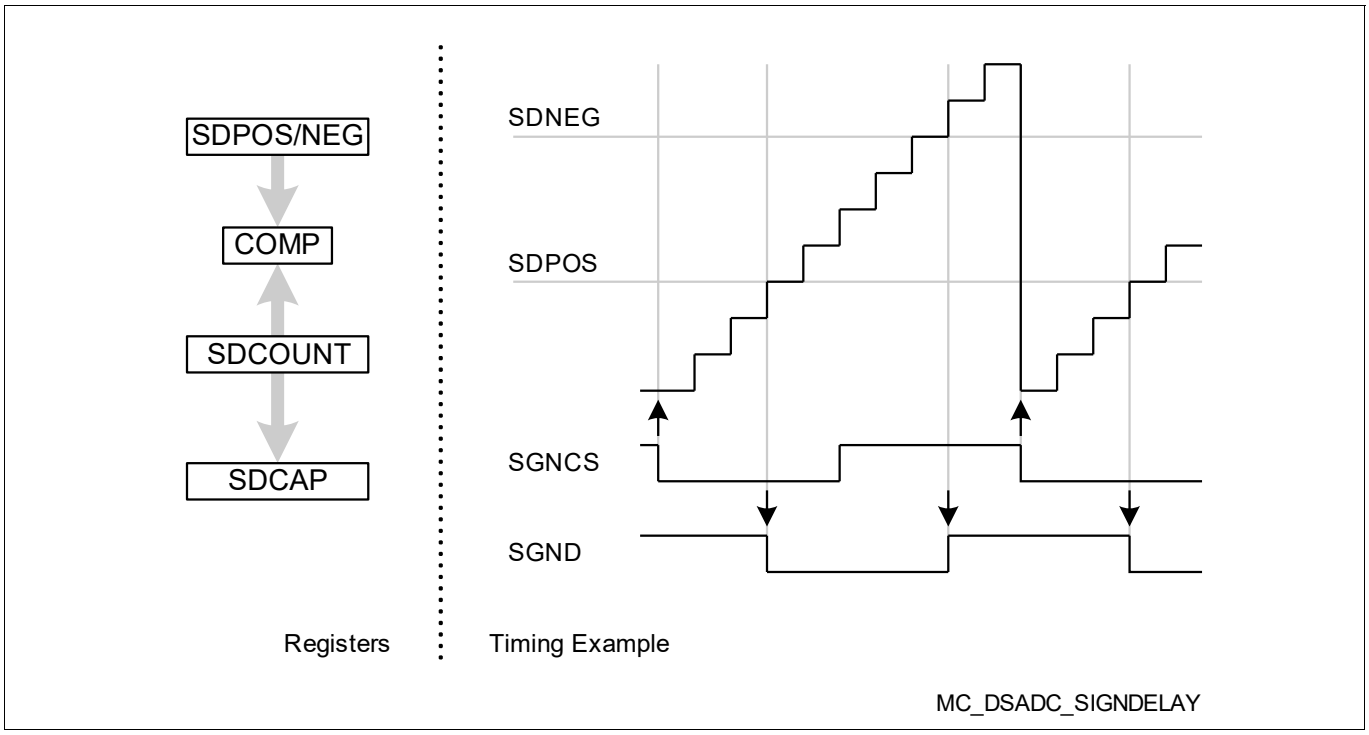

Figure 323 Sign Delay Example

Note: Whenever a new result value becomes available from the filter chain, the rectification counter is updated and the rectified value is forwarded to the integrator.

Rectification Configuration Register x

RECTCFGx (x=0-13)

Rectification Configuration Register x **($01A8_H$+x*100_H)** **Application Reset Value: 8000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SGND	SGNCS	0													
rh	rh	r													

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDCVAL	0			SSCH				0		SSRC		0			RFEN
rh	r			rw				r		rw		r			rw

Field	Bits	Type	Description
RFEN	0	rw	**Rectification Enable** General control of the rectifier circuit. *Note: Rectification is only active while the integrator is active.* 0_B No rectification, data not altered 1_B Data are rectified according to SGND
SSRC	5:4	rw	**Sign Source** Selects the sign signal that is to be delayed. 00_B On-chip carrier generator 01_B Sign of result of channel selected by bitfield SSCH 10_B External sign signal A 11_B External sign signal B
SSCH	11:8	rw	**Sign Source Channel** Selects the channel providing the sign signal if SSRC = 01_B. Other products of the family may have less channels and, consequently, less valid SSCH codes. Not listed combinations are reserved. 0_H Sign result from channel 0 … D_H Sign result from channel 13
SDCVAL	15	rh	**Valid Flag** Indicates a new value in bitfield SDCAP. 0_B No new result available 1_B Bitfield SDCAP has been updated with a new captured value and has not yet been read
SGNCS	30	rh	**Selected Carrier Sign Signal** 0_B Positive values 1_B Negative values
SGND	31	rh	**Sign Signal Delayed** 0_B Positive values 1_B Negative values

Field	Bits	Type	Description
0	3:1, 7:6, 14:12, 29:16	r	**Reserved, write 0, read as 0**