28.12 Time Base Unit (TBU)

28.12.1 Overview

The Time Base Unit TBU provides common time bases for the GTM. The TBU sub-module is organized in channels, where the number of channels is device dependent. There are up to four channels implemented inside the TBU. The time base register **TBU_CH0_BASE** of TBU channel 0 is 27 bits wide and it is configurable whether the lower 24 bit or the upper 24 bit are provided to the GTM as signal *TBU_TS0*. The two TBU channels 1 and 2 have a time base register **TBU_CH[y]_BASE** (y: 1, 2) of 24 bit length. The time base register value *TBU_TS[y]* is provided to subsequent sub-modules of the GTM.

The time base register of TBU channel 3 **TBU_CH3_BASE** is 24 bit wide. It used as a modulo counter by **TBU_CH3_BASE_MARK** to get a relative angle clock to **TBU_CH[y]_BASE**. The absolute angle clock value for the current **TBU_CH3_BASE** is captured in **TBU_CH3_BASE_CAPTURE**.

TBU_CH[y]_BASE = TBU_CH3_BASE_CAPTURE + **... + TBU_CH3_BASE*TBU_CH3_BASE_MARK**

DIRy: direction value for time base y (y:1…2)

0 up counter

1 down counter

Note: The right-hand sum is limited to 24 bit.

The *TBU_UP[y]* (y: 1…2) signals are set to high for a single SYS_CLK period, whenever the corresponding signal *TBU_TS[y]* (y: 1…2) is getting updated. The signal *TBU_UP0_L* is set to high for a single SYS_CLK period if the signal TBU_TS0 and TBU_TS0x is getting updated and *TBU_UP0_H* is set to high for a single SYS_CLK period, whenever the upper 24 bit of TBU_TS0 are updated.

The time base channels can run independently of each other and can be enabled and disabled synchronously by control bits in a global TBU channel enable register **TBU_CHEN**. **Figure 30** shows a block diagram of the Time Base Unit.

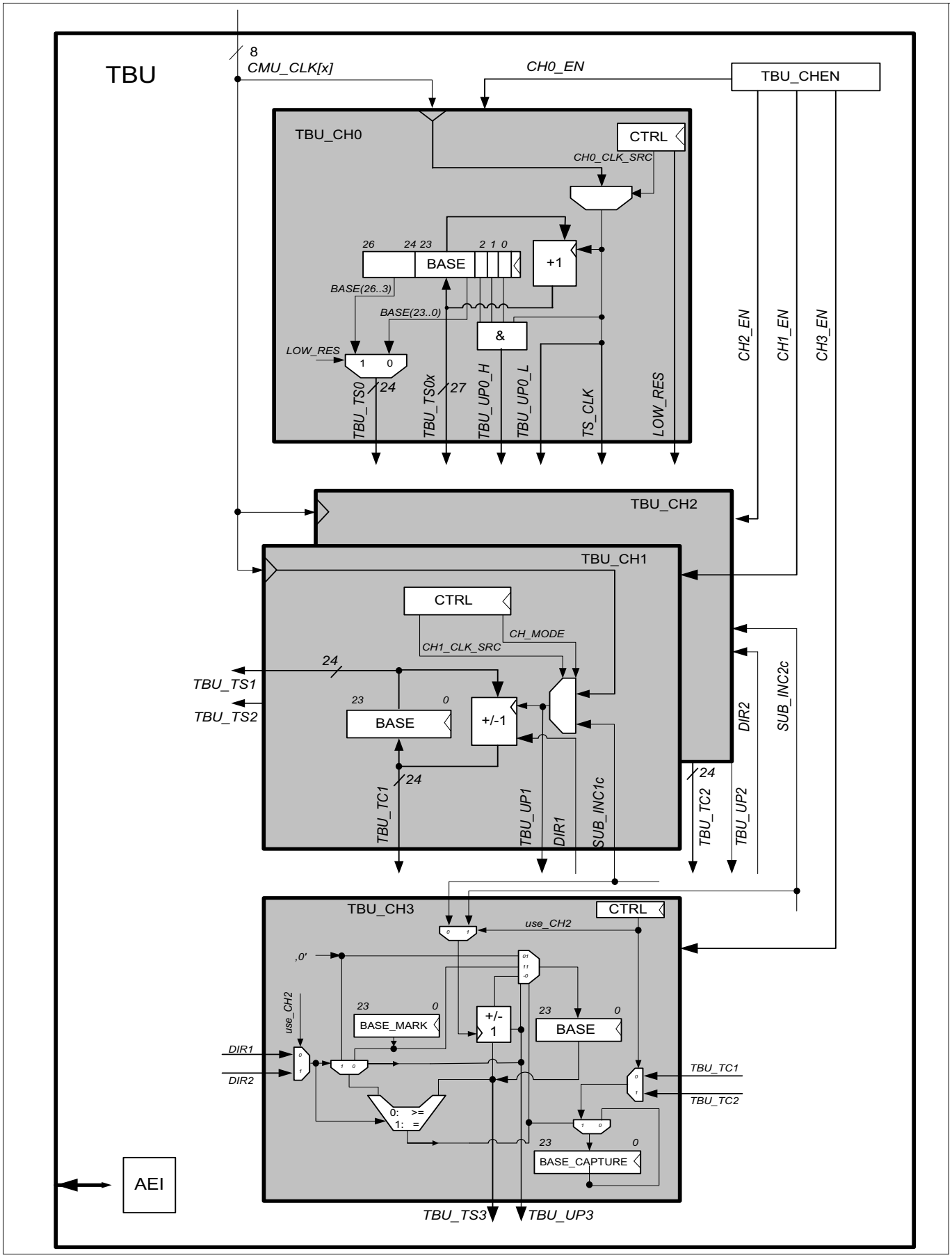

Figure 30 TBU Block Diagram