33.4 Input Channel Configuration

The input data for a channel can be obtained from different sources:

- **On-Chip Modulator**: The on-chip modulator can directly convert a differential or single-ended analog input signal to an input data stream. The on-chip modulator runs on the internal clock.
  The figure below summarizes the data path through the on-chip modulator.
- **External Modulator Without Clock Source**: This type of modulator requires a modulator clock signal. This clock signal is provided by the EDSADC, the data stream produced by the modulator is input as a digital signal.
- **External Modulator With Clock Source**: This type of modulator generates the modulator clock signal along with the data stream. In this case, both the modulator clock and the data stream produced by the modulator are input as digital signals.

Note: An external modulator can be used, in particular, in systems where high voltages are to be sampled. This allows for galvanic decoupling.
Several input pins can be selected.

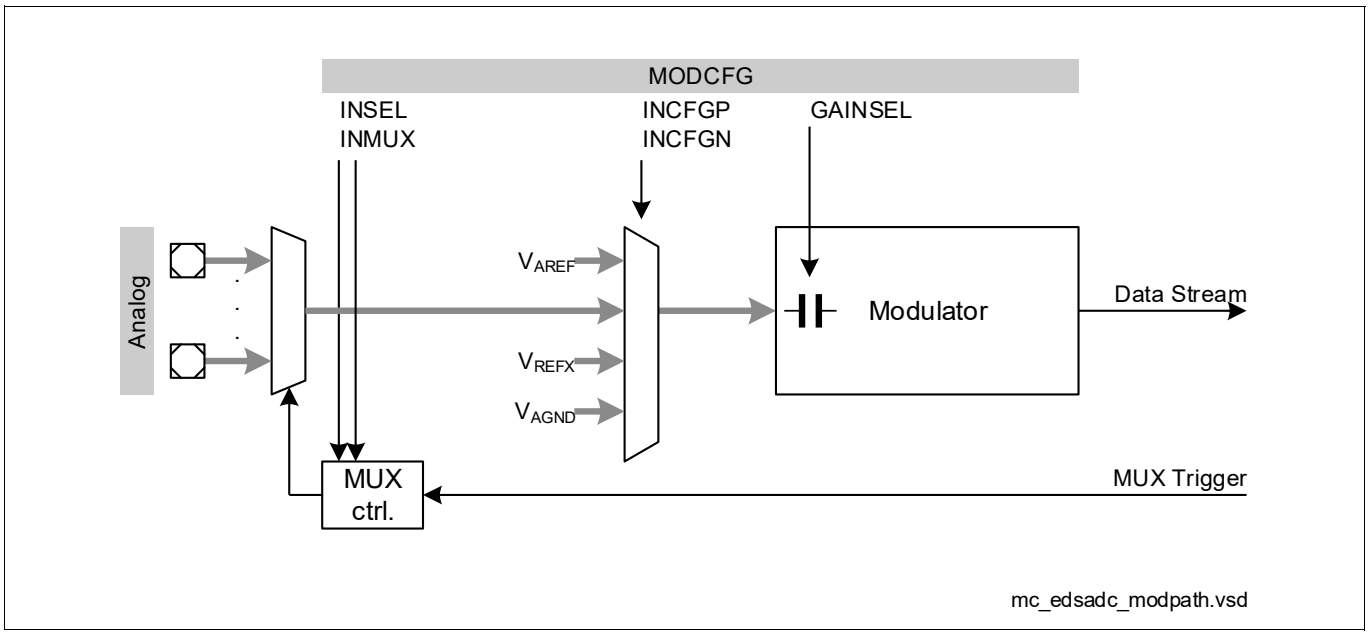

Figure 287 Analog Input Path

Note: To avoid clipping due to overdrive (the data stream contains all 1s) the on-chip modulator is built with an intrinsic gain factor of FM = 0.6945. This allows to handle a certain level of overshoots without entering overdrive.
The behavior of external modulators is described in the respective specification.

The modulator clock can be generated in different ways:

- The modulator clock is derived on-chip from the peripheral clock f_{ADC}. It is used for the on-chip modulators and can be output via a selectable modulator clock pin to be used by an external modulator. It also is the time basis for the timestamp counter.
- The external modulator can generate the clock signal which is then input via one of the modulator clock pins.

A trigger signal can be selected from different inputs. These inputs are connected to on-chip peripherals or to pins. The digital connection table in the product-specific appendix describes the available connections.

This trigger signal can be used for different purposes:

- Integration trigger:
  The external signal defines the integration window, i.e. the timespan during which result values are integrated.
- Timestamp trigger:
  The external signal requests the actualization of the timestamp register.
- Input multiplexer trigger:
  The external signal requests the switching of the analog input multiplexer to the next lower input or to the defined start value, respectively.
- Modulator run gate:
  The on-chip modulator can be controlled by an external gate signal while it is enabled. In this case it can be disabled temporarily to save power.
- Service request gate:
  Service requests for the filter chain can be restricted to the high or low times of the selected trigger signal.

Note: Trigger signals shall be active for at least 1 period of f_{ADC} to properly trigger an action.

The figure below summarizes these three signal paths and indicates the source of the corresponding control information.

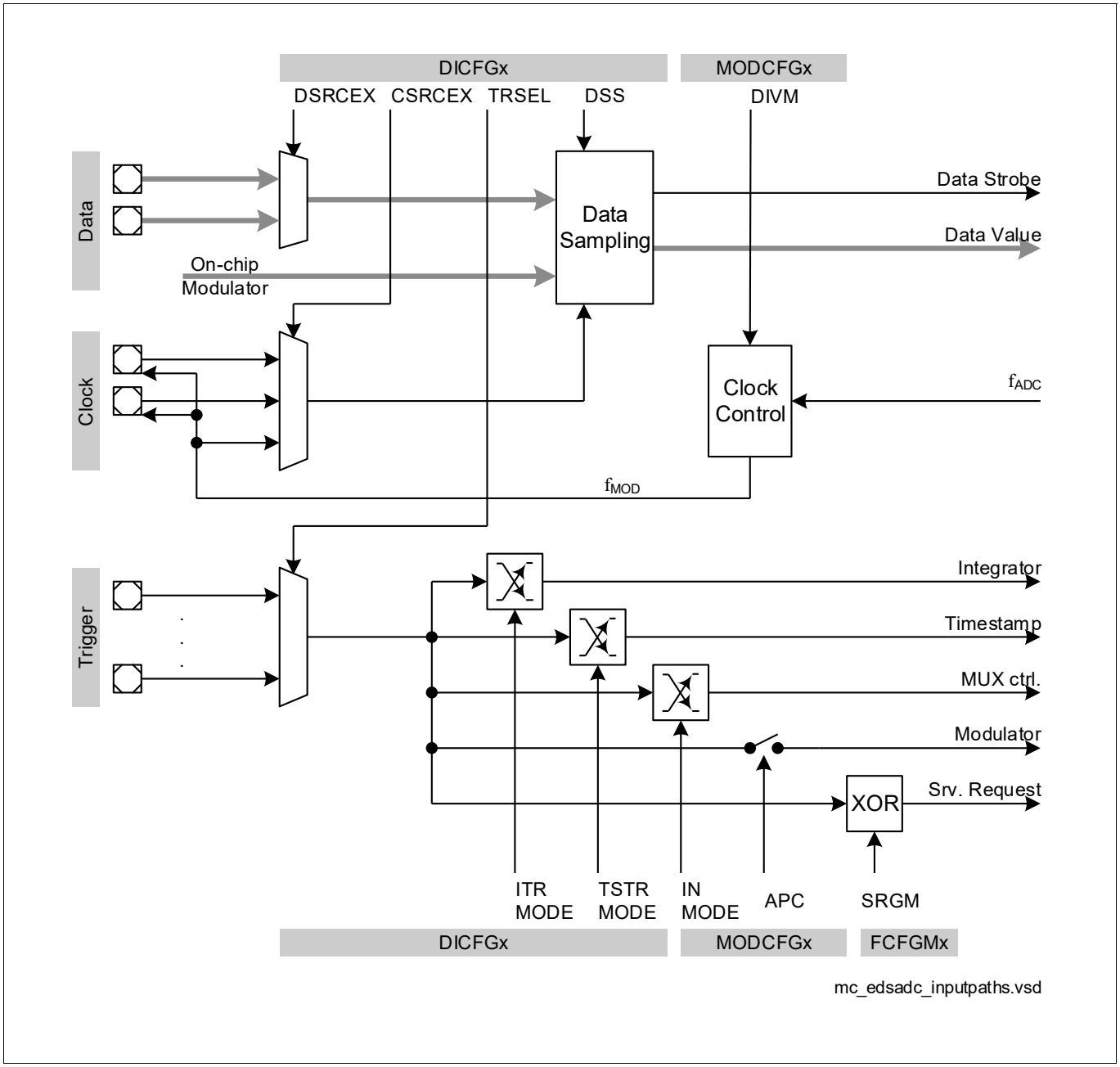

Figure 288 Input Path Summary

33.4.1 Modulator Clock Generation

The modulator clock signal can be generated on-chip or can be generated by an external modulator and be input through a pin (clock input).

The on-chip clock signal is used for the on-chip modulator or can be used for an external modulator through a selectable clock output pin. The on-chip modulator clock is based on the analog phase synchronizer. The phase synchronizer defines the rising edges of the modulator clock, the period is defined by bitfield DIVM (modulator clock period).

For proper operation the duty cycle of the on-chip modulator clock must be 50%. A separate 2:1 prescaler flipflop ensures this while the modulator clock is generated on-chip.

*Note: The EDSADC evaluates the rising edge of the phase synchronizer signal. In synchronized mode, it will operate while the phase synchronizer signal is toggling. In unsynchronized mode (**GLOBCFG**.USC = 1), the modulator clock is generated independent of the phase synchronizer signal.*
For proper operation, only change the configuration of the phase synchronizer while the converters are idle.

The bus interface is clocked with the system clock f_{SPB}.

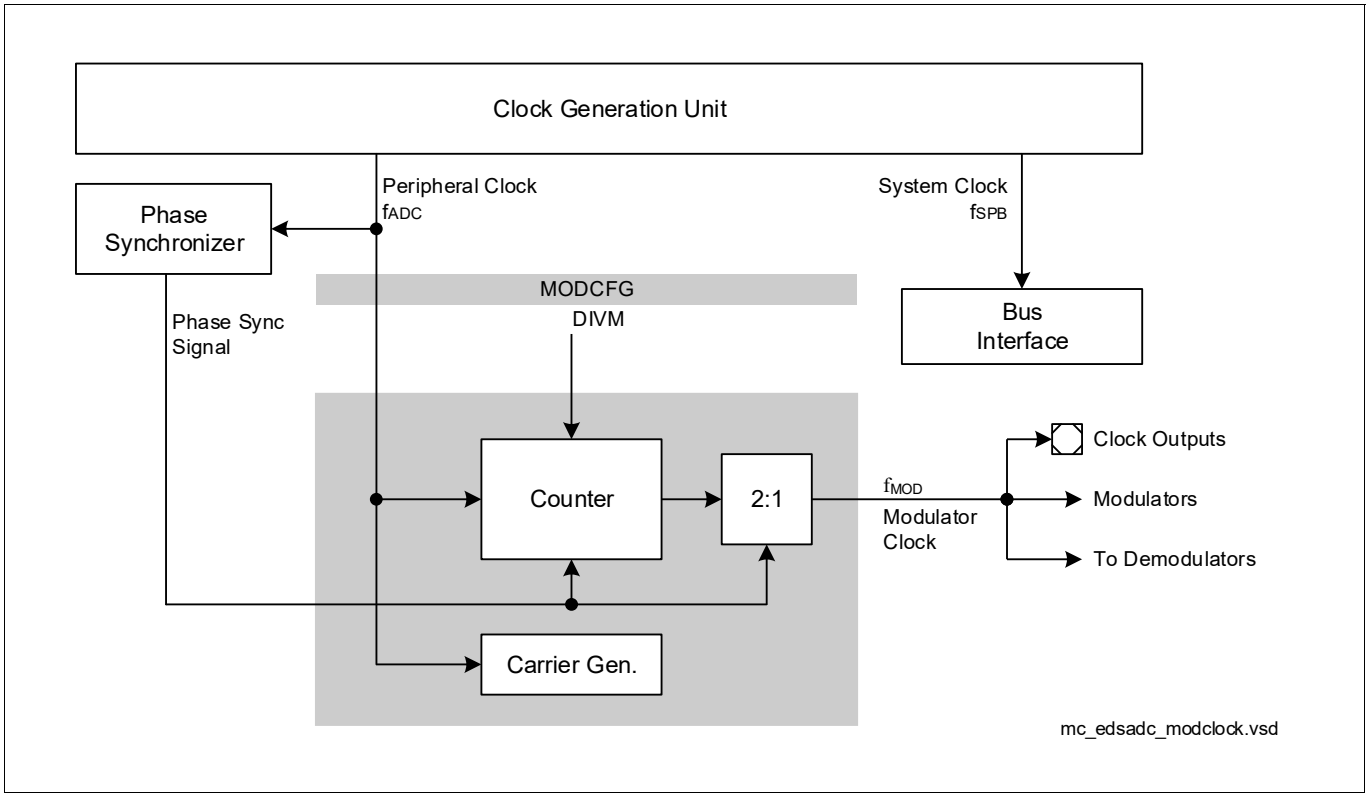

Figure 289 Modulator Clock Configuration

An external clock signal is synchronized to the module clock. A configurable edge detector selects the clock signal edges that generate the data strobes which read the next input data and trigger the demodulator (see **Figure 290**).

Note: To ensure proper synchronization, an external clock signal must have high/low phases of at least two periods of f_{ADC} to be safely synchronized (f_{IN} <= f_{ADC}/4).

When the clock signal is generated on-chip (see **Figure 289**) and is selected as an output signal at a connected pin, this clock signal can drive an external modulator.

Bitfield DSS in register **DICFGx (x=0-13)** selects the data source for each channel. For external modulators it also selects the clocking mode, i.e. the clock edges that put a new input data sample into the filter chain. In this case also the clock source can be selected.

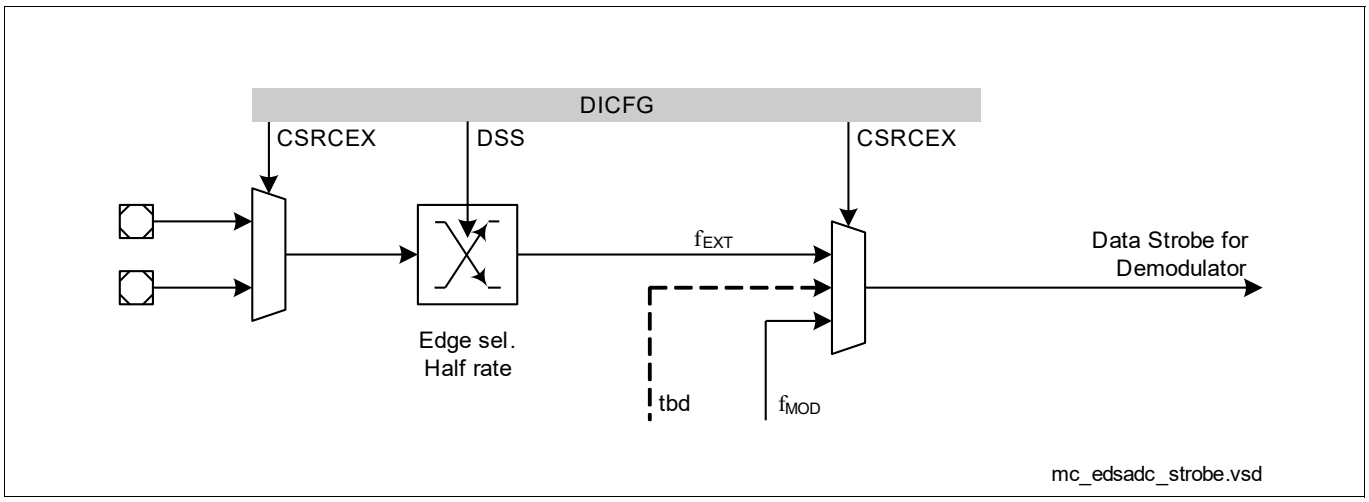

Figure 290 Demodulator Data Strobe Selection

33.4.2 Input Data Selection

The data stream of an external modulator can be input from a selectable pin. This signal can optionally be inverted.

The data stream can also be generated by the on-chip modulator. The selected input datastream is converted to the CIC filter's input format.

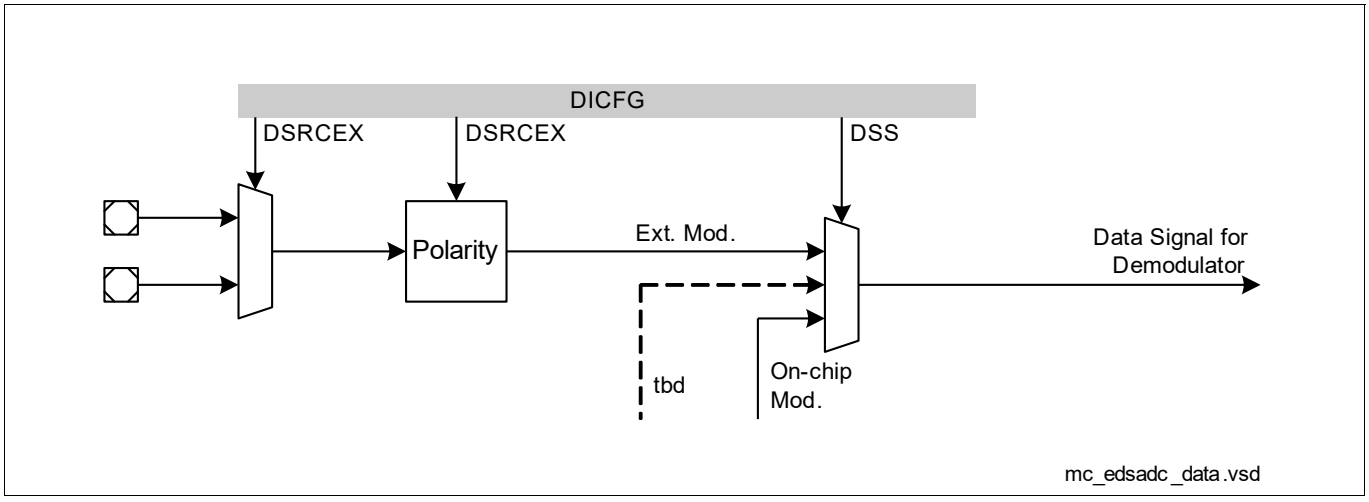

Figure 291 Demodulator Data Signal Selection

All options are configured by the demodulator input configuration register **DICFGx (x=0-13)**.

33.4.3 External Modulator

The input data stream can be obtained from an external modulator via a selectable pin. This modulator may, for example, be connected to a high driving voltage and be galvanically decoupled.

In this case, the modulator's data output is connected to the selected pin and is fed to the filter chain. The data input signal can optionally be inverted.

The sample clock signal can be generated on-chip or can be input from the external modulator. The data strobe that enters a new value into the filter chain can be generated upon configurable clock edges of the modulator clock to support different types of modulators.

33.4.4 On-Chip Modulator

The on-chip modulator is a 2nd order feed-forward modulator. It operates at a sample frequency of 40 MHz, 26.67 MHz, 20 MHz or 16 MHz. This sample frequency is derived from the actual module frequency (see **“Modulator Clock Generation” on Page 22**).

The analog input signal is fed to the sample stage via two input lines (differential input) or via one input line with the other input internally grounded (single-ended input).

Analog input multiplexers connect the input lines to different pins. The product-specific appendix details the available channels and their inputs. The input multiplexers are controlled by register **MODCFGx (x=0-13)**.

The gain factor of the input stage can be programmed to 1, 2, 4. The common mode voltage can be enabled or disabled.

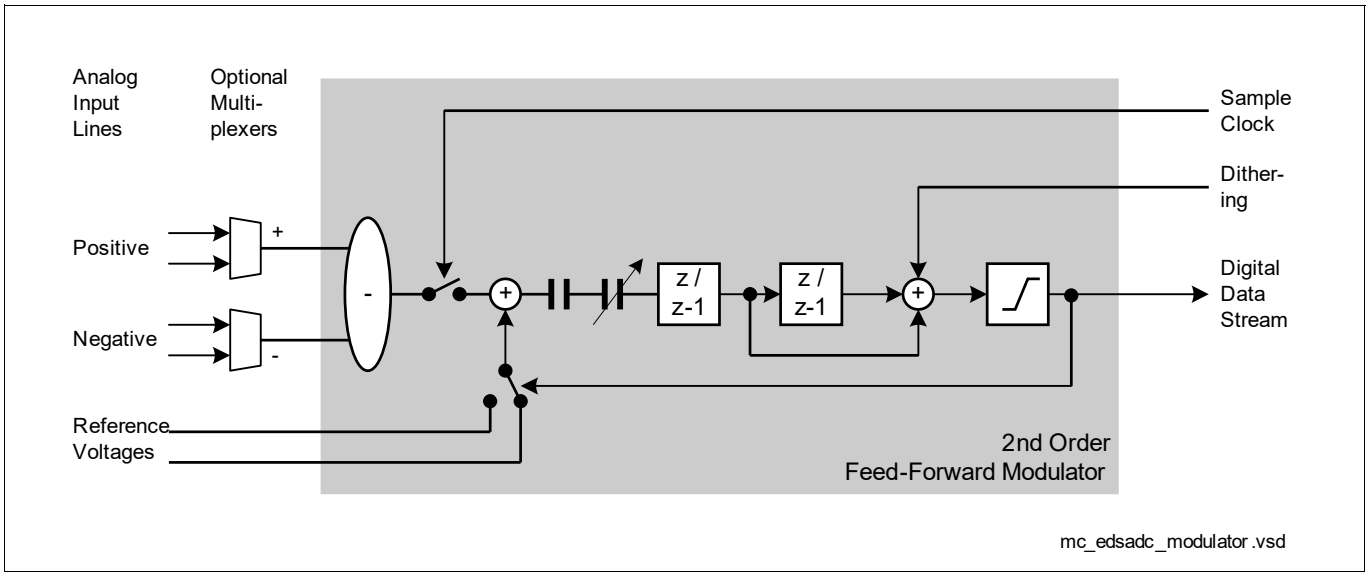

Figure 292 Structure of the On-Chip Modulator

Offset compensation and gain compensation improve the performance of the modulator. The calibration algorithm can be enabled during the initialization phase and also during operation, e.g. to compensate temperature drift.

Power Reduction via External Run Control

If an application does not require permanent activity of a channel, it can disable its modulator intermittently to save energy. This can be done under software control or automatically.

The operating mode is determined by bitfield **MODCFGx (x=0-13)**.APC:

- APC = 00_B: **Normal Operation**: The modulator is controlled by software.
- APC = 01_B: **Slow Standby mode**: Voltage regulator and on-chip modulator are switched off while the gate signal is inactive. They automatically return to normal operation when the gate signal becomes active. Requires the standard wakeup time (see below).
- APC = 10_B: **Fast Standby mode**: The on-chip modulator is switched off while the gate signal is inactive. It automatically returns to normal operation when the gate signal becomes active. Requires the standard wakeup time (see below).

Note: The standard wakeup time is also required after initially enabling the converter. If an external modulator is used, no wakeup time has to be considered. Slow Standby mode and Fast Standby mode are identical.

Wakeup Time from Analog Powerdown

When the modulator is activated, it needs a certain wakeup time (depending on the operating mode) to settle before proper data can be delivered. Make sure to include this settling time in the on-off cycles of the gate signal.

The standard wakeup time is maximum 20 µs.

Internal Dithering

Static or low-frequency input signals can generate so-called idle tones which could degrade the SNR. The internal dithering avoids this phenomenon.

The internal dithering can also reduce the so-called dead-zone.

Internal dithering is disabled by default, see bit DITHEN in register **MODCFGx (x=0-13)**.

Handling of Overload, Overdrive and Overflow Conditions

Operating an EDSADC channel outside its specified operating range requires additional careful handling and precautions. This ensures the generation of useful result values and prevents damaging the device.

An overload condition occurs if the input voltage on the respective pin exceeds the supply voltage. In this case the protection diodes try to limit the input voltage by becoming conducting. The resulting current must be limited to prevent damage to the protection structures. This is specified in the Datasheet.

An overdrive condition occurs if the resulting input voltage to the on-chip modulator becomes too high so the modulator can only generate a bitstream of all 1s. This may happen when an analog gain factor of 2 or 4 is selected. The susceptibility to an increased input voltage (e.g. overshoots) is reduced by the modulator's intrinsic gain factor of FM = 0.6945 (see also section **"CIC Filter" on Page 44**). The overdrive condition is determined by the input voltage, the analog gain factor selected by bitfield MODCFGx.GAINSEL and the reference voltage.

An overdrive condition, therefore, exists if ($V_{AIN} \times 2^{GAINSEL} \times 0.6945$) > V_{AREF}. In this case, the result value is <CALTARGET> × 1/0.6945.

The recovery from an overdrive condition would cause a non-constant group delay for the subsequent filter chain. This can be avoided by clearing the analog integrator stages of the modulator. Integrator clearing is done automatically if enabled by setting bit MODCFGx.IREN = 1[1)].

An overflow condition can, in turn, be generated by an overdrive condition. This can result in an overflow of the digital result that is obtained from the filter chain's output. To avoid this, the calibration target value must be selected below $2^{15} \times 0.6945$ = 22 757 and the data shifter after the CIC filter and the corresponding correction factor be set accordingly (see formula for CICSHIFT in section **"CIC Filter" on Page 44**).

Calibration targets above 22 757 do not cause overdrive if the input voltage V_{AIN} is limited by the system and does not exceed (2^{15} / <CALTARGET>) * (V_{AREF} / $2^{GAINSEL}$). The default value (after reset) of 25 000, for example, provides result values with a resolution of 0.2 mV/LSB.

The subsequent filter chain provides a normalized gain of 1.

Attention: ***Overload conditions while a gain factor of 4:1 is selected lead to an internal stress condition which can reduce the product's life time if the overall duration of this condition exceeds a total of 10 s. Make sure the application software recognizes this stress condition (easiest way is to detect the overdrive condition) and disables the respective modulator or reduces the gain factor within 10 ms. Limit checking can help to detect this situation automatically. This supervision allows to tolerate approx. 1000 occurrences of the internal stress condition over life time.***

1) It is recommended to enable integrator reset as a standard means to deal with on-chip modulator overdrive for applications where overdrive conditions can occur.

33.4.5 Input Path Control

The input for the EDSADC is fed through several stages before being evaluated and filtered. Registers MODCFGx and DICFGx select the available options for these signal stages.

The following features can be configured:

- Signal input pin selection
- Configuration of input stage and on-chip modulator
- Generation method of input data
- Modulator clock source and/or frequency
- Trigger input pin selection

Signal Input Pin Selection

Some modulator inputs provide analog input multiplexers which connect them to several input pins. These input multiplexers can be controlled directly by software or can be switched triggered by an external control signal. Software selects the desired position via bitfield INSEL, bitfield INMUX indicates the actual setting of the input multiplexer. Bitfield INMODE defines the condition for a trigger event, bitfield INMAC selects the way in which the multiplexer is controlled:

- Software control:
  Control bitfield INMUX follows bitfield INSEL, software directly selects the intended input pins.
- Preset mode:
  The (software-written) value in bitfield INSEL is copied to bitfield INMUX upon a trigger event. Software can preselect the next intended multiplexer setting which then becomes active when the next trigger event occurs.
- Single-step mode:
  Bitfield INMUX is decremented upon each trigger event. If INMUX = 00_B when the trigger occurs, it is loaded from bitfield INSEL instead. In this mode, a predefined sequence of input pins can be scanned automatically.

The trigger signal itself is selected by bitfield TRSEL in register **DICFGx (x=0-13)**.

Note: Not all channels provide input multiplexers. Also, the width of the input multiplexers may differ from channel to channel. The product-specific appendix details the available channels and their inputs inputs.

Modulator Configuration Register x

The modulator configuration register selects the operation mode of the on-chip modulator:

- Input line clamping
- Gain factor of input signal path
- Modulator operating mode
- Divider factor for modulator clock

Note: Changes to bitfields INCFGP, INCFGN, GAINSEL only become active after switching the analog multiplexer setting (if available) or after restarting the channel (MxRUN = 1).

MODCFGx (x=0-13)
Modulator Configuration Register x **(0100_H+x*100_H)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MMWC	0	APC		IREN	DITHEN	0			ACSD			0	DIVM		
w	r	rw		rw	rw	r			rw			r	rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INCWC	INMAC	INMODE		INMUX		INSEL		GAINSEL				INCFGN		INCFGP	
w	rw	rw		rh		rw		rw				rw		rw	

Field	Bits	Type	Description
INCFGP	1:0	rw	**Configuration of Positive Input Line** Defines the internal connection of the positive input. 00_B Input pin 01_B Reference voltage V_{AREF} 10_B V_{REFX} (see VREFXSEL setting in register VCM) 11_B Reference ground V_{AGND}
INCFGN	3:2	rw	**Configuration of Negative Input Line** Defines the internal connection of the negative input. 00_B Input pin 01_B Reference voltage V_{AREF} 10_B V_{REFX} (see VREFXSEL setting in register VCM) 11_B Reference ground V_{AGND}
GAINSEL	7:4	rw	**Gain Select of Analog Input Path** Not listed combinations are reserved. 0_H Gain factor 1 1_H Gain factor 2 2_H Gain factor 4
INSEL	9:8	rw	**Input Pin Selection** Defines the initial or permanent setting for the input multiplexer (bitfield INMUX) depending on the selected operating mode (bitfield INMODE).
INMUX	11:10	rh	**Input Multiplexer Setting** Indicates the current setting of the input multiplexer connecting the input pins to the buffer inputs. The product-specific appendix details the available channels and their inputs. 00_B Input pin position A 01_B Input pin position B 10_B Input pin position C 11_B Input pin position D

Field	Bits	Type	Description
INMODE	13:12	rw	**Input Multiplexer Control Mode** Defines the condition for a trigger event to control the input multiplexer. Bitfield INMAC selects the action upon a trigger event. 00_B Software control (INMUX follows INSEL) 01_B Trigger event upon a falling edge 10_B Trigger event upon a rising edge 11_B Trigger event upon any edge
INMAC	14	rw	**Input Multiplexer Action Control** Defines the mechanism by which the input multiplexer is controlled. 0_B Preset mode (load INMUX upon a trigger) 1_B Single-step mode (decrement INMUX upon a trigger, wrap around to <INSEL>)
INCWC	15	w	**Write Control for Input Parameters** 0_B No write access to input parameters 1_B Bitfields INCFGP, INCFGN, GAINSEL, INSEL, INMODE, INMAC can be written
DIVM	18:16	rw	**Modulator Clock Period** Defines the period of the modulator clock (on-chip/external), derived from the peripheral clock: $t_{MOD} = t_{ADC} \times CP$ ($f_{MOD} = f_{ADC} / CP$), with CP = 4 + DIVM × 2. 000_B CP = 4 … 111_B CP = 18
ACSD	22:20	rw	**Analog Clock Synchronization Delay** Defines the delay in clocks after the sync signal. *Note: Valid only if the phase synchronizer is selected (USC = 0_B).* 000_B 0, no delay 001_B 1 clock cycle delay 010_B 2 clock cycles delay … 111_B 7 clock cycles delay
DITHEN	26	rw	**Dithering Function Enable** Controls the dithering function for each modulator separately. 0_B Disable dithering 1_B Dithering is enabled
IREN	27	rw	**Integrator Reset Enable** Controls the modulator overdrive handling 0_B No integrator reset 1_B Integrators are reset in case of an overdrive

Field	Bits	Type	Description
APC	29:28	rw	**Automatic Power Control** 00_B Off: Modulator active while its associated bit MxRUN is set 01_B Slow standby mode on-chip modulator and voltage regulator are deactivated, external modulator clock is disabled, while the gate signal (selected trigger) is inactive 10_B Fast standby mode:on-chip modulator is deactivated, external modulator clock is disabled, while the gate signal (selected trigger) is inactive 11_B Reserved
MMWC	31	w	**Write Control for Modulator Mode Settings** 0_B No write access to mode settings 1_B Bitfields APC, IREN, DITHEN, ACSD, DIVM can be written
0	19, 25:23, 30	r	**Reserved, write 0, read as 0**

Table 278 Access Mode Restrictions of MODCFGx (x=0-13) sorted by descending priority

Mode Name	Access Mode		Description
write 1 to **INCWC**	rw	GAINSEL, INCFGN, INCFGP, INMAC, INMODE, INSEL	Set INCWC during write access
write 1 to **MMWC**	rw	ACSD, APC, DITHEN, DIVM, IREN	Set MMWC during write access
(default)	r	ACSD, APC, DITHEN, DIVM, GAINSEL, INCFGN, INCFGP, INMAC, INMODE, INSEL, IREN	

Demodulator Input Config. Register x

The demodulator input configuration register selects input signal sources for each channel:

- Source of the data stream
- Input for an external data stream
- Input for an external clock
- Trigger signal source and modes
- Read mode for the result register

Note:

DICFGx (x=0-13)

Demodulator Input Config. Register x **(0108_H+x*100_H)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSWC	**0**	**RDM**	**TSM**	**DRM**		**0**		**TSTRMODE**		**ITRMODE**		**TRSEL**			
w	r	rw	rw	rw		r		rw		rw		rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DSWC	**0**				**CSRCEX**			**0**	**DSRCEX**			**0**	**DSS**		
w	r				rw			r	rw			r	rw		

Field	Bits	Type	Description
DSS	2:0	rw	**Data Stream Select** 000_B On-chip modulator 001_B Reserved 010_B Reserved 011_B External modulator, use rising and falling clock edge (double data) 100_B External modulator, use each falling clock edge (direct clock) 101_B External modulator, use each rising clock edge (direct clock) 110_B External modulator, use every 2nd falling clock edge (dbl. clock) 111_B External modulator, use every 2nd rising clock edge (dbl. clock)
DSRCEX	6:4	rw	**Data Source for External Modulator** 000_B External, from input A, direct 001_B External, from input A, inverted 010_B External, from input B, direct 011_B External, from input B, inverted 100_B External, from input C, direct 101_B External, from input C, inverted 110_B External, from input D, direct 111_B External, from input D, inverted
CSRCEX	10:8	rw	**Clock Source for External Modulator** 000_B Internal clock 001_B Reserved 010_B Reserved 011_B External, from input A 100_B External, from input B 101_B External, from input C 110_B Reserved 111_B Reserved
DSWC	15	w	**Write Control for Data Stream Selection** 0_B No write access to data parameters 1_B Bitfields CSRCEX, DSRCEX, DSS can be written

Field	Bits	Type	Description
TRSEL	19:16	rw	**Trigger Select** Selects an input for the trigger signal used for the following features (see also **Figure 288**): [1] integrator control, timestamp, multiplexer control, modulator control (APC), service request gating. The product-specific appendix details the connected trigger input signals.
ITRMODE	21:20	rw	**Integrator Trigger Mode** To ensure proper operation, ensure that bitfield ITRMODE is 00_B before selecting any other trigger mode.[2] Bit INTEN is set when ITRMODE = 11_B or when the selected trigger signal transition occurs. Bit INTEN is cleared when ITRMODE = 00_B, after REPVAL+1 integration cycles (IWS = 0) or when the inverse trigger signal transition occurs (IWS = 1). 00_B No integration trigger, integrator bypassed 01_B Trigger event upon a falling edge 10_B Trigger event upon a rising edge 11_B No trigger, integrator active all the time
TSTRMODE	23:22	rw	**Timestamp Trigger Mode** The timestamp trigger mode controls capturing the timestamp information to register **TSTMPx**. 00_B No timestamp trigger 01_B Trigger event upon a falling edge 10_B Trigger event upon a rising edge 11_B Trigger event upon each edge
DRM	27:26	rw	**Data Read Mode** Selects the data that is returned when register RESMx is read (see **Table 290**). 00_B Single: Issue one 16-bit value per read access (sign on high bits) 01_B Single: Issue one 16-bit value per read access (timestamp or zero on high bits) 10_B Double: Issue two 16-bit values per read access 11_B Reserved
TSM	28	rw	**Time-Stamp Mode** See **Table 290**. 0_B No timestamp, only issue result values 1_B Insert timestamp upon the trigger (when the gate opens)
RDM	29	rw	**Result Display Mode** 0_B Signed mode result values range from -2^{15} to $+2^{15}-1$ 1_B Unsigned mode result values range from 0 to $+2^{16}-1$ (shifted by 2^{15})
MSWC	31	w	**Write Control for Mode Settings** 0_B No write access to mode settings 1_B Bitfields RDM, TSM, DRM, TSTRMODE, ITRMODE, TRSEL can be written

Field	Bits	Type	Description
0	3, 7, 14:11, 25:24, 30	r	**Reserved, write 0, read as 0**

1) To avoid unintended triggers, select the trigger source first before enabling the corresponding function.
2) The integration trigger mode controls bit INTEN in register **IWCTRx** and hence the operation of the integrator:

Table 279 Access Mode Restrictions of DICFGx (x=0-13) sorted by descending priority

Mode Name	Access Mode		Description
write 1 to **DSWC**	rw	CSRCEX, DSRCEX, DSS	Set DSWC during write access
write 1 to **MSWC**	rw	DRM, ITRMODE, RDM, TRSEL, TSM, TSTRMODE	Set MSWC during write access
(default)	r	CSRCEX, DRM, DSRCEX, DSS, ITRMODE, RDM, TRSEL, TSM, TSTRMODE	

33.4.6 Common Mode Voltage

Some applications require the assertion of a common mode voltage e.g. to support passive differential sensors. The common mode voltage V_{CM} is derived from the analog reference voltage V_{AREF}: $V_{CM} = V_{AREF} / X$ and is enabled via bit VXON and configured via bitfield VREFXSEL in register **VCMx (x=0-13)**.

Bits INyVCz in register **VCMx (x=0-13)** select the connection to V_{CM} for each of the possible input pins. Two nibbles are assigned to each channel (positive and negative inputs) and contain the control bits for each possible input of the respective channel.

While the input pins are not connected to the input lines of the channel (e.g. while the analog input multiplexer selects different pins or while the modulator is off), each individual analog input pin that is intended to be used for the EDSADC can remain connected to the common mode voltage V_{CM}. This ensures that the sensor input is biased and does not float away while the respective input line is disconnected or the modulator is disabled.

Note: The available channels provide different numbers of input pins. The product-specific appendix details the available channels and their inputs inputs. Only those INyVCz bits in VCMx are valid that correspond to an existing input pin.

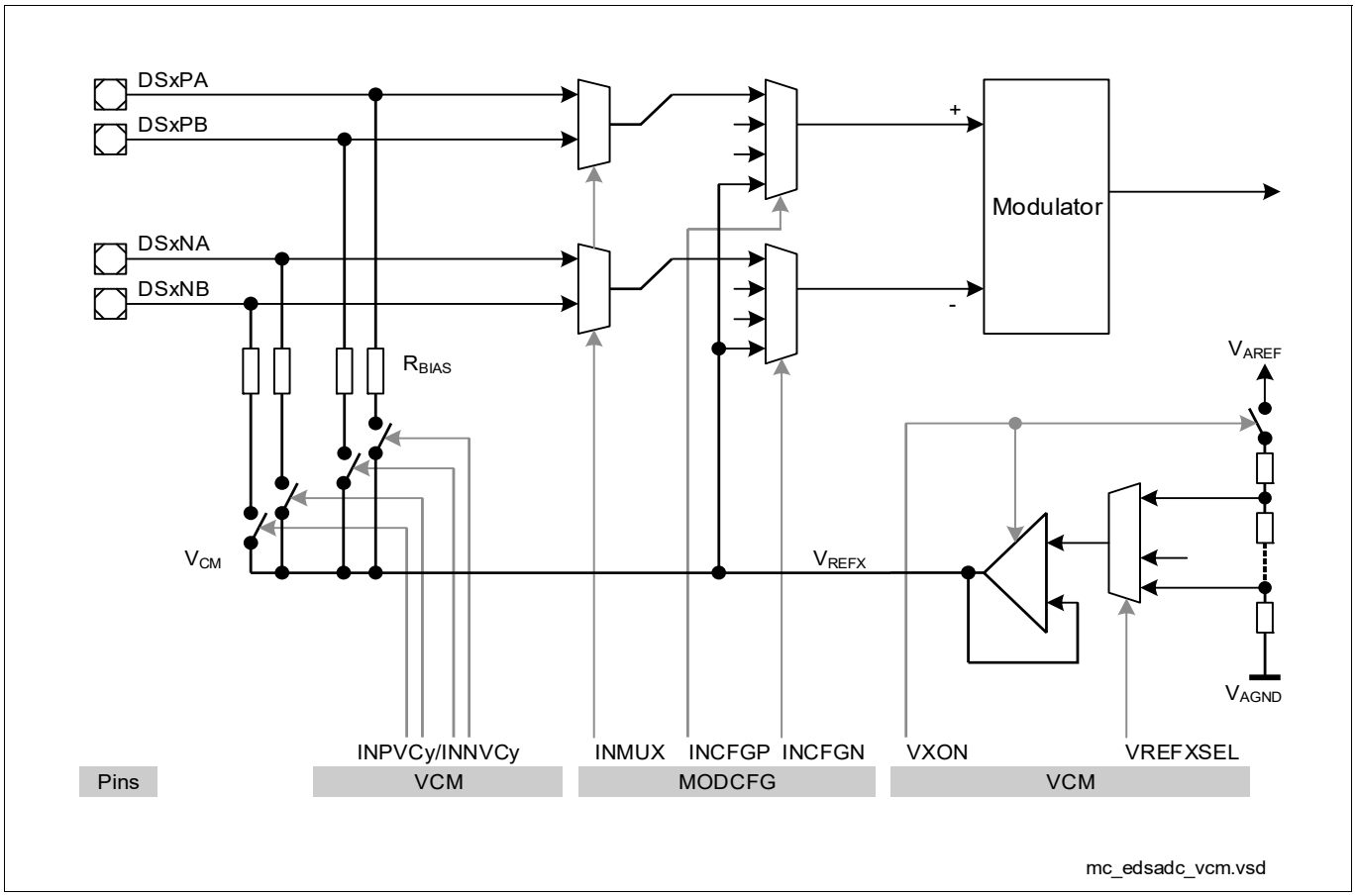

Figure 293 Control of VCM Switches

Common Mode Voltage Register x

The common mode voltage registers enable the voltage generators and select which input pins are connected to the common mode hold voltage.

Only those bits are valid that correspond to an existing input pin (see product-specific appendix).

VCMx (x=0-13)

Common Mode Voltage Register x **($01B0_H$+x*100_H)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								INNVC3	INNVC2	INNVC1	INNVC0	INPVC3	INPVC2	INPVC1	INPVC0
r								rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0													VXON	VREFXSEL	
r													rw	rw	

Field	Bits	Type	Description
VREFXSEL	1:0	rw	**Fractional Reference Voltage Selection** 00_B $V_{REFX} = V_{AREF} / 2$ 01_B $V_{REFX} = V_{AREF} / 4$ 10_B $V_{REFX} = V_{AREF} / 8$ 11_B Reserved
VXON	2	rw	**Fractional Reference Voltage Enable** 0_B V_{REFX} is not connected 1_B V_{REFX} is connected, value according to VREFXSEL
INPVCy (y=0-3)	y+16	rw	**Voltage Control of Positive Inputs y of CHx** Defines the connection of the respective positive input y to the common mode voltage. y indicates the input of the analog multiplexers (if available). 0_B No connection to common mode voltage 1_B This pin is connected to the common mode voltage
INNVCy (y=0-3)	y+20	rw	**Voltage Control of Negative Inputs y of CHx** Defines the connection of the respective negative input y to the common mode voltage. y indicates the input of the analog multiplexers (if available). 0_B No connection to common mode voltage 1_B This pin is connected to the common mode voltage
0	15:3, 31:24	r	**Reserved, write 0, read as 0**

33.4.7 Calibration Support

The performance of the EDSADC can be improved by applying some calibration techniques.

The calibration algorithm for gain and offset is executed automatically. Since it takes a certain time during which no conversions can be executed, two modes can be used:

- Software can determine when the algorithm is executed by setting bit CALIB in register **FCFGMx (x=0-13)**.
- In the case of gated operation the calibration algorithm can also be started automatically when the gate closes (set bit AUTOCAL in register **FCFGMx (x=0-13)**).

The calibration algorithm supports differential and single-ended mode with gain settings of 1 and 2. The respective calibration mode is derived from registers **MODCFGx (x=0-13)** and **VCMx (x=0-13)** as shown in the table below:

Table 280 Supported Calibration Modes

Selected Mode	Corresponding Bitfields in MODCFG
Differential, gain 1 / gain 2	INCFGP = INCFGN = 00_B, GAINSEL = 0000_B or 0001_B
Single-ended, gain 1	INCFGx = 00_B, INCFGy = 11_B, GAINSEL = 0000_B
Single-ended, gain 2	INCFGx = 00_B, INCFGy = 10_B, GAINSEL = 0001_B, VCMx.VREFXSEL = 00_B

Note: An initial calibration must be triggered once after a reset.
Calibration for a gain factor of 4 is executed with gain setting 2.

Repeated Calibration During Operation

To compensate temperature effects it is recommended to repeat the calibration sequence when the device temperature has changed by approximately 20°C. This can be done by simply setting bit CALIB in register **FCFGMx (x=0-13)** or by enabling automatic calibration (AUTOCAL = 1). After calibration, the channel will resume its normal operation.

Calibration Timing

The calibration uses a sequential search algorithm to determine the correct calibration factor. The duration of the calibration algorithm, therefore, depends on the deviation to be calibrated (algorithm), and also on the configuration of the module, i.e. on the modulator frequency ($f_{MOD} = f_{ADC} / (4 + 2\times DIVM)$) and on the decimation rate used for calibration ($DC = 8 \times 2^{CICDEC}$).

The calibration time, therefore, is determined by $t_{ADC} = 1 / f_{ADC}$ and $t_{MOD} = 1 / f_{MOD}$.

The following formula describes the required maximum calibration time: $t_{CAL} = 16 \times DC \times t_{MOD} + 4\,200 \times t_{ADC}$.
If gain factor 2 is selected the calibration algorithm is extended by: $t_{2nd} = 12 \times DC \times t_{MOD} + 8\,300 \times t_{ADC}$,
so the total maximum calibration time will be: $t_{CAL2} = 28 \times DC \times t_{MOD} + 12\,500 \times t_{ADC}$.

Table 281 Calibration Times [µs] for f_{ADC} = 160 MHz, Gain1 (Gain2)

DIVM [f_{MOD}] --->	0 [40]	1 [26.7]	2 [20]	3 [16]
CICDEC = 4, DC = 128	78 (168)	104 (213)	129 (258)	155 (303)
CICDEC = 5, DC = 256	129 (258)	180 (347)	232 (437)	283 (527)
CICDEC = 6, DC = 512	232 (437)	334 (616)	436 (795)	539 (975)

Note: Higher decimation rates require more calibration time but offer a higher calibration precision.
*The end of calibration is indicated in bitfield CAL in register **FCNTCx (x=0-13)**.*

Range Adaptation

The application can select the digital full-scale result value that corresponds to an input of $V_{AIN} = V_{AREF}$.

The intended full-scale value (CALTARGET) is reached by configuring the decimation rate of the CIC filters, selecting the corresponding position of the data shifter and configuring the resulting multiplication factor for the gain adjust unit, written to register **GAINCORRx (x=0-13)** (see links below).

The signal to noise ratio defines the effective number of result bits: ENOB = (SNR - 1.76) / 6.02.

Since (80 dB - 1.76) / 6.02 = 13 bit, selecting a minimum 14-bit target value is recommended.

When choosing the full-scale value, note, however, that using the full 15-bit range may lead to overflows in case of overshoots. See **"Handling of Overload, Overdrive and Overflow Conditions" on Page 26**.

Summary of Calibration Parameters

During calibration the settings of CIC filter and gain correction are replaced by specific values which are valid for the calibration algorithm. The application needs to compute and configure these values in addition to the values used during operation.

The calibration algorithm will trim the channel according to the configured calibration target value (CALTARGET).

Note: The formula to determine the GAINFACTOR is given in section ***"Data Shifter and Decimation Factor" on Page 45***.

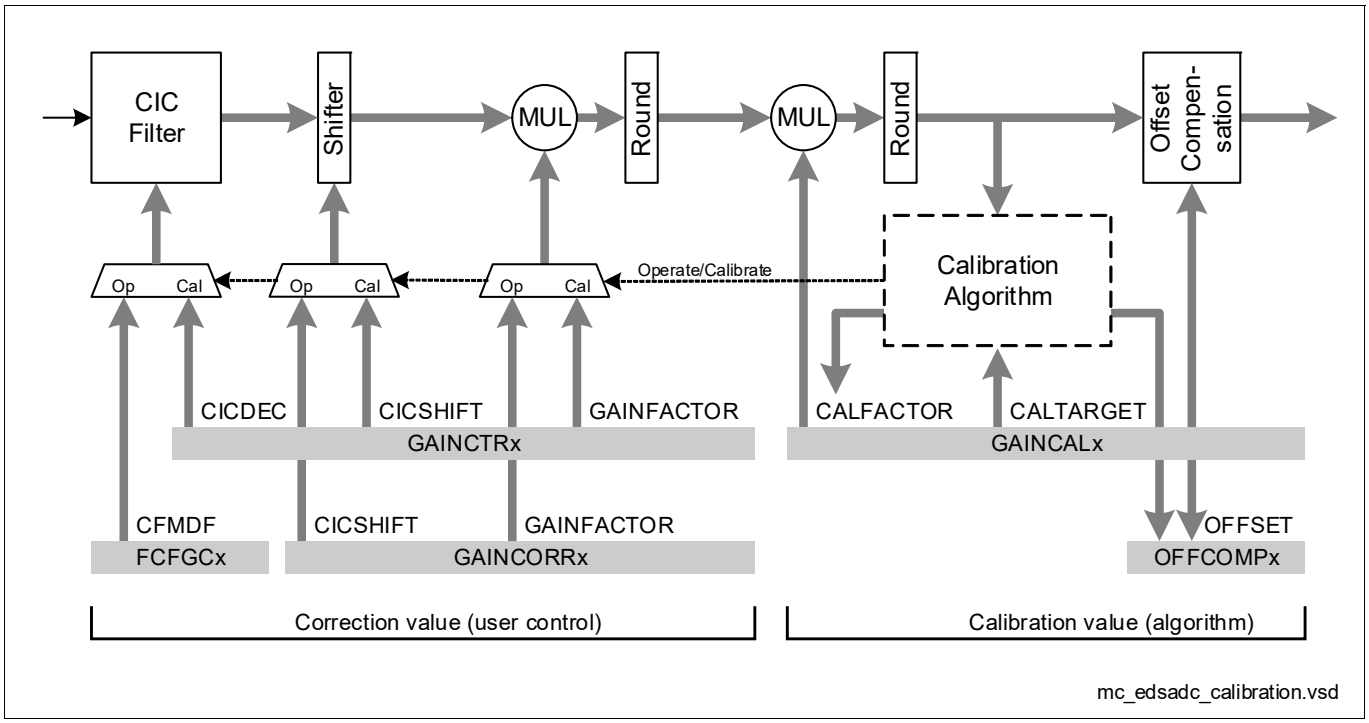

Figure 294 Calibration Overview

Gain Calibration Register x

GAINCALx (x=0-13)

Gain Calibration Register x **($013C_H$+x*100_H)** **Application Reset Value: 61A8 1000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								CALTARGET							
r								rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0			CALFACTOR												
r			rwh												

Field	Bits	Type	Description
CALFACTOR	12:0	rwh	**Multiplication Factor for Gain Calibration** The resulting factor is (<CALFACTOR> / 4 096) *Note: The initial value of 4 096 (1000_H) corresponds to a factor of 1.000.*
CALTARGET	30:16	rw	**Target Value for Calibrated Fullscale** Defines the target value for the calibration algorithm. *Note: The initial value of 25 000 ($61A8_H$) corresponds to 0.2 mV per LSB.*
0	15:13, 31	r	**Reserved, write 0, read as 0**

Gain Control Register x

GAINCTRx (x=0-13)

Gain Control Register x **(0140_H+x*100_H)** **Application Reset Value: 0000 1000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0					CICDEC			0			CICSHIFT				
r					rw			r			rw				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0			GAINFACTOR												
r			rw												

Field	Bits	Type	Description
GAINFACTOR	12:0	rw	**Multiplication Factor for Gain Correction During Calibration** The resulting factor is (<GAINFACTOR> / 4 096)

Field	Bits	Type	Description
CICSHIFT	20:16	rw	**Position of the CIC Filter Output Shifter During Calibration** Selects the valid outputs bits from the CIC filter, depending on the chosen decimation factor (see data shifter formula), $1D_H$ … $1F_H$ are reserved. 00_H Use bits 0 ... 16 … $1C_H$ Use bits 28 ... 44
CICDEC	26:24	rw	**Decimation Rate of the CIC Filter During Calibration** Factor = 2 ^ (CICDEC + 3) 000_B 8 … 110_B 512 111_B Reserved
0	15:13, 23:21, 31:27	r	**Reserved, write 0, read as 0**

33.4.8 Correction for External Circuitry

The built-in calibration support is optimized for low-impedance inputs. Operation using higher impedances (>100 Ohm) incurs gain errors due to the external circuitry (series resistance and buffer capacitor.

- Single-ended operation (see **Figure 295**):
  One input line usually internally connected to ground.
  An additional compensation factor can be calculated to compensate the error caused by the average input current I_{RMS} flowing through the resistance of the external path R_{EXT}:
  $F_{GR} = 1 + (I_{RMS} \times R_{EXT}) / 5\ V$
- Differential operation (see **Figure 296**):
  Both input lines connected to signal source.
  An additional compensation factor can be calculated to compensate the error caused by the average input current I_{RMS} flowing through the resistances of the external path R_{EXTP} and R_{EXTN}:
  $F_{GR} = 1 + (I_{RMS} \times (R_{EXTP} + R_{EXTN})) / 5\ V$

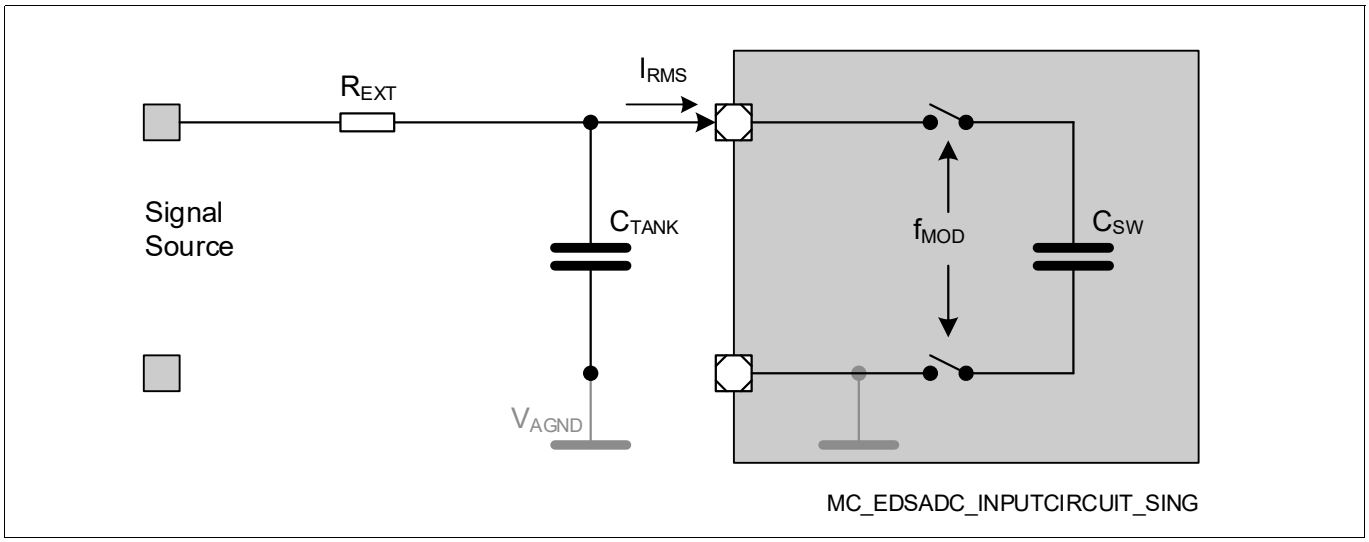

Figure 295 Single-Ended Input Circuitry of a Channel

*Note: This description example assumes the single-ended sensor signal to be connected to the positive input and the negative input to be grounded internally (indicated in grey in **Figure 295**).*

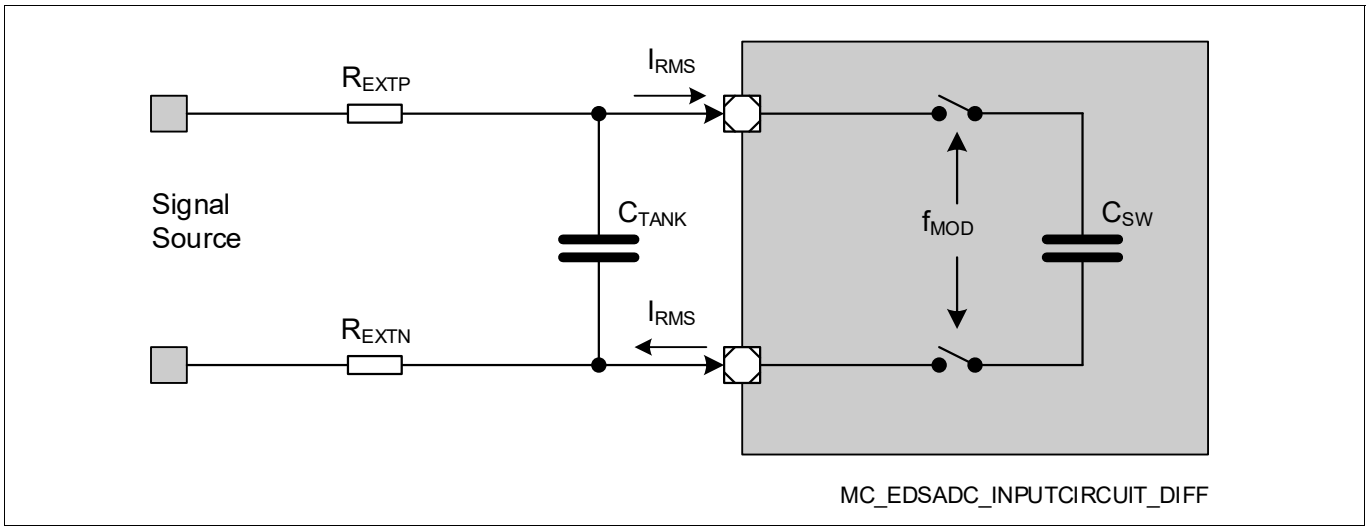

Figure 296 Differential Input Circuitry of a Channel

The buffer capacitor C_{TANK} not only is a part of the anti-alias filter but also minimizes the gain error of the complete input path. The maximum value for C_{TANK} is determined by the maximum signal frequency that shall be converted by the respective channel.

Also the buffer capacitor itself causes a small additional gain error. This can be compensated with the following formula:

$F_{GC} = 1 + I_{RMS} / (f_{MOD} \times C_{TANK} \times 5\ V)$

These factors can be combined with the range adaptation factor and CIC correction factor and be written into register **GAINCORRx (x=0-13)**.

Stored Calibration Values

The average input current is measured during production and the value is stored in the on-chip Flash (value IRMS, see below). The application can, therefore, calculate a device-specific correction factor.

The stored measurement value is referenced to a voltage of 5.0 V, a modulator frequency of 26.67 MHz and a gain factor of 1:1. So the actual input current is $I_{RMS} = (IRMSx / 100) \times (f_{MOD} / 26.67) \times 2^{GAINSEL}$.

The device-specific calibration values are stored in the User Configuration Block (UCB_USER) within the on-chip Flash memory. The area assigned to the EDSADC begins at offset 0080_H and provides records of two 32-bit words per channel. The channel-specific records, therefore, can be read from offset [0080_H + 8×CHNr.] within block UCB_USER. The table below shows the structure of a record.

Table 282 Structure of EDSADC Calibration Records (Generated at f_{MOD} = 26.67 MHz)

	Halfword 3	Halfword 2	Halfword 1	Halfword 0
Location CH0	0086_H	0084_H	0082_H	0080_H
Location CH1	$008E_H$	$008C_H$	$008A_H$	0088_H
:	:	:	:	:
Stored value	IRMS	Reserved	Reserved	Reserved

The parameters are stored in the following format:

Current = IRMSx × 0.01 µA, i.e. $03E8_H$ = 10 µA.

Example:

For R_{EXT} = 10 kOhm, IRMS = $042E_H$ (10.7 µA), C_{TANK} = 330 pF, f_{MOD} = 40 MHz, GAINSEL = 0:

The real current at 40 MHz, therefore, is I_{RMS} = 10.7 µA × 40 / 26.67 × 2^0 = 16.05 µA:

F_{GR} = 1 + (16.05 µA × 10 kOhm) / 5 V = 1.0321

F_{GC} = 1 + 16.05 µA / (40 MHz × 330 pF × 5 V) = 1.00024

The total factor will be $F_G = F_{GR} \times F_{GC}$ = 1.0321 × 1.00024 = 1.03235

Assuming a range adaptation factor of 1.2 (25 000 to 30 000), the overall factor would be 1.2 × 1.03235 = 1.2388, so the value for bitfield GAINFACTOR is 5 074 = $13D2_H$.