28.5.6 ARU Configuration Register Overview

Table 14 ARU Configuration Register Overview

Register name	Description	see Page
ARU_ACCESS	ARU access register	53
ARU_DATA_H	ARU access register upper data word	54
ARU_DATA_L	ARU access register lower data word	55
ARU_DBG_ACCESS0	ARU debug access channel 0	55
ARU_DBG_DATA0_H	ARU debug access 0 transfer register upper data word	57
ARU_DBG_DATA0_L	ARU debug access 0 transfer register lower data word	57
ARU_DBG_ACCESS1	ARU debug access channel 0	58
ARU_DBG_DATA1_H	ARU debug access 1 transfer register upper data word	59
ARU_DBG_DATA1_L	ARU debug access 1 transfer register lower data word	60
ARU_IRQ_NOTIFY	ARU interrupt notification register	60
ARU_IRQ_EN	ARU interrupt enable register	61
ARU_IRQ_FORCINT	ARU force interrupt register	62
ARU_IRQ_MODE	ARU interrupt mode register	63
ARU_CADDR_END	ARU caddr counter end value	63
ARU_CADDR	ARU caddr counter value	64
ARU_CTRL	ARU enable dynamic routing	65
ARU_[z]_DYN_CTRL	ARU z dynamic routing control register	66
ARU_[z]_DYN_RDADDR	ARU z read ID for dynamic routing	66
ARU_[z]_DYN_ROUTE_LOW	ARU z lower bits of DYN_ROUTE register	67
ARU_[z]_DYN_ROUTE_HIGH	ARU z higher bits of DYN_ROUTE register	68
ARU_[z]_DYN_ROUTE_SR_LOW	ARU z shadow register for ARU_[z]_DYN_ROUTE_LOW	68
ARU_[z]_DYN_ROUTE_SR_HIGH	ARU z shadow register for ARU_[z]_DYN_ROUTE_HIGH	69