- FIFO for buffering data from/to CPU with following features:
  - 8 FIFO stages based on 32 bit width
  - Configurable data alignment (byte, half word, word)
  - Configurable sizes for burst, transmit and receive package
  - FIFO usable as flow controller (seamless DMA flow)
- Advanced interrupt handling:
  - 4 data transfer interrupts (burst, last burst, single, last single)
  - Protocol interrupt with 7 sources (address match, general call, master code, arbitration lost, not-acknowledge received, transmission end, receive mode)
  - Error interrupt with 4 sources (FIFO transmit/receive overflow/underflow)
- Pretended Networking:
  - High-speed mode, fast mode and standard mode work with a minimum frequency of 5MHz in spb domain.

34.2 Overview

The I2C module communicates with the external world via a pair of I/O lines. A serial data line (SDA) and a serial clock line (SCL) carry the information between the devices. These lines are connected to a positive supply voltage via pull-up resistors. In quiescent state, when the bus is free, both lines are high. During communication the lines are alternatively pulled to low. The output stages of devices connected to the bus must have an open-drain (CMOS) or open-collector (bipolar) to perform a wired-AND function.

Figure 324 shows a block diagram of the I2C module.

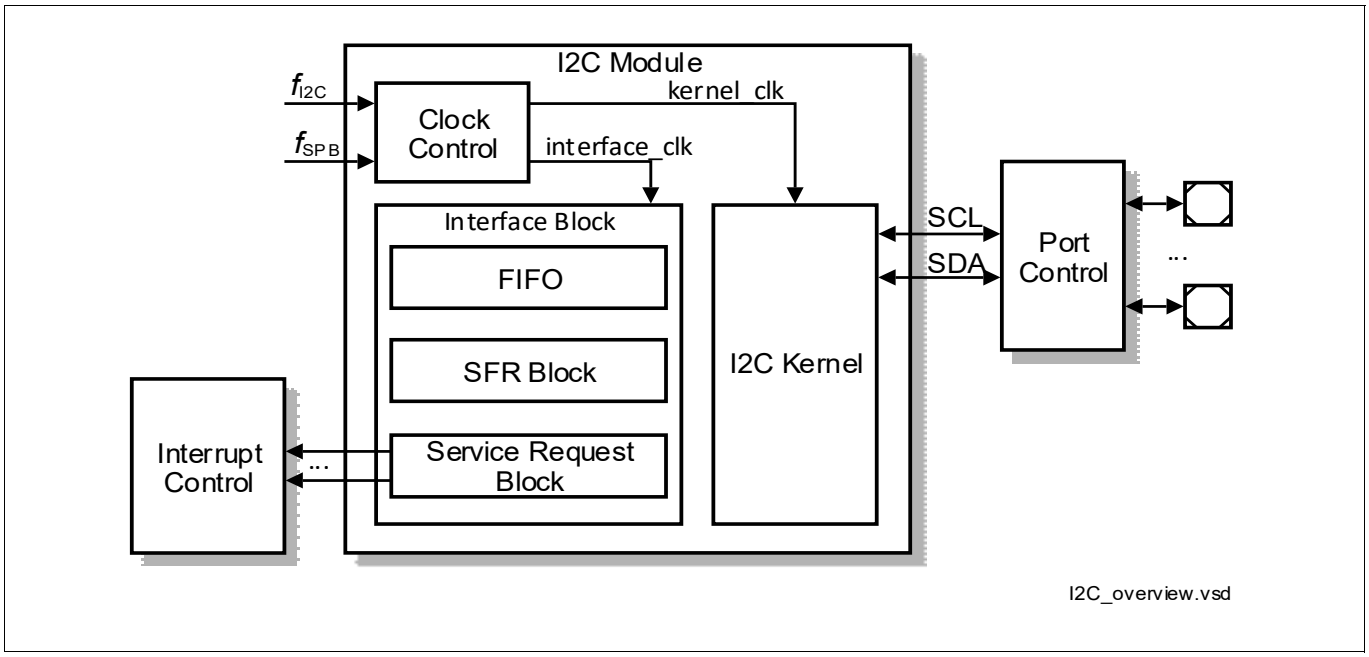

Figure 324 Block Diagram of the I2C Module

The I2C protocol was developed to provide a simple and efficient data transfer between multiple devices over a short distance. It uses a bidirectional serial bus with two wires.

The device can work as master or as slave. The master initiates the transfer, generates the clock pulses and terminates the transfer; it addresses a slave via a 7-bit or 10-bit address. Data can flow in either direction. In many applications there is only one master, typically a single-chip microcontroller, which communicates with several