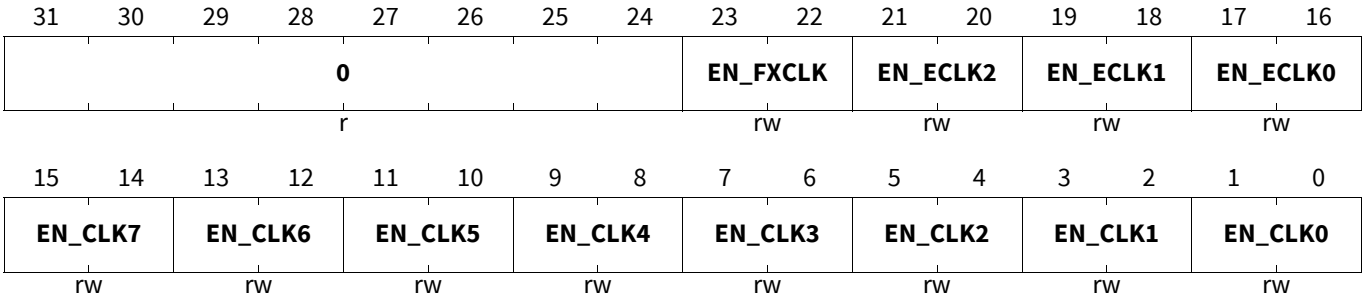
28.10.7 CMU Configuration Register Description

28.10.7.1 Register CMU_CLK_EN

CMU Clock Enable Register

CMU_CLK_EN
CMU Clock Enable Register **(000300_H)** **Application Reset Value: $0000\ 0000_H$**

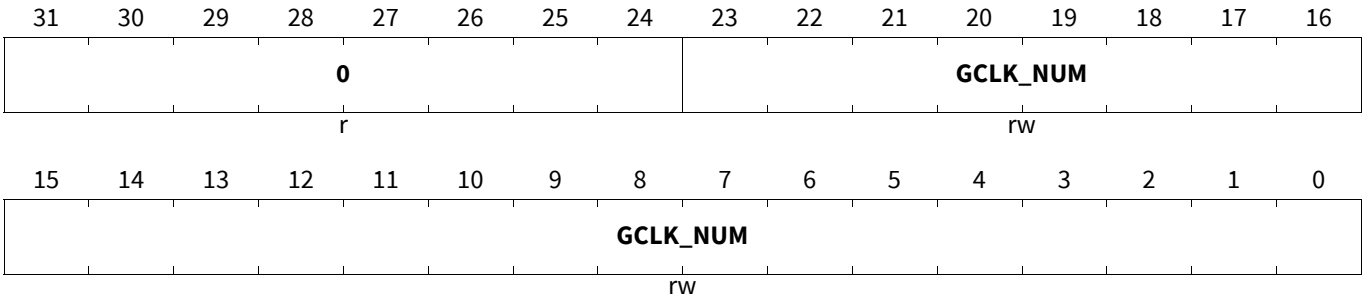


Field	Bits	Type	Description
EN_CLKx (x=0-7)	2*x+1:2*x	rw	**Enable clock source x** Any read access to an **EN_CLK[x]**, **EN_ECLK[z]** or **EN_FXCLK** bit field will always result in a value 00 or 11 indicating current state. A modification of the state is only performed with the values 01 and 10. Writing the values 00 and 11 is always ignored. Any disabling to **EN_CLK[x]** will be reset internal counters for configurable clocks. 00_B Clock source is disabled (ignore write access) 01_B Disable clock signal and reset internal states 10_B Enable clock signal 11_B Clock signal enabled (ignore write access)
EN_ECLKx (x=0-2)	2*x+17:2*x +16	rw	**Enable ECLK x generation sub-unit** Coding see bit EN_CLKx.
EN_FXCLK	23:22	rw	**Enable all CMU_FXCLK, see bits 1:0** An enable to **EN_FXCLK** from disable state will be reset internal fixed clock counters.
0	31:24	r	**Reserved** Read as zero, shall be written as zero

28.10.7.2 Register CMU_GCLK_NUM

CMU Global Clock Control Numerator

CMU_GCLK_NUM
CMU Global Clock Control Numerator **(000304_H)** **Application Reset Value: $0000\ 0001_H$**



Field	Bits	Type	Description
GCLK_NUM	23:0	rw	**GCLK_NUM** Value can only be modified when all clock enables **EN_CLK[x]** and the **EN_FXCLK** are disabled. The CMU hardware alters the content of **CMU_GCLK_NUM** and **CMU_GCLK_DEN** automatically to 0x1, if **CMU_GCLK_NUM** is specified less than **CMU_GCLK_DEN** or one of the values is specified with a value zero. Thus, a secure way for altering the values is writing twice to the register **CMU_GCLK_NUM** followed by a single write to register **CMU_GCLK_DEN**.
0	31:24	r	**Reserved** Read as zero, shall be written as zero

28.10.7.3 Register CMU_GCLK_DEN

CMU Global Clock Control Denominator

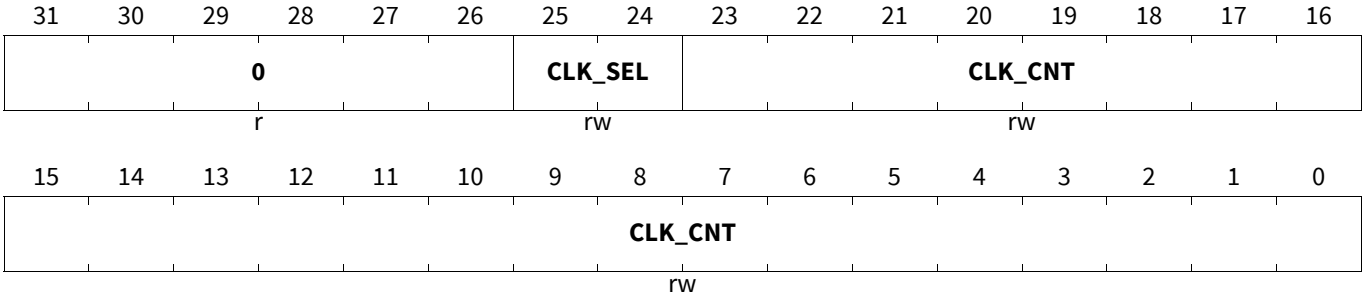
CMU_GCLK_DEN
CMU Global Clock Control Denominator **(000308_H)** **Application Reset Value: $0000\ 0001_H$**

Field	Bits	Type	Description
GCLK_DEN	23:0	rw	**GCLK_DEN** Value can only be modified when all clock enables **EN_CLK[x]** and the **EN_FXCLK** are disabled. The CMU hardware alters the content of **CMU_GCLK_NUM** and **CMU_GCLK_DEN** automatically to 0x1, if **CMU_GCLK_NUM** is specified less than **CMU_GCLK_DEN** or one of the values is specified with a value zero. Thus, a secure way for altering the values is writing twice to the register **CMU_GCLK_NUM** followed by a single write to register **CMU_GCLK_DEN**.
0	31:24	r	**Reserved** Read as zero, shall be written as zero

28.10.7.4 Register CMU_CLK_[z]_CTRL

CMU Control for Clock Source z

CMU_CLK_z_CTRL (z=0-7)
CMU Control for Clock Source z **($00030C_H$+z*4)** **Application Reset Value: 0000 0000_H**

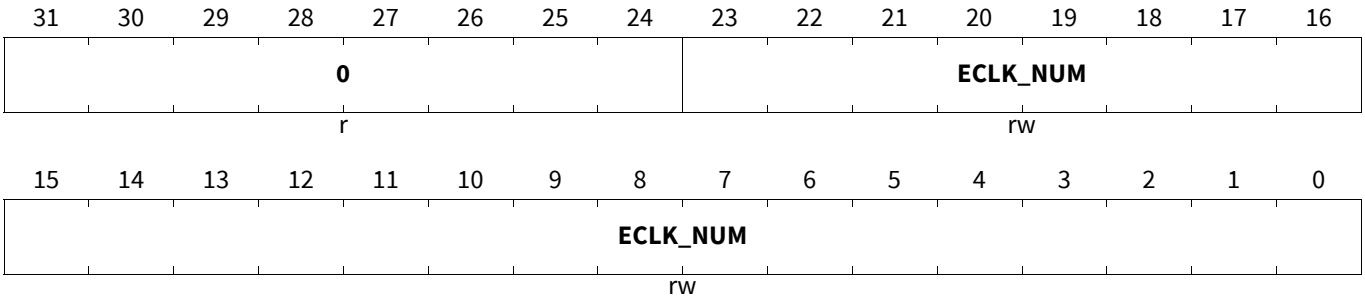


Field	Bits	Type	Description
CLK_CNT	23:0	rw	**Clock count** Defines count value for the clock divider. Value can only be modified when clock enable **EN_CLKz** and **EN_ECLK1** are disabled.
CLK_SEL	25:24	rw	**Clock source selection for CMU_CLKz** Value can only be modified when clock enable **EN_CLKz** and **EN_ECLK1** are disabled. *Note: The existence and interpretation of this bit field depends on z. z>5*
0	31:26	r	**Reserved** Read as zero, shall be written as zero.

28.10.7.5 Register CMU_ECLK_[z]_NUM

CMU External Clock z Control Numerator

CMU_ECLK_z_NUM (z=0-2)
CMU External Clock z Control Numerator (00032C$_H$+z*8) Application Reset Value: 0000 0001$_H$



Field	Bits	Type	Description
ECLK_NUM	23:0	rw	**ECLK_NUM** Numerator for external clock divider. Defines numerator of the fractional divider. *Note: Value can only be modified when clock enable **EN_ECLK[z]** disabled.* *Note: The CMU hardware alters the content of **CMU_ECLK_[z]_NUM** and **CMU_ECLK_[z]_DEN** automatically to 0x1, if **CMU_ECLK_[z]_NUM** is specified less than **CMU_ECLK_[z]_DEN** or one of the values is specified with a value zero. Thus, a secure way for altering the values is writing twice to the register **CMU_ECLK_[z]_NUM** followed by a single write to register **CMU_ECLK_[z]_DEN**.*
0	31:24	r	**Reserved** Read as zero, shall be written as zero

28.10.7.6 Register CMU_ECLK_[z]_DEN

CMU External Clock z Control Denominator

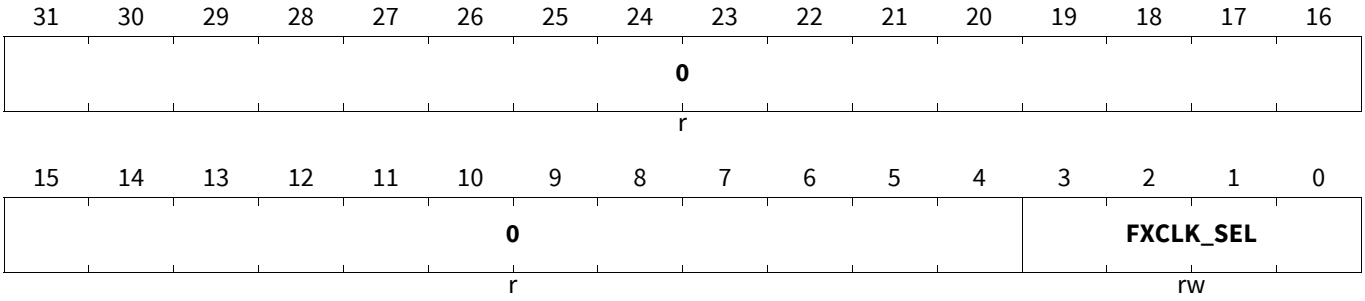
CMU_ECLK_z_DEN (z=0-2)
CMU External Clock z Control Denominator (000330$_H$+z*8) Application Reset Value: 0000 0001$_H$

Field	Bits	Type	Description
ECLK_DEN	23:0	rw	**ECLK_DEN** Denominator for external clock divider. Defines denominator of the fractional divider *Note: Value can only be modified when clock enable **EN_ECLK[z]** disabled.* *Note: The CMU hardware alters the content of **CMU_ECLK_[z]_NUM** and **CMU_ECLK_[z]_DEN** automatically to 0x1, if **CMU_ECLK_[z]_NUM** is specified less than **CMU_ECLK_[z]_DEN** or one of the values is specified with a value zero. Thus, a secure way for altering the values is writing twice to the register **CMU_ECLK_[z]_NUM** followed by a single write to register **CMU_ECLK_[z]_DEN**.*
0	31:24	r	**Reserved** Read as zero, shall be written as zero

28.10.7.7 Register CMU_FXCLK_CTRL

CMU Control FXCLK Sub-Unit Input Clock

CMU_FXCLK_CTRL
CMU Control FXCLK Sub-Unit Input Clock (000344$_H$) Application Reset Value: 0000 0000$_H$



Field	Bits	Type	Description
FXCLK_SEL	3:0	rw	**Input clock selection for EN_FXCLK line** This value can only be written when the CMU_FXCLK generation is disabled. See bits 23..22 in register **CMU_CLK_EN**. Other values for FXCLK_SEL are reserved and should not be used, but they behave like FXCLK_SEL = 0. 0_H CMU_GCLK_EN selected 1_H CMU_CLK0 selected 2_H CMU_CLK1 selected 3_H CMU_CLK2 selected 4_H CMU_CLK3 selected 5_H CMU_CLK4 selected 6_H CMU_CLK5 selected 7_H CMU_CLK6 selected 8_H CMU_CLK7 selected CMU_CLK7 selected
0	31:4	r	**Reserved** Read as zero, shall be written as zero.

28.10.7.8 Register CMU_GLB_CTRL

CMU Synchronizing ARU and Clock Source

CMU_GLB_CTRL
CMU Synchronizing ARU and Clock Source (000348$_H$) Application Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0															ARU_ADDR_RSTGLB
r															rw

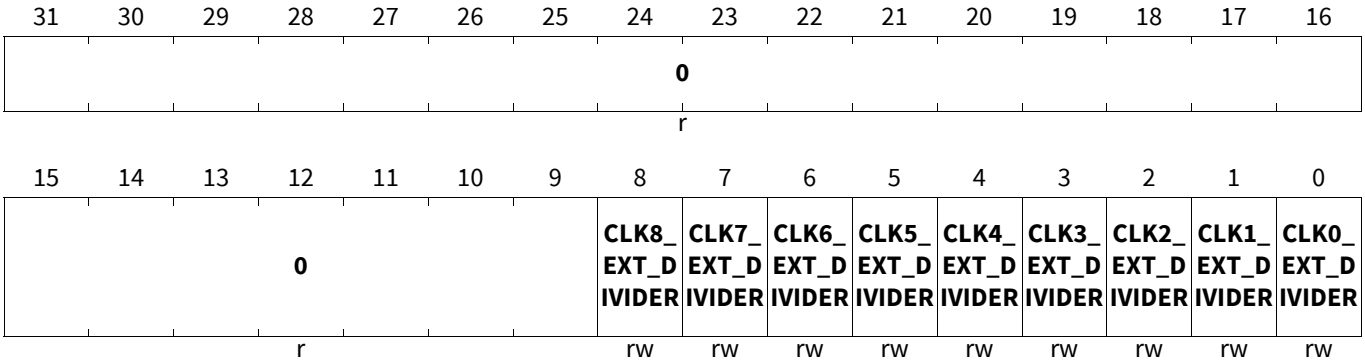
Field	Bits	Type	Description
ARU_ADDR_RSTGLB	0	rw	**Reset ARU caddr counter and ARU dynamic route counter** Writing value 1 to this bit field results in a request to reset the ARU caddr counter and ARU dynamic route counter. The next following write access to register **CMU_CLK_EN** applies the ARU caddr counter reset, ARU dynamic route counter reset and resets this bit. This feature can be used to synchronize the ARU round trip time to the CMU clocks. This bit is write protected. Before writing to this bit set bit RF_PROT of register **GTM_CTRL** to 0.

Field	Bits	Type	Description
0	31:1	r	**Reserved** Read as zero, shall be written as zero

28.10.7.9 Register CMU_CLK_CTRL

CMU Control for Clock Source Selection

CMU_CLK_CTRL
CMU Control for Clock Source Selection **(00034C$_H$)** **Application Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
CLK0_EXT_DIVIDER	0	rw	**Clock source selection for CMU_CLK_0_CTRL** Value can only be modified when clock enable **EN_CLK0** and **EN_ECLK1** are disabled. 0_B Use Clock Source CMU_GCLK_EN 1_B Use Clock Source CMU_ECLK1
CLK1_EXT_DIVIDER	1	rw	**Clock source selection for CMU_CLK_1_CTRL** Value can only be modified when clock enable **EN_CLK1** and **EN_ECLK1** are disabled.
CLK2_EXT_DIVIDER	2	rw	**Clock source selection for CMU_CLK_2_CTRL** Value can only be modified when clock enable **EN_CLK2** and **EN_ECLK1** are disabled.
CLK3_EXT_DIVIDER	3	rw	**Clock source selection for CMU_CLK_3_CTRL** Value can only be modified when clock enable **EN_CLK3** and **EN_ECLK1** are disabled.
CLK4_EXT_DIVIDER	4	rw	**Clock source selection for CMU_CLK_4_CTRL** Value can only be modified when clock enable **EN_CLK4** and **EN_ECLK1** are disabled.
CLK5_EXT_DIVIDER	5	rw	**Clock source selection for CMU_CLK_5_CTRL** Value can only be modified when clock enable **EN_CLK5** and **EN_ECLK1** are disabled.
CLK6_EXT_DIVIDER	6	rw	**Clock source selection for CMU_CLK_6_CTRL** Value can only be modified when clock enable **EN_CLK6** and **EN_ECLK1** are disabled.

Field	Bits	Type	Description
CLK7_EXT_DIVIDER	7	rw	**Clock source selection for CMU_CLK_7_CTRL** Value can only be modified when clock enable **EN_CLK7** and **EN_ECLK1** are disabled.
CLK8_EXT_DIVIDER	8	rw	**Clock source selection for CMU_CLK8** Value can only be modified when **EN_ECLK0** is disabled. 0_B Use Clock Source CLS0_CLK 1_B Use Clock Source CMU_ECLK0
0	31:9	r	**Reserved** Read as zero, shall be written as zero.