28.3.2 Document Structure

The structure of this document is motivated out of the aforementioned sub-module classes. **Section 28.4** describes the dedicated GTM implementation this specification is written for. It gives an overview about the implemented sub-modules.

The following sections **Section 28.5** up to **Section 28.12** deals with the so called infrastructure components for routing, clock management and common time base functions. Sections **Section 28.13** to **Section 28.16** describe the signal input and output modules while the following **Section 28.17** explains the signal processing and generation sub-module with **Section 28.18** its memory configuration. The next sections **Section 28.19** to **Section 28.21** provides a detailed description of application specific modules like the MAP, DPLL and SPE. The last sections **Section 28.23** to **Section 28.24** provide to safety related modules (not part of the Infineon safety manual) like CMP and MON sub-modules. **Section 28.22** describes a module that bundles several interrupts coming from the other sub-modules and connect them to the outside world.

Note: Infineon: CMP and MON are not part of the safety manual. As safety measure the IOM is provided in combination with GTP1/2 or CCU6.

Table 5 Sub-module groups

Chapter	Sub-module	Group
Section 28.5	Advanced Routing Unit (ARU)	Infrastructure components
Section 28.6	Broadcast Module (BRC)	Infrastructure components
Section 28.7	First In First Out Module (FIFO)	Infrastructure components
Section 28.8	AEI-to-FIFO Data Interface (AFD)	Infrastructure components
Section 28.9	FIFO-to-ARU Interface (F2A)	Infrastructure components
Section 28.10	Clock Management Unit (CMU)	Infrastructure components
Section 28.11	Cluster Configuration Module (CCM)	Infrastructure components
Section 28.12	Time Base Unit (TBU)	Infrastructure components
Section 28.13	Timer Input Module (TIM)	IO Modules
Section 28.14	Timer Output Module (TOM)	IO Modules
Section 28.15	ARU-connected Timer Output Module (ATOM)	IO Modules
Section 28.16	Dead Time Module (DTM)	IO Modules
Section 28.17	Multi Channel Sequencer (MCS)	Signal generation and processing
Section 28.18	Memory Configuration (MCFG)	Memory for signal generation and processing
Section 28.19	TIM0 Input Mapping Module (MAP)	Dedicated