Field	Bits	Type	Description
STR6_CONF	5:4	rw	**Reconfiguration of stream 6 to FIFO channel 2** Write of following double bit values is possible: The write protected bits of register **F2A[i]_CTRL** are only writable if the corresponding enable bit STR2_EN and STR6_EN of register **F2A_ENABLE** is cleared. 00_B Write: don't care, bits 1:0 will not be changed / Read: Stream 6 is mapped to FIFO buffer 6 01_B Stream 6 is mapped to FIFO buffer 6 10_B Stream 6 s mapped to FIFO buffer 2 11_B Write: don't care, bits 1:0 will not be changed / Read: Stream 6 is mapped to FIFO buffer 2
STR7_CONF	7:6	rw	**Reconfiguration of stream 7 to FIFO channel 3** Write of following double bit values is possible: The write protected bits of register **F2A[i]_CTRL** are only writable if the corresponding enable bit STR3_EN and STR7_EN of register **F2A_ENABLE** is cleared. 00_B Write: don't care, bits 1:0 will not be changed / Read: Stream 7 is mapped to FIFO buffer 7 01_B Stream 7 is mapped to FIFO buffer 7 10_B Stream 7 s mapped to FIFO buffer 3 11_B Write: don't care, bits 1:0 will not be changed / Read: Stream 7 is mapped to FIFO buffer 3
0	31:8	r	**Reserved** Read as zero, shall be written as zero.

28.10 Clock Management Unit (CMU)

28.10.1 Overview

The Clock Management Unit (CMU) is responsible for clock generation of the counters and of the GTM. The CMU consists of three sub-units that generate different clock sources for the whole GTM. The primary clock source for this sub-module is the cluster 0 clock signal cls0_clk which is defined by the value of bit field CLS0_CLK_DIV in the register GTM_CLS_CLK_CFG. **Figure 27** shows a block diagram of the CMU.

The Configurable Clock Generation (CFGU) sub-unit provides eight dedicated clock sources for the following GTM modules: TIM, ATOM, TBU, and MON. Each instance of such a module can choose an arbitrary clock source, in order to specify wide-ranging time bases.

The Fixed Clock Generation (FXU) sub-unit generates predefined non-configurable clocks *CMU_FXCLK[y]* (y: 0…4) for the TOM modules and the MON module. The *CMU_FXCLK[y]* signals are derived from the *CMU_GCLK_EN* signal generated by the Global Clock Divider. The dividing factors are defined as 2^0, 2^4, 2^8, 2^{12}, and 2^{16}.

The External Clock Generation (EGU) sub-unit is able to generate up to three chip external clock signals visible at *CMU_ECLK[z]* (z: 0…2) with a duty cycle of about 50%.

The External Clock Generation (EGU) sub-unit is able to generate clock *CMU_CLK8* for module CCM to manage 2 clock domains.

The clock source signals *CMU_CLK[x]* (x: 0…7) and *CMU_FXCLK[y]* are implemented in form of enable signals for the corresponding registers, which means that the actual clock signal of all registers always use the *CLS0_CLK* signal.

The four configurable clock signals *CMU_CLK0*, *CMU_CLK1*, *CMU_CLK6* and *CMU_CLK7* are used for the TIM filter counters.

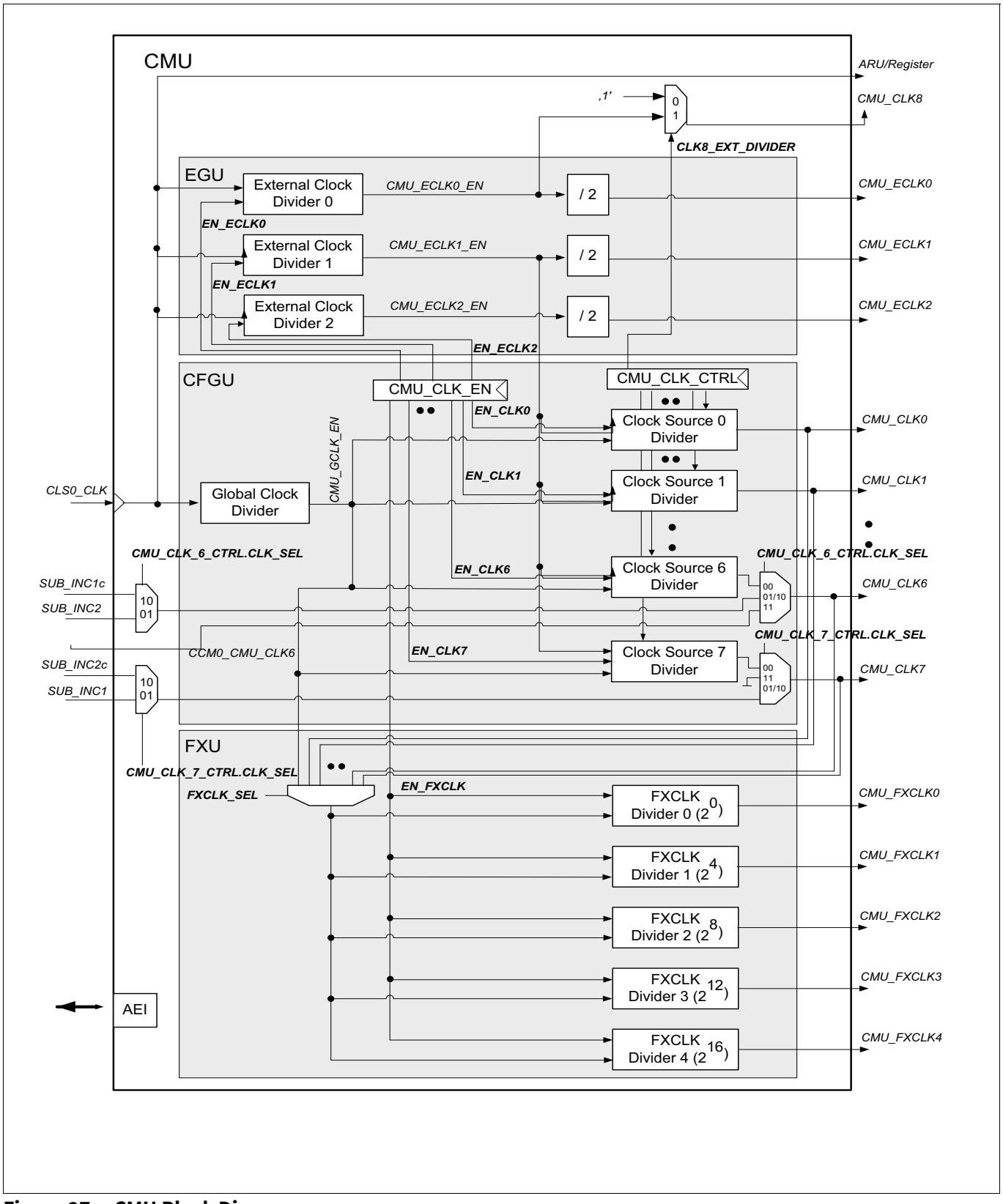

Figure 27 CMU Block Diagram