27.4.4 Interrupt Registers

Interrupt Control Register

The two compare match interrupts of the STM are controlled by the STM Interrupt Control Register.

ICR
Interrupt Control Register **(003C$_H$)** **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0									CMP1OS	CMP1IR	CMP1EN	0	CMP0OS	CMP0IR	CMP0EN
r									rw	rh	rw	r	rw	rh	rw

Field	Bits	Type	Description
CMP0EN	0	rw	**Compare Register CMP0 Interrupt Enable Control** This bit enables the compare match interrupt with compare register CMP0. 0_B Interrupt on compare match with CMP0 disabled 1_B Interrupt on compare match with CMP0 enabled
CMP0IR	1	rh	**Compare Register CMP0 Interrupt Request Flag** This bit indicates whether or not a compare match event of compare register CMP0 has occured. CMP0IR can be cleared by software and can be set by software, too (see ISCR register). After a STM reset operation, CMP0IR is immediately set as a result of a compare match event with the reset values of the STM and the compare registers CMP0. *Note: This flag does not gate the interrupt generation. i.e., even if this flag is not cleared, compare match event interrupts are forwarded if CMPxEN is set.* 0_B A compare match event has not been detected since the bit was last cleared. 1_B A compare match event has been detected.
CMP0OS	2	rw	**Compare Register CMP0 Interrupt Output Selection** This bit determines the interrupt output that is activated on a compare match event of compare register CMP0. 0_B Interrupt output STMIR0 selected 1_B Interrupt output STMIR1 selected

Field	Bits	Type	Description
CMP1EN	4	rw	**Compare Register CMP1 Interrupt Enable Control** This bit enables the compare match interrupt with compare register CMP1. 0_B Interrupt on compare match with CMP1 disabled 1_B Interrupt on compare match with CMP1 enabled
CMP1IR	5	rh	**Compare Register CMP1 Interrupt Request Flag** This bit indicates whether or not a compare match event of compare register CMP1 has occured. CMP1IR can be cleared by software and can be set by software, too (see ISCR register). After a STM reset operation, CMP1IR is immediately set as a result of a compare match event with the reset values of the STM and the compare register CMP1. *Note: This flag does not gate the interrupt generation. i.e., even if this flag is not cleared, compare match event interrupts are forwarded if CMPxEN is set.* 0_B A compare match event has not been detected since the bit was last cleared. 1_B A compare match event has been detected.
CMP1OS	6	rw	**Compare Register CMP1 Interrupt Output Selection** This bit determines the interrupt output that is activated on a compare match event of compare register CMP1. 0_B Interrupt output STMIR0 selected 1_B Interrupt output STMIR1 selected
0	3, 31:7	r	**Reserved** Read as 0; should be written with 0.

Interrupt Set/Clear Register

The bits in the STM Interrupt Set/Clear Register make it possible to set or cleared the compare match interrupt request status flags of register ICR.

Note: Reading register ISCR always returns 0000 0000$_H$.

ISCR

Interrupt Set/Clear Register (0040$_H$) Application Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0												CMP1IRS	CMP1IRR	CMP0IRS	CMP0IRR
r												w	w	w	w

Field	Bits	Type	Description
CMP0IRR	0	w	**Reset Compare Register CMP0 Interrupt Flag** 0_B Bit ICR.CMP0IR is not changed. 1_B Bit ICR.CMP0IR is cleared.
CMP0IRS	1	w	**Set Compare Register CMP0 Interrupt Flag** 0_B Bit ICR.CMP0IR is not changed. 1_B Bit ICR.CMP0IR is set. The state of bit CMP0IRR is “don’t care” in this case.
CMP1IRR	2	w	**Reset Compare Register CMP1 Interrupt Flag** 0_B Bit ICR.CMP1IR is not changed. 1_B Bit ICR.CMP1IR is cleared.
CMP1IRS	3	w	**Set Compare Register CMP1 Interrupt Flag** 0_B Bit ICR.CMP1IR is not changed. 1_B Bit ICR.CMP1IR is set. The state of bit CMP1IRR is “don’t care” in this case.
0	31:4	r	**Reserved** Read as 0; should be written with 0.