33.5 Filter Chain

The result data words are generated by feeding the input data stream through a chain of filter elements and decimating it by a selectable ratio.

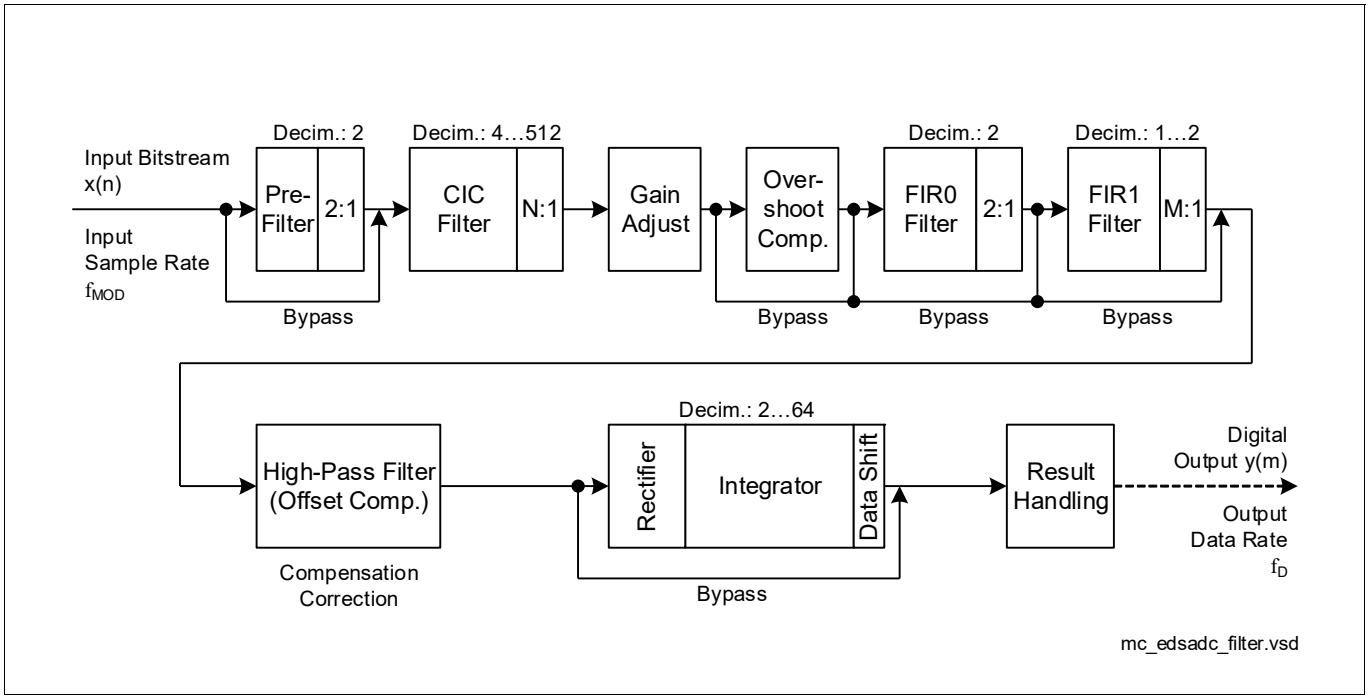


Figure 297 Structure of the Filter Chain

Most elements of the filter can be bypassed, i.e. the filter chain is configurable and its behavior can be adapted to the requirements of the actual application. This comprises the frequency attenuation as well as the total decimation rate.

The filter chain consists of the following elements:

- **CIC Filter**
- **Gain Correction**
- **Overshoot Compensation**
- **FIR Filters**
- **Offset Compensation**
- **Integrator Stage**

*Note: Reconfiguring filter parameters while the channel is active incurs some implications. Refer to **Section 33.3.1**.*

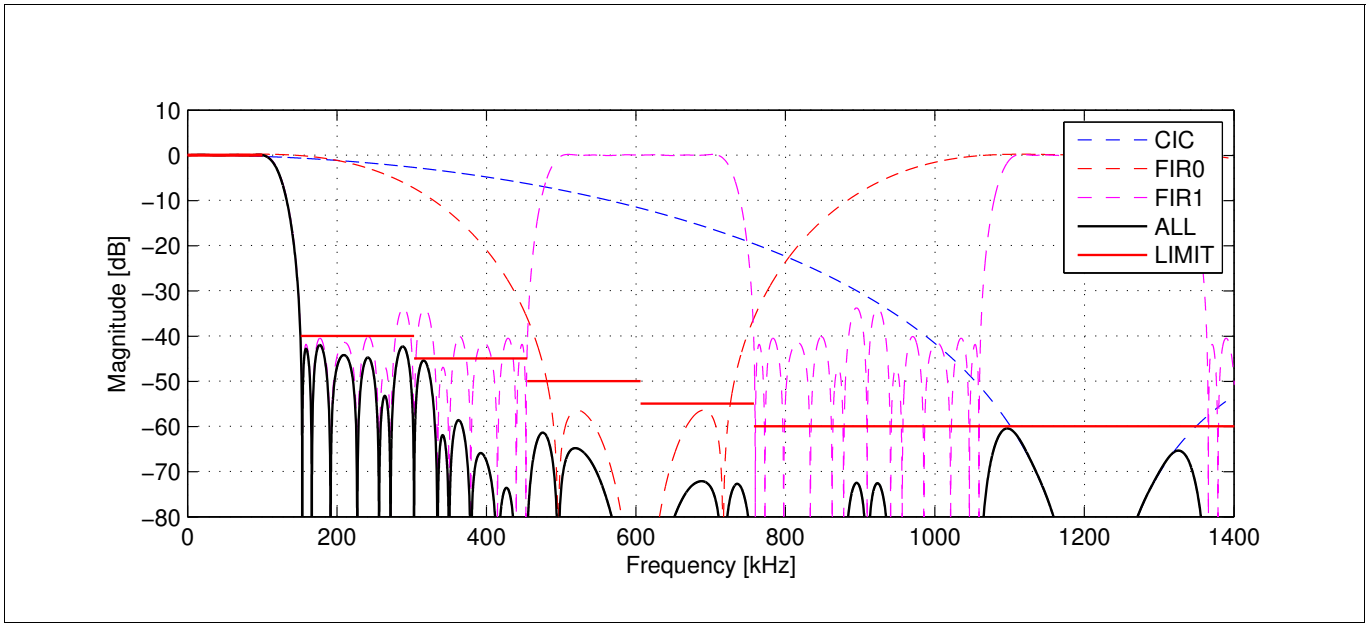


Figure 298 Frequency Response of the Complete Filter Chain (Example for 100 kHz Passband Setup)

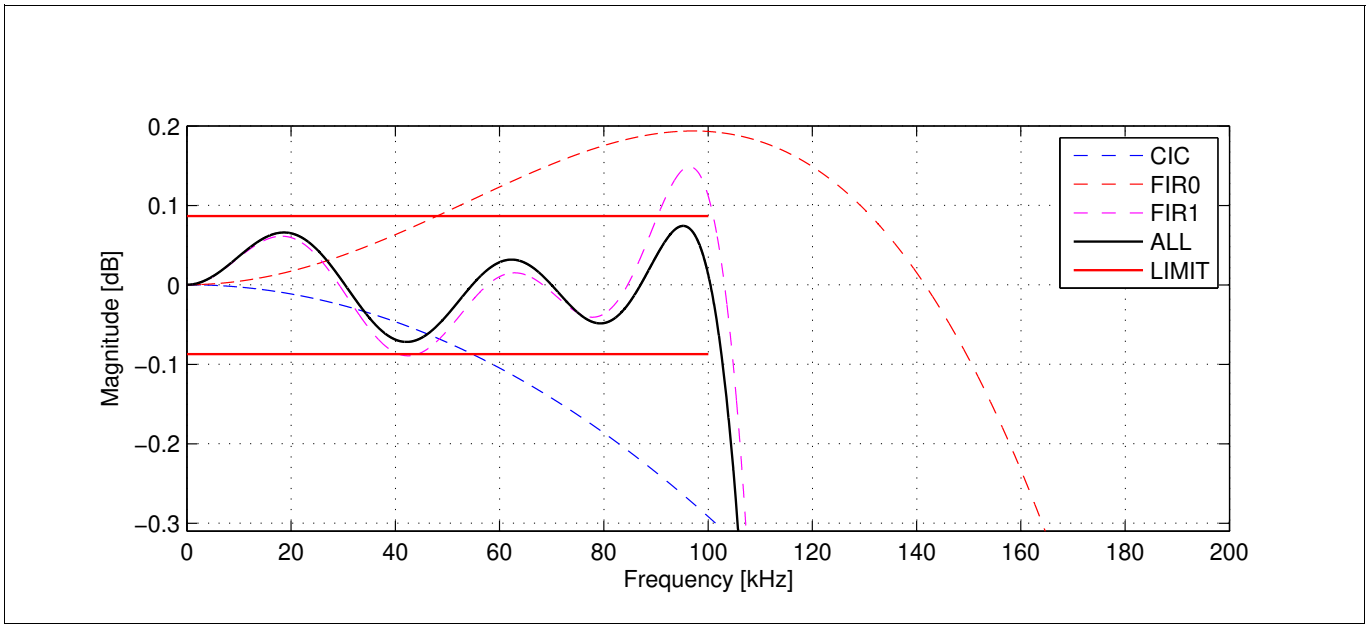


Figure 299 Passband Ripple (Example for 100 kHz Passband Setup)

33.5.1 CIC Filter

The Cascaded Integrator Comb filter (CIC filter, a.k.a. SINC filter) is a simple but very efficient low-pass filter. Three comb filter stages are cascaded to improve the frequency characteristics (CIC3). The decimation rate is programmable within a wide range from 4 to 512.

A prefilter reduces the data rate for modulator frequencies above 20 MHz. The prefilter is a CIC3 filter with a fixed decimation rate of 2.

To synchronize filters of different channels with fine granularity, the decimation counter starts from an arbitrary start value. This start value can be different from the decimation factor and is loaded only once when the counter is started.

The decimation counter is also restarted (i.e. loaded with the start value) when the selected integration trigger event occurs (see **Section 33.5.6**).

Table 283 CIC Filter Properties (N = Decimation Rate)

Stages	Data Width	Maximum Delay	Peak Output Value
CIC3	25 bits signed	3N	[-N^3, +N^3]

The CIC3 filter consists of 3 cascaded CIC filter stages.

Frequency domain, frequency response function:

$$H(z) = \left(\frac{1 - z^{-N}}{1 - z^{-1}} \right)^{k}$$

$$\left| H(j\omega) \right| = \left(\frac{\sin(\omega N / 2)}{\sin(\omega / 2)} \right)^{3}$$

Time domain:

The figure below illustrates the response of the CIC3 filter:

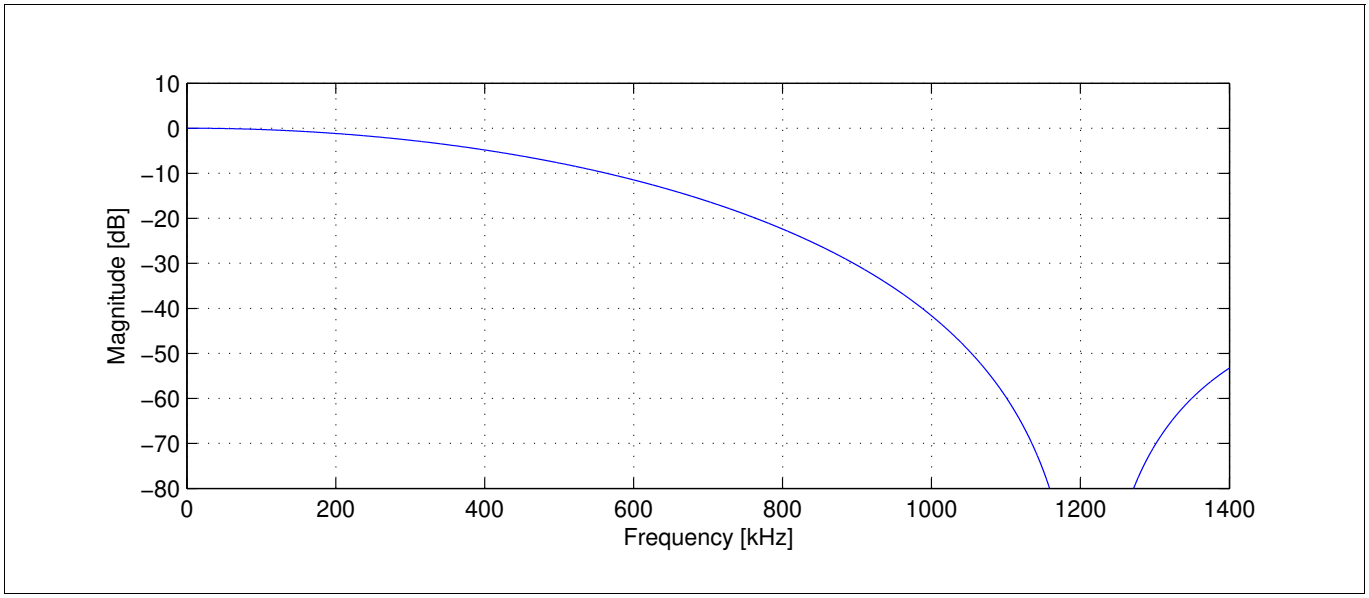


Figure 300 CIC3 Filter Frequency Response (Example for 1.212 MHz Output Data Rate)

Data Shifter and Decimation Factor

At the CIC filter output the valid data bits are selected for the subsequent blocks. The selected portion of the filter output is determined by the selected decimation factor and the employed modulator. These parameters define the maximum possible data value and, hence, the proper position for the extracted output value. During operation, the data shifter is controlled by bitfield GAINCORRx.CICSHIFT, during calibration by bitfield GAINCTRx.CICSHIFT.

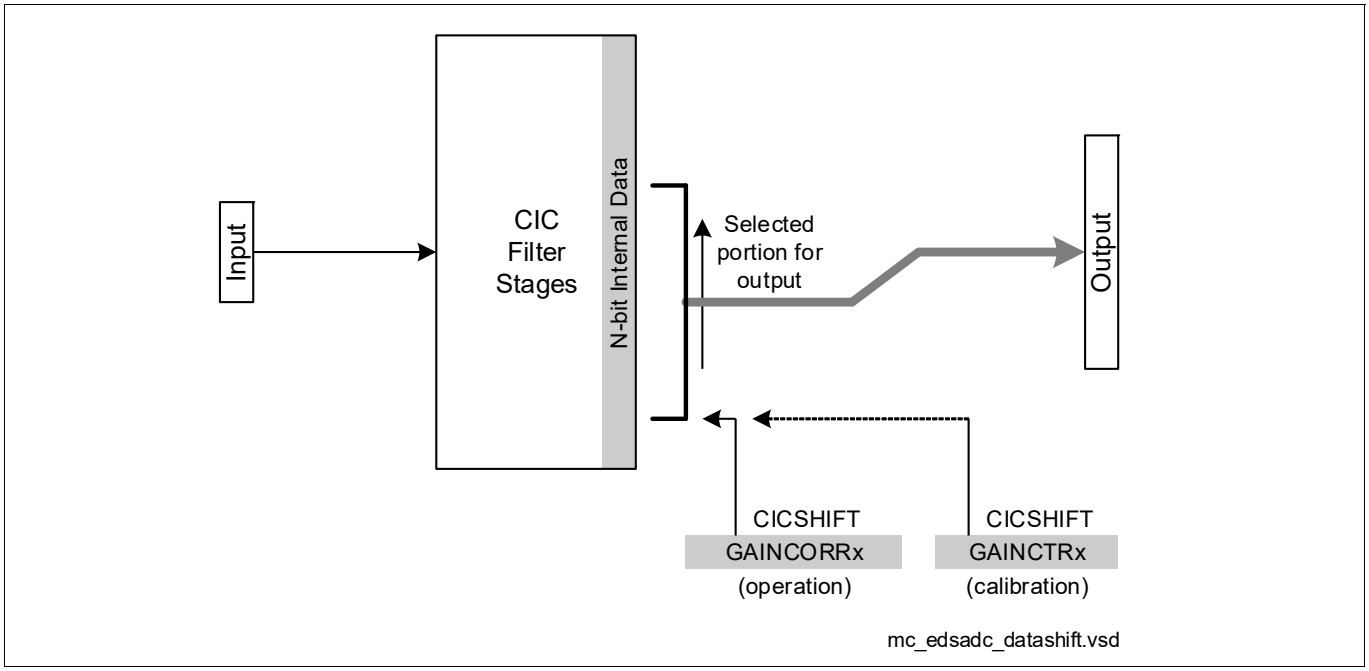


Figure 301 Data Shift Unit

The value for bitfield CICSHIFT is determined with this formula:

<CICSHIFT> = roundup(14 - ld(2 × AFS / (N^3 × 4 × FM)))

The following parameters are used:

- N = selected decimation factor
- AFS = calibrated full-scale value (25 000 after reset), refers to the analog full-scale ($V_{IN} = V_{AREF}$)
- FM = modulator gain factor
  - on-chip modulator: FM = 0.6945
  - external modulator: FM depends on used type

The gap that comes from the rounding in above formula can be closed by computing a corresponding gain correction factor:

<GAINFACTOR> = truncate(((2 × AFS / (N^3 × 4 × FM)) × 2^(<CICSHIFT>-14)) × 4096)

Example:

For N = 50, on-chip modulator:

N^3 × 4 × 0.6945 = 347 250

<CICSHIFT> = roundup(14 - ld(2 × 25 000 / 347 250)) = roundup(14 - (-2.796)) = 17 (11_H)

The correction factor will be:

<GAINFACTOR> = (2 × 25 000 / 347 250) × 2^3 = 1.1519

The bitfield value will then be truncate(1.1519 × 4 096) = truncate(4 718.1824) = 4 718 = $126E_H$.

33.5.2 Gain Correction

Gain calibration is done by multiplying the raw results with a correction value and a calibration value.

The application correction value is determined by the application based on the selected decimation factor etc., and is used to compensate the reduced digital gain that results from decimation factors in the CIC filter that are not 2^N (see **"Data Shifter and Decimation Factor" on Page 45**).

The calibration value is determined during the calibration sequence by the calibration algorithm. The automatic calibration algorithm normalizes the overall gain factor of the filter chain to 1.000, independent of their configuration. The full-scale value of the result is adapted to <CALTARGET> (25 000 after reset), representing the reference voltage.

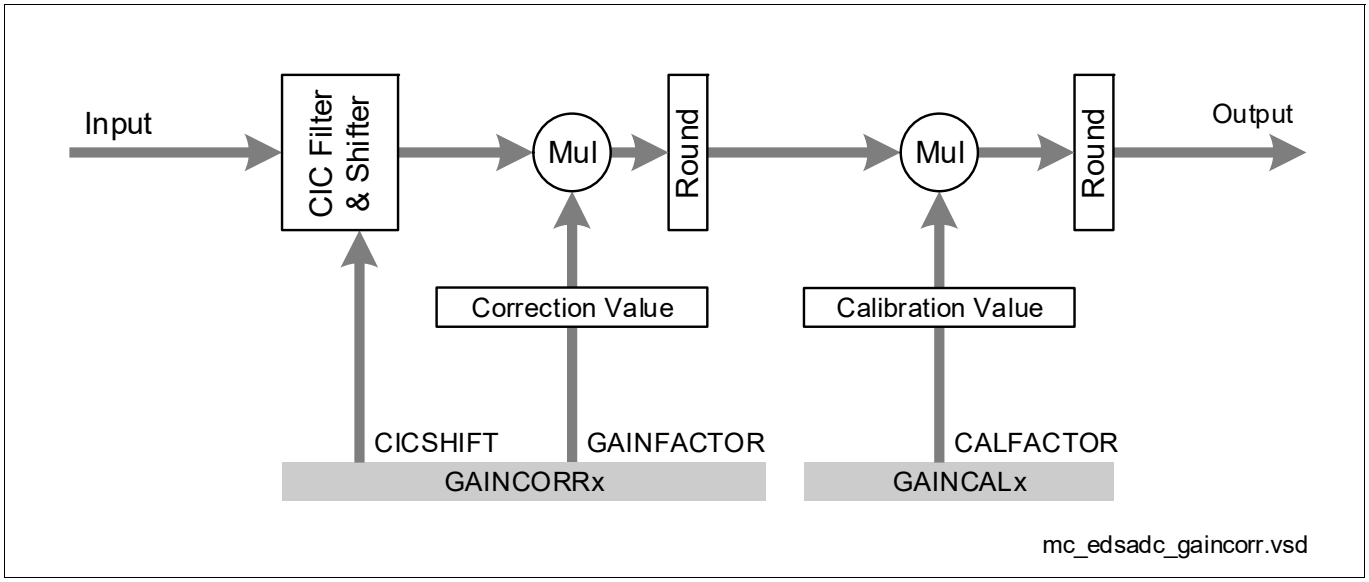


Figure 302 Gain Correction

Note: The calibration algorithm ensures that the configured target value (CALTARGET) is reached at the output of the gain correction unit within the specified precision when $V_{IN} = V_{AREF}$.

The correction value in register GAINCORR is calculated from application parameters either during compile time for static configurations, or during run time for dynamic configurations.

The calibration value in register GAINCAL is generated automatically by the calibration algorithm. This value is generated during the initial startup calibration and is adapted by subsequent calibration cycles that are triggered either by software or automatically.

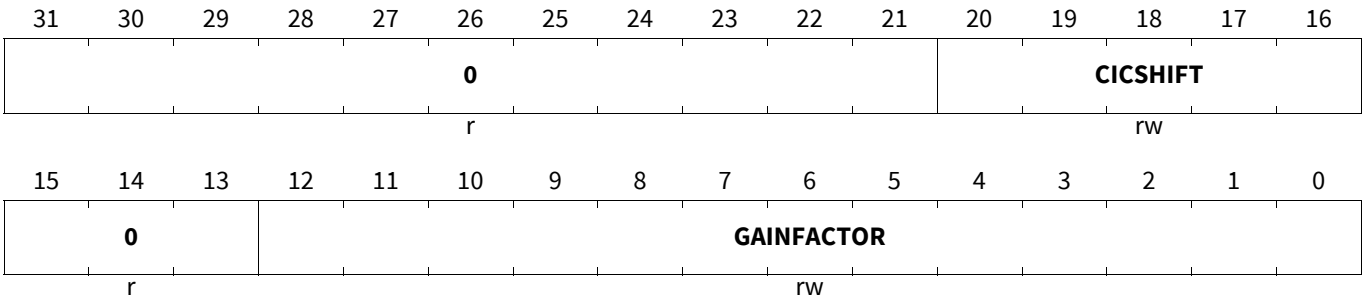
Both factors can be in the range of 0.000 to 1.999, with an initial value of 1.000.

While the calibration sequence is executing, the configuration selected for operation is replaced with the configuration selected for calibration (in register **GAINCTRx (x=0-13)**). Configure both settings before starting a channel.

*Note: An overview of the calibration mechanism is given in **"Calibration Support" on Page 36**. The formula to determine the GAINFACTOR is given in section **"Data Shifter and Decimation Factor" on Page 45**.*

Gain Correction Register x

GAINCORRx (x=0-13)
Gain Correction Register x **(0144_H+x*100_H)** **Application Reset Value: 0000 1000_H**



Field	Bits	Type	Description
GAINFACTOR	12:0	rw	**Multiplication Factor for Gain Correction** The resulting factor is (<GAINFACTOR> / 4 096)
CICSHIFT	20:16	rw	**Position of the CIC Filter Output Shifter** Selects the valid outputs bits from the CIC filter, depending on the chosen decimation factor (see formula above) $1D_H$ … $1F_H$ are reserved. 00_H Use bits 0 ... 16 … $1C_H$ Use bits 28 ... 44
0	15:13, 31:21	r	**Reserved, write 0, read as 0**

33.5.3 Overshoot Compensation

Due to their properties, the FIR filters tend to produce overshoots when the input signal changes rapidly. The overshoot compensation block monitors the data flow, detects a step in the input signal (rapid change), and recontours the signal so the FIR filters do not produce the unwanted overshoot.

Several aspects of the overshoot compensation are configurable via register **OVSCFGx (x=0-13)**:

- **Step Detection Threshold**
  Defines the numeric difference between samples that activates the overshoot compensation (SDTH). The threshold is compared to the magnitude of the difference, i.e. it is valid for both directions signal change.
- **Step Detection Mode**
  Defines if the current sample is compared to the last sample or to the second-last sample (SDM).
- **Slew Rate Filter Run Time**
  Defines the duration of the overshoot compensation (SRFRT).
- **Slew Rate Filter Strength**
  Defines the signal recontouring effect (SRFS).

The figure below shows how overshoot compensation modifies the output signal generated by the FIR filters.

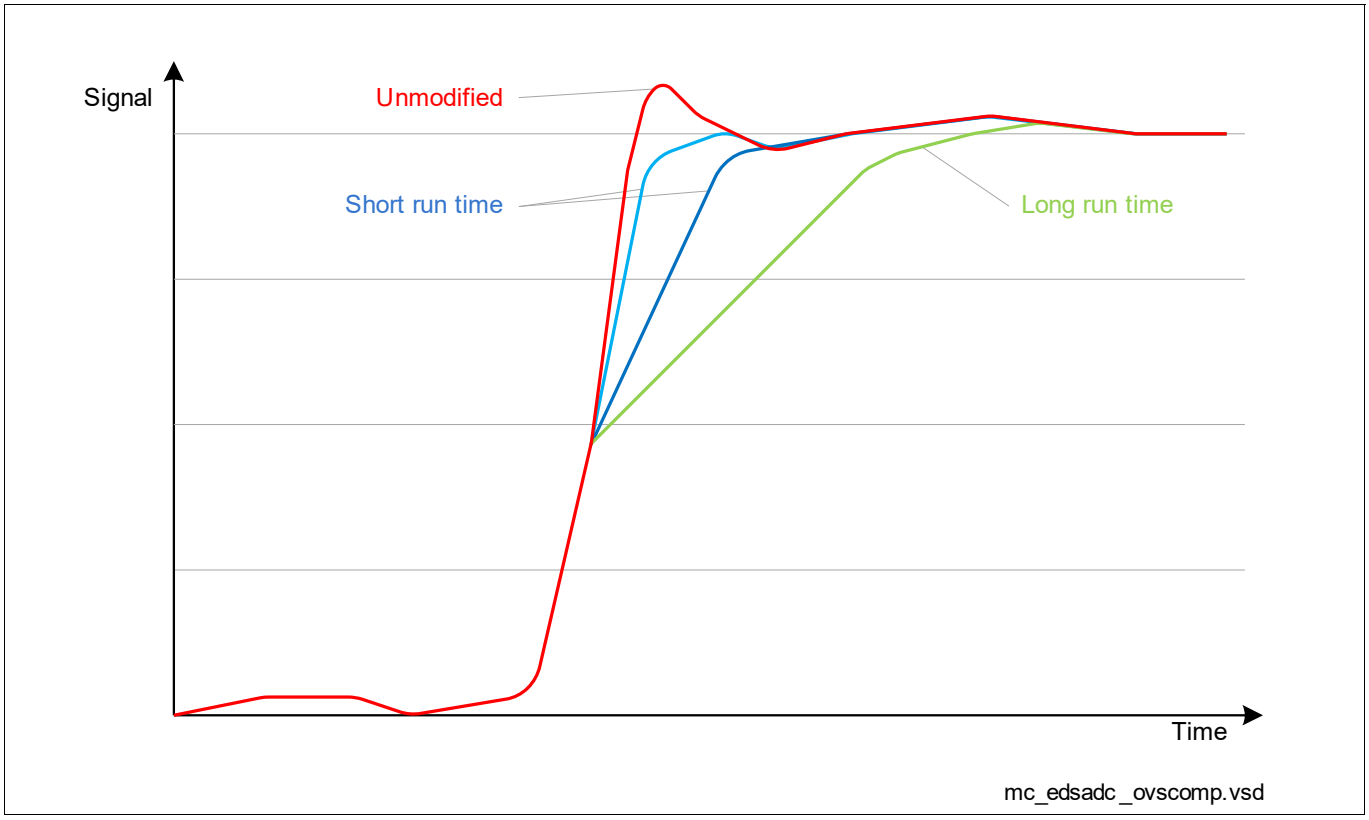


Figure 303 Overshoot Compensation Effects

Overshoot Compensation Cfg. Register x

OVSCFGx (x=0-13)

Overshoot Compensation Cfg. Register x (011C$_H$+x*100$_H$) Application Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0					SDTH										
r					rw										

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0											SDM	SRFRT		SRFS	
r											rw	rw		rw	

Field	Bits	Type	Description
SRFS	1:0	rw	**Slew Rate Filter Strength** Defines the time constant for the slew rate filter. 00_B Minimum filter effect, early attenuation, linear operation 01_B Weak filter effect 10_B Medium filter effect 11_B Maximum filter effect, steep beginning, smooth end
SRFRT	3:2	rw	**Slew Rate Filter Run Time** Defines the time constant for the slew rate filter. 00_B 2 input cycles 01_B 4 input cycles 10_B 8 input cycles 11_B 16 input cycles
SDM	4	rw	**Step Detection Mode** Defines when the slew rate filter is activated. 0_B Compare threshold to difference of current and last input 1_B Compare threshold to difference of current and second-last input
SDTH	26:16	rw	**Step Detection Threshold** Defines the threshold value (magnitude) used for step detection. The threshold value is <SDTH> × 32 000_H 0 (slew rate filter active all the time) 001_H 32 … $7FF_H$ 65504
0	15:5, 31:27	r	**Reserved, write 0, read as 0**

33.5.4 FIR Filters

The FIR filter further attenuates the higher frequency bands that pass the CIC filter. This improves the overall frequency response of the filter chain.

The FIR filter is realized as two subsequent FIR blocks. FIR0 adds a decimation factor of 2, FIR1 adds a decimation factor of 1 or 2, so the total decimation factor (i.e. the oversampling rate, including the CIC filter) is 2×N or 4×N.

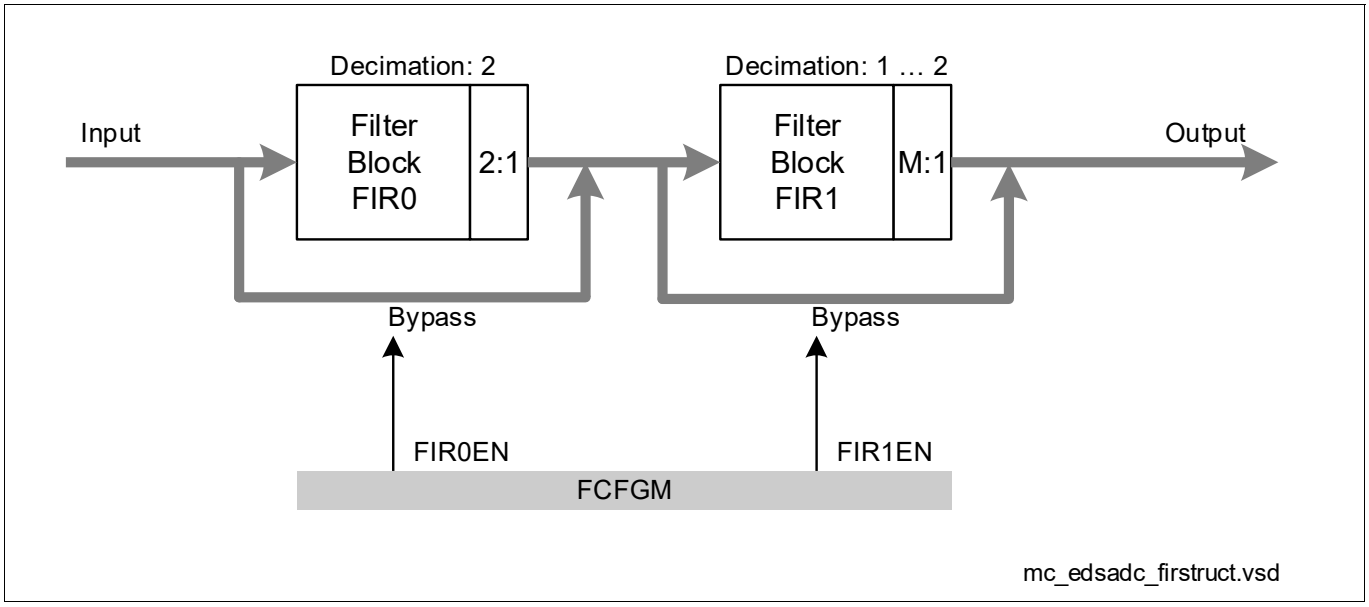


Figure 304 FIR Filter Blocks

The FIR filters can be described as:

$$y_1(m_1) = \sum_{i=0}^{N_1-1} a_1(i)\,x(2m_1 - i)$$

$$y(m) = \sum_{i=0}^{N_2-1} a_2(i)\,y_1(2m - i)$$

The coefficients of both FIR filters are fixed (see **Table 284** and **Table 285**). The filters are symmetric and have linear phase.

FIR0 has N1 = 8 coefficients, and generates the following response:

Table 284 Coefficients of FIR0

a0	a1	a2	a3	a4	a5	a6	a7
-29	-43	143	441	441	143	-43	-29

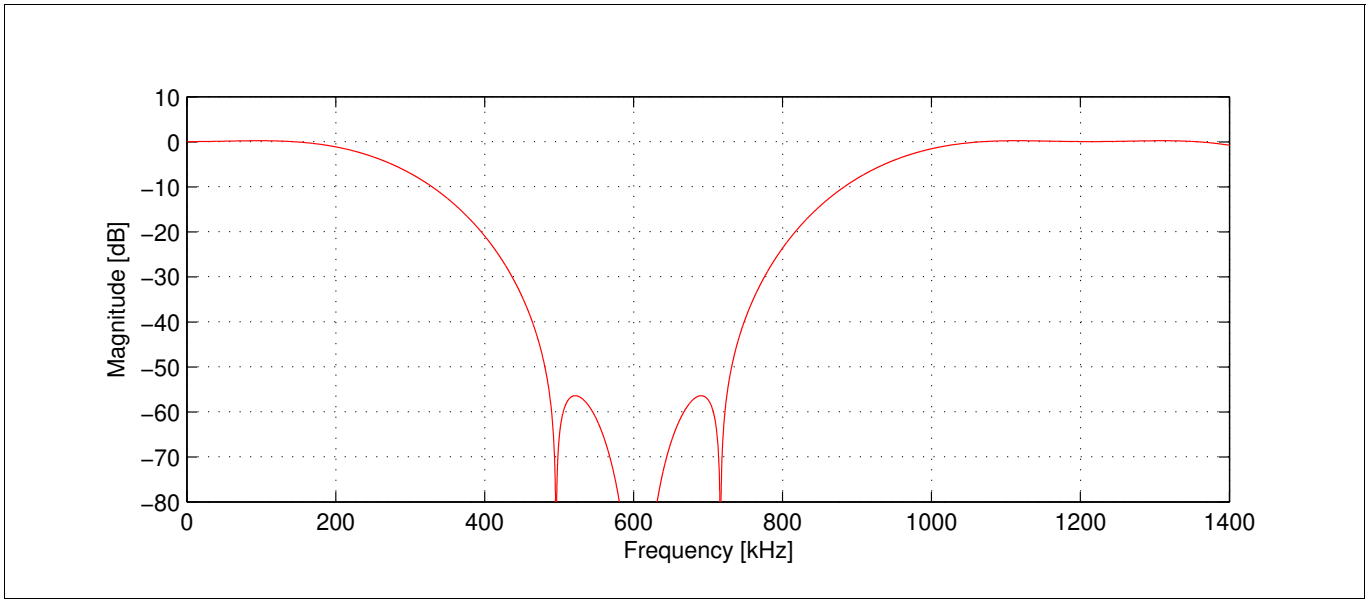


Figure 305 FIR0 Filter Frequency Response (Example for 606.06 kHz Output Data Rate)

FIR1 N2 = 28 coefficients and provides the following response:

Table 285 Coefficients of FIR1

a0, a27	a1, a26	a2, a25	a3, a24	a4, a23	a5, a22	a6, a21	a7, a20	a8, a19	a9, a18	a10, a17	a11, a16	a12, a15	a13, a14
-5	-3	3	14	-2	-22	-12	30	39	-20	-86	-19	196	399

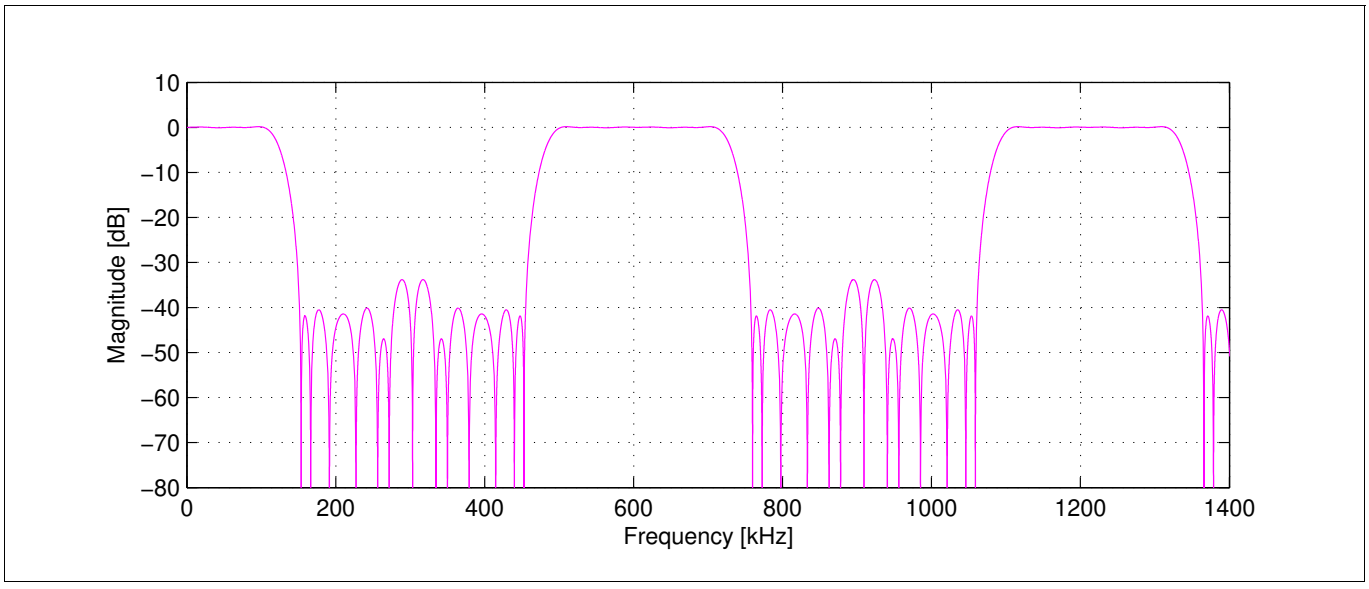


Figure 306 FIR1 Filter Frequency Response (Example for 303.03 kHz Output Data Rate)

33.5.5 Offset Compensation

The offset component that is present in most input signals can be removed automatically in order to receive the original sensor signal. The offset compensation stage can operate in two basic modes:

- **Highpass Filter**
  in this mode, the offset compensation can automatically remove the static component of a cyclic differential signal. This is achieved by the implemented IIR filter.
- **Offset Correction**
  in this mode, the offset compensation can remove the offset component of a static signal by subtracting a predefined value from the raw results. The IIR filter is disabled in this mode.

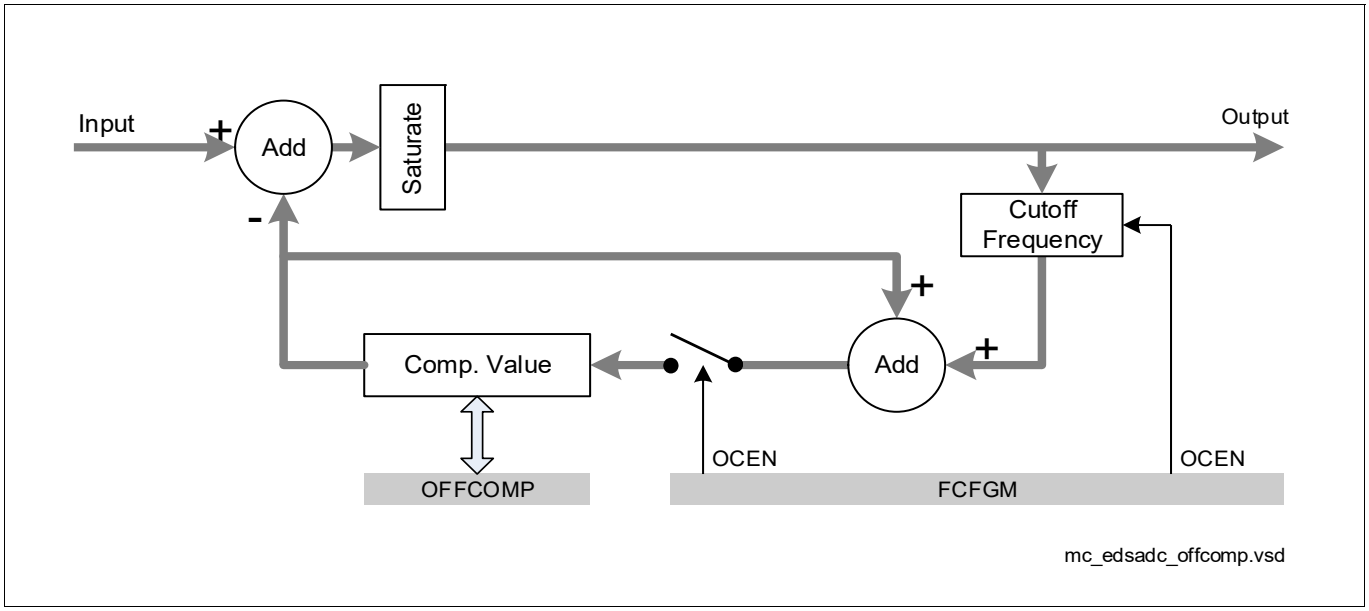


Figure 307 Offset Compensation

- **When the highpass filter is active**, the compensation value in register **OFFCOMPx (x=0-13)** is automatically updated by the filter. This attenuates the signal by a factor of at least DCF = -3 dB for frequencies below the selected cutoff frequency ($\geq 10^{-5} \times f_d$).
  The settling time of the highpass filter can be reduced by writing an initial compensation value instead of using the default value of zero. The general settling time is also adjustable by changing the filter properties, see bitfield **FCFGMx (x=0-13)**.OCEN and **Figure 308**.
- **When the highpass filter is off**, half of the current value in register **OFFCOMPx (x=0-13)** is subtracted from each raw value. The correction value can be determined and updated by the calibration sequence. Alternatively, it can be defined by the application or the calibrated value can be adjusted.
  Updating the offset value by the calibration sequence can be prohibited by setting bit OFFPROT in register **FCFGMx (x=0-13)**. This preserves the value written by the user.

*Note: An overview of the calibration mechanism is given in **"Calibration Support" on Page 36**.*

Since the filter chain internally uses more than 16 bits, the value in bitfield OFFSET is used shifted by one. This adds an additional bit to the LSB, which reduces the quantization error when several result values are accumulated. This, for example, is done when using the integrator.

A correction value of 233, therefore, is stored as $01D2_H$, $01D3_H$ would equal 233.5.

The high-pass filter can be described as (α = OCEN for OCEN > 000_B):

$$H(z) = \frac{1 - z^{-1}}{1 + (2^{2\alpha-16} - 1)z^{-1}}$$

The high-pass filter provides the following frequency responses:

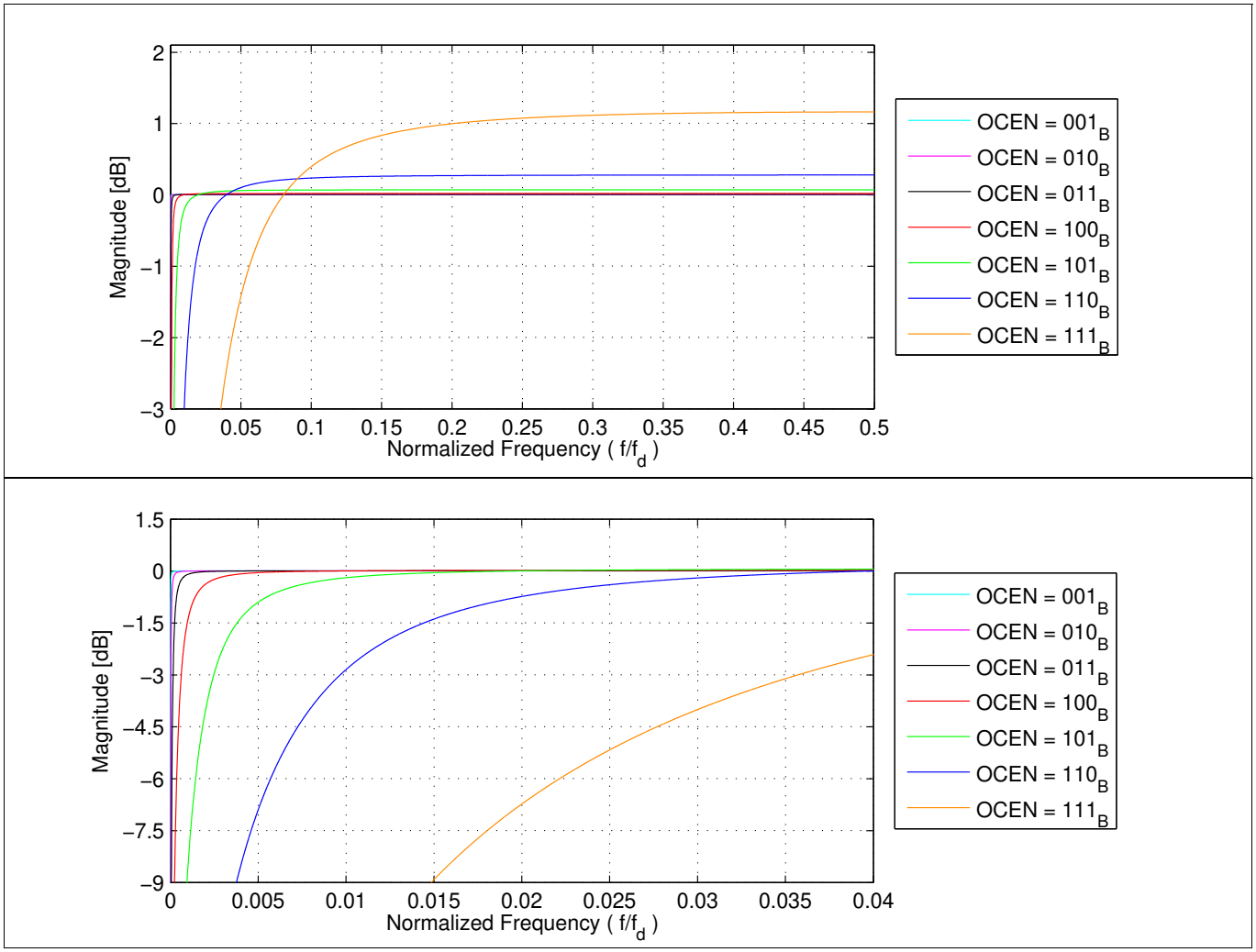


Figure 308 High-Pass Filter Frequency Responses

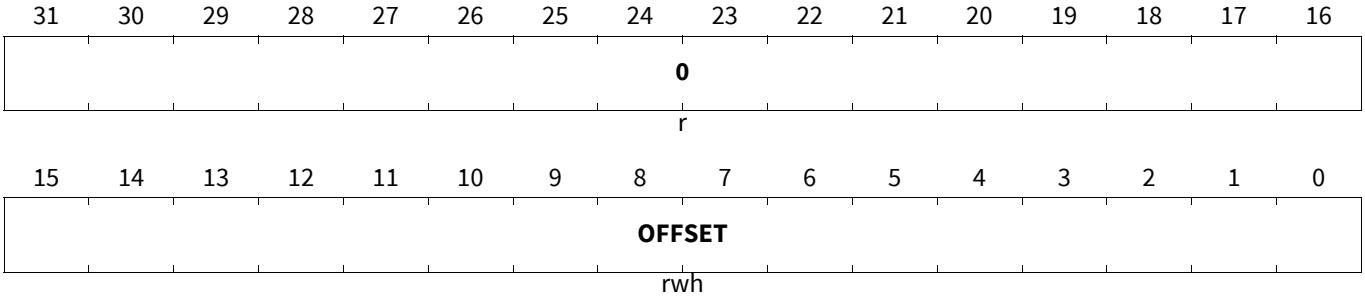
As shown in the figure above, bitfield **FCFGMx (x=0-13)**.OCEN selects different filter parameters:

Table 286 Offset Compensation Filter Parameters

OCEN	Cutoff Frequency (-3 dB)	Note
000_B	---	Offset compensation filter off
001_B	$1 \times 10^{-5} \times f_d$	Lowest cutoff frequency
010_B	$4 \times 10^{-5} \times f_d$	
011_B	$16 \times 10^{-5} \times f_d$	
100_B	$62 \times 10^{-5} \times f_d$	
101_B	$25 \times 10^{-4} \times f_d$	
110_B	$1 \times 10^{-2} \times f_d$	
111_B	$4 \times 10^{-2} \times f_d$	Highest cutoff frequency

Offset Compensation Register x

OFFCOMPx (x=0-13)
Offset Compensation Register x **(0138_H+x*100_H)** **Application Reset Value: 0000 0000_H**



Field	Bits	Type	Description
OFFSET	15:0	rwh	**Offset Value** Half of this signed value is subtracted from each result produced by the filter chain. *Note: Bit 0 represents 1/2 LSB. This increases the precision in case of accumulated result values, e.g. in the integrator.*
0	31:16	r	**Reserved, write 0, read as 0**

33.5.6 Integrator Stage

The integrator integrates the result values generated during the defined integration window by adding a configurable number of values to build the final result value. The integration window can be started triggered by an internal or external signal.

A configurable number of values can automatically be discarded after the trigger before the integration window is started. This positions the integration window exactly into a timeframe where the filter is stable or where the signal to be measured is free of system-generated noise.

Integration can be used to measure currents through shunt resistors at defined positions in the signal waveform. It also can remove the carrier signal component in resolver applications. In this case, the values to be integrated can be rectified to yield the maximum amplitude of the receiver signal. The delay between the carrier signal (generated by the on-chip carrier generator) and the received position signals can be compensated automatically. also refer to **Section 33.12**.

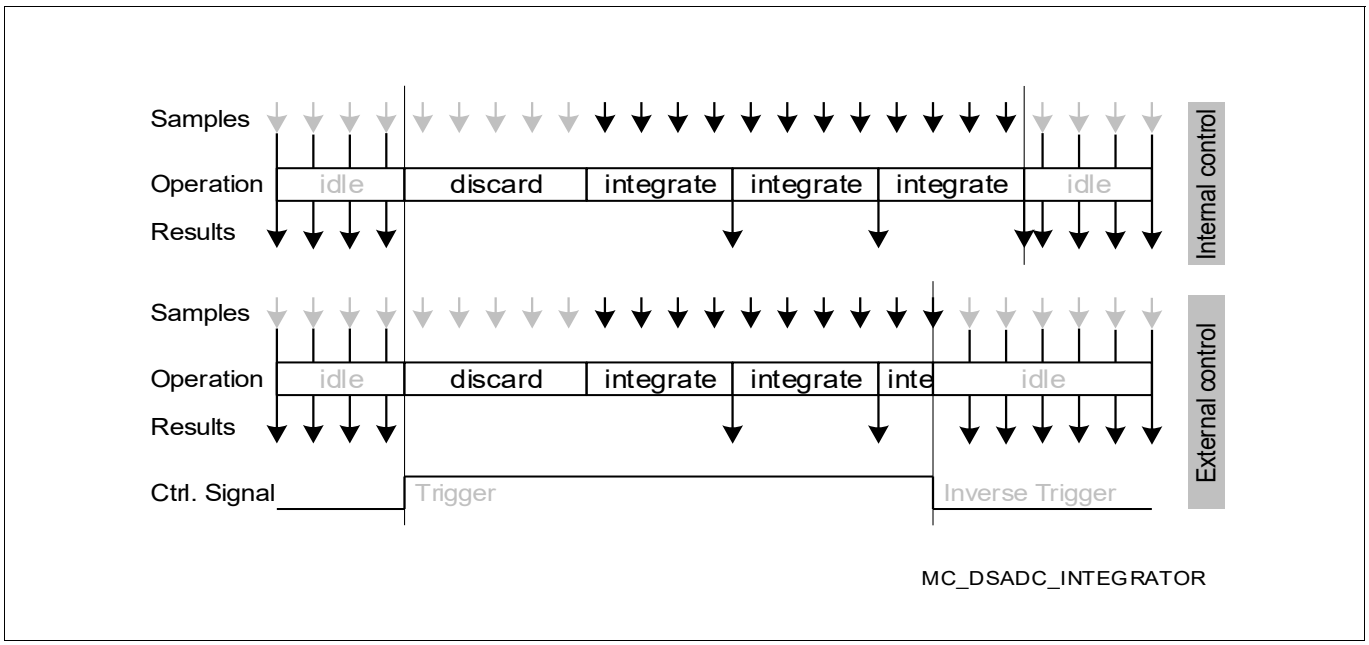


Figure 309 Integrator Operation

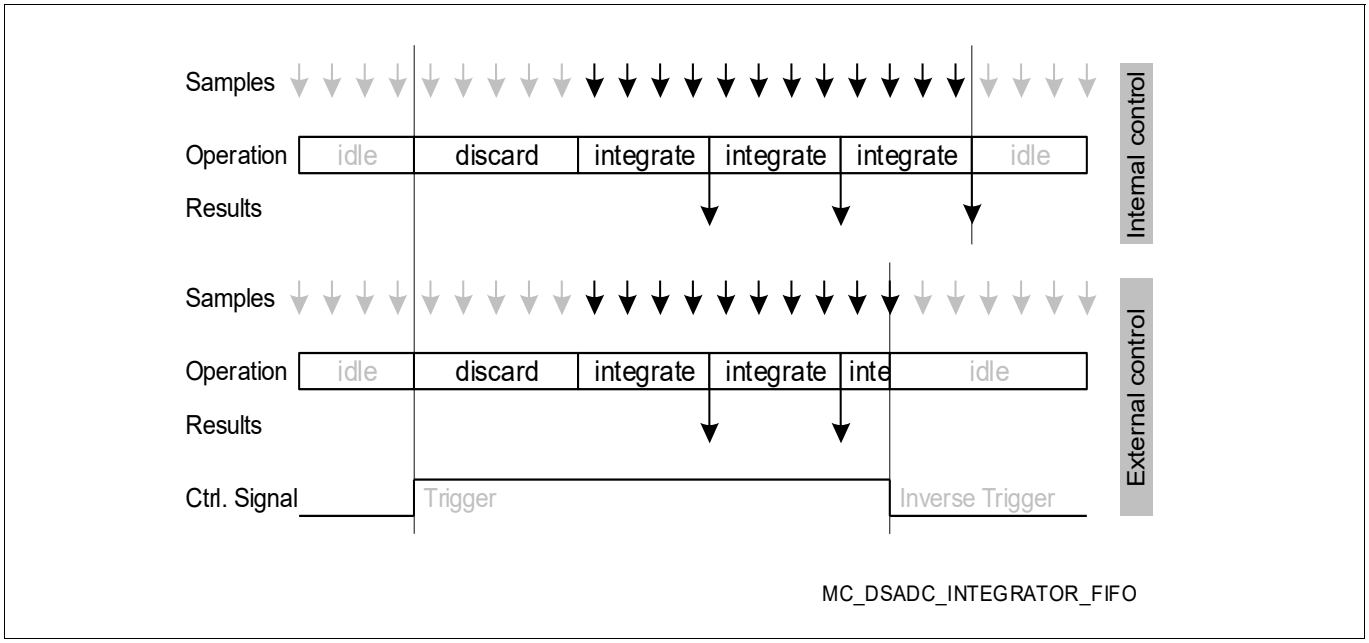


Figure 310 Integrator Operation with FIFO

Starting the Integration Window

The integration window starts when bit INTEN becomes 1:

- Software-Controlled Mode:
  Select software-controlled integration mode by setting bitfield ITRMODE = 11_B
- Trigger-Controlled Mode:
  Select trigger-controlled integration mode (ITRMODE = 01_B or 10_B)
  and generate the selected trigger edge at the configured trigger input

The external integration trigger signal is selected by bitfield TRSEL in register **DICFGx (x=0-13)**. Bitfield ITRMODE selects the transition of the selected signal to generate the trigger event. Select the trigger source first before enabling it.

When the integration window is started (INTEN becomes 1) the filter chain can be restarted (FRC = 0). This means, every non recursive filter element of the Filter Chain (CIC3, FIR0, FIR1, Integrator Stage) is cleared to zero and the related decimation counters are loaded with their start value (see **Section 33.5.1**). This ensures a deterministic start of an integration sequence. Simultaneously, the CIC filter of the Auxiliary Filter is cleared to zero and the related decimation counter is set to its initial value (see **Section 33.6**). This allows a synchronous operation of Filter Chain and Auxiliary Filter.
Keeping the filter chain running (FRC = 1) avoids the group delay until the first valid result values. In this case, the delay between start of integration window and the first result value depends on the current status of the filter chain.

After this the integration counter starts counting. After <NVALDIS> values the counter is reset and the integrator is started (if NVALDIS is zero the integration starts immediately).

Executing Integration Cycles

During an integration cycle <NVALINT+1> input values are integrated. After that, the integration result is stored in the result register and the integrator and the counter are cleared. If bit INTEN = 1 the next integration cycle is started.

Stopping the Integration Window

The integration window stops when bit INTEN becomes 0:

- Software-Controlled Mode:
  Disable software-controlled integration mode by setting bitfield ITRMODE = 00_B
- Trigger-Controlled Mode:
  - Internally controlled end of integration (IWS = 0, see upper part of **Figure 309**):
    After <REPVAL+1> integration cycles INTEN is cleared and the integration window closes after (<NVALINT+1> × <REPVAL+1>) input values
  - Externally controlled end of integration (IWS = 1, see lower part of **Figure 309**):
    Generate the selected inverse trigger edge at the configured trigger input (ITRMODE = 01_B or 10_B)
  - Integration may also be stopped by software by setting bitfield ITRMODE = 00_B
  - The source for the result register (RESMx) changes from the integrator output to the upstreamed filter chain. This means, the last result of the trigger-controlled integration is available in the result register (RESMx) only for the timeframe that is defined by the data rate period of the upstreamed filter chain. Using the result FIFO (DICFGx.DSM=0B and DICFGx.TSM=0_B), the integration result is kept in the result register up to the time where another trigger-controlled integration is initiated. For this purpose, the result FIFO has to use one of the following configuration:
    DICFGx.ITRMODE=10_B, FCFGMx.SRGM=10_B, RFCx.SRLVL=00_B
    DICFGx.ITRMODE=01_B, FCFGMx.SRGM=10_B, RFCx.SRLVL=00_B
    These configurations have the effect that service requests are only generated during integration window. In case of disabled integrator stage (ISTATx.INTEN=0_B), results generated by the upstreamed filter chain will not trigger service requests. However, results from the upstreamed filter chain will be stored in higher stages of the result FIFO. When the FIFO stages are fully loaded, all other results from the upstreamed filter chain are discarded.

After the integration has stopped, the current integration value can be read from register **IIVALx (x=0-13)**.

Integrator Data Output Format

Since the integrator accumulates a series of result values, the magnitude of its output increases depending on the size of the selected integration interval. A data shifter (controlled by bitfield ISC) compensates this for intervals of 2^N. If intervals other than 2^N are selected, the magnitude of the result value will be decreased accordingly.

Integration Window Control Register x

IWCTRx (x=0-13)
Integration Window Control Register x **(0120_H+x*100_H)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		NVALINT						0		NVALDIS					
r		rw						r		rw					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				REPVAL				0		FRC	IWS	0	ISC		
r				rw				r		rw	rw	r	rw		

Field	Bits	Type	Description
ISC	2:0	rw	**Integrator Shift Control** Controls the data shifter after the integrator that selects the portion of the integrator data for the result register. 110_B … 111_B are reserved. *Note: ISC selects the respective bits in register IIVAL. The lowest selected bit is used for rounding and is then removed.* 000_B Select bits 4 … 20 (integration of 2 values) 001_B Select bits 5 … 21 (integration of 3 … 4 values) … 101_B Select bits 9 … 25 (integration of 33 … 64 values)
IWS	4	rw	**Integration Window Size** 0_B Internal control: stop integrator after REPVAL+1 integration cycles 1_B External control: stop integrator upon the inverse trigger event
FRC	5	rw	**Filter Chain Restart Control** 0_B Restart the filter chain when an integration window starts 1_B No influence on filter chain when an integration window starts, except for the integrator itself
REPVAL	11:8	rw	**Number of Integration Cycles** Defines the number of integration cycles to be counted by REPCNT if activated (IWS = 0). The number of cycles is REPVAL+1.
NVALDIS	21:16	rw	**Number of Values Discarded** Start the integration cycle after NVALDIS values
NVALINT	29:24	rw	**Number of Values to be Accumulated** Stop the integration cycle after NVALINT+1 values *Note: Use intervals of 2 minimum, so no data is lost due to the data shifter.*
0	3, 7:6, 15:12, 23:22, 31:30	r	**Reserved, write 0, read as 0**

Integrator Status Register x

ISTATx (x=0-13)

Integrator Status Register x **(0128_H+x*100_H)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTEN	0			REPCNT				0		NVALCNT					
rh	r			rh				r		rh					

Field	Bits	Type	Description
NVALCNT	5:0	rh	**Number of Values Counted** Counts the number of integrated values until integration is started (NVALDIS) or completed (NVALINT)
REPCNT	11:8	rh	**Integration Cycle Counter** Counts the number of integration cycles if activated (IWS = 0). This number is selected via bitfield REPVAL.
INTEN	15	rh	**Integration Enable** Indicates the activity of the integrator. 1) 0_B Integration stopped. INTEN is cleared at the end of the integration window, i.e. after REPVAL cycles or upon the inverse trigger event transition of the external trigger signal. 1_B Integration enabled. INTEN is set when the channel is started while permanent integration is selected (ITRMODE = 11_B) or upon the defined trigger event.
0	7:6, 14:12, 31:16	r	**Reserved, write 0, read as 0**

1) For the control of bit INTEN, see also bitfield ITRMODE in register **DICFGx**.

Intermediate Integration Value

IIVALx (x=0-13)

Intermediate Integration Value **(0124_H+x*100_H)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0						IVAL									
r						rh									

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IVAL															
rh															

Field	Bits	Type	Description
IVAL	25:0	rh	**Result of most recent accumulation**
0	31:26	r	**Reserved, write 0, read as 0**

33.5.7 Group Delay and Settling Time

Data that enter a digital filter need a certain number of filter clocks before they appear at the filter's output and can be used by the system. When the digital filter chain is in steady state, the corresponding delay is defined by the group delay. The effective group delay depends on the configuration of the filter chain. **Table 287** summarizes the delays incurred by the elements of the filter chain. "N" indicates the selected oversampling rate (decimation factor) of the CIC filter. Delays are listed in modulator clock cycles.

Steady state condition is reached as soon the digital filter chain is settled. The effective settling time depends on the configuration of the filter chain. Due to the cascaded topology of the filter chain, the configuration specific settling time is defined by the step response of the terminating filter chain element. Generally, the filter chain characteristics like passband frequency (f_{PB}) and settling time are normalized to the data output rate (f_D). The data output rate (f_D) depends on the selected oversampling rate of the CIC filter and the enabled filter chain elements. **Table 288** summarizes the settling time for the different filter chain elements.

Table 287 Group Delay Summary

Filter Chain Element	Delay [t_{MOD}]	Notes
On-chip modulator	1	Delay of analog frontend
Input select/adjust unit	0.5	Synchronization of input signal
CIC3	$3 \times (2^{PRE} \times N - 1) / 2$	PRE = 0 or 1 if the prefilter is off (0) or on (1)
FIR0	$3.5 \times 2^{PRE} \times N$	To be added to CIC delay
FIR1	$13.5 \times 2^{PRE} \times N \times 2^{F0}$	F0 = 0 or 1 if FIR0 decimation is off (0) or on (1)
Offset correction/compensation	0	
Integrator	IWCTRx.NVALINT × $2^{PRE} \times N \times 2^{F0} \times 2^{F1} / 2$	Depends on the number of integrated values. F1 = 0 or 1 depending if FIR1 decimates (1) i.e. FIR1DEC = 0 or not (0) i.e. FIR1DEC = 1

Table 288 Settling Time Summary

Filter Chain Element	Settling Time [t_D]	Notes
CIC3	3 + 1	Settling time is defined by 3rd order of the CIC filter
FIR0	8 / 2 + 1	Settling time is defined by the 8 taps of FIR0 and the decimation of 2
FIR1	$28 / 2^{1\text{-FCFGMx.FIR1DEC}} + 1$	Settling time is defined by the 28 taps of FIR1 and the configurable decimation (FCFGMx.FIR1DEC)
Offset correction/compensation	$1 / (5 \times f_{-3dB})$	Cutoff frequency (f_{-3dB}) can be configured by bit-field FCFGMx.OCEN
Integrator	1 + 2	Mathematically, the integrator behave like a 1st order CIC filter

Example

f_{MOD} = 40 MHz, t_{MOD} = 25 ns,

prefilter active, OSR(CIC3) = 32, FIR0 active, FIR1 active and decimating, OC off, integration of 10 values.

$f_D = f_{MOD} / (2 \times 32 \times 2 \times 2 \times 10) = 15.625$ kHz

$t_D = 1 / f_D$

Group delay:
$[1 + 0.5 + (3 \times 63 / 2) + (3.5 \times 2 \times 32) + (13.5 \times 2 \times 32 \times 2) + (9 \times 2 \times 32 \times 2 \times 2 / 2)] \times t_{MOD} =$
$(1.5 + 94.5 + 224 + 1\,728 + 1\,152) \times t_{MOD} = 3\,200 \times 25$ ns = 80.0 µs
At the given oversampling rate of 2×32×2×2×10 = 2 560 this equals a delay of $1.25 \times t_D$ (data output rate cycles).
Without integration we get $(1.5 + 94.5 + 224 + 1\,728) \times t_{MOD} / 2{\times}32{\times}2{\times}2 = 2\,048 / 256 = 8 \times t_D$.
Settling time:
$[1 + 2] \times t_D$ = 192 µs
Without integration, data output rate (f_D) is defined by $f_D = f_{MOD} / (2 \times 32 \times 2 \times 2) = 156.25$ kHz, tD = 1/ f_D = 6.4 µs
Corresponding settling time is defined by
[28 / 2 + 1] × 6.4 µs = 96 µs

Note: When changing the input source (e.g. by switching the analog input multiplexer, if available), the second result value will safely belong to the newly selected input. Result values that correspond to the new input level, however, can only be retrieved after the corresponding group delay.

Note: With a configuration for the filter chain where only the CIC3 filter is used and the calibration is triggered (FCFGM.CALIB) immediately after modulator enabling (GLOBRC.MxRUN), the settling time of the filter chain reduces to a single cycle of t_D. The calibration algorithm uses the CIC3 filter and the settling occurs during execution of the calibration algorithm. When calibration is running, the filter chain provides no data.

33.5.8 Filter Configuration Options

The filter chain can be configured according to the requirements of the intended application. The following pages describe the available bitfields in the control registers.

Filter Configuration Register x, Main

FCFGMx (x=0-13)
Filter Configuration Register x, Main **(0110_H+x*100_H)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CSRWC	0	AUTOCAL	CALIB	0			EGT	ESEL		SRGA		0		SRGM	
w	r	rw	w	r			rw	rw		rw		r		rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FMWC	0			OFFPROT	OCEN			0		PFEN	CICMOD	FIR1DEC	OVCEN	FIR1EN	FIR0EN
w	r			rw	rw			r		rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
FIR0EN	0	rw	**FIR0 Filter Enable** 0_B FIR0 disabled and bypassed 1_B FIR0 filter enabled
FIR1EN	1	rw	**FIR1 Filter Enable** 0_B FIR1 disabled and bypassed 1_B FIR1 filter enabled
OVCEN	2	rw	**Overshoot Compensation Enable** 0_B Disabled, feed FIR filter directly 1_B Attenuate response to fast edges
FIR1DEC	3	rw	**FIR1 Filter Decimation Rate** 0_B Decimation 2:1 for FIR1 1_B FIR1 filter does not decimate
CICMOD	4	rw	**CIC Filter Mode** 0_B CIC3 1_B Reserved
PFEN	5	rw	**Prefilter Enable** 0_B Off 1_B Prefilter enabled
OCEN	10:8	rw	**Offset Compensation Filter Enable** 000_B Offset compensation filter disabled, register OFFCOMP not changed 001_B Enable offset compensation filter, set cutoff frequency to rate 1 … 111_B Enable offset compensation filter, set cutoff frequency to rate 7

Field	Bits	Type	Description
OFFPROT	11	rw	**Offset Protection** Controls the influence of the calibration sequence on register OFFCOMP. 0_B Unprotected, calibration sequence updates bitfield OFFSET 1_B Protected, bitfield OFFSET is locked and not modified by calibration
FMWC	15	w	**Write Control for Filter Modes** 0_B No write access to filter modes 1_B Bitfields OFFPROT, OCEN, PFEN, CICMOD, FIR1DEC, OVCEN, FIR1EN, FIR0EN can be written
SRGM	17:16	rw	**Service Request Generation for Main Service Request** 00_B Never, service request disabled 01_B While gate (selected trigger signal) is high 10_B While gate (selected trigger signal) is low 11_B Always, as selected by bitfield SRLVL
SRGA	21:20	rw	**Service Request Generation for Alternate Service Request** *Note:* 00_B Never, service request disabled 01_B Comparator event, as selected by bitfield ESEL/EGT 10_B Timestamp event 11_B Alternate source: Capturing of a sign delay value to register CGSYNC
ESEL	23:22	rw	**Event Select** Defines when a comparator event is generated. 00_B Always, for each new result value 01_B If result is inside the boundary band 10_B If result is outside the boundary band 11_B Reserved
EGT	24	rw	**Event Gating** Defines if alarm events are coupled to the integration window. 0_B Separate: generate events according to ESEL 1_B Coupled: generate events only when the integrator is enabled and after the discard phase defined by bitfield NVALDIS[1)]
CALIB	28	w	**Calibration Trigger** 0_B No action 1_B Start the calibration algorithm now
AUTOCAL	29	rw	**Automatic Calibration Control** 0_B Calibration algorithm started by software (set bit CALIB) 1_B Automatically start the calibration algorithm when the selected service request gate closes (trailing edge, see bitfield SRGM)
CSRWC	31	w	**Write Control for Calibration and Service Request Modes** 0_B No write access to calibration and service request modes 1_B Bitfields AUTOCAL, CALIB, EGT, ESEL, SRGA, SRGM can be written

Field	Bits	Type	Description
0	7:6, 14:12, 19:18, 27:25, 30	r	**Reserved, write 0, read as 0**

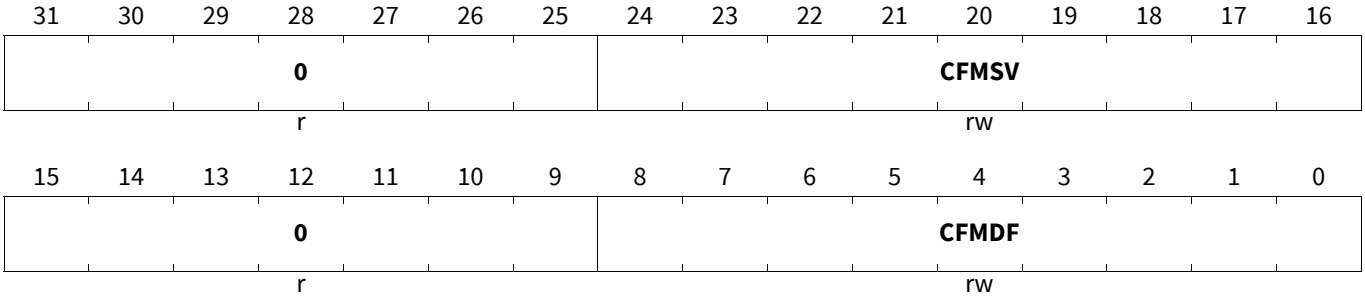
1) While the integrator is bypassed, event gating suppresses alarm service requests, result values are still generated and stored.

Table 289 Access Mode Restrictions of FCFGMx (x=0-13) sorted by descending priority

Mode Name	Access Mode		Description
write 1 to **FMWC**	rw	CICMOD, FIR0EN, FIR1DEC, FIR1EN, OCEN, OFFPROT, OVCEN, PFEN	Set FMWC during write access
write 1 to **CSRWC**	rw	AUTOCAL, EGT, ESEL, SRGA, SRGM	Set CSRWC during write access
write 1 to **CSRWC**	w	CALIB	Set CSRWC during write access
otherwise	r	AUTOCAL, CICMOD, EGT, ESEL, FIR0EN, FIR1DEC, FIR1EN, OCEN, OFFPROT, OVCEN, PFEN, SRGA, SRGM	
(default)	rX	CALIB	

Filter Configuration Register x, CIC Filter

FCFGCx (x=0-13)
Filter Configuration Register x, CIC Filter (0114_H+x*100_H) Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
CFMDF	8:0	rw	**CIC Filter Decimation Factor** Defines the oversampling rate of the CIC filter: OSR = CFMDF + 1. Valid values are 003_H to $1FF_H$ (OSR = 4 to 512).
CFMSV	24:16	rw	**CIC Filter Start Value** The decimation counter begins counting at value CFMSV, when started or restarted. Valid values are 003_H to CFMDF (4 to selected OSR).[1)]

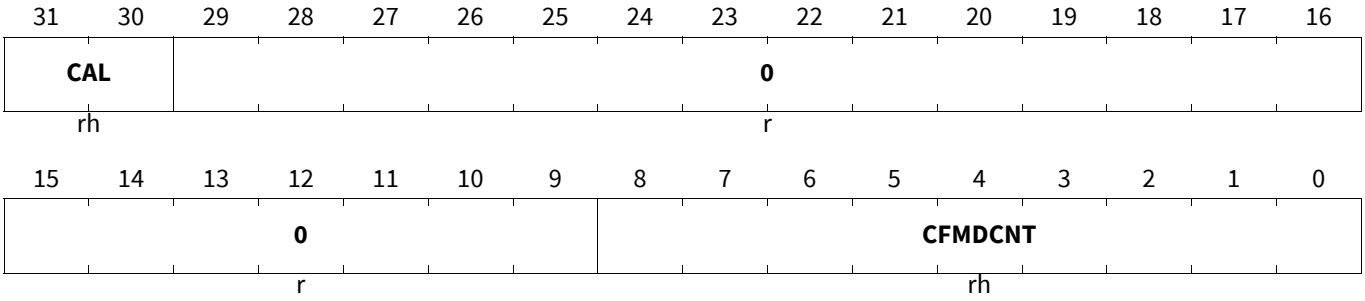
Field	Bits	Type	Description
0	15:9, 31:25	r	**Reserved, write 0, read as 0**

1) Start values above the selected oversampling rate may lead to overflows in the CIC filter!

Filter Counter Register x, CIC Filter

FCNTCx (x=0-13)

Filter Counter Register x, CIC Filter **(0118_H+x*100_H)** **Application Reset Value: 0000 0000_H**



Field	Bits	Type	Description
CFMDCNT	8:0	rh	**CIC Filter Decimation Counter** The decimation counter counts the filter cycles until an output is generated, i.e. the oversampling rate. CFMDCNT counts down from the respective start value.
CAL	31:30	rh	**Calibration Status Flag** *Note: Bitfield CAL is set to 01_B in the next clock cycle after setting bit CALIB or after detecting the selected trigger (if auto-calibration is activated).* 00_B Uncalibrated, initial state after reset 01_B The calibration algorithm is currently running 10_B Calibrated, normal operation is possible 11_B Calibration terminated incorrectly
0	29:9	r	**Reserved, write 0, read as 0**