

Enhanced Delta-Sigma Analog-to-Digital Converter (EDSADC)

33.10 Safety Features

Most analog inputs are connected to both EVADC and EDSADC channels, thus providing a basic redundancy.

On-Chip Supervision Signals

Information about the basic functionality of the EDSADC can be obtained via special on-chip signals, which supports common cause diagnosis. Every channel can output a replica of a reference voltage generated by a bandgap inside the power management system (PMS). The selected output voltage can be measured via a specific channel of the EVADC.

The selection of the supervision signal is controlled centrally via register **GLOBCFG**:

- Bitfield SVSIG enables the supervision function by selecting one of two voltages
- Bitfield SVCH selects the channel for which the supervision signal is connected to the common output.

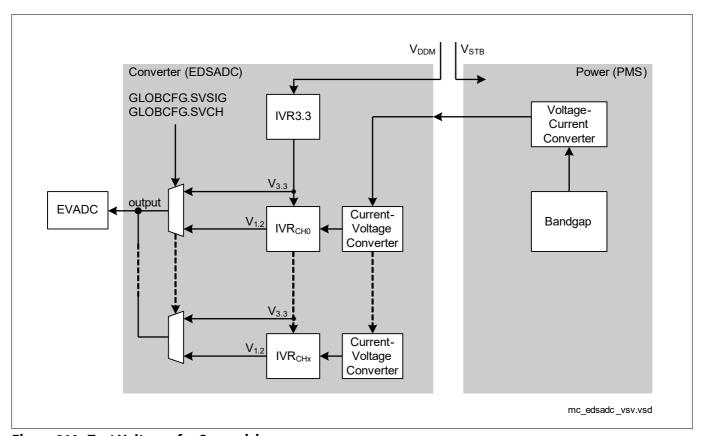


Figure 319 Test Voltages for Supervision

Measuring these voltages enables two test features:

- Compare the result with the expected value (RESULT = $V_{\rm Test}$ / $V_{\rm AREF}$ × 2¹²). With $V_{\rm AREF}$ = 5.0 V and $V_{\rm DDK}$ = 1.2 V, RESULT = 3D7_H.
- Compare the individual results of all channels to find deviations.