Table 17 FIFO Interrupt Signals (cont'd)

Signal	Description
FIFO[i]_CH[x]_LOWER_WM	Indicating FIFO x (x:0…7) reached lower watermark.
FIFO[i]_CH[x]_UPPER_WM	Indicating FIFO x (x:0…7) reached upper watermark.

28.7.4 FIFO Configuration Register Overview

Table 18 FIFO Configuration Register Overview

Register Name	Description	see Page
FIFO[i]_CH[z]_CTR	FIFOi channel z control register	84
FIFO[i]_CH[z]_END_ADDR	FIFOi channel z end address register	85
FIFO[i]_CH[z]_START_ADDR	FIFOi channel z start address register	85
FIFO[i]_CH[z]_UPPER_WM	FIFOi channel z upper watermark register	86
FIFO[i]_CH[z]_LOWER_WM	FIFOi channel z lower watermark register	86
FIFO[i]_CH[z]_STATUS	FIFOi channel z status register	87
FIFO[i]_CH[z]_FILL_LEVEL	FIFOi channel z fill level register	88
FIFO[i]_CH[z]_WR_PTR	FIFOi channel z write pointer register	88
FIFO[i]_CH[z]_RD_PTR	FIFOi channel z read pointer register	89
FIFO[i]_CH[z]_IRQ_NOTIFY	FIFOi channel z interrupt notification register	90
FIFO[i]_CH[z]_IRQ_EN	FIFOi channel z interrupt enable register	91
FIFO[i]_CH[z]_EIRQ_EN	FIFOi channel z error interrupt enable register	94
FIFO[i]_CH[z]_IRQ_FORCINT	FIFOi channel z force interrupt register	92
FIFO[i]_CH[z]_IRQ_MODE	FIFOi channel z interrupt mode control register	93