28.7.2.2 Ring Buffer Operation Mode

The ring buffer mode can be used to provide a continuous data or configuration stream to the other GTM sub-modules without CPU interaction. In ring buffer mode the FIFO provides a continuous data stream to the F2A sub-module. The first word of the FIFO is delivered first and after the last word is provided by the FIFO to the ARU, the first word can be obtained again.

If in ring buffer mode the read pointer reaches the write pointer it will be set again to the configured start address. So the read pointer always rotates cyclic between the configured start address of the regarding FIFO channel (first written data) and the write pointer which points to the last written data of the channel.

It is possible to add data to the FIFO channel via the AEI to FIFO interface (AFD) using the register AFD[i]_CH[x]_BUF_ACC while running in ring buffer mode. The new written data will be added in the next ring buffer cycle.

However, the register AFD[i]_CH[x]_BUF_ACC should not be read in read buffer mode.

It is recommended to fill the FIFO channel first before enabling the data stream in the FIFO to ARU interface (F2A).

Modifications of the continuous data stream can be achieved by using direct memory access which is provided by the FIFO AEI interface.

28.7.2.3 DMA Hysteresis Mode

The DMA hysteresis mode can be enabled by setting bit DMA_HYSTERESIS=1 in the **FIFO[i]_CH[x]_IRQ_MODE** register.

In the DMA hysteresis mode the lower and upper watermark will be masked to generate the DMA request (=*fifo_irq*) in the following manner.

If a DMA is writing data to a FIFO (configured by setting bit DMA_HYST_DIR=1 in register **FIFO[i]_CH[x]_IRQ_MODE)**, the DMA request will be generated by the lower watermark. The upper watermark does not generate a DMA request. The next DMA request will be generated by the next lower watermark until the upper watermark was reached.

If a DMA is reading data from a FIFO (configured by setting bit DMA_HYST_DIR=0 in register **FIFO[i]_CH[x]_IRQ_MODE)**, the DMA request will be generated by the upper watermark. The lower watermark does not generate a DMA request. The next DMA request will be generated by the next upper watermark until the lower watermark was reached.

Note that the watermarks have to achieve the following condition depending on the irq mode

- IRQ_MODE = Level / Pulse / Pulse-Notify mode:
  - Upper watermark > Lower watermark
- IRQ_MODE = Single-Pulse mode:
  - Upper watermark > Lower watermark + 1

28.7.3 FIFO Interrupt

Table 17 FIFO Interrupt Signals

Signal	Description
FIFO[i]_CH[x]_EMPTY	Indicating empty FIFO x (x:0…7) was reached
FIFO[i]_CH[x]_FULL	Indicating full FIFO x (x:0…7) was reached