28.6 Broadcast Module (BRC)

28.6.1 Overview

Since each write address for the sub-module channels of the GTM that are able to write to the ARU can only be read by a single module, it is impossible to provide a data stream to different modules in parallel (This statement holds not for sources, which do not invalidate their data after the data were read by any consumer, e.g. DPLL).

To overcome this issue for regular modules, the sub-module Broadcast (BRC) enables to duplicate data streams multiple times.

The BRC sub-module provides 12 input channels as well as 22 output channels.

In order to clone an incoming data stream, the corresponding input channel can be mapped to zero or more output channels.

When mapped to zero no channel is read.

To destroy an incoming data stream, the **EN_TRASHBIN** bit inside the **BRC_SRC_[x]_DEST** register has to be set.

The total number of output channels that are assigned to a single input channel is variable. However, the total number of assigned output channels must be less than or equal to 22.

28.6.2 BRC Configuration

As it is the case with all other sub-modules connected to the ARU, the input channels can read arbitrary ARU address locations and the output channels provide the broadcast data to fixed ARU write address locations.

The associated write addresses for the BRC sub-module are fixed and can be obtained from the product specific appendix.

The read address for each input channel is defined by the corresponding register **BRC_SRC_[x]_ADDR** (x: 0…11).

The mapping of an input channel to several output channels is defined by setting the appropriate bits in the register **BRC_SRC_[x]_DEST** (x: 0…11). Each output channel is represented by a single bit in the register **BRC_SRC_[x]_DEST**.

If no output channel bit is set within a register **BRC_SRC_[x]_DEST**, no data is provided to the corresponding ARU write address location from the defined read input specified by **BRC_SRC_[x]_ADDR**. This means that the channel does not broadcast any data and is disabled (reset state).

Besides the possibility of mapping an input channel to several output channels, the bit **EN_TRASHBIN** of register **BRC_SRC_[x]_DEST** may be set, which results in dropping an incoming data stream. In this case the data of an input channel defined by **BRC_SRC_[x]_ADDR** is consumed by the BRC module and not routed to any succeeding sub-module. In consequence, the output channels defined in the register **BRC_SRC_[x]_DEST** are ignored. Therefore, the bits 0 to 21 are set to zero (0) when trash bin functionality is enabled.

In general, the BRC sub-module can work in two independent operation modes. In the first operation mode the data consistency is guaranteed since a BRC channel requests only new data from a source when all destination channels for the BRC have consumed the old data value. This mode is called *Data Consistency Mode* (DCM).

In a second operation mode the BRC channel always requests data from a source and distributes this data to the destination regardless whether all destinations have already consumed the old data. This mode is called *Maximum Throughput Mode* (MTM).

MTM ensures that always the newest available data is routed through the system, while it is not guaranteed data consistency since some of the destination channels can be provided with the old data while some other destination channels are provided with the new data. If this is the case, the Data Inconsistency Detected Interrupt *BRC_DID_IRQ[x]* is raised but the channel continues to work.