

Generic Timer Module (GTM)

28.4.2 GTM Interfaces

In general the GTM can be divided into four interface groups. Two interface groups represent the ports of the GTM where incoming signals are assembled and outgoing signals are created. These interfaces are therefore connected to the GTM input sub-module TIM and to the GTM output sub-modules DTM.

Another interface is the bus interface where the GTM can be connected to the SoC system bus. This generic bus interface is described in more detail in [Section 28.4.2.1](#). The last interface is the interrupt controller interface. The GTM provides several interrupt lines coming from the various sub-modules. These interrupt lines are concentrated inside the ICM and have to be adapted to the dedicated micro controller environment where each interrupt handling can look different. The interrupt concept is described in more detail in [Section 28.4.5](#).

28.4.2.1 GTM Generic Bus Interface (AEI)

The GTM is equipped with a generic bus interface that can be widely adapted to different SoC bus systems. This generic bus interface is called AE-Interface (AEI). The adaptation of the AEI to SoC buses is typically done with a bridge module translating the AEI signals to the SoC bus signals of the silicon vendor. The AEI bus signals are depicted in the following table:

Table 6 AEI bus signals

Signal name	I/O	Description	Bit width
AEI_SEL	I	GTM select line	1
AEI_ADDR	I	GTM address	32
AEI_PIPE	I	AEI Address phase signal	1
AEI_W1R0	I	Read/Write access	1
AEI_WDATA	I	Write data bus	32
AEI_RDATA	O	Read data bus	32
AEI_READY	O	Data ready signal	1
AEI_STATUS	O	AEI Access status	2

The AEI Status Signal may drive one of the following values:

Table 7 AEI Status Signal

AEI_STATUS	Description
0b00	No Error
0b01	Illegal Byte Addressing
0b10	Illegal Address Access
0b11	Unsupported Address

The signal value 0b00 is returned if no error occurred during AEI access.

The signal value 0b01 is returned if the bus address is not an integer multiple of 4 (byte addressing).

The signal value 0b11 is returned if the address is not handled in the GTM.

The signal value 0b10 is returned if the written register is a protected register (e.g. protected by bit RF_PROT) or if the register is temporarily not writable because of sub-module internal state or the clock of the relevant cluster is disabled.

In case of an illegal write access signaled by status 0b10 the register will not be modified.

Reading registers will never return status 0b10.