28.4.9 GTM TOP-Level Configuration Registers Description

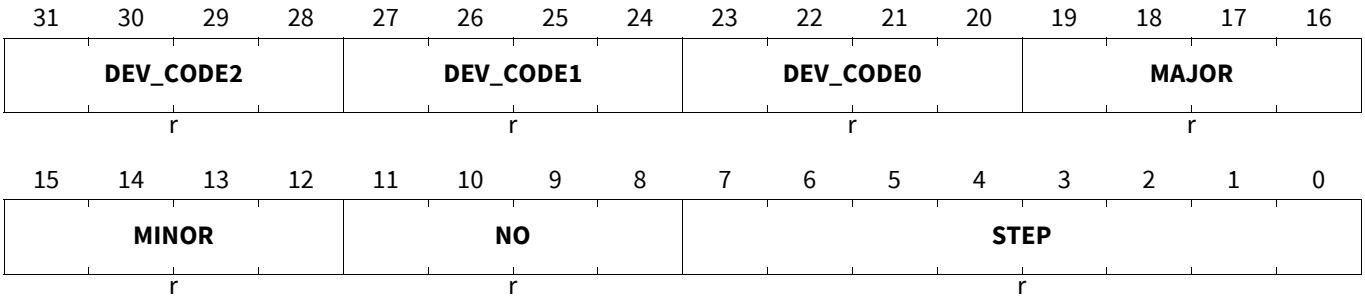
28.4.9.1 Register GTM_REV

Please keep in mind, that the actual Revision number is the reset value. This reset value is dependent on the delivery done by Bosch AE for the actual device. In case of Infineon's decision to change via metal fix for a different version, the reset value contains the initial version.

GTM Version Control Register

Note: The numbers are encoded in BCD. Values "A" - "F" are characters.

REV
GTM Version Control Register **(000000_H)** **Application Reset Value: $3153\ 15B6_H$**



Field	Bits	Type	Description
STEP	7:0	r	**Release step** GTM Release step
NO	11:8	r	**Delivery number** Define delivery number of GTM specification.
MINOR	15:12	r	**Minor version number** Define minor version number of GTM specification.
MAJOR	19:16	r	**Major version number** Define major version number of GTM specification.
DEV_CODE0	23:20	r	**Device encoding digit 0** Device encoding digit 0.
DEV_CODE1	27:24	r	**Device encoding digit 1** Device encoding digit 1.
DEV_CODE2	31:28	r	**Device encoding digit 2** Device encoding digit 2.

28.4.9.2 Register GTM_RST

GTM Global Reset Register

RST

GTM Global Reset Register **(000004$_H$)** **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0				BRIDGE_MODE_WRDIS	0										
r				rw	r										

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0															0
r															r

Field	Bits	Type	Description
BRIDGE_MODE_WRDIS	27	rw	**GTM_BRIDGE_MODE write disable** This bit is write protected by bit RF_PROT 0_B Writing of GTM_BRIDGE_MODE register is enabled 1_B Writing of GTM_BRIDGE_MODE register is disabled
0	0, 26:1, 31:28	r	**Reserved** Read as zero, shall be written as zero.

28.4.9.3 Register GTM_CTRL

GTM Global Control Register

CTRL

GTM Global Control Register **(000008$_H$)** **Application Reset Value: 0000 0001$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AEIM_CLUSTER				0			TO_VAL					0		TO_MODE	RF_PROT
r				r			rw					r		rw	rw

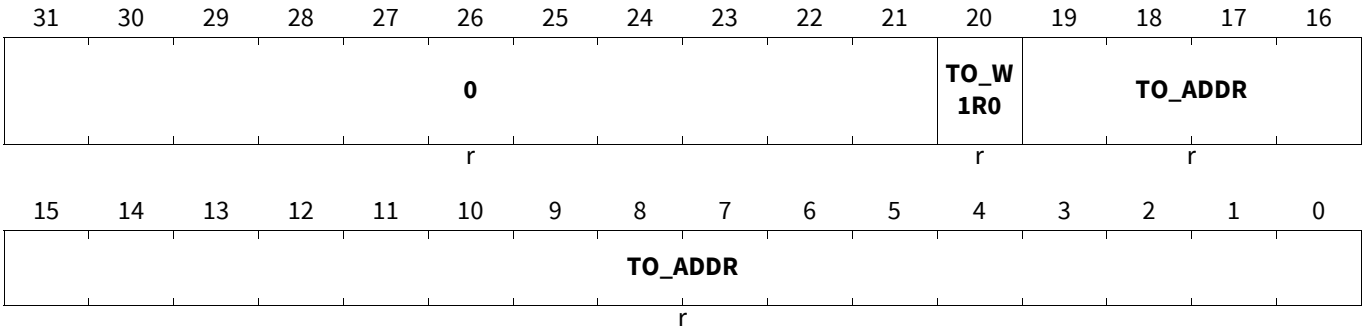
Field	Bits	Type	Description
RF_PROT	0	rw	**RST and FORCINT protection** 0_B SW RST (global), SW interrupt FORCINT, and SW RAM reset functionality is enabled 1_B SW RST (global), SW interrupt FORCINT, and SW RAM reset functionality is disabled
TO_MODE	1	rw	**AEI timeout mode** 0_B Observe: If timeout_counter=0 the address and rw signal in addition with timeout flag will be stored to the GTM_AEI_ADDR_XPT register. Following timeout_counter=0 accesses will not overwrite the first entry in the aei_addr_timeout register. Clearing the timeout flag/aei_status error_code will reenable the storing of a next faulty access. 1_B Abort: In addition to observe mode, the pending access will be aborted by signaling an illegal module access on aei_status and sending ready. In case of a read, deliver as data 0 by serving of next AEI accesses.
TO_VAL	8:4	rw	**AEI timeout value** These bits define the number of cycles after which a timeout event occurs. When TO_VAL equals zero (0) the AEI timeout functionality is disabled.
AEIM_CLUSTER	15:12	r	**AEIM cluster number** These bits show the number of the AEI master port cluster which throws the interrupts *AEIM_USP_ADDR, AEIM_IM_ADDR* and *AEIM_USP_BE* depending on the AEI master port access status.Note: If one of the corresponding irq notify bits (6:4) is set, this bit field will be frozen until the interrupt notify bits (6:4) are cleared.
0	3:2, 11:9, 31:16	r	**Reserved** Read as zero, shall be written as zero.

28.4.9.4 Register GTM_AEI_ADDR_XPT

GTM AEI Timeout Exception Address Register

AEI_ADDR_XPT

GTM AEI Timeout Exception Address Register (00000C$_H$) **Application Reset Value: 0000 0000$_H$**

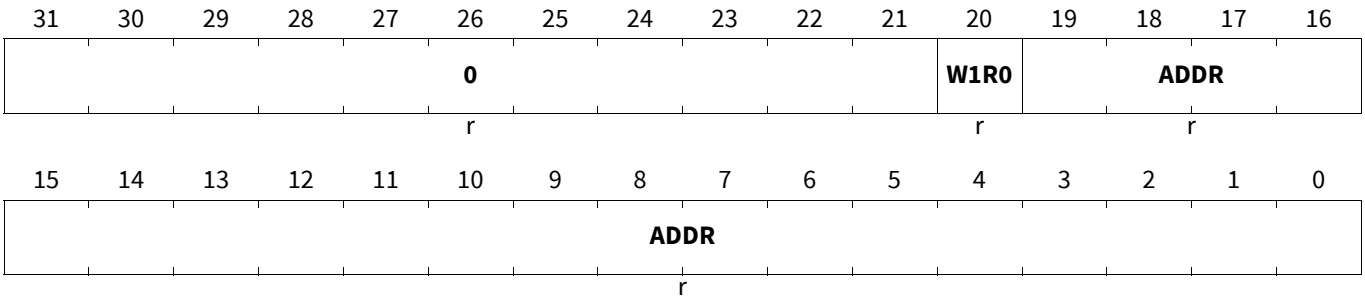


Field	Bits	Type	Description
TO_ADDR	19:0	r	**AEI timeout address** This bit field defines the AEI address for which the AEI timeout event occurred.
TO_W1R0	20	r	**AEI timeout Read/Write flag** This bit defines the AEI Read/Write flag for which the AEI timeout event occurred.
0	31:21	r	**Reserved** Read as zero, shall be written as zero.

28.4.9.5 Register GTM_AEI_STA_XPT

GTM AEI Non Zero Status Register

AEI_STA_XPT
GTM AEI Non Zero Status Register **(00002C$_H$)** **Application Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
ADDR	19:0	r	**AEI exception address** This bit field captures the address of the first AEI access resulting with a non-zero AEI status signal. The bit field can be cleared by clearing the interrupt flags AEI_USP_ADDR,AEI_USP_BE, and AEI_IM_ADDR in the register GTM_IRQ_NOTIFY.
W1R0	20	r	**AEI exception Read/Write flag** This bit defines the AEI Read/Write flag for which the AEI non-zero event occurred. This bit field captures the address of the first AEI access resulting with a non-zero AEI status signal. The bit field can be cleared by clearing the interrupt flags AEI_USP_ADDR, AEI_USP_BE, and AEI_IM_ADDR in the register GTM_IRQ_NOTIFY.
0	31:21	r	**Reserved** Read as zero, shall be written as zero.

28.4.9.6 Register GTM_IRQ_NOTIFY

GTM Interrupt Notification Register

IRQ_NOTIFY

GTM Interrupt Notification Register (000010$_H$) Application Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		CLK_EN_EXP_STATE1	CLK_EN_EXP_STATE0	0		CLK_EN_ERR_STATE1	CLK_EN_ERR_STATE0	0							
r		r	r	r		r	r	r							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							CLK_PER_ERR	CLK_EN_ERR	AEIM_USP_BE	AEIM_IM_ADDR	AEIM_USP_ADDR	AEI_USP_BE	AEI_IM_ADDR	AEI_USP_ADDR	AEI_TO_XPT
r							rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
AEI_TO_XPT	0	rw	**AEI timeout exception occurred** This bit will be cleared on a CPU write access of value '1'. (As the bit is rw, otherwise no clear.) A read access leaves the bit unchanged. 0_B No interrupt occurred 1_B AEI_TO_XPT interrupt was raised by the AEI Timeout detection unit
AEI_USP_ADDR	1	rw	**AEI unsupported address interrupt** This bit will be cleared on a CPU write access of value '1'. A read access leaves the bit unchanged. 0_B No interrupt occurred 1_B AEI_USP_ADDR interrupt was raised by the AEI interface
AEI_IM_ADDR	2	rw	**AEI illegal Module address interrupt** This bit will be cleared on a CPU write access of value '1'. A read access leaves the bit unchanged. 0_B No interrupt occurred 1_B AEI_IM_ADDR interrupt was raised by the AEI interface
AEI_USP_BE	3	rw	**AEI unsupported byte enable interrupt** This bit will be cleared on a CPU write access of value '1'. A read access leaves the bit unchanged. 0_B No interrupt occurred 1_B AEI_USP_BE interrupt was raised by the AEI interface
AEIM_USP_ADDR	4	rw	**AEI master port unsupported address interrupt** This bit will be cleared on a CPU write access of value '1'. A read access leaves the bit unchanged. 0_B No interrupt occurred 1_B AEIM_USP_ADDR interrupt was raised by the AEI master port interface

Field	Bits	Type	Description
AEIM_IM_ADDR	5	rw	**AEI master port illegal Module address interrupt** This bit will be cleared on a CPU write access of value '1'. A read access leaves the bit unchanged. 0_B No interrupt occurred 1_B AEIM_IM_ADDR interrupt was raised by the AEI master port interface
AEIM_USP_BE	6	rw	**AEI master port unsupported byte enable interrupt** This bit will be cleared on a CPU write access of value '1'. A read access leaves the bit unchanged. 0_B No interrupt occurred 1_B AEIM_USP_BE interrupt was raised by the AEI master port interface
CLK_EN_ERR	7	rw	**Clock enable error interrupt** This bit will be cleared on a CPU write access of value '1'. A read access leaves the bit unchanged. Read as zero in case of INT_CLK_EN_GEN = 0b1. 0_B No interrupt occurred 1_B CLK_EN_ERR interrupt was raised by clock enable watchdog
CLK_PER_ERR	8	rw	**Clock period error interrupt** This bit will be cleared on a CPU write access of value '1'. A read access leaves the bit unchanged. Read as zero in case of INT_CLK_EN_GEN = 0b1. 0_B No interrupt occurred 1_B CLK_PER_ERR interrupt was raised by clock enable watchdog
CLK_EN_ERR_STATE0	24	r	**Erroneous clock enable state** This bit field defines the GTM external clk enable state for internal clock aei_sys_clkat occurrence of the CLK_EN_ERR event. **Function only available with INT_CLK_EN_GEN = 0b0:** Read as zero in case of INT_CLK_EN_GEN = 0b1. 0_B Internal clock aei_sys_clk disabled 1_B Internal clock aei_sys_clk enabled
CLK_EN_ERR_STATE1	25	r	**Erroneous clock enable state** This bit field defines the GTM external clk enable state for internal clock aei_sys_clk / 2 at occurrence of the CLK_EN_ERR event. **Function only available with INT_CLK_EN_GEN = 0b0:** Read as zero in case of INT_CLK_EN_GEN = 0b1. 0_B Internal clock aei_sys_clk / 2 disabled 1_B Internal clock aei_sys_clk / 2 enabled
CLK_EN_EXP_STATE0	28	r	**Expected clock enable state** This bit field defines the GTM expected clk enable state for internal clock aei_sys_clk at occurrence of the CLK_EN_ERR event. **Function only available with INT_CLK_EN_GEN = 0b0:** Read as zero in case of INT_CLK_EN_GEN = 0b1. 0_B Internal clock aei_sys_clk disabled 1_B Internal clock aei_sys_clk enabled

Field	Bits	Type	Description
CLK_EN_EXP_STATE1	29	r	**Expected clock enable state** This bit field defines the GTM expected clk enable state for internal clock aei_sys_clk / 2 at occurrence of the CLK_EN_ERR event. **Function only available with INT_CLK_EN_GEN = 0b0:** Read as zero in case of INT_CLK_EN_GEN = 0b1. 0_B Internal clock aei_sys_clk / 20 disabled 1_B Internal clock aei_sys_clk / 20 enabled
0	23:9, 27:26, 31:30	r	**Reserved** Read as zero, shall be written as zero.

28.4.9.7 Register GTM_IRQ_EN

GTM Interrupt Enable Register

IRQ_EN
GTM Interrupt Enable Register **(000014_H)** **Application Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							CLK_PER_ERR_IRQ_EN	CLK_EN_ERR_IRQ_EN	AEIM_USP_BE_IRQ_EN	AEIM_IM_ADDR_IRQ_EN	AEIM_USP_ADDR_IRQ_E	AEI_USP_BE_IRQ_EN	AEI_IM_ADDR_IRQ_EN	AEI_USP_ADDR_IRQ_EN	AEI_TO_XPT_IRQ_EN
r							rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
AEI_TO_XPT_IRQ_EN	0	rw	**AEI_TO_XPT_IRQ interrupt enable** 0_B Disable interrupt, interrupt is not visible outside GTM 1_B Enable interrupt, interrupt is visible outside GTM
AEI_USP_ADDR_IRQ_EN	1	rw	**AEI_USP_ADDR_IRQ interrupt enable** 0_B Disable interrupt, interrupt is not visible outside GTM 1_B Enable interrupt, interrupt is visible outside GTM
AEI_IM_ADDR_IRQ_EN	2	rw	**AEI_IM_ADDR_IRQ interrupt enable** 0_B Disable interrupt, interrupt is not visible outside GTM 1_B Enable interrupt, interrupt is visible outside GTM
AEI_USP_BE_IRQ_EN	3	rw	**AEI_USP_BE_IRQ interrupt enable** 0_B Disable interrupt, interrupt is not visible outside GTM 1_B Enable interrupt, interrupt is visible outside GTM
AEIM_USP_ADDR_IRQ_EN	4	rw	**AEI_MUSP_ADDR_IRQ interrupt enable** 0_B Disable interrupt, interrupt is not visible outside GTM 1_B Enable interrupt, interrupt is visible outside GTM

Field	Bits	Type	Description
AEIM_IM_ADDR_IRQ_EN	5	rw	**AEIM_IM_ADDR_IRQ interrupt enable** 0_B Disable interrupt, interrupt is not visible outside GTM 1_B Enable interrupt, interrupt is visible outside GTM
AEIM_USP_BE_IRQ_EN	6	rw	**AEIM_USP_BE_IRQ interrupt enable** 0_B Disable interrupt, interrupt is not visible outside GTM 1_B Enable interrupt, interrupt is visible outside GTM
CLK_EN_ERR_IRQ_EN	7	rw	**CLK_EN_ERR_IRQ interrupt enable** Read as zero in case of INT_CLK_EN_GEN = 0b1. 0_B Disable interrupt, interrupt is not visible outside GTM 1_B Enable interrupt, interrupt is visible outside GTM
CLK_PER_ERR_IRQ_EN	8	rw	**CLK_PER_ERR_IRQ interrupt enable** Read as zero in case of INT_CLK_EN_GEN = 0b1. 0_B Disable interrupt, interrupt is not visible outside GTM 1_B Enable interrupt, interrupt is visible outside GTM
0	31:9	r	**Reserved** Read as zero, shall be written as zero.

28.4.9.8 Register GTM_IRQ_FORCINT

GTM Software Interrupt Generation Register

IRQ_FORCINT
GTM Software Interrupt Generation Register (000018$_H$) **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							TRG_CLK_PER_ERR	TRG_CLK_EN_ERR	TRG_AEIM_USP_BE	TRG_AEIM_IM_ADDR	TRG_AEIM_USP_ADDR	TRG_AEI_USP_BE	TRG_AEI_IM_ADDR	TRG_AEI_USP_ADDR	TRG_AEI_TO_XPT
r							rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
TRG_AEI_TO_XPT	0	rw	**Trigger AEI_TO_XPT_IRQ interrupt by software** This bit is cleared automatically after write. This bit is write protected by bit RF_PROT of **CTRL** 0_B No interrupt triggering 1_B Assert AEI_TO_XPT_IRQ interrupt for one clock cycle
TRG_AEI_USP_ADDR	1	rw	**Trigger AEI_USP_ADDR_IRQ interrupt by software** This bit is cleared automatically after write. This bit is write protected by bit RF_PROT of **CTRL** 0_B No interrupt triggering 1_B Assert AEI_USP_ADDR_IRQ interrupt for one clock cycle

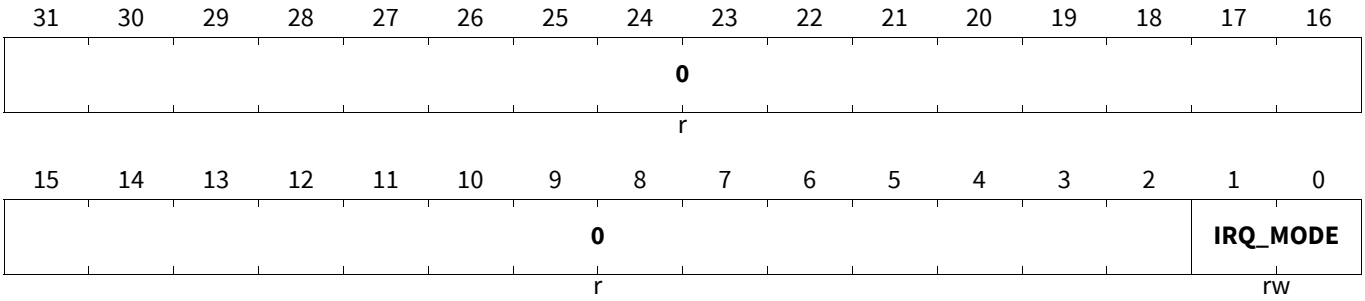
Field	Bits	Type	Description
TRG_AEI_IM_ADDR	2	rw	**Trigger AEI_IM_ADDR_IRQ interrupt by software** This bit is cleared automatically after write. This bit is write protected by bit RF_PROT of **CTRL** 0_B No interrupt triggering 1_B Assert AEI_IM_ADDR_IRQ interrupt for one clock cycle
TRG_AEI_USP_BE	3	rw	**Trigger AEI_USP_BE_IRQ interrupt by software** This bit is cleared automatically after write. This bit is write protected by bit RF_PROT of **CTRL** 0_B No interrupt triggering 1_B Assert AEI_USP_BE_IRQ interrupt for one clock cycle
TRG_AEIM_USP_ADDR	4	rw	**Trigger AEIM_USP_ADDR_IRQ interrupt by software** This bit is cleared automatically after write. This bit is write protected by bit RF_PROT of **CTRL** 0_B No interrupt triggering 1_B Assert AEIM_USP_ADDR_IRQ interrupt for one clock cycle
TRG_AEIM_IM_ADDR	5	rw	**Trigger AEIM_IM_ADDR_IRQ interrupt by software** This bit is cleared automatically after write. This bit is write protected by bit RF_PROT of **CTRL** 0_B No interrupt triggering 1_B Assert AEIM_IM_ADDR_IRQ interrupt for one clock cycle
TRG_AEIM_USP_BE	6	rw	**Trigger AEIM_USP_BE_IRQ interrupt by software** This bit is cleared automatically after write. This bit is write protected by bit RF_PROT of **CTRL** 0_B No interrupt triggering 1_B Assert AEIM_USP_BE_IRQ interrupt for one clock cycle
TRG_CLK_EN_ERR	7	rw	**Trigger CLK_EN_ERR_IRQ interrupt by software** This bit is cleared automatically after write. This bit is write protected by bit RF_PROT of **CTRL** Read as zero in case of INT_CLK_EN_GEN = 0b1. 0_B No interrupt triggering 1_B Assert CLK_EN_ERR_IRQ interrupt for one clock cycle
TRG_CLK_PER_ERR	8	rw	**Trigger CLK_PER_ERR_IRQ interrupt by software** This bit is cleared automatically after write. This bit is write protected by bit RF_PROT of **CTRL** Read as zero in case of INT_CLK_EN_GEN = 0b1. 0_B No interrupt triggering 1_B Assert CLK_PER_ERR_IRQ interrupt for one clock cycle
0	31:9	r	**Reserved** Read as zero, shall be written as zero.

28.4.9.9 Register GTM_IRQ_MODE

GTM Top Level Interrupts Mode Selection Register

IRQ_MODE

GTM Top Level Interrupts Mode Selection Register(00001C$_H$) **Application Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
IRQ_MODE	1:0	rw	**Interrupt strategy mode selection for the AEI timeout and address monitoring interrupts** The interrupt modes are described in **Section 28.4.5**.Note: This mode selection is only valid for the six interrupts described in section **Register GTM_IRQ_NOTIFY** 00_B Level mode 01_B Pulse mode 10_B Pulse-Notify mode 11_B Single-Pulse mode
0	31:2	r	**Reserved** Read as zero, shall be written as zero.

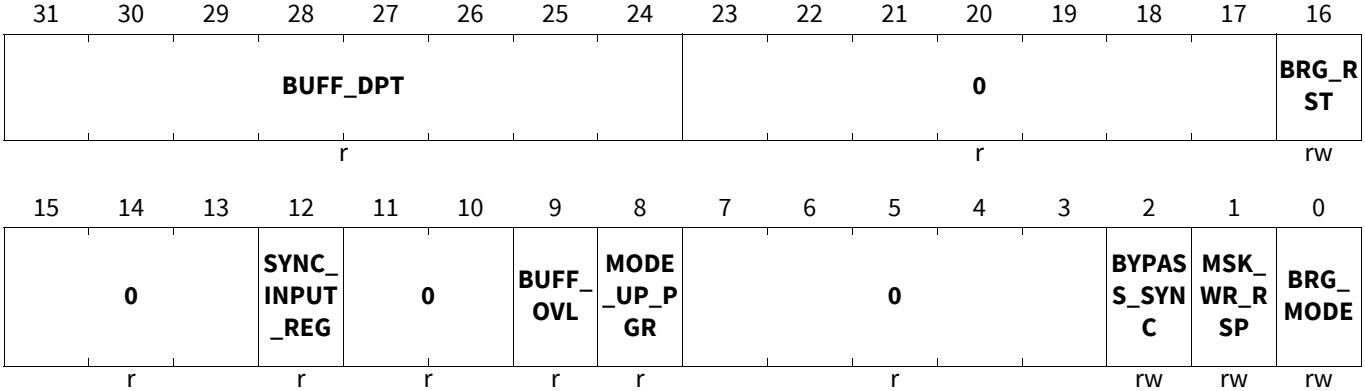
28.4.9.10 Register GTM_BRIDGE_MODE

GTM AEI Bridge Mode Register

Note: *All writable bits are write protected by bit BRIDGE_MODE_WRDIS*

BRIDGE_MODE

GTM AEI Bridge Mode Register **(000030$_H$)** **Application Reset Value: 0200 1001$_H$**



Field	Bits	Type	Description
BRG_MODE	0	rw	**Defines the operation mode for the AEI bridge** Reset value depends on the hardware configuration chosen by silicon vendor. BRG_MODE shall not be written with 0. 0_B AEI bridge operates in sync_bridge mode 1_B AEI bridge operates in async_bridge mode
MSK_WR_RSP	1	rw	**Mask write response** With active write buffer MSK_WR_RSP=1, execution of actions can be delayed due to previous inserted write actions in the transaction buffer which wait to be serviced. This can lead to the fact that an access on the bus to a different peripheral than the GTM might be executed earlier in time than the write access buffered in the GTM. Applications must be setup up with this in mind otherwise unexpected operation can happen. 0_B Do not mask the write response. Depending on the selected address the latency for execution can vary due to GTM internal arbitration. After this time the status of the access will be signaled by the signal AEI_STATUS to the bus interface. 1_B Mask write response. The write buffer of the bridge is activated, the actual access will be stored to the write buffer, and without latency on the bus interface; the acceptance of the access is signaled. AEI_STATUS=0b00 will be signaled. In case of a full write buffer, the actual access will be postponed until the next write buffer entry becomes free. Note: The status of the executed write accesses can be observed by using the notify bits AEI_USP_ADDR ,AEI_IM_ADDR, AEI_USP_BE in the register GTM_IRQ_NOTIFY.
BYPASS_SYNC	2	rw	**Bypass synchronizer flipflops** Function only available with BRG_MODE=1 0_B Synchronizer flip-flops in use, latency increase due to synchronization (aei_clk -> aei_sys_clk and back aei_sys_clk -> aei_clk). This setting must be used if aei_clk and aei_sys_clk operate fully asynchronous by independent clock sources. 1_B Synchronizer flip-flops are bypassed. No additional latency due to synchronization. This setting can be used if aei_clk and aei_sys_clk are generated by clock gating or clock division out of a common clock source. Clock edges on aei_clk and aei_sys_clk generated out of the same clock edge of the common clock source must have zero skew.
MODE_UP_PGR	8	r	**Mode update in progress** 0_B No update in progress 1_B Update in progress
BUFF_OVL	9	r	**Buffer overflow register** A buffer overflow can occur while multiple aborts are issued by the external bus or a pipelined instruction is started while FBC = 0 (see GTM_BRIDGE_PTR1 register). 0_B No buffer overflow occurred 1_B Buffer overflow occurred

Field	Bits	Type	Description
SYNC_INPUT_REG	12	r	**Additional pipelined stage in synchronous bridge mode** Reset value depends on the hardware configuration chosen by silicon vendor. 0_B No additional pipelined stage implemented 1_B Additional pipelined stage implemented. All accesses in synchronous mode will be increased by one clock cycle.
BRG_RST	16	rw	**Bridge software reset** This bit is cleared automatically after write. 0_B No bridge reset request 1_B Bridge reset request
BUFF_DPT	31:24	r	**Buffer depth of AEI bridge** Signals the buffer depth of the GTM AEI bridge implementation. Reset value depends on the hardware configuration chosen by silicon vendor.
0	7:3, 11:10, 15:13, 23:17	r	**Reserved** Read as zero, shall be written as zero.

28.4.9.11 Register GTM_BRIDGE_PTR1

GTM AEI Bridge Pointer 1 Register

Note: This register operates on the AEI_CLK domain.

Note: This register holds diagnosis information about the AEI bus bridge. Each access to the GTM_IP will update the defined pointer bit fields. Depending on the mode of GTM_MODE_BRIDGE (BRG_MODE, MSK_WR_RESP), the AEI protocol and operating frequency which is use, the 4 pointer bit fields will change at different clock cycles relative to the start of the transaction. This leads to the fact that reading the register can show values not equal to the defined Initial Value, even directly after a write to GTM_BRIDGE_MODE with BRG_RST=1 was done.

BRIDGE_PTR1
GTM AEI Bridge Pointer 1 Register **(000034_H)** **Application Reset Value: $0020\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSP_TRAN_RDY						FBC						ABT_TRAN_PGR			
r						r						r			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABT_TRAN_PGR	TRAN_IN_PGR					FIRST_RSP_PTR					NEW_TRAN_PTR				
r	r					r					r				

Field	Bits	Type	Description
NEW_TRAN_PTR	4:0	r	**New transaction pointer** Signals the actual value of the new transaction pointer.

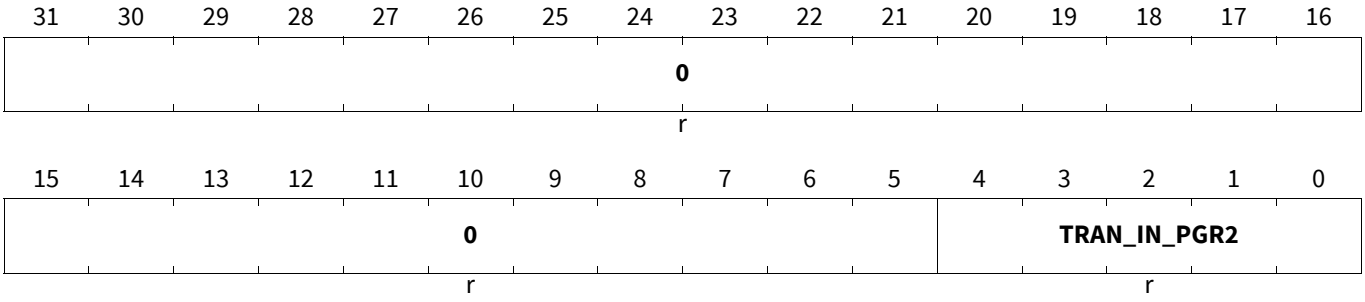
Field	Bits	Type	Description
FIRST_RSP_PTR	9:5	r	**First response pointer** Signals the actual value of first response pointer.
TRAN_IN_PGR	14:10	r	**Transaction in progress pointer (acquire)** Transaction in progress pointer.
ABT_TRAN_PGR	19:15	r	**Aborted transaction in progress pointer** Aborted transaction in progress pointer.
FBC	25:20	r	**Free buffer count** Number of free buffer entries. Initial value depends on the hardware configuration chosen by silicon vendor. (see BUFF_DPT in GTM_BRIDGE_MODE register).
RSP_TRAN_RDY	31:26	r	**Response transactions ready.** Amount of ready response transactions.

28.4.9.12 Register GTM_BRIDGE_PTR2

GTM AEI Bridge Pointer 2 Register

Note: This register operates on the GTM_CLK domain.

BRIDGE_PTR2
GTM AEI Bridge Pointer 2 Register **(000038_H)** **Application Reset Value: $0000\ 0000_H$**

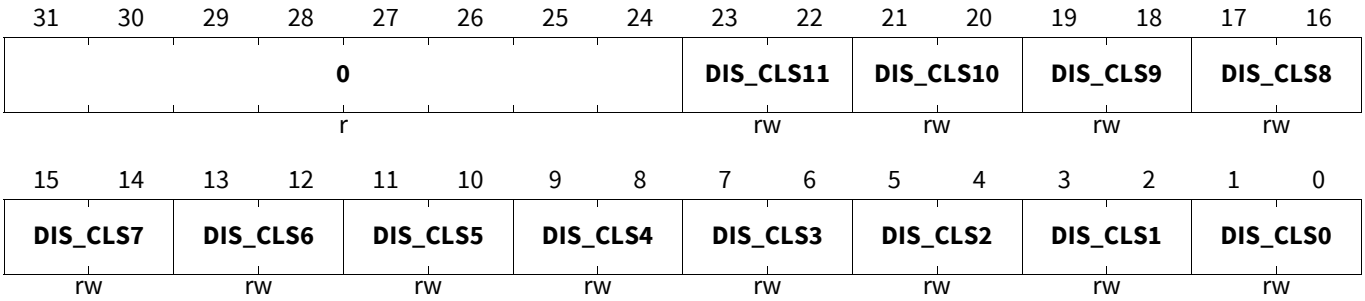


Field	Bits	Type	Description
TRAN_IN_PGR2	4:0	r	**Transaction in progress pointer (aquire2)** Transaction in progress pointer 2.
0	31:5	r	**Reserved** Read as zero, shall be written as zero.

28.4.9.13 Register GTM_MCS_AEM_DIS

GTM MCS Master Port Disable Register

MCS_AEM_DIS
GTM MCS Master Port Disable Register (00003C$_H$) Application Reset Value: 0000 0000$_H$



Field	Bits	Type	Description
DIS_CLS0	1:0	rw	**Disable MCS AEIM access in cluster 0** Multicore encoding in use (**DIS_CLSx(1)** defines the state of the signal) Any read access to a **DIS_CLSx** bit field will always result in a value 00 or 11 indicating current state. A modification of the state is only performed with the values 01 and 10. Writing the values 00 and 11 is always ignored. 00_B State is 0; MCS AEM access in cluster x enabled (ignore write access) 01_B Change state to 0 10_B Change state to 1 11_B State is 1; MCS AEM access in cluster x disabled (ignore write access)
DIS_CLS1	3:2	rw	**Disable MCS AEIM access in cluster 1, see bit DIS_CLS0**
DIS_CLS2	5:4	rw	**Disable MCS AEIM access in cluster 2, see bit DIS_CLS0**
DIS_CLS3	7:6	rw	**Disable MCS AEIM access in cluster 3, see bit DIS_CLS0**
DIS_CLS4	9:8	rw	**Disable MCS AEIM access in cluster 4, see bit DIS_CLS0**
DIS_CLS5	11:10	rw	**Disable MCS AEIM access in cluster 5, see bit DIS_CLS0**
DIS_CLS6	13:12	rw	**Disable MCS AEIM access in cluster 6, see bit DIS_CLS0**
DIS_CLS7	15:14	rw	**Disable MCS AEIM access in cluster 7, see bit DIS_CLS0**
DIS_CLS8	17:16	rw	**Disable MCS AEIM access in cluster 8, see bit DIS_CLS0**
DIS_CLS9	19:18	rw	**Disable MCS AEIM access in cluster 9, see bit DIS_CLS0**
DIS_CLS10	21:20	rw	**Disable MCS AEIM access in cluster 10, see bit DIS_CLS0**
DIS_CLS11	23:22	rw	**Disable MCS AEIM access in cluster 11, see bit DIS_CLS0**
0	31:24	r	**Reserved** Read as zero, shall be written as zero.

28.4.9.14 Register GTM_EIRQ_EN

GTM Error Interrupt Enable Register

EIRQ_EN
GTM Error Interrupt Enable Register **(000020_H)** **Application Reset Value: $0000\ 0180_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							CLK_PER_ERR_EIRQ_EN	CLK_EN_ERR_EIRQ_EN	AEIM_USP_BE_EIRQ_EN	AEIM_IM_ADDR_EIRQ_E	AEIM_USP_ADDR_EIRQ_E	AEI_USP_BE_EIRQ_EN	AEI_IM_ADDR_EIRQ_E	AEI_USP_ADDR_EIRQ_E	AEI_TO_XPT_EIRQ_EN
r							rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
AEI_TO_XPT_EIRQ_EN	0	rw	**AEI_TO_XPT_EIRQ error interrupt enable** 0_B Disable error interrupt, interrupt is not visible outside GTM 1_B Enable error interrupt, interrupt is visible outside GTM
AEI_USP_ADDR_EIRQ_EN	1	rw	**AEI_USP_ADDR_EIRQ error interrupt enable** 0_B Disable error interrupt, interrupt is not visible outside GTM 1_B Enable error interrupt, interrupt is visible outside GTM
AEI_IM_ADDR_EIRQ_EN	2	rw	**AEI_IM_ADDR_EIRQ error interrupt enable** 0_B Disable error interrupt, interrupt is not visible outside GTM 1_B Enable error interrupt, interrupt is visible outside GTM
AEI_USP_BE_EIRQ_EN	3	rw	**AEI_USP_BE_EIRQ error interrupt enable** 0_B Disable error interrupt, interrupt is not visible outside GTM 1_B Enable error interrupt, interrupt is visible outside GTM
AEIM_USP_ADDR_EIRQ_EN	4	rw	**AEIM_USP_ADDR_EIRQ error interrupt enable** 0_B Disable error interrupt, interrupt is not visible outside GTM 1_B Enable error interrupt, interrupt is visible outside GTM
AEIM_IM_ADDR_EIRQ_EN	5	rw	**AEIM_IM_ADDR_EIRQ error interrupt enable** 0_B Disable error interrupt, interrupt is not visible outside GTM 1_B Enable error interrupt, interrupt is visible outside GTM
AEIM_USP_BE_EIRQ_EN	6	rw	**AEIM_USP_BE_EIRQ error interrupt enable** 0_B Disable error interrupt, interrupt is not visible outside GTM 1_B Enable error interrupt, interrupt is visible outside GTM
CLK_EN_ERR_EIRQ_EN	7	rw	**CLK_EN_ERR_EIRQ interrupt enable** Read as zero in case of INT_CLK_EN_GEN = 0b1. 0_B Disable error interrupt, interrupt is not visible outside GTM 1_B Enable error interrupt, interrupt is visible outside GTM

Field	Bits	Type	Description
CLK_PER_ERR_EIRQ_EN	8	rw	**CLK_PER_ERR_EIRQ interrupt enable** Read as zero in case of INT_CLK_EN_GEN = 0b1. Read as zero, shall be written as zero. 0_B Disable error interrupt, interrupt is not visible outside GTM 1_B Enable error interrupt, interrupt is visible outside GTM
0	31:9	r	**Reserved** Read as zero, shall be written as zero.

28.4.9.15 Register GTM_CLS_CLK_CFG

GTM Cluster Clock Configuration

Note: For clusters greater than 4 (only MAX 100 MHz capable), the allowed setting for the CLS_CLK_DIV are 00_B and 10_B (clock divider 2). For clusters < 5, 200 MHz is available. In case a device has a single 100 MHz cluster, the ARU will run with 100 MHz.

Note: Writing a value to a bit field CLS[c]_CLK_DIV that is not available in the device, an AEI status 10_B is returned.

Note: The availability of configuration bits is indicated by value of bit CFG_CLOCK_RATE in register CCM[c]_HW_CFG. If CFG_CLOCK_RATE=0, only the values 00_B and 01_B are valid for bit fields CLS[c]_CLK_DIV.

CLS_CLK_CFG
GTM Cluster Clock Configuration **($0000B0_H$)** **Application Reset Value: $00AA\ AAAA_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								CLS11_CLK_DIV		CLS10_CLK_DIV		CLS9_CLK_DIV		CLS8_CLK_DIV	
r								rw		rw		rw		rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CLS7_CLK_DIV		CLS6_CLK_DIV		CLS5_CLK_DIV		CLS4_CLK_DIV		CLS3_CLK_DIV		CLS2_CLK_DIV		CLS1_CLK_DIV		CLS0_CLK_DIV	
rw		rw		rw		rw		rw		rw		rw		rw	

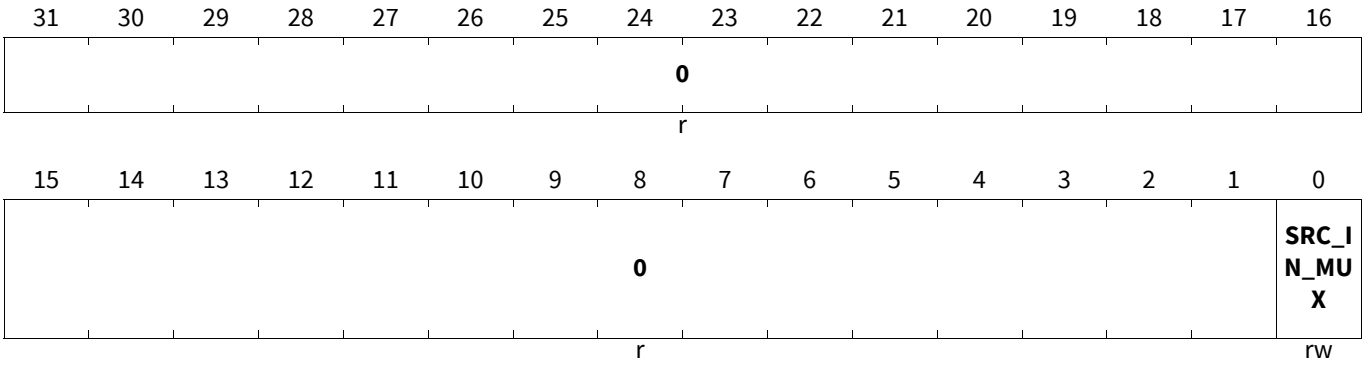
Field	Bits	Type	Description
CLSc_CLK_DIV (c=0-11)	2*c+1:2*c	rw	**Cluster c Clock Divider** This bit is only writable if bit field **RF_PROT** of register **GTM_CTRL** is cleared. 00_B Cluster c is disabled 01_B Cluster c is enabled without clock divider 10_B Cluster c is enabled with clock divider 11_B Reserved, do not use.
0	31:24	r	**Reserved** Read as zero, shall be written as zero.

28.4.9.16 Register GTM_CFG

GTM Configuration Register

CFG

GTM Configuration Register **(000028_H)** **Application Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
SRC_IN_MUX	0	rw	**GTM_TIM[i]_AUX_IN input source selection** See **Figure 9** for details. 0_B Use for TIM[i] output of TOM[n] 1_B Use for TIM[i] output of TOM[i] (same cluster)
0	31:1	r	**Reserved** Read as zero, shall be written as zero.