28.15 ARU-connected Timer Output Module (ATOM)

28.15.1 Overview

The ARU-connected Timer Output Module (ATOM) is able to generate complex output signals without CPU interaction due to its connectivity to the ARU. Typically, output signal characteristics are provided over the ARU connection through sub-modules connected to ARU like e.g. the MCS, DPLL or PSM. Each ATOM sub-module contains eight output channels which can operate independently from each other in several configurable operation modes. A block diagram of the ATOM sub-module is depicted in **Figure 62**.

The following design variables are used inside this chapter. Please refer to device specific appendix for correct value.

cCATO: ATOM channel count; number of channels per instance - 1

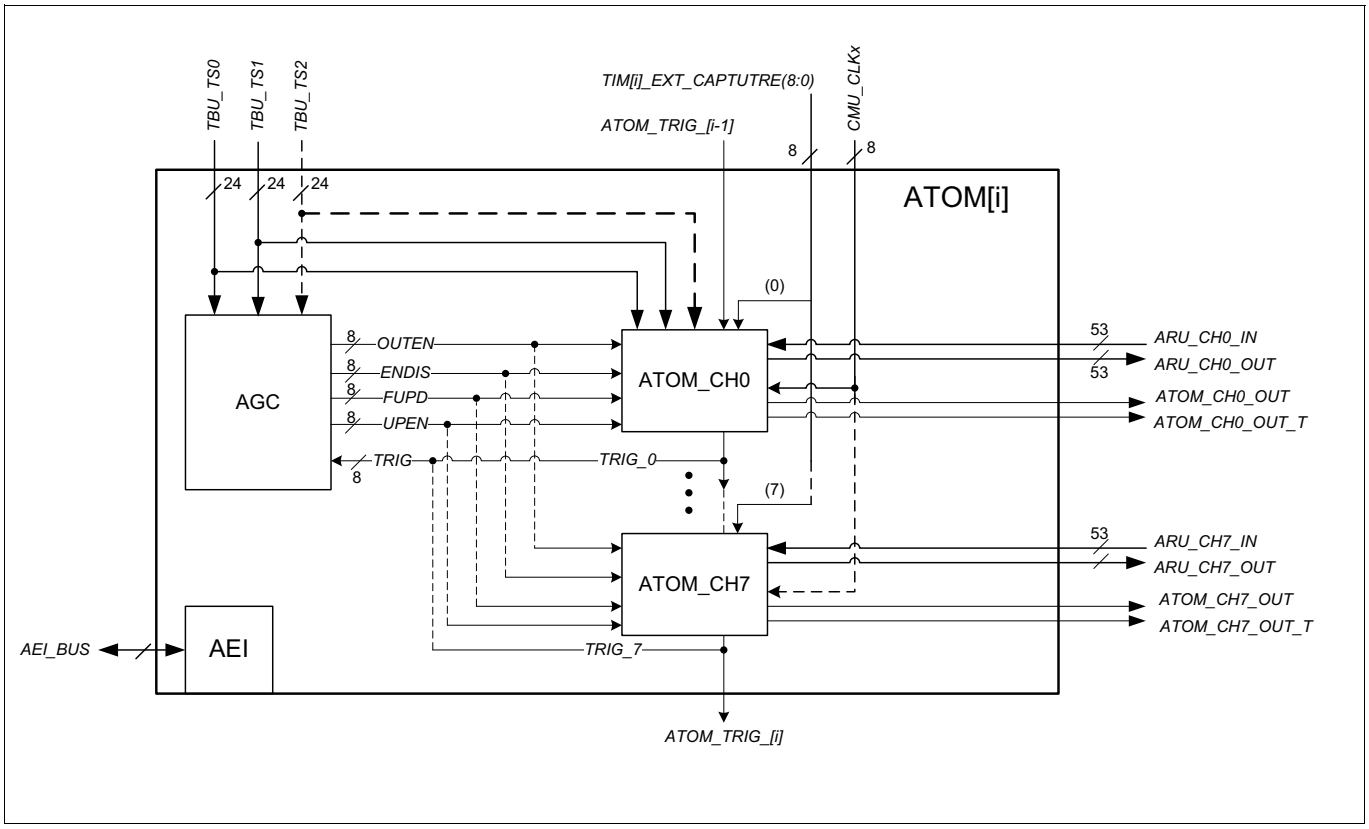


Figure 62 ATOM block diagram

The architecture of the ATOM sub-module is similar to the TOM sub-module, but there are some differences. First, the ATOM integrates only eight output channels. Hence, there exists one ATOM Global Control sub-unit (AGC) for the ATOM channels. The ATOM is connected to the ARU and can set up individual read requests from the ARU and write requests to the ARU. Furthermore, the ATOM channels are able to generate signals on behalf of time stamps and the ATOM channels are able to generate a serial output signal on behalf of an internal shift register.

Each ATOM channel provides five modes of operation:

- ATOM Signal Output Mode Immediate (SOMI)
- ATOM Signal Output Mode Compare (SOMC)
- ATOM Signal Output Mode PWM (SOMP)
- ATOM Signal Output Mode Serial (SOMS)

- ATOM Signal Output Mode Buffered Compare (SOMB)

These modes are described in more detail in **Section 28.15.3**.

The ATOM channels' operation registers (e.g. counter, compare registers) are 24 bit wide. Moreover, the input clocks for the ATOM channels come from the configurable *CMU_CLKx* signals of the CMU sub-module. This gives the freedom to select a programmable input clock for the ATOM channel counters. The ATOM channel is able to generate a serial bit stream, which is shifted out at the *ATOM[i]_CH[x]_OUT* output. When configured in this serial shift mode (SOMS) the selected CMU clock defines the shift frequency.

Each ATOM channel provides a so called *operation* and *shadow* register set. With this architecture it is possible to work with the operation register set, while the shadow register set can be reloaded with new parameters over CPU and/or ARU.

When update via ARU is selected, it is possible to configure for ATOM SOMP mode if both shadow registers are updated via ARU or only one of the shadow registers is updated.

On the other hand, the shadow registers can be used to provide data to the ARU when one or both of the compare units inside an ATOM channel match. This feature is only applicable in SOMC mode.

In TOM channels it is possible to reload the content of the operation registers with the content of the corresponding shadow registers and change the clock input signal for the counter register simultaneously. This simultaneous change of the input clock frequency together with reloading the operation registers is also implemented in the ATOM channels.

In addition to the feature that the CPU can select another *CMU_CLKx* during operation (i.e. updating the shadow register bit field CLK_SRC_SR of the **ATOM[i]_CH[x]_CTRL** register), the selection can also be changed via the ARU. Then, for the clock source update, the ACBI register bits of the **ATOM[i]_CH[x]_STAT** register are used as a shadow register for the new clock source.

In general, the behavior of the compare units CCU0 and CCU1 and the output signal behavior is controlled with the ACB bit field inside the **ATOM[i]_CH[x]_CTRL** register when the ARU connection is disabled and the behavior is controlled via ARU through the ACBI bit field of the **ATOM[i]_CH[x]_STAT** register, when the ARU is enabled.

Since the ATOM is connected to the ARU, the shadow registers of an ATOM channel can be reloaded via the ARU connection or via CPU over its AEI interface. When loaded via the ARU interface, the shadow registers act as a buffer between the ARU and the channel operation registers. Thus, a new parameter set for a PWM can be reloaded via ARU into the shadow registers, while the operation registers work on the actual parameter set.

The trigger signal *ATOM_TRIG_[i-1]* of ATOM instance i comes from the preceding instance i-1, the trigger *ATOM_TRIG_[i]* is routed to succeeding instance i+1. Note, ATOM0 is connected to its own output ATOM_TRIG_0, i.e. the last channel of ATOM instance 0 can trigger the first channel of ATOM instance 0 (this path is registered, which means delayed by one SYS_CLK period).

28.15.1.1 ATOM Global Control (AGC)

Synchronous start, stop and update of work register of up to 8 channels is possible with the AGC sub-unit. This sub-unit has the same functionality as the TGC sub-unit of the TOM sub-module.

28.15.1.1.1 Overview

There exists one global channel control unit (AGC) to drive a number of individual ATOM channels synchronously by external or internal events.

An AGC can drive up to eight ATOM channels.

The ATOM sub-module supports four different kinds of signaling mechanisms:

- Global enable/disable mechanism for each ATOM channel with control register **ATOM[i]_AGC_ENDIS_CTRL** and status register **ATOM[i]_AGC_ENDIS_STAT**

- Global output enable mechanism for each ATOM channel with control register **ATOM[i]_AGC_OUTEN_CTRL** and status register **ATOM[i]_AGC_OUTEN_STAT**
- Global force update mechanism for each ATOM channel with control register **ATOM[i]_AGC_FUPD_CTRL**
- Update enable of the register **CM0**, **CM1** and **CLK_SRC** for each ATOM channel with the control bit field **UPEN_CTRL[z]** of **ATOM[i]_AGC_GLB_CTRL**

28.15.1.1.2 AGC Sub-unit

Each of the first three individual mechanisms (enable/disable of the channel, output enable and force update) can be driven by three different trigger sources. The three trigger sources are:

- the host CPU (bit **HOST_TRIG** of register **ATOM[i]_AGC_GLB_CTRL**)
- the TBU time stamp (signal *TBU_TS0…2* if available)
- the internal trigger signal *TRIG* (bunch of trigger signals *TRIG_[x]* which can be either the trigger *TRIG_CCU0* of channel x, the trigger of preceding channel x-1 (i.e. signal *TRIG_[x-1]*) or the external trigger *TIM_EXT_CAPTURE(x)* of assigned TIM channel x.

The first way is to trigger the control mechanism by a direct register write access via host CPU (bit **HOST_TRIG** of register **AOM[i]_AGC_GLB_CTRL**).

The second way is provided by a compare match trigger on behalf of a specified time base coming from the module TBU (selected by bits **TBU_SEL**) and the time stamp compare value defined in the bit field **ACT_TB** of register **ATOM[i]_AGC_ACT_TB**. Note, a cyclic event compare of **ACT_TB** and selected *TBU_TS*[*x*] is performed.

The third possibility is the input *TRIG* (bunch of trigger signals *TRIG_[x]*) coming from the ATOM channels 0 to 7.

The corresponding trigger signal *TRIG_[x]* coming from channel [x] can be masked by the register **ATOM[i]_AGC_INT_TRIG**.

To enable or disable each individual ATOM channel, the registers **ATOM[i]_AGC_ENDIS_CTRL** and/or **ATOM[i]_AGC_ENDIS_STAT** have to be used.

The register **ATOM[i]_AGC_ENDIS_STAT** controls directly the signal *ENDIS*. A write access to this register is possible.

The register **ATOM[i]_AGC_ENDIS_CTRL** is a shadow register that overwrites the value of register **AOM[i]_AGC_ENDIS_STAT** if one of the three trigger conditions matches.

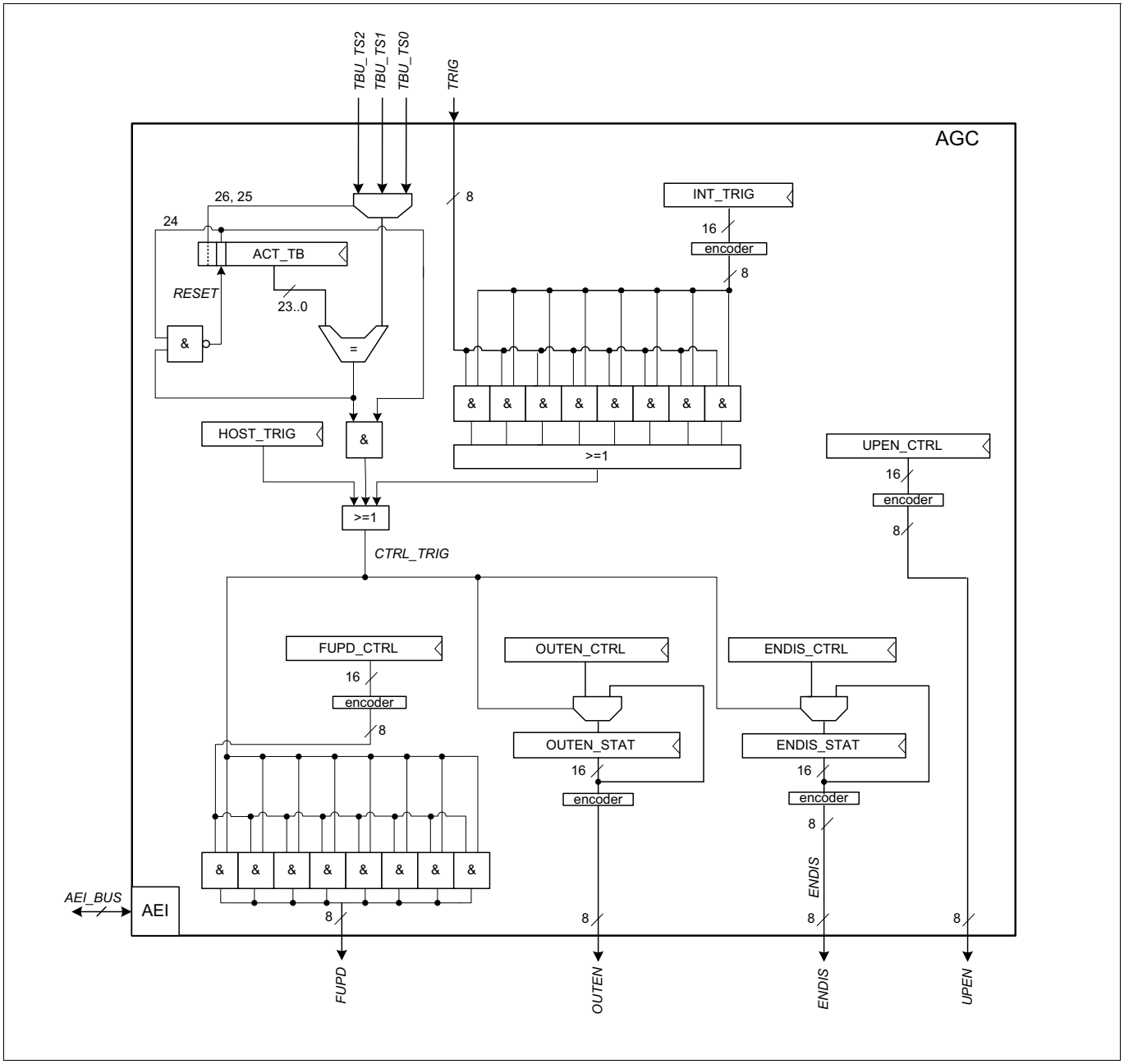


Figure 63 ATOM Global channel control mechanism

The output of the individual ATOM channels can be controlled using the register **ATOM[i]_AGC_OUTEN_CTRL** and **ATOM[i]_AGC_OUTEN_STAT**.

The register **ATOM[i]_AGC_OUTEN_STAT** controls directly the signal *OUTEN*. A write access to this register is possible.

The register **ATOM[i]_AGC_OUTEN_CTRL** is a shadow register that overwrites the value of register **ATOM[i]_AGC_OUTEN_STAT** if one of the three trigger conditions matches.

If an ATOM channel is disabled by the register **ATOM[i]_AGC_OUTEN_STAT**, the actual value of the channel output at *ATOM_CH[x]_OUT* is defined by the signal level bit (**SL**) defined in the channel control register **ATOM[i]_CH[x]_CTRL**.If the output is enabled, the output at *ATOM_CH[x]_OUT* depends on value of FlipFlop **SOUR**.

The register **ATOM[i]_AGC_FUPD_CTRL** defines which of the ATOM channels receive a *FORCE_UPDATE* event if the trigger signal *CTRL_TRIG* is raised. Note: In SOMP mode the force update request is stored and executed synchronized to the selected CMU_CLK. In all other modes the force update request is executed immediately.

The register bits **UPEN_CTRL[x]** defines for which ATOM channel the update of the working register **CM0**, **CM1** and **CLK_SRC** by the corresponding shadow register **SR0**, **SR1** and **CLK_SRC_SR** is enabled. If update is enabled, the register **CM0**, **CM1** and **CLK_SRC** will be updated on reset of counter register **CN0** (see **Figure 64**).

28.15.1.2 ATOM Channel Mode Overview

Each ATOM channel offers the following different operation modes:

In ATOM Signal Output Mode Immediate (**SOMI**), the ATOM channels generate an output signal immediately after receiving an ARU word according to the two signal level output bits of the ARU word received through the ACBI bit field. Due to the fact, that the ARU destination channels are served in a round robin order, the output signal can jitter in this mode with a jitter of the ARU round trip time.

In ATOM Signal Output Mode Compare (**SOMC**), the ATOM channel generates an output signal on behalf of time stamps that are located in the ATOM operation registers. These time stamps are compared with the time stamps, the TBU generates. The ATOM is able to receive new time stamps either by CPU or via the ARU. The new time stamps are directly loaded into the channels operation register. The shadow registers are used as capture registers for two time base values, when a compare match of the channels operation registers occurs.

In ATOM Signal Output Mode PWM (**SOMP**), the ATOM channel is able to generate simple and complex PWM output signals like the TOM sub-module by comparing its operation registers with a sub-module internal counter. In difference to the TOM, the ATOM shadow registers can be reloaded by the CPU and by the ARU in the background, while the channel operates on the operation registers.

In ATOM Signal Output Mode Serial (**SOMS**), the ATOM channel generates a serial output bit stream on behalf of a shift register. The number of bits shifted and the shift direction is configurable. The shift frequency is determined by one of the *CMU_CLKx* clock signals. Please refer to **Section 28.15.3.4** for further details.

In ATOM Signal Output Buffered Compare (**SOMB**), the ATOM channel generates an output signal on behalf of time stamps that located in the ATOM operation registers. These time stamps are compared with the time stamps, the TBU generates. The ATOM is able to receive new compare values either by CPU or via the ARU. The new compare values received via ARU are stored first in the shadow register and only if previous compare match is occurred, the operation register are updated with the content of the shadow register.

28.15.2 ATOM Channel Architecture

Each ATOM channel is able to generate output signals according to five operation modes. The architecture of the ATOM channels is similar to the architecture of the TOM channels. The general architecture of an ATOM channel is depicted in **Figure 64**.

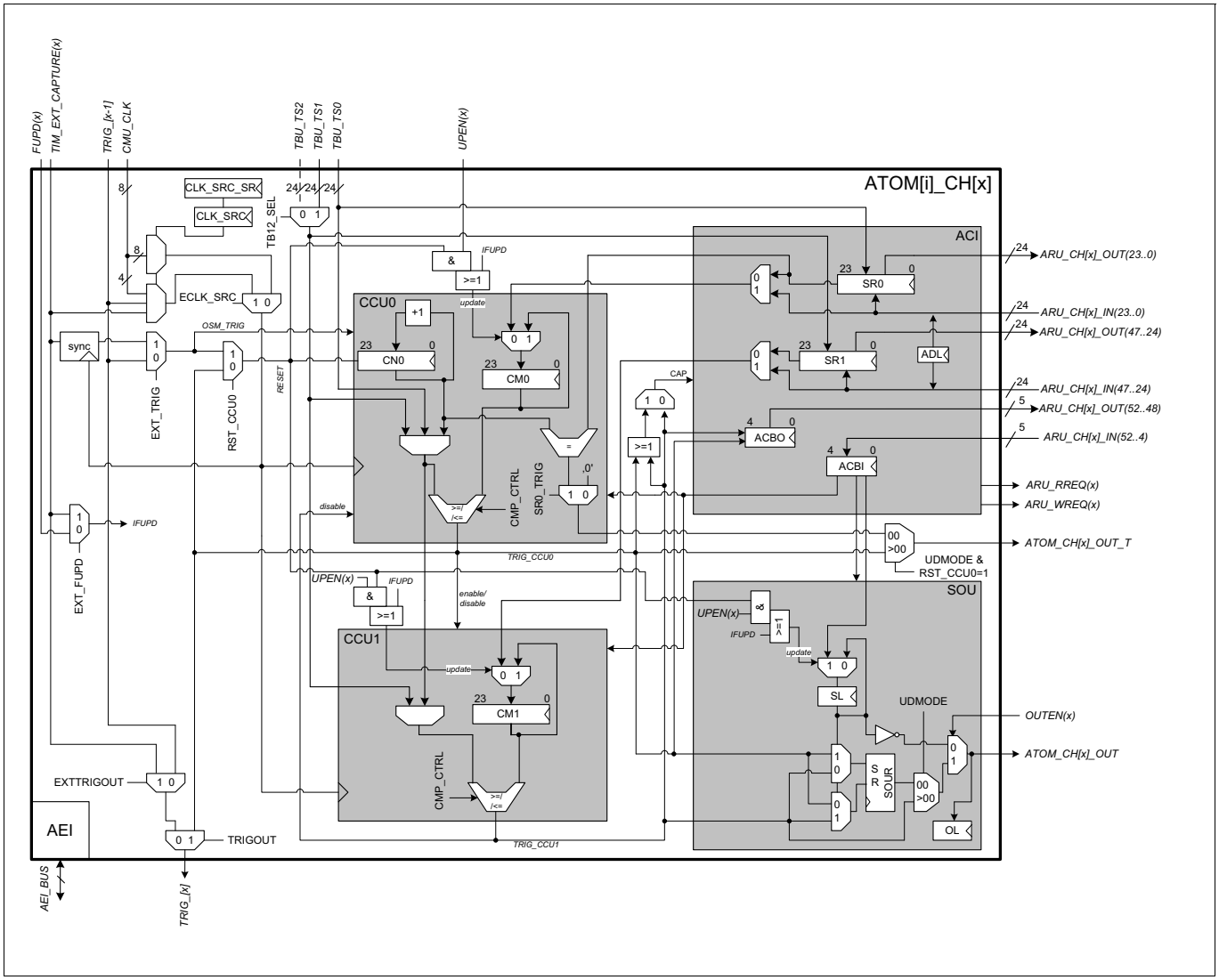


Figure 64 ATOM channel architecture

In all ATOM channels the operation registers **CN0**, **CM0** and **CM1** and the shadow registers **SR0** and **SR1** are the 24 bit width. The comparators inside CCU0 and CCU1 provide a selectable signed greater-equal or less-equal comparison to compare against the GTM time bases *TBU_TS0*, *TBU_TS1* and, if available, *TBU_TS2*. Please refer to TBU (chapter: “Time Base Unit”) for further details. The CCU0 and CCU1 units have different tasks for the different ATOM channel modes.

The cyclic event compare is used to detect time base overflows and to guarantee, that a compare match event can be set up for the future even when the time base will first overflow and then reach the compare value. Please note, that for a correct behavior of this cyclic event compare, the new compare value must not be specified larger/smaller than half of the range of the total time base value (0x7FFFFF).

In SOMC/SOMB mode, the two compare units CCUx can be used in combination to each other. When used in combination, the trigger lines *TRIG_CCU0* and *TRIG_CCU1* can be used to enable/disable the other compare unit on a match event. Please refer to **Section 28.15.3.2** and **Section 28.15.3.5** for further details.

The Signal Output Unit (SOU) generates the output signal for each ATOM channel. This output signal level depends on the ATOM channel mode and on the **SL** bit of the **ATOM[i]_CH[x]_CTRL** register in combination with the two control bits. These two control bits **ACB(1)** and **ACB(0)** can either be received via CPU in the ACB register field of the **ATOM[i]_CH[x]_CTRL** register or via ARU in the ACBI bit field of the **ATOM[i]_CH[x]_STAT** register.

The **SL** bit in the **ATOM[i]_CH[x]_CTRL** register defines in all modes the operational behavior of the ATOM channel.

When the channel and its output are disabled, the output signal level of the channel is the inverse of the **SL** bit.

In SOMI, SOMC and SOMB mode the output signal level depends on the **SL**, **ACB0** and **ACB1** bits. In SOMP mode the output signal level depends on the two trigger signals *TRIG_CCU0* and *TRIG_CCU1* since theses two triggers define the PWM timing characteristics and the **SL** bit defines the level of the duty cycle. In SOMS mode the output signal level is defined by the bit pattern that has to be shifted out by the ATOM channel. The bit pattern is located inside the **CM1** register.

The ARU Communication Interface (ACI) sub-unit is responsible for requesting data routed through ARU to the ATOM channel in SOMI, SOMP, SOMB and SOMS modes, and additionally for providing data to the ARU in SOMC mode.

In SOMC mode the ACI shadow registers have a different behavior and are used as output buffer registers for data send to ARU.

28.15.2.1 ARU Communication Interface

The ATOM channels have an ARU Communication Interface (ACI) sub-unit. This sub-unit is responsible for data exchange from and to the ARU. This is done with the two implemented registers **SR0**, **SR1**, and the **ACBI** and **ACBO** bit fields that are part of the **ATOM[i]_CH[x]_STAT** register. The ACI architecture is shown in **Figure 65**.

If the **ARU_EN** bit is set inside the **ATOM[i]_CH[x]_CTRL** register, the ATOM channel is enabled by setting the enable bits inside the **ATOM[i]_AGC_ENDIS_STAT** register and the CPU hasn't written data not equal to zero into the **CM0**, **CM1, SR0, SR1** register, the ATOM channel will first request data from the ARU before the signal generation starts in SOMP, SOMS, SOMC and SOMB mode.

Note: if in SOMP mode there is data inside the **CM0** or **SR0** register not equal to 0 the channel counter **CN0** will start counting immediately, regardless whether the channel has received ARU data yet.

Note: if in SOMS mode there is data inside the **CM0** or **SR0** register not equal to 0 the channel will start shifting immediately, regardless whether the channel has received ARU data yet.

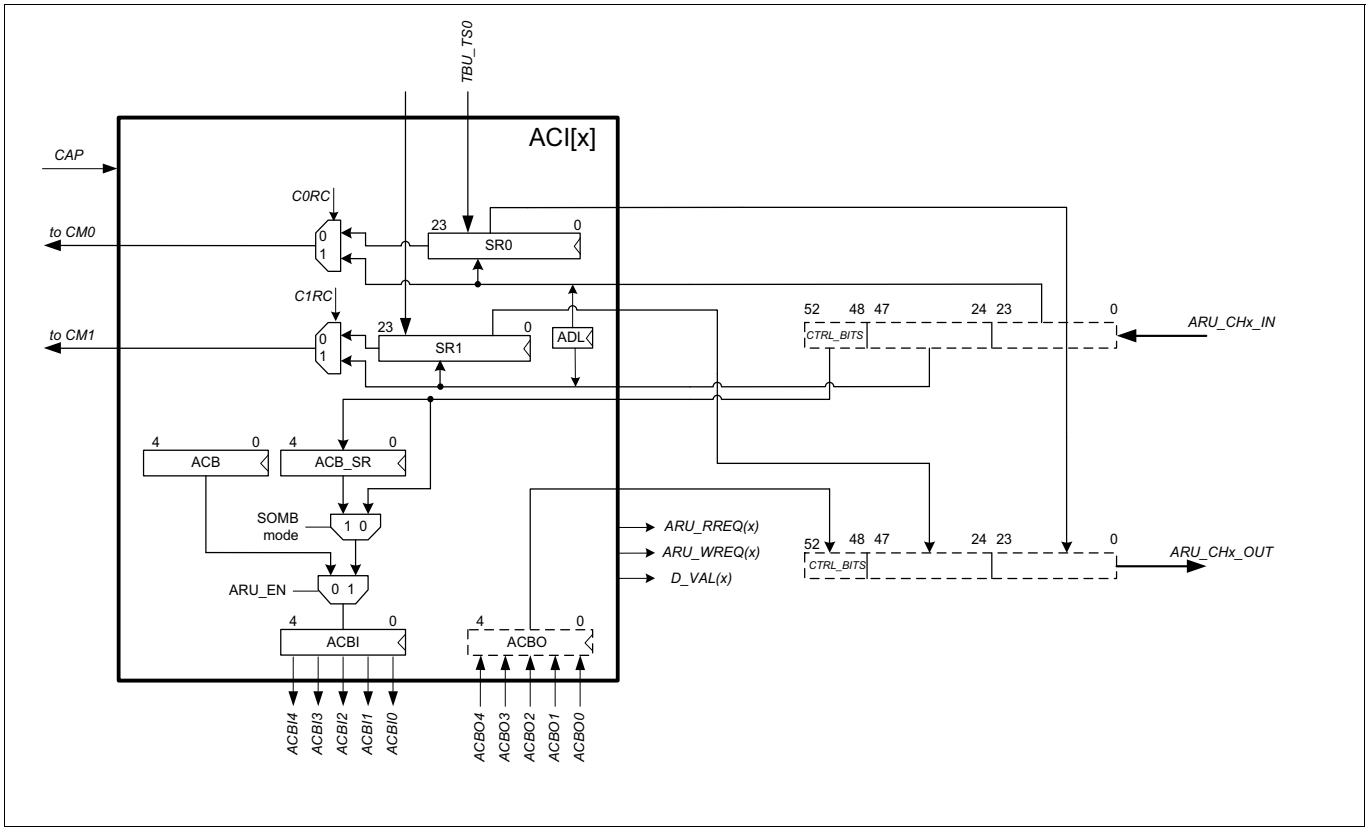


Figure 65 ACI architecture overview

Incoming ARU data (53 bit width signal *ARU_CHx_IN*) is split into three parts by the ACI and communicated to the ATOM channel registers. In SOMI, SOMP, SOMS and SOMB modes incoming ARU data *ARU_CHx_IN* is split in a way that the lower 24 bits of the ARU data (23 downto 0) are stored in the **SR0** register, the upper bits (47 downto 24) are stored in the **SR1** register. The bits 52 downto 48 (*CTRL_BITS*) are stored in SOMI, SOMP and SOMS mode in the **ACBI** bit field of the register **ATOM[i]_CH[x]_STAT**, in SOMB mode in the internal ACB_SR register.

The ATOM channel has to ensure, that in a case when the channel operation registers **CM0** and **CM1** are updated with the **SR0** and **SR1** register content and an ARU transfer to these shadow registers happens in parallel that either the old data in both shadow registers is transferred into the operation registers or both new values from the ARU are transferred.

In SOMC mode incoming ARU data *ARU_CHx_IN* is written directly to the ATOM channel operation register in the way that the lower 24 bits (23 down to 0) are written to **CM0**, and the bits 47 down to 24 are written to register **CM1**. The bits 52 down to 48 are stored in the **ACBI** bit field of the **ATOM[i]_CH[x]_STAT** register and control the behavior of the compare units and the output signal of the ATOM channel.

In SOMC mode the **SR0** and **SR1** registers serve as capture registers for the time stamps coming from TBU whenever a compare match event is signaled by the CCU0 and/or CCU1 sub-units via the *CAP* signal line. These two time stamps are then provided together with actual ATOM channel status information located in the **ACBO** bit field to the ARU at the dedicated ARU write address of the ATOM channel when the ARU is enabled.

The encoding of the ARU control bits in the different ATOM operation modes is described in more detail in the following chapters.

28.15.3 ATOM Channel Modes

As described above, each ATOM channel can operate independently from each other in one of five dedicated output modes:

- ATOM Signal Output Mode Immediate (SOMI)
- ATOM Signal Output Mode Compare (SOMC)
- ATOM Signal Output Mode PWM (SOMP)
- ATOM Signal Output Mode Serial (SOMS)
- ATOM Signal Output Mode Buffered Compare (SOMB)

The Signal Output Mode PWM (SOMP) is principally the same like the output mode for the TOM sub-module. In addition, it is possible to reload the shadow registers via the ARU without the need of a CPU interaction. The other modes provide additional functionality for signal output control. All operation modes are described in more detail in the following sections.

Note that in any output mode, if a channel is enabled, one-shot mode is disabled (**OSM**=0; only used in modes SOMP and SOMS) and CM0 >= CN0, the counter CN0 is incrementing until it reaches CM0.To avoid unintended counting of **CN0** after enabling a channel, it is recommended to reset a channel (or at least CN0 and CM0) before any change on the mode bits **MODE**, **ARU_EN** and **OSM**.

28.15.3.1 ATOM Signal Output Mode Immediate (SOMI)

In ATOM Signal Output Mode Immediate (SOMI), the ATOM channel generates output signals on the *ATOM[i]_CH[x]_OUT* output port immediate after update of the bit **ACBI(0)** of register **ATOM[i]_CH[x]_STAT** or **ACB(0)** bit of register **ATOM[i]_CH[x]_CTRL**.

If ARU access is enabled by setting bit ARU_EN in register **ATOM[i]_CH[x]_CTRL**, the update of the output *ATOM[i]_CH[x]_OUT* depends on the bit ACBI(0) of register **ATOM[i]_CH[x]_STAT** received at the ACI sub-unit and the bit **SL** bit of register **ATOM[i]_CH[x]_CTRL**. The remaining 48 ARU bits (47 downto 0) have no meaning in this mode.

If ARU access is disabled, the update of the output *ATOM[i]_CH[x]_OUT* depends on the bit **ACB(0)** and the bit **SL** of register **ATOM[i]_CH[x]_CTRL**.

The initial ATOM channel port pin *ATOM[i]_CH[x]_OUT* signal level has to be specified by the **SL** bit field of the **ATOM[i]_CH[x]_CTRL** register when **OUTEN_CTRL** register bit field **OUTEN_CTRLx** is disabled (see **Section 28.15.6.5**) for details.

In SOMI mode the output behavior depends on the **SL** bit of register **ATOM[i]_CH[x]_CTRL** and the bit **ACBI(0)** of the **ATOM[i]_CH[x]_STAT** register or the bit **ACB0** of register **ATOM[i]_CH[x]_CTRL**:

Table 50 Output behavior in SOMI mode

SL	ACBI(0)/ ACB(0)	Output behavior
0	0	Set output to inverse of SL (1)
0	1	Set output to SL (0)
1	0	Set output to inverse of SL (0)
1	1	Set output to SL (1)

The signal level bit **ACBI(0)** is transferred to the SOU sub-unit of the ATOM and made visible at the output port according to the table above immediately after the data was received by the ACI. This can introduce a jitter on the output signal since the ARU channels are served in a time multiplexed fashion.

28.15.3.1.1 Register ATOM[i]_CH[x]_CTRL in SOMI mode

Register ATOM[i]_CH[x]_CTRL in SOMI mode

GTM_ATOMi_CHx_SOMI (i=0-11; x=0-7)

ATOMi Channel x Control Register in SOMI Mode ($E8004_H$ + i*800_H+ x*80_H) **Reset Value: 00000800_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FREEZE	Not_used	Not_used	Reserved	Not_used	Not_used	Not_used	Not_used	Not_used			Not_used	Not_used		Not_used	Not_used
rw	rw	rw	r	rw	rw	r	rw	rw			rw	rw		rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not_used	Not_used			SL	Not_used	Not_used	Not_used				ACB0	ARU_EN	Not_used	MODE	
rw	rw			rw	rw	rw	rw				rw	rw	rw	rw	

Field	Bits	Type	Description
MODE	1:0	rw	**ATOM channel mode select.** 00_B ATOM Signal Output Mode Immediate (SOMI)
Not_used	2	rw	**Not used** Note: Not used in this mode.
ARU_EN	3	rw	**ARU Input stream enable** 0_B ARU Input stream disabled 1_B ARU Input stream enabled
ACB0	4	rw	**ACB bit 0** 0_B Set output to inverse of SL bit 1_B Set output to SL bit
Not_used	8:5	rw	**Not used** Note: Not used in this mode.
Not_used	9	rw	**Not used** Note: Not used in this mode.
Not_used	10	rw	**Not used** Note: Not used in this mode.
SL	11	rw	**Initial signal level after channel is enabled** 0_B Low signal level 1_B High signal level Reset value depends on the hardware configuration chosen by silicon vendor. If the output is disabled, the output ATOM_OUT[x] is set to inverse value of SL. If FREEZE=0, following note is valid: If the channel is disabled, the output register of SOU unit is set to inverse value of SL. If FREEZE=1, following note is valid: If the channel is disabled, the output register of SOU unit is not changed and output ATOM_OUT[x] is not changed.

Field	Bits	Type	Description
Not_used	14:12	rw	**Not used** Note: Not used in this mode.
Not_used	15	rw	**Not used** Note: Not used in this mode.
Not_used	16	rw	**Not used** Note: Not used in this mode.
Not_used	17	rw	**Not used** Note: Not used in this mode.
Not_used	19:18	rw	**Not used** Note: Not used in this mode.
Not_used	20	rw	**Not used** Note: Not used in this mode.
Not_used	23:21	rw	**Not used** Note: Not used in this mode.
Not_used	24	rw	**Not used** Note: Not used in this mode.
Not_used	25	r	**Not used** Note: Not used in this mode.
Not_used	26	rw	**Not used** Note: Not used in this mode.
Not_used	27	rw	**Not used** Note: Not used in this mode.
Reserved	28	r	**Reserved** Read as zero, should be written as zero.
Not_used	29	rw	**Not used** Note: Not used in this mode.
Not_used	30	rw	**Not used** Note: Not used in this mode.
FREEZE	31	rw	**FREEZE** 0_B a channel disable/enable may change internal register and output register 1_B a channel enable/disable does not change an internal or output register but stops counter CN0 (in SOMP mode), comparison (in SOMC/SOMB mode) and shifting (in SOMS mode)

28.15.3.2 ATOM Signal Output Mode Compare (SOMC)

28.15.3.2.1 Overview

In ATOM Signal Output Mode Compare (SOMC) the output action is performed in dependence of the comparison between input values located in **CM0** and/or **CM1** registers and the two (three) time base values *TBU_TS0* or *TBU_TS1* (or *TBU_TS2*) provided by the TBU. For a description of the time base generation please refer to the TBU specification in chapter “Time Base Unit”. It is configurable, which of the two (three) time bases is to be compared with one or both values in **CM0** and **CM1**.

The behavior of the two compare units CCU0 and CCU1 is controlled either with the bits 4 downto 2 of **ACB** bit field inside the **ATOM[i]_CH[x]_CTRL** register, when the ARU connection is disabled or with the ACBI bit field of the **ATOM[i]_CH[x]_STAT** register, when the ARU is enabled. In that case the **ACB** bit field is updated via the ARU control bits 52 downto 48.

The CCUx trigger signals *TRIG_CCU0* and *TRIG_CCU1* always create edges, dependent on the predefined signal level in **SL** bit in combination with two control bits that can be specified by either ARU or CPU within the aforementioned **ATOM[i]_CH[x]_CTRL** or **ATOM[i]_CH[x]_STAT** registers.

In SOMC mode the channel is always disabled after the specified compare match event occurred. The shadow registers are used to store two time stamp values at the match time. The channel compare can be re-enabled by first reading the shadow registers, either by CPU or ARU and by providing new data for CMx registers through CPU or ARU. For a detailed description please refer to the **Section 28.15.3.2.2** and **Section 28.15.3.2.3**.

If three time bases exist for the GTM there must be a preselection between *TBU_TS1* and *TBU_TS2* for the ATOM channel. This can be done with **TB12_SEL** bit in the **ATOM[i]_CH[x]_CTRL** register.

The comparison in CCU0/1 with time base TBU_TS1 or TBU_TS2 can be done on a greater-equal or less-equal compare according to the **CMP_CTRL** bit. This control bit has no effect to a compare unit CCU0 or CCU1 that compares against TBU_TS0. In this case always a greater-equal compare is done. The bit **CMP_CTRL** is part of the **ATOM[i]_CH[x]_CTRL** register.

When configured in SOMC mode, the channel port pin has to be initialized to an initial signal level. This initial level after enabling the ATOM channel is determined by the **SL** bit in the **ATOM[i]_CH[x]_CTRL** register. If the output is disabled, the signal level is set to the inverse level of the **SL** bit.

If the channel is disabled, the register SOUR is set to the **SL** bit in the **ATOM[i]_CH[x]_CTRL** register.

On a compare match event the shadow register **SR0** and **SR1** are used to capture the TBU time stamp values. **SR0** always holds *TBU_TS0* and **SR1** either holds *TBU_TS1* or *TBU_TS2* dependent on the **TB12_SEL** bit in the **ATOM[i]_CH[x]_CTRL** register.

Please note, that when the channel is disabled and the compare registers are written, the compare registers CMx are loaded with the written value and the channel starts with the comparison on behalf of this values, when the channel is enabled.

28.15.3.2.2 SOMC Mode under CPU control

As already mentioned above the ATOM channel can be controlled either by CPU or by ARU. When the channel should be controlled by CPU, the **ARU_EN** bit inside the **ATOM[i]_CH[x]_CTRL** register has to be reset.

The output of the ATOM channel is set on a compare match event depending on the **ACB10** bit field in combination with the **SL** bit both located in the **ATOM[i]_CH[x]_CTRL** register. The output behavior according to the **ACB10** bit field in the control register is shown in the following table:

Table 51 Output behavior according to the ACB10 bit field in the control register

SL	ACB10(5)	ACB10(4)	Output behavior
0	0	0	No signal level change at output (exception in table **Figure 67** mode ACB42=001)
0	0	1	Set output signal level to 1
0	1	0	Set output signal level to 0
0	1	1	Toggle output signal level (exception in table {REF:ATOM_1809} mode ACB42=001)
1	0	0	No signal level change at output (exception in table {REF:ATOM_1809} mode ACB42=001)

Table 51 Output behavior according to the ACB10 bit field in the control register (cont'd)

SL	ACB10(5)	ACB10(4)	Output behavior
1	0	1	Set output signal level to 0
1	1	0	Set output signal level to 1
1	1	1	Toggle output signal level (exception in table **Figure 67** mode ACB42=001)

The capture/compare strategy of the two CCUx units can be controlled with the **ACB42** bit field inside the **ATOM[i]_CH[x]_CTRL** register. The meaning of these bits is shown in the following table:

Table 52 Capture/compare strategy of the two CCUx units controlled by ACB42 bit field

ACB42(8)	ACB42(7)	ACB42(6)	CCUx control
0	0	0	Serve First: Compare in CCU0 using TBU_TS0 and in parallel in CCU1 using TBU_TS1 or TBU_TS2. Disable other CCUx on compare match. Output signal level on the compare match of the matching CCUx unit is defined by combination of SL, ACB10(5) and ACB10(4). Details see table**Section 67**
0	0	1	Serve First: Compare in CCU0 using TBU_TS0 and in parallel in CCU1 using TBU_TS1 or TBU_TS2. Disable other CCUx on compare match. Output signal level on the compare match of the matching CCUx unit is defined by combination of SL, ACB10(5) and ACB10(4). Details see **Section 67**
0	1	0	Compare in CCU0 only, use time base TBU_TS0. Output signal level is defined by combination of SL, ACB10(5) and ACB10(4) bits.
0	1	1	Compare in CCU1 only, use time base TBU_TS1 or TBU_TS2. Output signal level is defined by combination of SL, ACB10(5) and ACB10(4) bits.
1	0	0	Serve Last: Compare in CCU0 and then in CCU1 using TBU_TS0. Output signal level when CCU0 matches is defined by combination of SL, ACB10(5) and ACB10(4). On the CCU1 match the output level is toggled.
1	0	1	Serve Last: Compare in CCU0 and then in CCU1 using TBU_TS1 or TBU_TS2. Output signal level when CCU0 matches is defined by combination of SL, ACB10(5) and ACB10(4). On the CCU1 match the output level is toggled.
1	1	0	Serve Last: Compare in CCU0 using TBU_TS0 and then in CCU1 using TBU_TS1 or TBU_TS2. Output signal level when CCU1 matches is defined by combination of SL, ACB10(5) and ACB10(4).
1	1	1	Cancels pending comparison independent on ARU_EN

The behavior of the **ACBI**/**ACB42** bit combinations 0b000 and 0b001 is described in more detail in the tables of **Figure 66** and **Figure 67**.

ACB4	ACB3	ACB2	ACB1	ACB0	SL	CCU0 match	CCU1 match	Pin level new
0	0	0	0	0	0	0	1	hold
						1	0	hold
						1	1	hold
0	0	0	0	1	0	0	1	1
						1	0	1
						1	1	1
0	0	0	1	0	0	0	1	0
						1	0	0
						1	1	0
0	0	0	1	1	0	0	1	toggle
						1	0	toggle
						1	1	toggle
0	0	0	0	0	1	0	1	hold
						1	0	hold
						1	1	hold
0	0	0	0	1	1	0	1	0
						1	0	0
						1	1	0
0	0	0	1	0	1	0	1	1
						1	0	1
						1	1	1
0	0	0	1	1	1	0	1	toggle
						1	0	toggle
						1	1	toggle

Figure 66 ATOM CCUx Serve first definition ACB42 = 0b000

ACB4	ACB3	ACB2	ACB1	ACB0	SL	CCU0 match	CCU1 match	Pin level new
0	0	1	0	0	0	0	1	hold
						1	0	toggle
						1	1	hold
0	0	1	0	1	0	0	1	0
						1	0	1
						1	1	0
0	0	1	1	0	0	0	1	1
						1	0	0
						1	1	1
0	0	1	1	1	0	0	1	toggle
						1	0	hold
						1	1	toggle
0	0	1	0	0	1	0	1	hold
						1	0	toggle
						1	1	hold
0	0	1	0	1	1	0	1	1
						1	0	0
						1	1	1
0	0	1	1	0	1	0	1	0
						1	0	1
						1	1	0
0	0	1	1	1	1	0	1	toggle
						1	0	hold
						1	1	toggle

Figure 67 ATOM CCUx Serve first definition ACB42 = 0b001

If the ATOM channel is enabled, the **CM0** and/or **CM1** registers and the **ACB42** bit field of the **ATOM[i]_CH[x]_CTRL** register can be updated by the CPU as long as the first match event occurs in case of a ‘serve last’ compare strategy or as long as the overall match event in case of the other compare strategies.

After a compare match event that causes an update of the shadow registers **SR0**/**SR1** and before reading the **SR0** and/or **SR1** register via ARU, the update of the registers **CM0** and/or **CM1** is possible but has no effect.

To set up a new compare action, first the **SR0** and/or **SR1** register containing captured values have to be read and then new compare values have to be written into the register **CM0** and/or **CM1**.

Which **CMx** register has to be updated depends on the compare strategy defined in the **ACB42** bit field of the channel control register. Since the channel immediately starts with the comparison after the **CMx** register was/were written, the compare strategy has to be updated before the **CMx** registers are written.

For the ‘serve last’ compare strategies, if the register **CM0** and **CM1** are updated, it can happen that one or both compare values are already located in the past. In any way the ATOM channel will first wait until both compare values are written before it starts the time base comparisons to avoid a deadlock.

The CPU can check at any time if at least one of the ATOM channels' capture compare register contains valid data and waits for a compare event to happen. This is signaled by the **DV** bit inside the **ATOM[i]_CH[x]_STAT** register. Note, for ‘serve last’ compare strategies, if **DV** bit is currently not set, writing to **CM0** or **CM1** sets immediately the **DV** bit although the compare is only started if both values are written.

An exception for update of register **CM0**/**CM1** exists in SOMC mode and CCUx control mode 'serve last'. If in this mode the CCU0 compare match event occurred, the update of register **CM0**/**CM1** via CPU is blocked until the CCU1 compare match event.

In the ‘serve last’ mode (ACB42= 0b100 or ACB42=0b101) it is possible to generate very small spikes on the output pin by loading **CM0** and **CM1** with two time stamp values for *TBU_TS0*, *TBU_TS1* or *TBU_TS2* close together. The output pin will then be set or reset dependent on the **SL** bit and the specified **ACB10(5)** and **ACB10(4)** bits in the **ACB10** bit field of the **ATOM[i]_CH[x]_CTRL** register on the first match event and the output will toggle on the second compare event in the CCU1 compare unit.

It is important to note, that the bigger (smaller) time stamp has to be loaded into the **CM1** register, since the CCU0 will enable the CCU1 once it has reached its comparison time stamp. The order of the comparison time stamps depends on the defined greater-equal or less-equal comparison of the CCUx units.

In addition to storing the captured time stamps in the shadow registers, the ATOM channel provides the result of the compare match event in the **ACBO(4)** and **ACBO(3)** bits of the **ATOM[i]_CH[x]_STAT** register. The meaning of the bits is shown in the following table:

Table 53 Compare match event ACBO(4) and ACBO(3) bits of ATOM[i]_CH[x]_STAT

ACBO(4)	ACBO(3)	Indication
0	1	CCU0 compare match occurred
1	0	CCU1 compare match occurred

Please note, that in case of the 'serve last' compare strategy, when the bit **SLA** in the **ATOM[i]_CH[x]_CTRL** register is not set, the **ACBO(4)** bit is always set and the **ACBO(3)** bit is always reset after the compare match event occurred.

The **ACBO** bit field is reset, when the **DV** bit is set.

Depending on the capture compare unit where the time base matched the interrupt *CCU0TCx_IRQ* or *CCU1TCx_IRQ* is raised. Note that in case of 'serve first' compare strategy, if both events CCU0 and CCU1 occur at the same point in time, both interrupts will be raised.

The behavior of an ATOM channel in SOMC mode under CPU control is depicted in **Figure 68**.

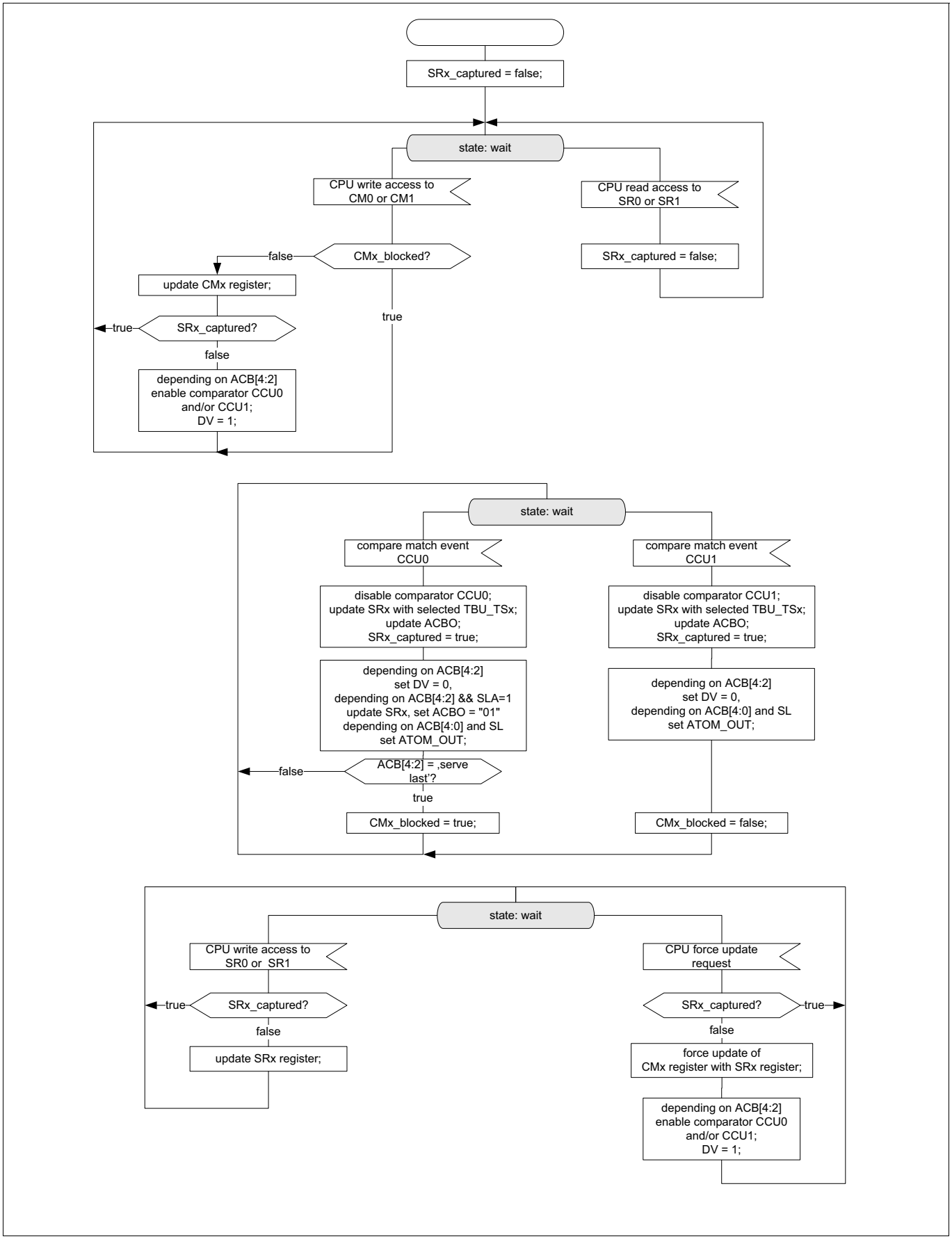


Figure 68 SOMC state diagram for channel under CPU control

28.15.3.2.3 SOMC Mode under ARU control

When the channel should be controlled by ARU, the **ARU_EN** bit inside the **ATOM[i]_CH[x]_CTRL** register has to be set.

In case, the ATOM channel is under ARU control the content for the compare registers **CM0** and **CM1** as well as the update of the compare strategy can be loaded via the 53 bit ARU word.

The ARU word 23 to 0 is loaded into the **CM0** register while the ARU word 47 to 24 is loaded into the **CM1** register. The five ARU control bits 52 to 48 are loaded into the **ACBI** bit field of the **ATOM[i]_CH[x]_STAT** register and control the channel compare strategy as well as the output behavior in case of compare match events.

For the five ARU control bits 52 to 48 the bits 49 and 48 are loaded into the **ACBI** bits 1 and 0. The output behavior also depends on the setting of the **SL** bit inside of the **ATOM[i]_CH[x]_CTRL** register and is shown in the following table:

Table 54 Output behavior depends on SL bit inside of the ATOM[i]_CH[x]_CTRL and ACBI bits 1 and 0

SL	ACBI(1)	ACBI(0)	Output behavior
0	0	0	No signal level change at output (exception in **Figure 66** and **Figure 67** mode ACB42=001)
0	0	1	Set output signal level to 1
0	1	0	Set output signal level to 0
0	1	1	Toggle output signal level (exception in **Figure 66** and **Figure 67** mode ACB42=001)
1	0	0	No signal level change at output (exception in **Figure 66** and **Figure 67** mode ACB42=001)
1	0	1	Set output signal level to 0
1	1	0	Set output signal level to 1
1	1	1	Toggle output signal level (exception in **Figure 66** and **Figure 67** mode ACB42=001)

For the five ARU control bits 52 to 48 the bits 52 to 50 are loaded into the **ACBI** bits 4 to 2. With these three bits the capture/compare units CCUx can be controlled as shown in the following table:

Table 55 Capture/compare units CCUx controlled by ACBI bits 4 to 2

ACBI(4)	ACBI(3)	ACBI(2)	CCUx control
0	0	0	Serve First: Compare in CCU0 using TBU_TS0 and in parallel in CCU1 using TBU_TS1 or TBU_TS2. Disable other CCUx on compare match. Output signal level on the compare match of the matching CCUx unit is defined by combination of SL, ACBI(1) and ACBI(0). Details see **Figure 67**
0	0	1	Serve First: Compare in CCU0 using TBU_TS0 and in parallel in CCU1 using TBU_TS1 or TBU_TS2. Disable other CCUx on compare match. Output signal level on the compare match of the matching CCUx unit is defined by combination of SL, ACBI(1) and ACBI(0). Details see **Figure 66**
0	1	0	Compare in CCU0 only, use time base TBU_TS0. Output signal level is defined by combination of SL, ACBI(1) and ACBI(0) bits.

Table 55 Capture/compare units CCUx controlled by ACBI bits 4 to 2 (cont'd)

ACBI(4)	ACBI(3)	ACBI(2)	CCUx control
0	1	1	Compare in CCU1 only, use time base TBU_TS1 or TBU_TS2. Output signal level is defined by combination of SL, ACBI(1) and ACBI(0) bits.
1	0	0	Serve Last: Compare in CCU0 and then in CCU1 using TBU_TS0. Output signal level when CCU0 matches is defined by combination of SL, ACBI(1) and ACBI(0). On the CCU1 match the output level is toggled.
1	0	1	Serve Last: Compare in CCU0 and then in CCU1 using TBU_TS1 or TBU_TS2. Output signal level when CCU0 matches is defined by combination of SL, ACBI(1) and ACBI(0). On the CCU1 match the output level is toggled.
1	1	0	Serve Last: Compare in CCU0 using TBU_TS0 and then in CCU1 using TBU_TS1 or TBU_TS2. Output signal level when CCU1 matches is defined by combination of SL, ACBI(1) and ACBI(0).
1	1	1	Change ARU read address to ATOM_RDADDR1 DV flag is not set. Neither ACBI(1) nor ACBI(0) is evaluated.

It is important to note that the bit combination 0b111 for the **ACBI(4)**, **ACBI(3)** and **ACBI(2)** bits forces the channel to request new compare values from another destination read address defined in the **ATOM_RDADDR1** bit field of the **ATOM[i]_CH[x]_RDADDR** register. After data was successfully received and the compare event occurred the ATOM channel switches back to **ATOM_RDADDR0** to receive the next data from there.

After the specified compare match event, the captured time stamps are stored in **SR0** and **SR1** and the compare result is stored in the **ACBO** bit field of the **ATOM[i]_CH[x]_STAT** register. The meaning of the **ACBO(4)** and **ACBO(3)** bits of the **ATOM[i]_CH[x]_STAT** is shown in the following table:

Table 56 Compare match event ACBO(4) and ACBO(3) bits of ATOM[i]_CH[x]_STAT

ACBO(4)	ACBO(3)	Return value to ARU
0	1	CCU0 compare match occurred
1	0	CCU1 compare match occurred

Please note, that in case of the 'serve last' compare strategy, when the bit **SLA** in the **ATOM[i]_CH[x]_CTRL** register is not set, the **ACBO(4)** bit is always set and the **ACBO(3)** bit is always reset after the compare match event occurred.

The **ACBO** bit field is reset, when the **DV** bit is set.

Depending on the capture compare unit where the time base matched the interrupt *CCU0TCx_IRQ* or *CCU1TCx_IRQ* is raised.

When CCU0 and CCU1 is used for comparison it is possible to generate very small spikes on the output pin by loading **CM0** and **CM1** with two time stamp values for *TBU_TS0*, *TBU_TS1* or *TBU_TS2* close together. The output pin will then be set or reset dependent on the **SL** bit and the specified **ACBI(0)** and **ACBI(1)** bits in the **ACBI** bit field of the **ATOM[i]_CH[x]_STAT** register on the first match event and the output will toggle on the second match event.

It is important to note, that the bigger (smaller) time stamp has to be loaded into the **CM1** register, since the CCU0 will enable the CCU1 once it has reached its comparison time stamp. The order of the comparison time stamps depends on the defined greater-equal or less-equal comparison of the CCUx units.

For compare strategy 'serve last' the CCU0 and CCU1 compare match may occur sequentially. During different phases of compare match the CPU access rights to register **CM0** and **CM1** as well as to **WR_REQ** bit is different.

For the case of bit **ABM**=0 and EUPM=0 (register **ATOM[i]_CH[x]_CTRL**) these access rights by CPU to register **CM0** and **CM1** and the **WR_REQ** are depicted in the following figure.

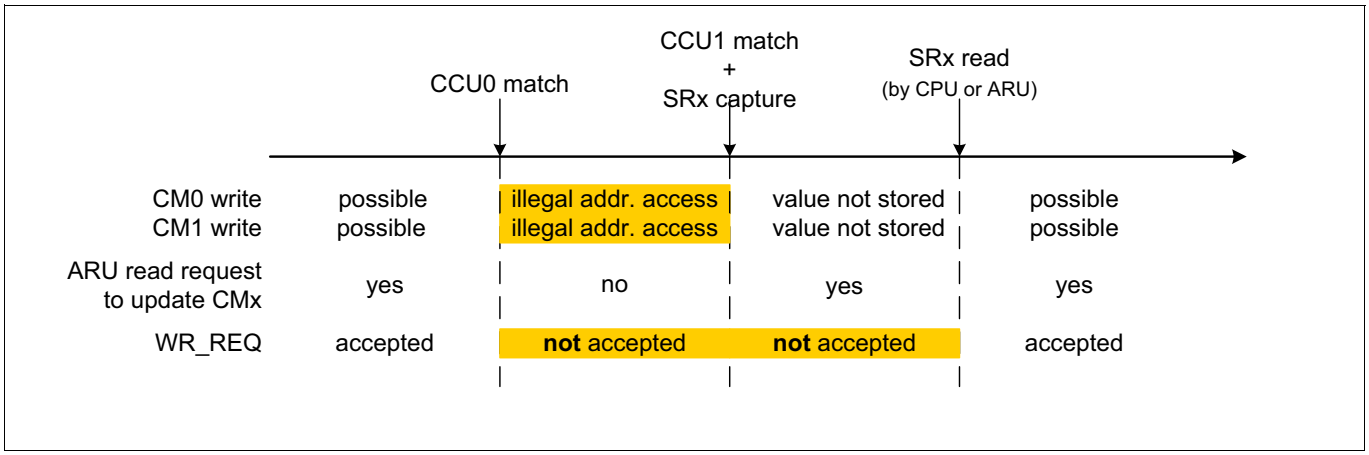


Figure 69 CPU access rights in case of compare strategy 'serve last', ABM=0 and EUPM=0

For the case of bit **ABM**=1 and **EUPM**=0 (register **ATOM[i]_CH[x]_CTRL**) these access rights by CPU to register **CM0** and **CM1** and the **WR_REQ** are depicted in the following figure.

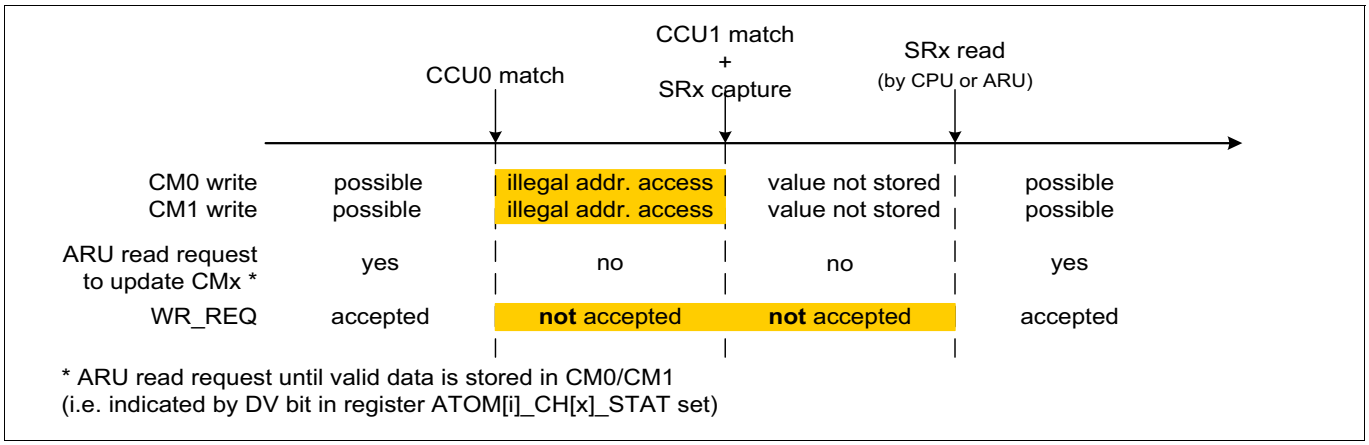


Figure 70 CPU access rights in case of compare strategy 'serve last', ABM=1 and EUPM=0

For the case of bit **EUPM**=1 (register **ATOM[i]_CH[x]_CTRL**), after CCU0 compare match (and before CCU1 compare match) an update of **CM1** as well as a late update via **WR_REQ** is possible. The value is used for compare. After CCU0 compare match an update of **CM0** is not possible, means the value is not stored. The ARU read request is not paused between the compare matches. This behavior is depicted in the following figures.

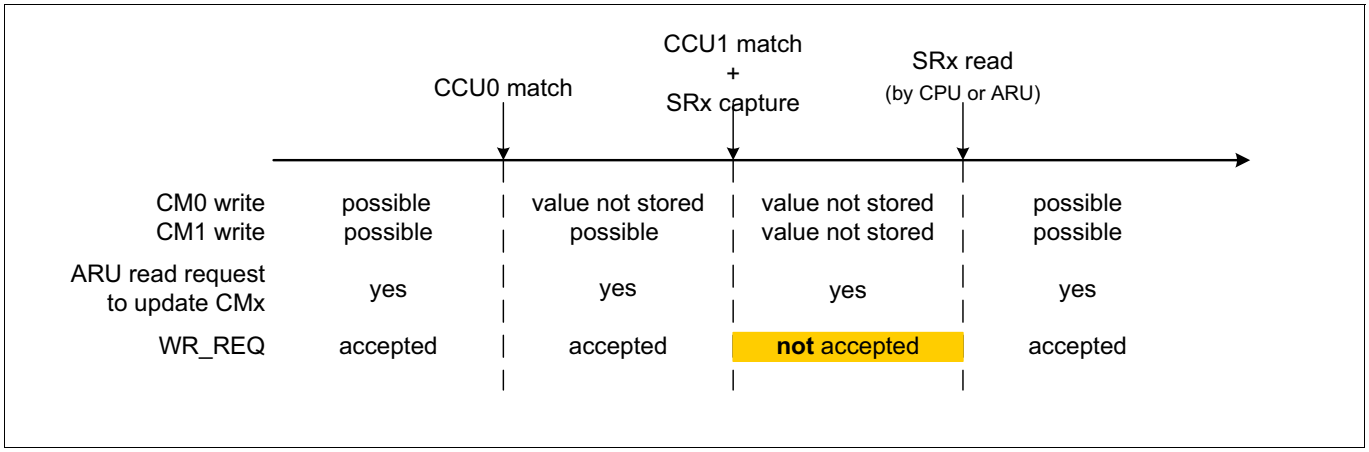


Figure 71 CPU access rights in case of compare strategy 'serve last' ,ABM=0 and EUPM=1

The behavior in case of EUPM=1 and ABM=1 is depicted in the following figure:

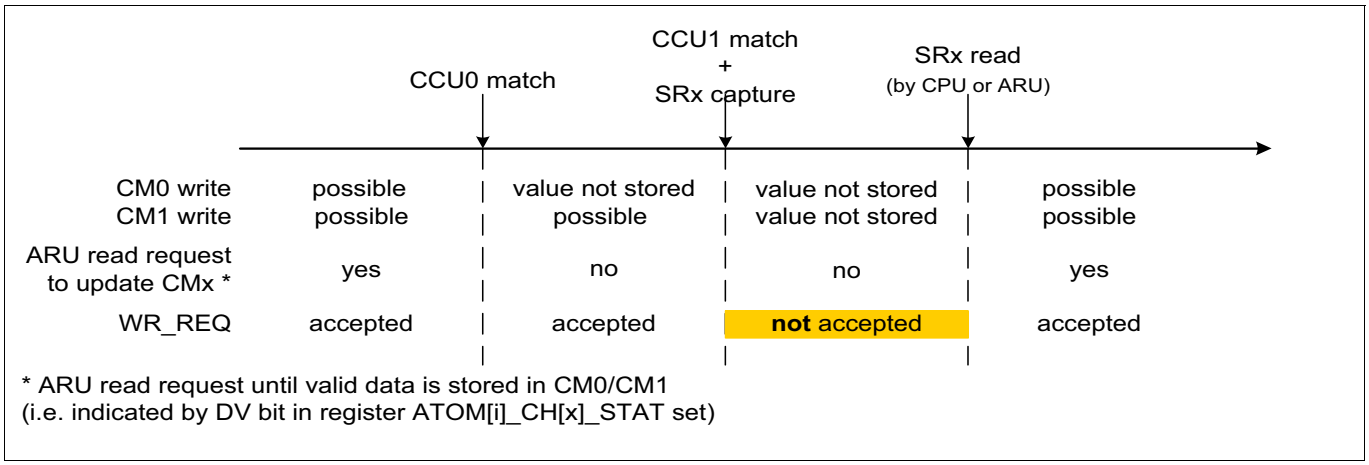


Figure 72 CPU access rights in case of compare strategy 'serve last' ,ABM=1 and EUPM=1

In case of EUPM=1 a write access to CM0 or CM1 never causes an AEI write status 0b10.

ARU Non-Blocking mode

When the compare registers are updated via ARU the update behavior of the channel is configurable with the ABM bit inside the **ATOM[i]_CH[x]_CTRL** register. When the **ABM** bit is reset, the ATOM channel is in ARU non-blocking mode.

In the ARU non-blocking mode, data received via ARU is continuously transferred to the registers **CM0** and **CM1** and the bit field **ACBI** of register **ATOM[i]_CH[x]_STAT** as long as no specified compare match event occurs.

After a compare match event that causes an update of the shadow register **SR0**/**SR1** and before reading the **SR0**/**SR1** register via CPU or ARU, the update of the registers **CM0**/ **CM1** via CPU or ARU is possible but the data is not accepted to be valid (no DV bit set in register ATOM[i]_CH[x]_CTRL).

To set up a new compare action, first the **SR0**/**SR1** register containing captured values have to be read and then new compare values have to be written into the register **CM0**/**CM1**. This can be done either by ARU or by CPU.

When the CPU does the register accesses, only one of the shadow registers has to be read. Dependent on the compare strategy, the CPU has to write one or both of the compare registers.

An exception for update of register **CM0**/**CM1** exists in SOMC mode and CCUx control mode 'serve last' if EUPM=0. If in this mode the CCU0 compare match event occurred, the update of register **CM0**/**CM1** via CPU is not possible until the CCU1 compare match event occurs.

Note that a write access to either CM0 or CM1 in this case leads to a write status 0b10.

The CPU can check at any time if the ATOM channel has received valid data from the ARU and waits for a compare event to happen. This is signaled by the **DV** bit inside the **ATOM[i]_CH[x]_STAT** register.

The behavior of an ATOM channel in SOMC mode, when ARU is enabled and ARU blocking mode is disabled is shown in **Figure 73**.

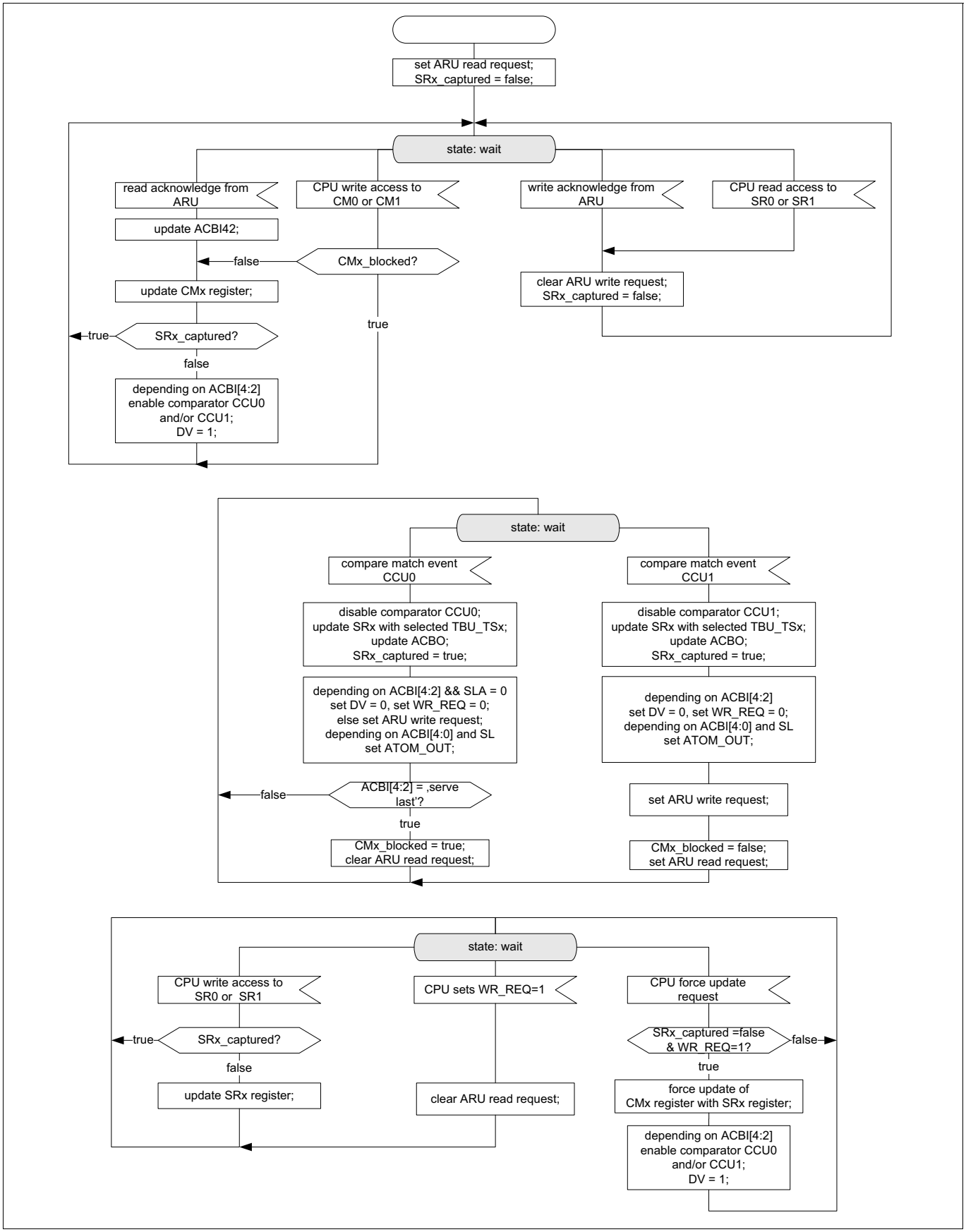


Figure 73 SOMC State diagram for SOMC mode, ARU enabled, ABM disabled

ARU Blocking mode

When the compare registers are updated by ARU, the ATOM channel can be configured to receive ARU data in a blocking manner. This can be configured by setting the **ABM** bit in the **ATOM[i]_CH[x]_CTRL** register.

If the **ABM** and **ARU_EN** bits are set, depending on compare strategy,**CM0** and/or **CM1** can be updated via ARU with new compare values. If the compare registers **CM0** and/or **CM1** are accepting these new data to be valid (indicated by bit DV in register ATOM[i]_CH[x]_STAT), the ATOM channel stops requesting new data via ARU and waits for the compare match event to happen.

When the specified compare match event happens, the shadow registers **SR0** and **SR1** are updated together with the **ACBO** bits in the **ATOM[i]_CH[x]_STAT** register. The data in the shadow registers is marked as valid for the ARU and the **DV** bit or register **ATOM[i]_CH[x]_CTRL** is reset.

If the register **SR0** and **SR1** holding the captured TBU time stamp values are read by either the ARU or the CPU, the next write access to or update of the register **CM0** or **CM1** via ARU or the CPU enables the new compare match check again.

At least one of the registers **SR0** or **SR1** has to be read either via ARU or by CPU, before new data is requested via ARU.

Note that in case of ABM=1 the application has to handle the situation that the ATOM does not request update of new data for CM0/CM1 until the captured values are read. E.g. if an MCS task starts to write via ARU new data (with AWR(I) command) after capture the data in SR0/SR1, the task sticks in the command until captured data is read by another task via ARU or via the CPU interface.

The CPU can check at any time if the ATOM channel has received valid data from the ARU and waits for a compare event to happen. This is signaled by a set **DV** bit inside the **ATOM[i]_CH[x]_STAT** register.

The behavior of an ATOM channel in SOMC mode, when ARU is enabled and ARU blocking mode is enabled is shown in **Figure 74**.

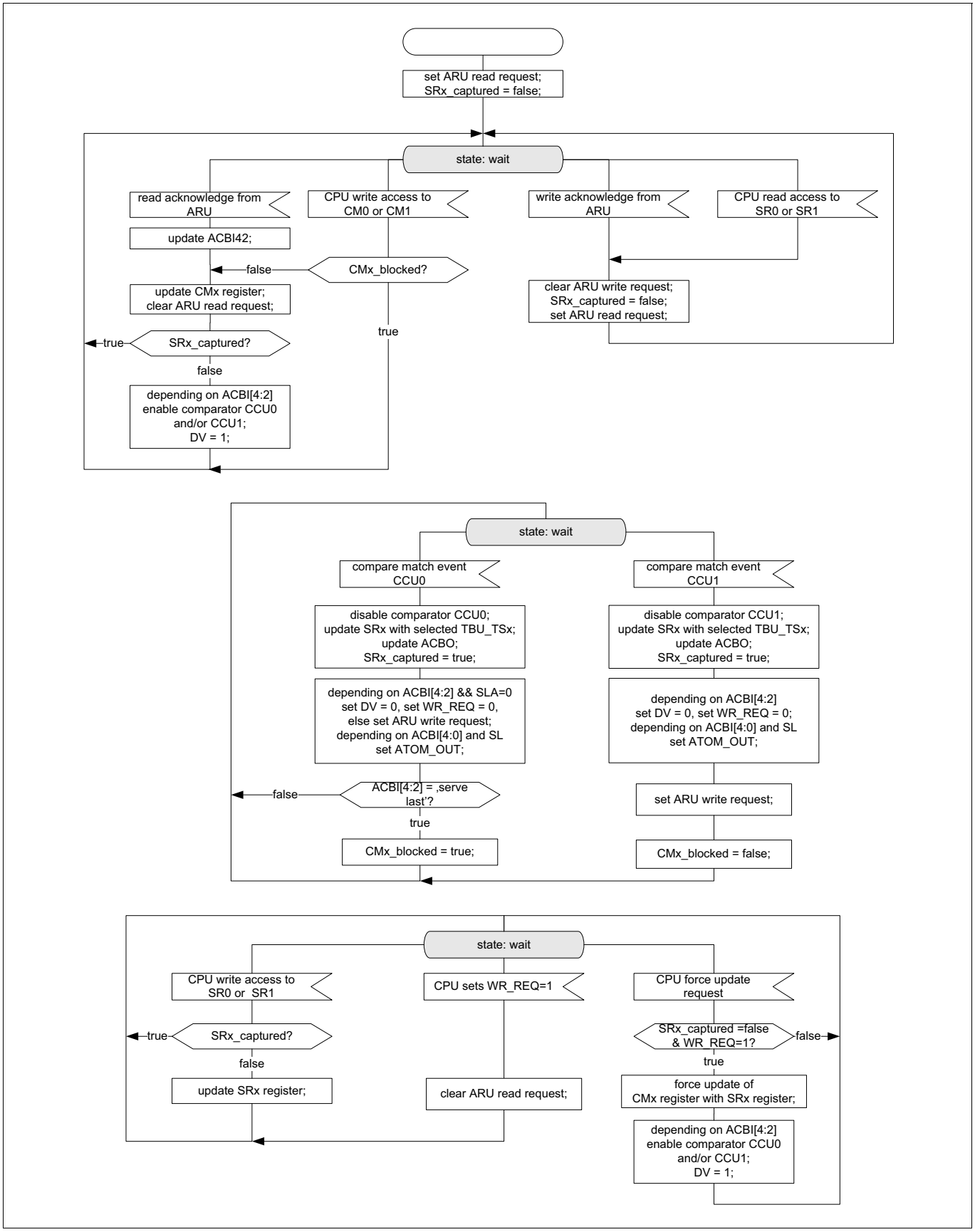


Figure 74 SOMC State diagram for SOMC mode, ARU enabled and ABM enabled

ATOM SOMC Late update mechanism

Although, the ATOM channel may be controlled by data received via the ARU, the CPU is able to request at any time a late update of the compare register. This can be initiated by setting the **WR_REQ** bit inside the **ATOM[i]_CH[x]_CTRL** register. By doing this, the ATOM will request no further data from ARU (if ARU access was enabled). The channel will in any case continue to compare against the values stored inside the compare registers (if bit **DV** was set). The CPU can now update the new compare values until the compare event happens by writing to the shadow registers, and force the ATOM channel to update the compare registers by writing to the force update register bits in the **AGC** register.

If the **WR_REQ** bit is set and a compare match event happens, any further access to the shadow registers **SR0**, **SR1** is blocked and the force update of this channel is blocked. In addition, the **WRF** bit is set in the **ATOM[i]_CH[x]_STAT** register. Thus, the CPU can determine that the late update failed by reading the **WRF** bit.

In case of bit **EUPM**=0 (register **ATOM[i]_CH[x]_CTRL**) the following statements are true:

If a compare match event already happened, the **WR_REQ** bit could not be set until the channel is unlocked for a new compare match event by reading the shadow registers. In addition, the **WRF** bit is set if the CPU tries to write the **WR_REQ** bit in that case.

In case of bit **EUPM**=1 (register **ATOM[i]_CH[x]_CTRL**) the following statements are true:

If in case of serve last strategy a CCU1 or in any other compare strategy a CCU0 or CCU1 compare match event already happened, the **WR_REQ** bit could not be set until the channel is unlocked for a new compare match event by reading the shadow registers. In addition, the **WRF** bit is set if the CPU tries to write the **WR_REQ** bit in that case.

In general, for a late update the following has to be taken into account:

If between a correct **WR_REQ** bit set, a correct shadow register write, and before the force update is requested by the AGC a match event occurs on the old compare values, the **WRF** bit will be set. The force update will be blocked.

The **WRF** bit will be set in any case if the CPU tries to write to a blocked shadow register.

The **WR_REQ** bit and the **DV** bit will be reset on a compare match event.

After a capture event for register **SR0** and/or **SR1** the force update mechanism will be blocked until a read access to the register **SR0** or **SR1** by either the ARU or the CPU happens.Writing to **SR0** or **SR1** after compare match causes an AEI write status 0b10.

The ATOM SOMC late update mechanism from CPU is shown in **Figure 75**.

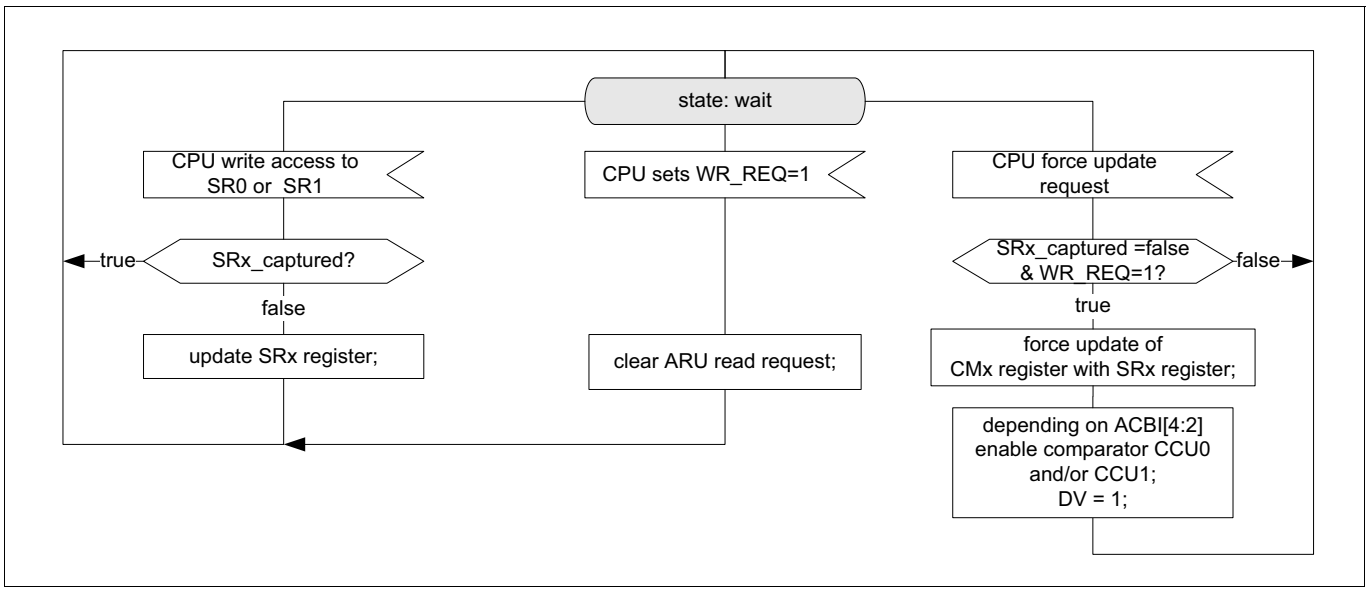


Figure 75 SOMC State diagram for late update requests by CPU

28.15.3.2.4 Register ATOM[i]_CH[x]_CTRL in SOMC mode

Register ATOM[i]_CH[x]_CTRL in SOMC mode

GTM_ATOMi_CHx_SOMC (i=0-11; x=0-7)
ATOMi Channel x Control Register in SOMC Mode ($E8004_H$ + i*800_H+ x*80_H) **Reset Value: 00000800_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FREEZE	Not_used	Not_used	Reserved	ABM	Not_used	SLA	TRIGOUT	EXTTRIGOUT	Not_used		Not_used	Not_used		Not_used	WR_REQ
rw	rw	rw	r	rw	rw	rw	rw	rw	r		rw	rw		rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not_used	Not_used			SL	EUPM	CMP_CTRL	ACB42			ACB10		ARU_EN	TB12_SEL	MODE	
rw	rw			rw	rw	rw	rw			rw		rw	rw	rw	

Field	Bits	Type	Description
MODE	1:0	rw	**ATOM channel mode select** 01_B ATOM Signal Output Mode Compare (SOMC)
TB12_SEL	2	rw	**Select time base value TBU_TS1 or TBU_TS2** 0_B T*BU_TS1* selected for comparison 1_B T*BU_TS2* selected for comparison Note: This bit is only applicable if three time bases are present in the GTM. Otherwise, this bit is reserved.
ARU_EN	3	rw	**ARU Input stream enable** 0_B ARU Input stream disabled 1_B ARU Input stream enabled
ACB10	5:4	rw	**Signal level control bits** 00_B No signal level change at output (exception in **Figure 66** and **Figure 67** mode ACB42=001). 01_B Set output signal level to 1 when SL bit = 0 else output signal level to 0. 10_B Set output signal level to 0 when SL bit = 0 else output signal level to 1. 11_B Toggle output signal level (exception in **Figure 66** and **Figure 67** mode ACB42=001). These bits are only applicable if ARU_EN = '0'.

Field	Bits	Type	Description
ACB42	8:6	rw	**ATOM control bits ACB(4), ACB(3), ACB(2)** 000_B Compare in CCU0 and CCU1 in parallel, disable the CCUx on a compare match on either of compare units. Use *TBU_TS0* in CCU0 and *TBU_TS1* or *TBU_TS2* in CCU1. 001_B Compare in CCU0 and CCU1 in parallel, disable the CCUx on a compare match on either compare units. Use *TBU_TS0* in CCU0 and *TBU_TS1* or *TBU_TS2* in CCU1. 010_B Compare in CCU0 only against *TBU_TS0*. 011_B Compare in CCU1 only against *TBU_TS1* or *TBU_TS2*. 100_B Compare first in CCU0 and then in CCU1. Use *TBU_TS0*. 101_B Compare first in CCU0 and then in CCU1. Use *TBU_TS1* or *TBU_TS2*. 110_B Compare first in CCU0 and then in CCU1. Use *TBU_TS0* in CCU0 and *TBU_TS1* or *TBU_TS2* in CCU1. 111_B Cancel pending compare events. Note: These bits are defining the compare strategy only if ARU_EN = 0. Independent of ARU_EN, a writing of 0b111 cancels any pending CCU0 or CCU1 compare.
CMP_CTRL	9	rw	**CCUx compare strategy select** 0_B Greater-equal compare against TBU time base values (TBU_TS1/2 >;= CM0/1) 1_B Less-equal compare against TBU time base values (TBU_TS1/2 <= CM0/1) The compare unit CCU0 or CCU1 that compares against TBU_TS0 (depending on CCUx control mode defined by ACBI(4:2) or ACB42) always performs a greater-equal comparison, independent on CMP_CTRL bit.
EUPM	10	rw	**Extended Update Mode** 0_B No extended update of CM0 and CM1 via CPU or ARU; 1_B Extended update mode: in case of compare strategy ‘serve last’: update of CM1 after CCU0 compare match possible, via ARU or CPU. Note: If EUPM=1, write access to CM0 never causes an AEI write status 0b10. This bit is only applicable in SOMC and SOMB mode.
SL	11	rw	**Initial signal level after channel enable** 0_B Low signal level 1_B High signal level Note: Reset value depends on the hardware configuration chosen by silicon vendor. Note: If the output is disabled, the output ATOM_OUT[x] is set to inverse value of SL. If FREEZE=0, following note is valid: If the channel is disabled, the output register of SOU unit is set to value of SL. If FREEZE=1, following note is valid: If the channel is disabled, the output register of SOU unit is not changed and output ATOM_OUT[x] is not changed.
Not_used	14:12	rw	**Not used** Note: Not used in this mode.

Field	Bits	Type	Description
Not_used	15	rw	**Not used** Note: Not used in this mode.
WR_REQ	16	rw	**CPU write request bit** 0_B No late update requested by CPU 1_B Late update requested by CPU Note: The CPU can disable subsequent ARU read requests by the channel and can update the shadow registers with new compare values, while the compare units operate on old compare values received by former ARU accesses, if occurred. Note: On a compare match event, the WR_REQ bit will be reset by hardware. Note: At the point of the force update only the shadow registers SR0 and SR1 are transferred into the CM0, CM1 registers. The output action is still defined by the ACBI bit field described by the ARU together with the old compare values for CM0/CM1.
Not_used	17	rw	**Not used** Note: Not used in this mode.
Not_used	19:18	rw	**Not used** Note: Not used in this mode.
Not_used	20	rw	**Not used** Note: Not used in this mode.
Not_used	22:21	r	**Not used** Note: Not used in this mode.
EXTTRIGOUT	23	rw	**Select TIM_EXT_CAPTURE(x) as potential output signal TRIG_[x]** 0_B signal *TRIG_[x-1]* is selected as output on *TRIG_[x]* (if TRIGOUT=0) 1_B signal *TIM_EXT_CAPTURE(x)* is selected as output on *TRIG_[x]* (if TRIGOUT=0)
TRIGOUT	24	rw	**TRIGOUT: Trigger output selection (output signal TRIG_CHx) of module ATOM_CHx** 0_B *TRIG_[x]* is *TRIG_[x-1]* or *TIM_EXT_CAPTURE(x)* 1_B *TRIG_[x]* is *TRIG_CCU0*

Field	Bits	Type	Description
SLA	25	rw	**'Serve last' ARU communication strategy** 0_B Capture SRx time stamps after CCU0 match event not provided to ARU 1_B Capture SRx time stamps after CCU0 match event provided to ARU Note: Please note, that setting of this bit has only effect, when ACBI(4:2) is configured for serve last compare strategy ("100", "101", or "110"). Note: When this bit is not set, the captured time stamps in the shadow registers SRx are only provided after the CCU1 match occurred. The ACBO(4:3) bits always return "10" in that case. Note: By setting this bit, the ATOM channel also provides the captured time stamps after the CCU0 match event to the ARU. The ACBO(4:3) bits are set to "01" in that case. After the CCU1 match event, the time stamps are captured again in the SRx registers and provided to the ARU. The ACBO(4:3) bits are set to "10". When the data in the shadow registers after the CCU0 match was not consumed by an ARU destination and the CCU1 match occurs, the data in the shadow registers is overwritten by the new captured time stamps. The ATOM channel does not request new data from the ARU when the CCU0 match values are read from an ARU destination.
Not_used	26	rw	**Not used** Note: Not used in this mode.
ABM	27	rw	**ARU blocking mode** 0_B ARU blocking mode disabled: ATOM reads continuously from ARU and updates CM0, CM1 and ACB bits independent of pending compare match event. 1_B ARU blocking mode enabled: after update of CM0, CM1 and ACB bit via ARU, no new data is read via ARU until compare match event occurred and SR0 and/or SR1 are read.
Reserved	28	r	**Reserved** Read as zero, should be written as zero.
Not_used	29	rw	**Not used** Note: Not used in this mode.
Not_used	30	rw	**Not used** Note: Not used in this mode.
FREEZE	31	rw	**FREEZE** 0_B a channel disable/enable may change internal register and output register 1_B a channel enable/disable does not change an internal or output register but stops counter CN0 (in SOMP mode), comparison (in SOMC/SOMB mode) and shifting (in SOMS mode)

28.15.3.3 ATOM Signal Output Mode PWM (SOMP)

In ATOM Signal Output Mode PWM (SOMP) the ATOM sub-module channel is able to generate complex PWM signals with different duty cycles and periods. Duty cycles and periods can be changed synchronously and asynchronously. Synchronous change of the duty cycle and/or period means that the duty cycle or period

duration changes after the end of the preceding period. An asynchronous change of period and/or duty cycle means that the duration changes during the actual running PWM period.

The signal level of the pulse generated inside the period can be configured inside the channel control register (**SL** bit of **ATOM[i]_CH[x]_CTRL** register). The initial signal output level for the channel is the inverse pulse level defined by the **SL** bit. **Figure 76** depicts this behavior.

The counter **CN0** of each channel can run in two different modes depending on configuration of **UDMODE** in register **ATOM[i]_CH[x]_CTRL.**By default the counter counts only up until it reaches **CM0** and is then reset to 0.In the up down counter mode **CN0** switches between counting up and counting down.

28.15.3.3.1 Continuous Counting Up Mode

In SOMP mode with **UDMODE**=0b00 (i.e. **CN0** counts only up), depending on configuration bits RST_CCU0 of register **ATOM[i]_CH[x]_CTRL** the counter register **CN0** can be reset either when the counter value is equal to the compare value **CM0** (i.e. CN0 counts only from 0 to CM0-1 and is then reset to 0) or when signaled by the ATOM[i] trigger signal *TRIG_[x-1]* of the preceding channel [x-1] (which can also be the last channel of preceding instance TOM[i-1]) or the trigger signal *TIM_EXT_CAPTURE*(x) of the assigned TIM channel [x].

In this case, if **UPEN_CTRL[x]**=1, also the working register **CM0,CM1** and **CLK_SRC** are updated.

Note: As an exception, the input TRIG_[0] of instance ATOM0 is triggered by its own last channel cCATO via signal TRIG_[cCATO].

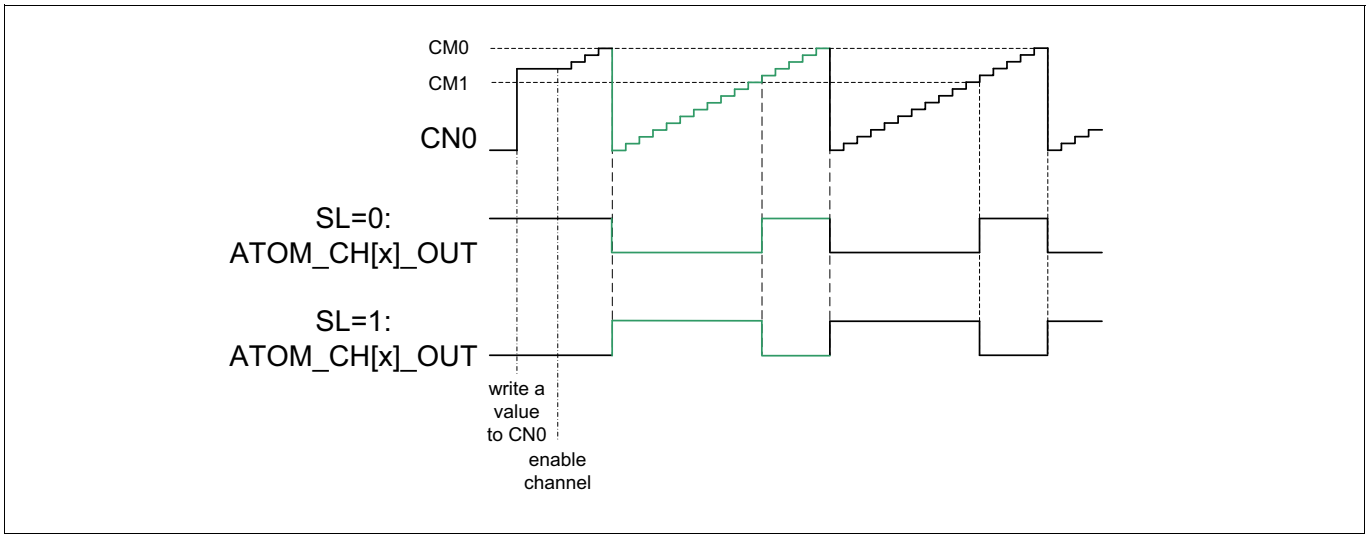


Figure 76 PWM Output behavior with respect to the SL bit in the ATOM[i]_CH[x]_CTRL register if UDMODE = 0b00

On an asynchronous update, it is guaranteed, that no spike occurs at the output port of the channel due to a too late update of the operation registers. The behavior of the output signal due to the different possibilities of an asynchronous update during a PWM period is shown in **Figure 77**.

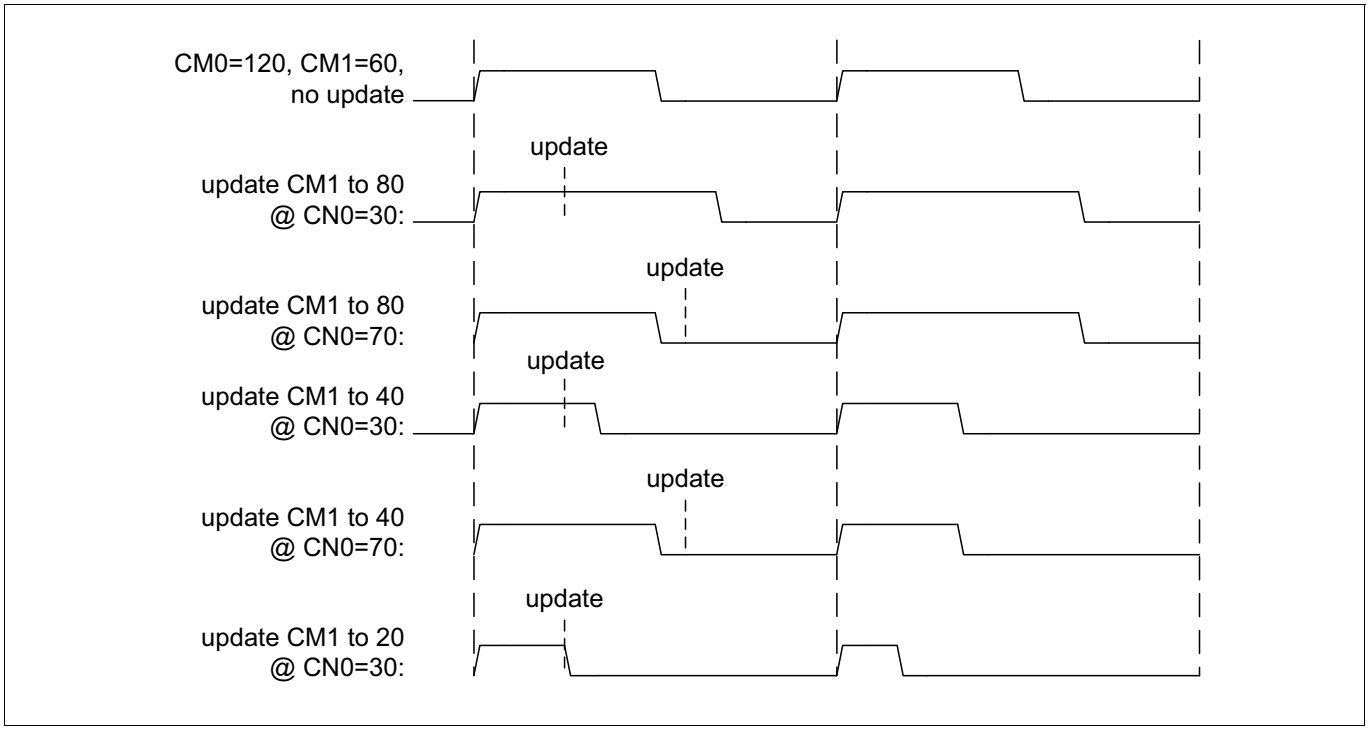


Figure 77 PWM Output behavior in case of an asynchronous update of the duty cycle

The duration of the pulse high or low time and period is measured with the counter in sub-unit CCU0. The trigger of the counter is one of the eight CMU clock signals configurable in the channel control register **ATOM[i]_CH[x]_CTRL**. The register **CM0** holds the duration of the period and the register **CM1** holds the duration of the duty cycle in clock ticks of the selected CMU clock.

If counter register **CN0** of channel x is reset by its own CCU0 unit (i.e. the compare match of **CN0** >=**CM0-1** configured by **RST_CCU0**=0), following statements are valid:

- **CN0** counts from 0 to **CM0**-1 and is then reset to 0
- When CN0 is reset from CM0 to 0, an edge to SL is generated.
- When CN0 is incrementing and reaches CN0 > CM1, an edge to !SL is generated.
- if **CM0**=0 or **CM0**=1, the counter **CN0** is constant 0.
- if **CM1**=0, the output is !SL = 0% duty cycle
- if **CM1** >= **CM0** and **CM0**>1, the output is **SL** = 100% duty cycle

If the counter register **CN0** of channel x is reset by the trigger signal coming from another channel or the assigned TIM module (configured by **RST_CCU0**=1), following statements are valid:

- **CN0** counts from 0 to MAX-1 and is then reset to 0 by trigger signal
- **CM0** defines the edge to **SL** value, **CM1** defines the edge to !**SL** value.
- if **CM0**=**CM1**, the output switches to **SL** if **CN0**=**CM0**=**CM1** (**CM0** has higher priority)
- if **CM0**=0 and **CM1**=MAX, the output is **SL** = 100% duty cycle
- if **CM0** > MAX, the output is !**SL** = 0% duty cycle, independent of **CM1**.

In case the counter value **CN0** reaches the compare value in register **CM0** (in fact CM0-1) or the channel receives an external update trigger via the *FUPD(x)* signal, a synchronous update is performed. A synchronous update means that the registers **CM0** and **CM1** are updated with the content of the shadow registers **SR0** and **SR1** and the **CLK_SRC** register is updated with the value of the **CLK_SRC_SR** register.

The clock source for the counter can be changed synchronously at the end of a period. If ARU access is disabled, this is done by using the bit field **CLK_SRC_SR** of register **ATOM[i]_CH[x]_CTRL** as shadow registers for the next CMU clock source.

28.15.3.3.2 Continuous Counting Up-Down Mode

In SOMP mode, if **CN0** counts up and down (**UDMODE** != 0b00), depending on configuration bit **RST_CCU0** of register **ATOM[i]_CH[x]_CTRL** the counter register **CN0** changes the direction either when the counter value is equal to the compare value **CM0** (in fact CM0-1), has counted down to 0 or when triggered by the ATOM[i] trigger signal *TRIG_[x-1]* of the preceding channel [x-1] (which can also be the last channel of preceding instance ATOM[i-1]) or the trigger signal *TIM_EXT_CAPTURE(x)* of the assigned TIM channel [x].

In this case, if **UPEN_CTRL[x]**=1, also the working register **CM0**, **CM1** and **CLK_SRC** are updated depending on **UDMODE**.

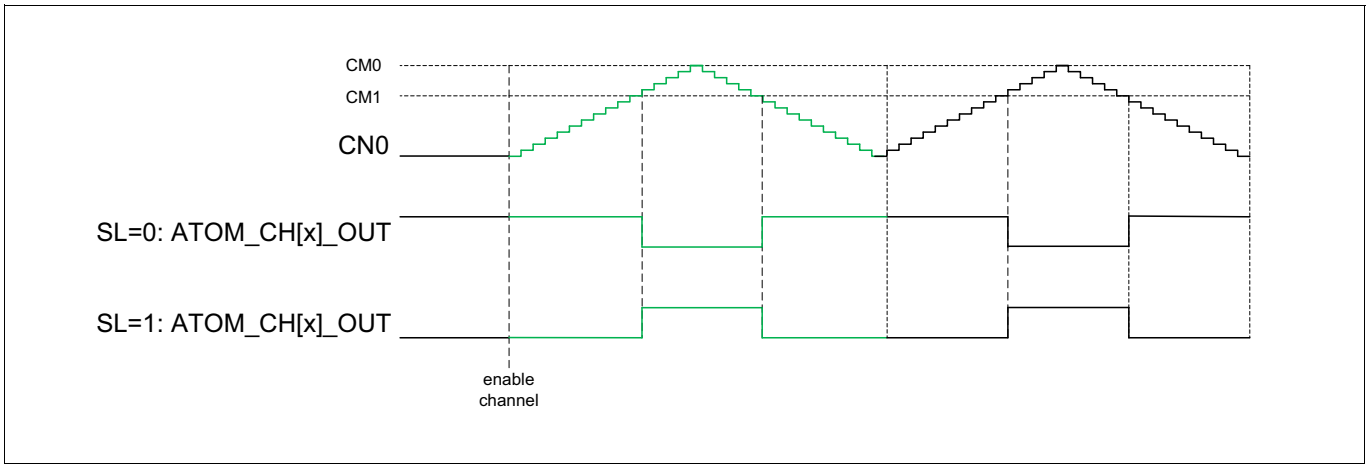


Figure 78 PWM Output behavior with respect to the SL bit in the ATOM[i]_CH[x]_CTRL register if UDMODE != 0b00

The clock of the counter register **CN0** can be one of the CMU clocks CMU_CLKx. If **ARU_EN**=0, the clock for **CN0** is defined by **CLK_SRC_SR** value in register **ATOM[i]_CH[x]_CTRL**.

If **ARU_EN**=1, the clock for **CN0** is defined by **CLK_SRC** value received via ARU.The duration of a period in multiples of selected **CN0** counter clock ticks is defined by the **CM0** configuration value (i.e. **CM0** defines half of period in up-down mode).

CM1 defines the duty cycle value in clock ticks of selected **CN0** counter clock (i.e. **CM0** defines half of duty cycle in up-down mode).

If counter register **CN0** of channel x is reset by its own CCU0 unit (i.e. the compare match of **CN0**>=**CM0-1** configured by **RST_CCU0**=0), following statements are valid:

- **CN0** counts continuously first up from 0 to **CM0**-1 and then down to 0
- if **CN0** >= **CM1**, the output is set to **SL**
- if **CM1**=0, the output is **SL** (i.e. 100% duty cycle)
- if **CM1** >= **CM0**, the output is !**SL** (i.e. 0% duty cycle)
- On output *ATOM[i]_CHx]_OUT* a PWM signal is generated. The period is defined by **CM0**, the duty cycle is defined by **CM1**.

This behavior is depicted in **Figure 78**.

If the counter register **CN0** of channel x is reset by the trigger signal coming from another channel or the assigned TIM module (configured by **RST_CCU0**=1), following statements are valid:

- **CN0** counts continuously first up. On a trigger signal the counter switches to count down mode. If **CN0** has reached 0, it counts up again.
- if **CN0** >= **CM1**, the output is set to **SL**
- if **CM1**=0, the output is **SL** (i.e. 100% duty cycle)
- if **CM1** >= **CM0**, the output is !**SL** (i.e. 0% duty cycle)
- On output *ATOM[i]_CHx]_OUT* a PWM signal is generated. The period is defined by the CCU0 trigger of triggering channel, the duty cycle is defined by **CM1**.
- On output *ATOM[i]_CHx]_OUT_T* a PWM signal is generated. The period is defined by the CCU0 trigger of triggering channel, the duty cycle is defined by **CM0**.

This behavior is depicted in **Figure 79**.

Note that in case of up-down counter mode and RST_CCU0=1 it is recommended that:

- The triggering channel and the triggered channel are both running in up-down mode.
- The time between two triggers signals is equal to the time needed for CN0 of triggered channel to count back to 0 and again up to the same upper value.

The second recommendation can be reached by synchronizing the start of triggering channel and of the triggered channel, i.e. let both channel start with a CN0 value 0.

Note that if there is a synchronization register in the trigger chain (indicated by value ATOM_TRIG_CHAIN in register CCM[i]_HW_CONF), the additional delay of the trigger by one clock period has to be taken into account by starting at triggering channel with a CN0 value 1 (+1 compared to CN0 of triggered channel).

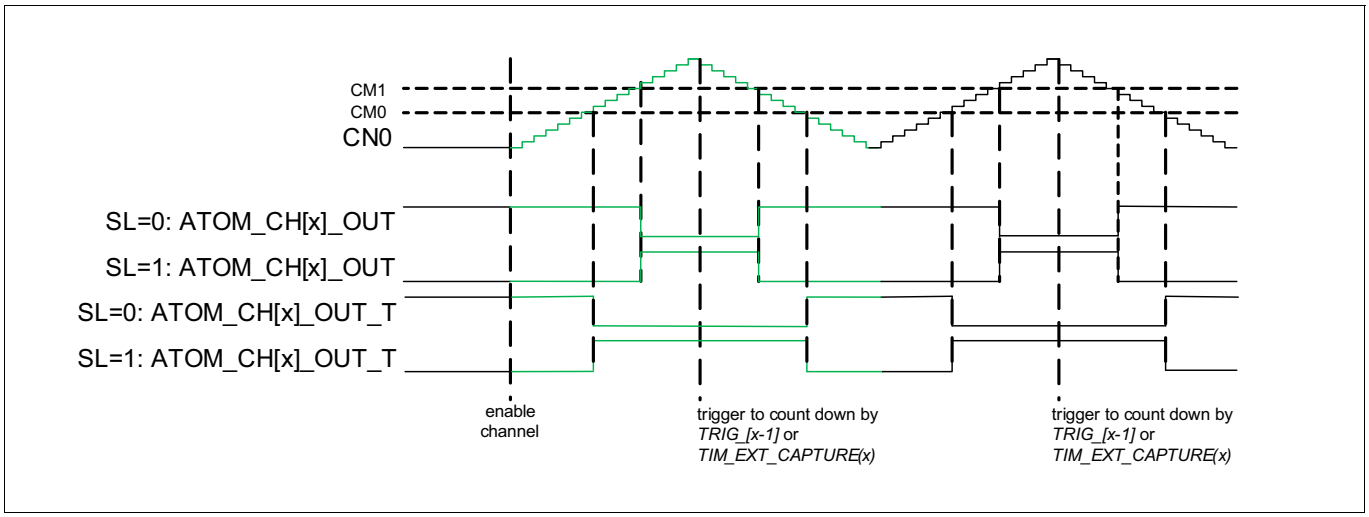


Figure 79 PWM Output behavior in case of RST_CCU0=1

28.15.3.3.3 ARU controlled update

If ARU access is enabled, the bits **ACBI(4)**, **ACBI(3)** and **ACBI(2)** received via ARU and stored in register **ATOM_[i]_CH[x]_STAT** are used as shadow register for the update of the CMU clock source register **CLK_SRC**.

For the synchronous update mechanism the generation of a complex PWM output waveform is possible without CPU interaction by reloading the shadow registers **SR0**, **SR1** and the **ACBI** bit field over the ACI sub-unit from the ARU, while the ATOM channel operates on the **CM0** and **CM1** registers.

This internal update mechanism is established, when the old PWM period ends. The shadow registers are loaded into the operation registers, the counter register is reset, the new clock source according to the **CLK_SRC_SR** and **ACBI(4)**, **ACBI(3)** and **ACBI(2)** bits is selected and the new PWM generation starts.

In parallel, the ATOM channel issues a read request to the ARU to reload the shadow registers with new values while the ATOM channel operates on the operation registers. To guarantee the reloading, the PWM period must not be smaller than the worst case ARU round trip time and source for the PWM characteristic must provide the new data within this time. Otherwise, the old PWM values are used from the shadow registers.

When updated over the ARU the user has to ensure that the new period duration is located in the lower (bits 23 to 0) and the duty cycle duration is located in the upper (bits 47 to 24) ARU data word and the new clock source is specified in the ARU control bits 52 to 50.

This pipelined data stream character is shown in **Figure 80**.

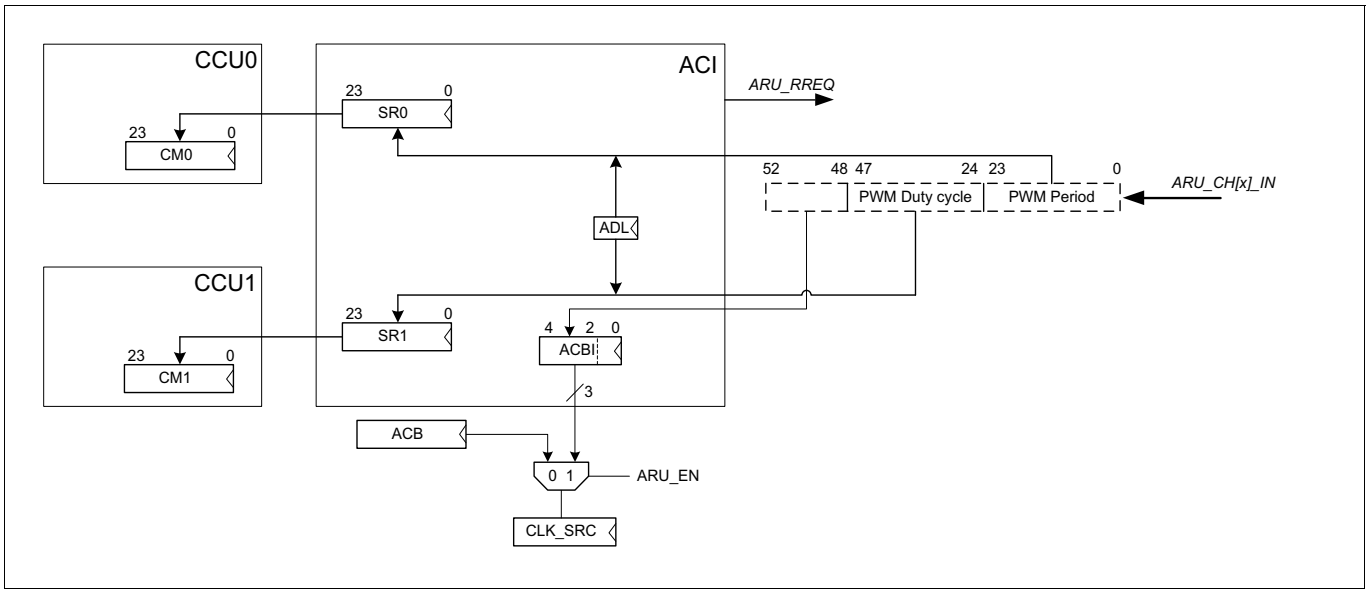


Figure 80 ARU Data input stream pipeline structure for SOMP mode

When an ARU transfer is in progress which means the *ARU_RREQ* is served by the ARU, the ACI locks the update mechanism of **CM0**, **CM1** and **CLK_SRC** until the read request has finished. The CCU0 and CCU1 operate on the old values when the update mechanism is locked.

28.15.3.3.4 CPU controlled update

The shadow registers **SR0** and **SR1** can also be updated over the AEI bus interface. In this case, **ARU_EN** hat to be set to 0.

When updated via the AEI bus the **CM0** and **CM1** update mechanism has to be locked via the **AGC_GLB_CTRL** register with the *UPENx* signal in the AGC sub-unit. To select the new clock source in this case, the CPU has to write to the CLK_SRC_SR bit field of the **ATOM[i]_CH[x]_CTRL** register.

For an asynchronous update of the duty cycle and/or period the new values must be written directly into the compare registers **CM0** and/or **CM1** while the counter **CN0** continues counting. This update can be done only via the AEI bus interface immediately by the CPU or by the *FUPD(x)* trigger signal triggered from the AGC global trigger logic. Values received through the ARU interface are never loaded asynchronously into the operation registers **CM0** and **CM1**. Therefore, the ATOM channel can generate a PWM signal on the output port pin *ATOM[i]_CH[x]_OUT* on behalf of the content of the **CM0** and **CM1** registers, while it receives new PWM values via the ARU interface ACI in its shadow registers.

On a compare match of **CN0** and **CM0** or **CM1** the output signal level of *ATOM[i]_CH[x]_OUT* is toggled according to the signal level output bit **SL** in the **ATOM[i]_CH[x]_CTRL** register.

Thus, the duty cycle output level can be changed during runtime by writing the new duty cycle level into the **SL** bit of the channel configuration register. The new signal level becomes active for the next trigger *CCU_TRIGx* (since bit **SL** is written).

Since the *ATOM[i]_CH[x]_OUT* signal level is defined as the reverse duty cycle output level when the ATOM channel is enabled, a PWM period can be shifted earlier by writing an initial offset value to **CN0** register. By doing this, the ATOM channel first counts until **CN0** reaches **CM0** and then it toggles the output signal at *ATOM[i]_CH[x]_OUT*.

28.15.3.3.5 One-shot Counting Up Mode

The ATOM channel can operate in One-shot mode when the **OSM** bit is set in the channel control register. One-shot mode means that a single pulse with the pulse level defined in bit **SL** is generated on the output line.

First the channel has to be enabled by setting the corresponding **ENDIS_STAT** value.

In one-shot mode the counter **CN0** will not be incremented once the channel is enabled.

A write access to the register **CN0** triggers the start of pulse generation (i.e. the increment of the counter register **CN0**).

If the counter **CN0** is reset from **CM0-1** back to zero, the first edge at *ATOM[i]_CH[x]_OUT* is generated.

To avoid an update of **CMx** register with content of **SRx** register at this point in time, the automatic update should be disabled by setting **UPEN_CTRL[x]** = 0b00 (in register **ATOM[i]_CH[x]_CTRL**)

The second edge is generated if **CN0** is greater or equal than **CM1** (i.e. **CN0** was incremented until it has reached **CM1** or **CN0** is greater than **CM1** after an update of **CM1**).

If the counter **CN0** has reached the value of **CM0-1** a second time, the counter stops.

The new value of **CN0** determines the start delay of the first edge. The delay time of the first edge is given by (**CM0-CN0**) multiplied with period defined by current value of **CLK_SRC**.

Figure 81 depicts the pulse generation in SOMP one-shot mode.

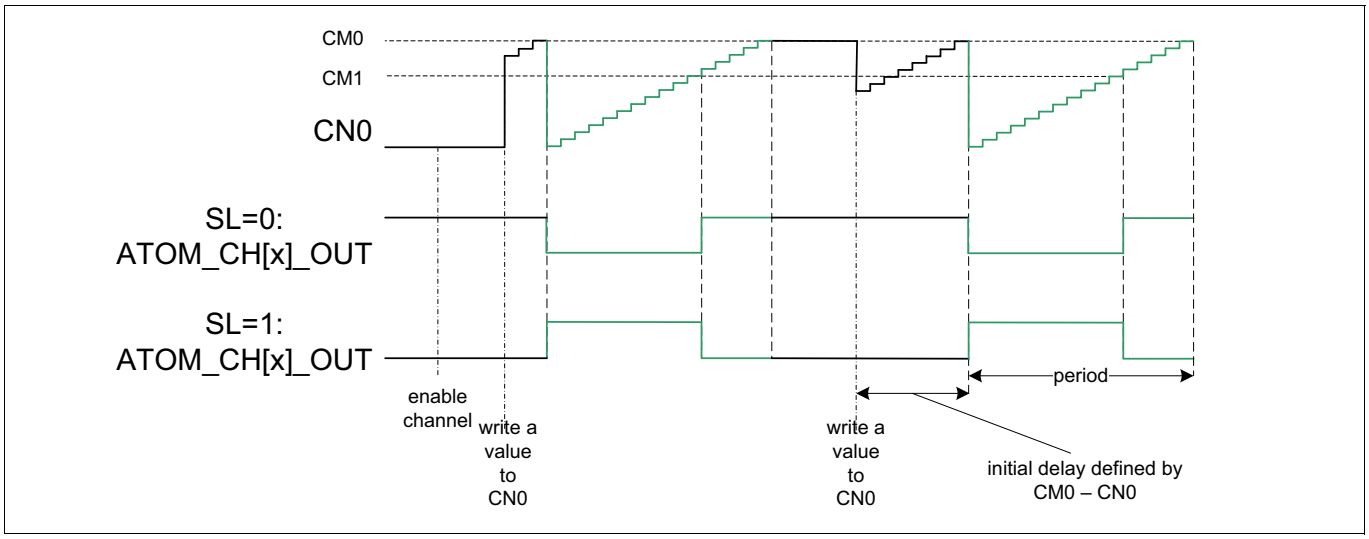


Figure 81 PWM Output with respect to configuration bit SL in One-shot counting up mode: trigger by writing to CN0

Further output of single pulses can be started by a write access to register **CN0**.

If **CN0** is already incrementing (i.e. started by writing to **CN0** a value CN0start < **CM0**), the effect of a second write access to **CN0** depends on the phase of **CN0**:

- phase 1: update of **CN0** before **CN0** reaches first time **CM0** (in fact CM0-1)
- phase 2: update of **CN0** after **CN0** has reached first time **CM0** but is less than **CM1**

- phase 3: update of **CN0** after **CN0** has reached first time **CM0** (in fact CM0-1) and **CN0** is greater than or equal **CM1**

In phase 1: writing to counter **CN0** a value CN0new < **CM0** leads to a shift of first edge (generated if **CN0** is reset first time from **CM0-1 back to 0**) by the time **CM0**-CN0new.

In phase 2: writing to incrementing counter **CN0** a value CN0new < **CM1** while CN0old is below **CM1** leads to a lengthening of the pulse. The counter **CN0** stops if it reaches **CM0**.

In phase 3: Writing to incrementing counter **CN0** a value CN0new while CN0old is already greater than or equal **CM1** leads to an immediate restart of a single pulse generation inclusive the initial delay defined by **CM0** - CN0new.

If a channel is configured to one-shot mode and configuration bit **OSM_TRIG** is set to 1, the trigger signal *OSM_TRIG* (i.e. *TRIG_[x-1]* or *TIM_EXT_CAPTURE(x)*) triggers start of one pulse generation.

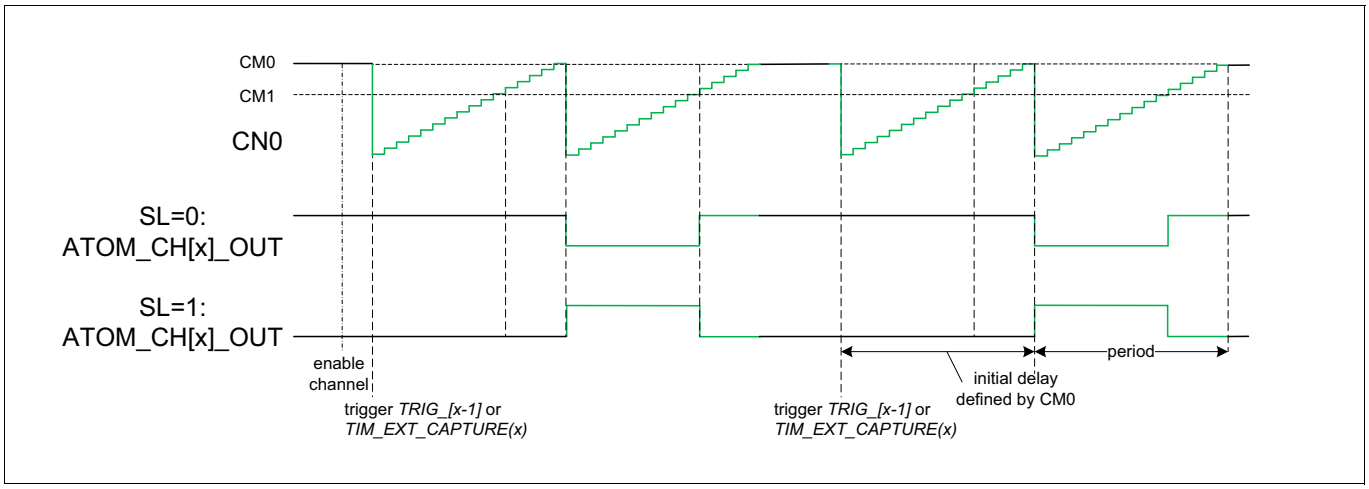


Figure 82 PWM Output with respect to configuration bit SL in one-shot mode: trigger by TRIG_[x-1] or TIM_EXT_CAPTURE(x)

28.15.3.3.6 One-shot Counting Up-Down Mode

The ATOM channel can operate in one-shot counting up-down mode when the bit **OSM** = 1 and the **UDMODE** != 0b00. One-shot mode means that a single pulse with the pulse level defined in bit **SL** is generated on the output line.

First the channel has to be enabled by setting the corresponding **ENDIS_STAT** value.

In one-shot mode the counter **CN0** will not be incremented once the channel is enabled.

A write access to the register **CN0** triggers the start of pulse generation (i.e. the increment of the counter register **CN0**).

To avoid an update of **CMx** register with content of **SRx** register at this point in time, the automatic update should be disabled by writing **UPEN_CTRL[x]** = 0b01 (see register **ATOM[i]_AGC_GLB_CTRL**)

If the counter **CN0** is greater or equal than **CM1**, the output *ATOM[i]_CH[x]_OUT* is set to **SL** value.

If the counter **CN0** is less than **CM1**, the output *ATOM[i]_CH[x]_OUT* is set to !**SL** value.

If the counter **CN0** has reached the value 0 (by counting down), it stops.

The new value of **CN0** determines the start delay of the first edge. The delay time of the first edge is given by (**CM1-CN0**) multiplied with period defined by current value of **CLK_SRC**.

Figure 83 depicts the pulse generation in SOMP one-shot mode.

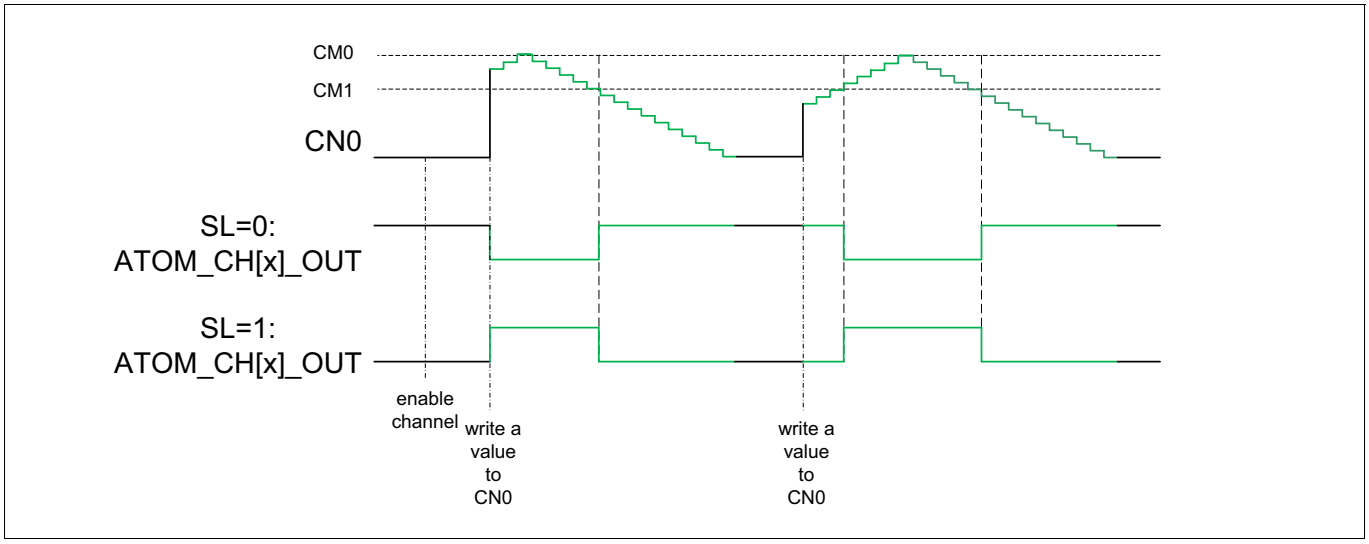


Figure 83 PWM Output with respect to configuration bit SL in one-shot counting up-down mode: trigger by writing to CN0

Further output of single pulses can be started by writing to register **CN0**.

If a channel is configured to one-shot counting up-down mode and configuration bit **OSM_TRIG** is set to 1, the trigger signal *OSM_TRIG* (i.e. *TRIG_[x-1]* or *TIM_EXT_CAPTURE(x)*) triggers start of one pulse generation.

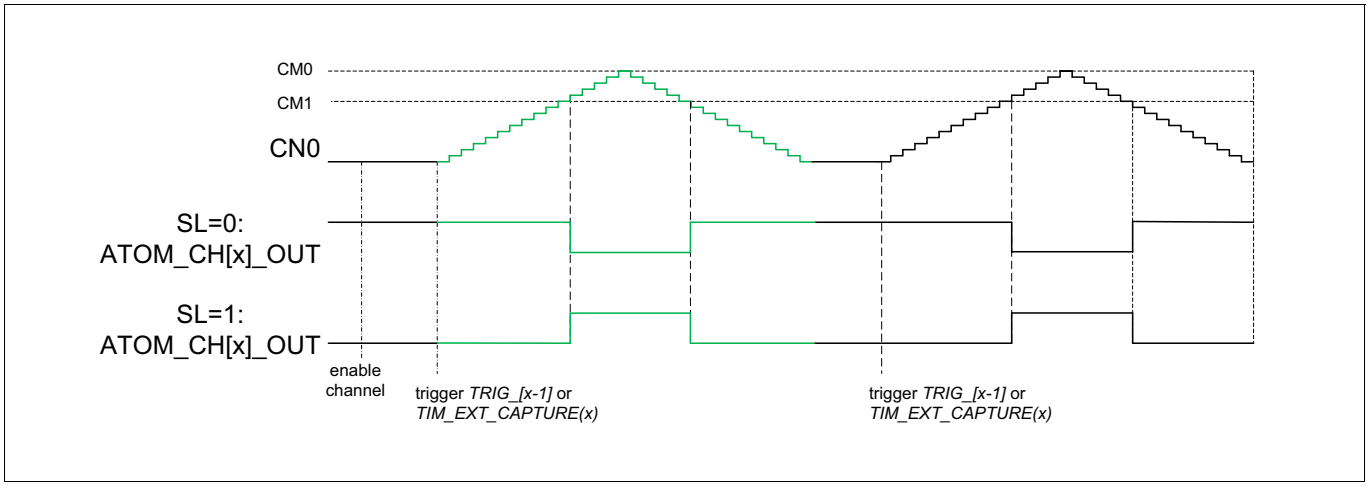


Figure 84 PWM Output with respect to configuration bit SL in one-shot counting up-down mode: trigger by TRIG_[x-1] or TIM_EXT_CAPTURE(x)

28.15.3.3.7 Pulse Count Modulation Mode

At the output *ATOM[i]_CH[x]_OUT* a pulse count modulated signal can be generated instead of the simple PWM output signal in SOMP mode.

The PCM mode is enabled by setting bit **BITREV** to 1 (bit 6 in **ATOM[i]_CH[x]_CTRL** register).Please note that it is device specific, in which channel the PCM mode is available. Please refer to device specific device specific appendix for this information.

With the configuration bit **BITREV**=1 a bit-reversing of the counter output **CN0** is configured. In this case the bits LSB and MSB are swapped, the bits LSB+1 and MSB-1 are swapped, the bits LSB+2 and MSB-2 are swapped and so on.

The effect of bit-reversing of the **CN0** register value is shown in the following **Figure 85**.

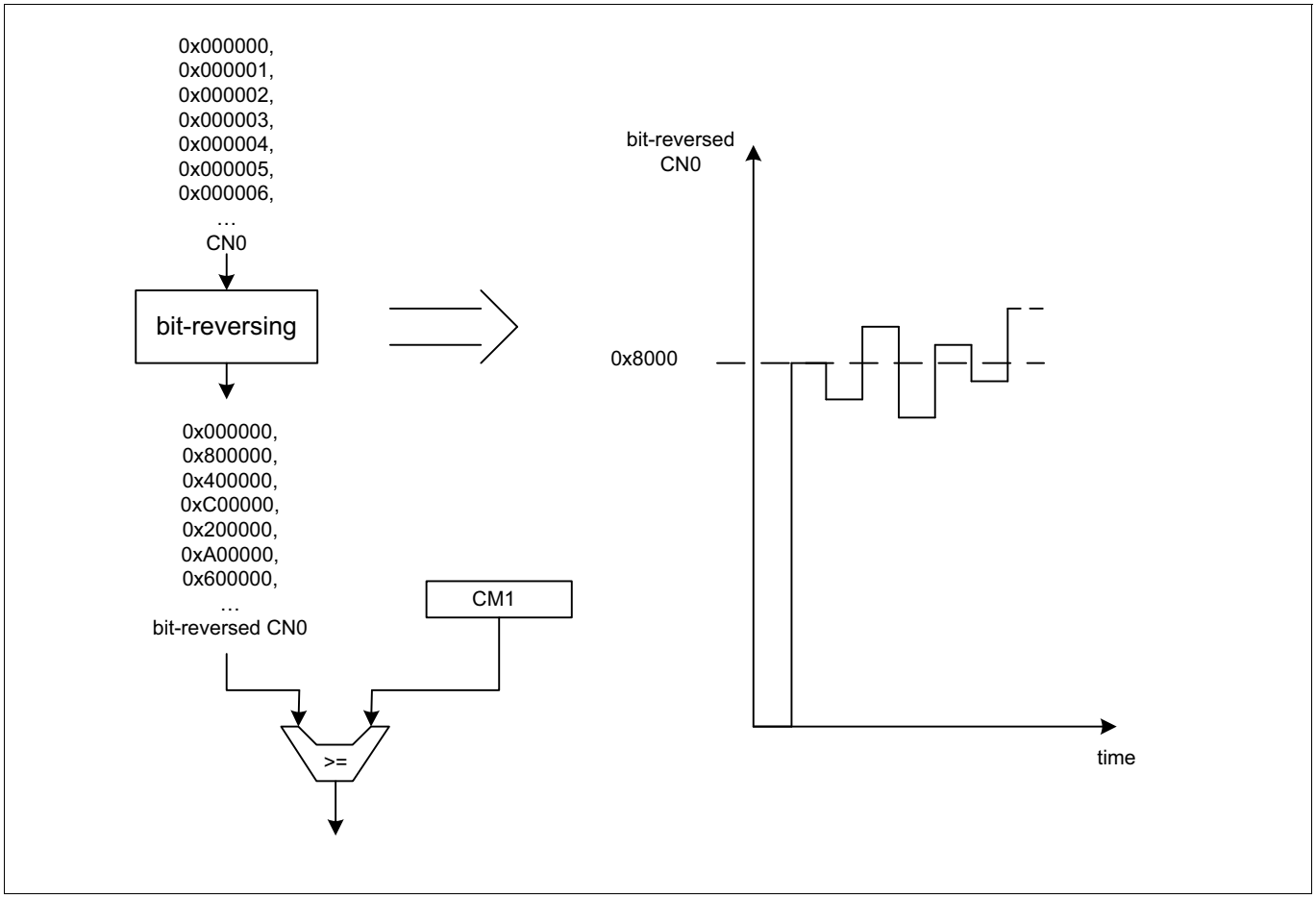


Figure 85 Bit reversing of counter CN0 output

In the PCM mode the counter register **CN0** is incremented by every clock tick depending on configured CMU clock (*CMU_CLK*).

The output of counter register **CN0** is first bit-reversed and then compared with the configured register value **CM1**.

If the bit-reversed value of register **CN0** is greater or equal than **CM1**, the SR-FlipFlop of sub-module SOU is set (i.e. set to inverse value of **SL**) otherwise the SR-FlipFlop is reset (i.e. to the value of **SL**). This generates at the output *ATOM[i]_CH[x]_OUT* a pulse count modulated signal.

In PCM mode the **CM0** register - in which the period is defined - normally has to be set to its maximum value 0xFFFFFF.

To reduce time period of updating duty cycle value in **CM1** register, it is additionally possible to setup period value in **CM0** register to smaller values than maximum value as described before.

Possible values for **CM0** register are each even numbered values to the power of 2 e.g. 0x800000, 0x400000, 0x200000….

In this case the duty cycle has to be configured in the following manner.

Depending on how much the period in **CM0** register is decreased - means shifted right starting from 0x1000000 - the duty cycle in **CM1** register has to be shifted left (= rotated: shift MSB back into LSB) with same value, e.g.:

period **CM0** = 0x001000 -> shifted 8 bits right from 0x1000000

--> so duty cycle has to be shifted left 8 bit:

e.g. 50% duty cycle = 0x0008000 -> shift 8 bits left -> **CM1** = 0x800000

More examples:

period CM0	-->	duty cycle	-->	no shift	-->	CM1
0xFFFFFF	-->	0x800000	-->	no shift	-->	0x800000
0x800000	-->	0x400000	-->	shift 1 bit left	-->	0x800000
0x400000	-->	0x100000	-->	shift 2 bits left	-->	0x400000
0x200000	-->	0x0FFFFF	-->	shift 3 bits left	-->	0x7FFFF8
0x100000	-->	0x033333	-->	shift 4 bits left	-->	0x333330
0x080000	-->	0x005555	-->	shift 5 bits left	-->	0x0AAAA0
…						
0x000020	-->	0x000008	-->	shift 19 bits left	-->	0x400000
0x000010	-->	0x000005	-->	shift 20 bits left	-->	0x500000
…						

In this mode the interrupt CCU1TC (see register **ATOM[i]_CH[x]_IRQ_NOTIFY**) is set every time if bit reverse value of **CN0** is greater or equal than **CM1** which may be multiple times during one period. Therefore, from application point of view it is not useful to enable this interrupt.

28.15.3.3.8 Trigger generation

For applications with constant PWM period defined by **CM0**, it is not necessary to update regularly the **CM0** register with **SR0** register. For these applications the **SR0** register can be used to define an additional output signal and interrupt trigger.

If bit **SR0_TRIG** in register **ATOM[i]_CH[x]_CTRL** is set, the register **SR0** is no longer used as a shadow register for register **CM0**. Instead, **SR0** is compared against **CN0** and if both are equal, a pulse of signal level 1 is generated at the output *ATOM[i]_CH[x]_OUT_T*.

The bit **SR0_TRIG** should only be set if bit RST_CCU0 of this channel is 0.

Note: If **ARU_EN**=1 and both **SR0** and **SR1** are updated via ARU, the new **SR0** value is used immediately after update. Update of **SR0** via ARU can be suppressed by ADL configuration in register **ATOM[i]_CH[x]_CTRL**.

If bit **SR0_TRIG** is set the interrupt notify flag **CCU1TC** is no longer set on a compare match of **CM1** and **CN0**. Instead, the **CCU1TC** interrupt notify flag is set in case of a compare equal match of **SR0** and **CN0**.

With configuration bit **TRIG_PULSE** one can select if the output *ATOM[i]_CH[x]_OUT_T* is high as long as **CN0**=**SR0** (**TRIG_PULSE**=0) or if there will be only one pulse of length one *SYS_CLK* period when **CN0** becomes **SR0** (**TRIG_PULSE**=1).

The ATOM output signal routing to DTM or GTM top level is described in subchapter “DTM connections on GTM-IP top level“.

28.15.3.3.9 Register ATOM[i]_CH[x]_CTRL in SOMP mode

Register ATOM[i]_CH[x]_CTRL in SOMP mode

GTM_ATOMi_CHx_SOMP (i=0-11; x=0-7)
ATOMi Channel x Control Register in SOMP Mode ($E8004_H$ + i*800_H+ x*80_H) **Reset Value: 00000800_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FREEZE	Not_used	EXT_FUPD	Reserved	Not_used	OSM	Not_used	TRIGOUT	EXTTRIGOUT	EXT_TRIG	OSM_TRIG	RST_CCU0	UDMODE		TRIG_PULSE	Not_used
rw	rw	rw	r	rw	rw	rw	rw	rw	rw	rw	rw	rw		rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECLK_SRC	CLK_SRC_SR			SL	Not_used	Not_used	Not_used	SR0_TRIG	BITREV	ADL		ARU_EN	Not_used	MODE	
rw	rw			rw	rw	rw	rw	rw	rw	rw		rw	rw	rw	

Field	Bits	Type	Description
MODE	1:0	rw	**ATOM channel mode select** 10_B ATOM Signal Output Mode PWM (SOMP)
Not_used	2	rw	**Not used** Note: Not used in this mode.
ARU_EN	3	rw	**ARU Input stream enable** 0_B ARU Input stream disabled 1_B ARU Input stream enabled
ADL	5:4	rw	**ARU data select for SOMP** 00_B Load both ARU words into shadow registers 01_B Load ARU low word (Bits 23…0) into shadow register SR0 10_B Load ARU high word (Bits 47…24) into shadow register SR1 11_B Reserved Note: This bit field is only relevant in SOMP mode to select the ARU data source.
BITREV	6	rw	**Bit-reversing of output of counter register CN0. This bit enables the PCM mode** It is device specific, in which channel the PCM mode is available. Please refer to device specific device specific appendix for this information.
SR0_TRIG	7	rw	**SR0 is used to generate a trigger on output ATOM[i]_CH[x]_OUT_T if equal to CN0** 0_B SR0 is used as a shadow register for register CM0. 1_B SR0 is not used as a shadow register for register CM0. SR0 is compared with CN0 and if both are equal, a trigger pulse is generated at output *ATOM[i]_CH[x]_OUT_T*. Note: This bit is only relevant in SOMP mode. Note: This bit should only be set if RST_CCU0 of this channel is 0.
Not_used	8	rw	**Not used** Note: Not used in this mode.

Field	Bits	Type	Description
Not_used	9	rw	**Not used** Note: Not used in this mode.
Not_used	10	rw	**Not used** Note: Not used in this mode.
SL	11	rw	**Signal level for pulse of PWM** 0_B Low signal level 1_B High signal level Note: Reset value depends on the hardware configuration chosen by silicon vendor. Note: If the output is disabled, the output ATOM_OUT[x] is set to inverse value of SL FREEZE=0, the following note is valid: If the channel is disabled, the output register of SOU unit is set to inverse value of SL. If FREEZE=1, the following note is valid: If the channel is disabled, the output register of SOU unit is not changed and output ATOM_OUT[x] is not changed.
CLK_SRC_SR	14:12	rw	**Shadow register for CMU clock source register CLK_SRC** If ECLK_SRC=0 / ECLK_SRC=1: 000_B *CMU_CLK0* selected / *CMU_CLK0* selected 001_B *CMU_CLK1* selected / *CMU_CLK1* selected 010_B *CMU_CLK2* selected / *CMU_CLK2* selected 011_B *CMU_CLK3* selected / Reserved 100_B *CMU_CLK4* selected / clock stopped 101_B *CMU_CLK5* selected / *TRIG[x-1]* selected 110_B *CMU_CLK6* selected / *TIM_EXT_CAPTURE[x]* selected 111_B *CMU_CLK7* selected / *CMU_CLK7* selected Note: This register is a shadow register for the register CLK_SRC. Thus, if the CMU_CLK source for PWM generation should be changed during operation, the old CMU_CLK has to operate until the update of the ATOM channels internal CLK_SRC register by the CLK_SRC_SR content is done either by an end of a period or a FORCE_UPDATE. Note: After (channel) reset the selected CLK_SRC value is the SYS_CLK (input of Global Clock Divider). To use in SOMP mode one of the CMU_CLKx, it is recommended to perform a forced update of CLK_SRC with the value of CLK_SRC_SR value before/with enabling the channel. Note: In case of ECLK_SRC=1 and CLK_SRC_SR = 0b11 / 0b100 / 0b101 / 0b110 a force update leads to an immediate update of CM0, CM1 and CLK_SRC.
ECLK_SRC	15	rw	**Extend CLK_SRC** 0_B CLK_SRC_SR set 1 selected 1_B CLK_SRC_SR set 2 selected See bit CLK_SRC_SR description for details.
Not_used	16	rw	**Not used** Note: Not used in this mode.

Field	Bits	Type	Description
TRIG_PULSE	17	rw	**Trigger output pulse length of one SYS_CLK period** 0_B output on TOM[i]_OUT[x]_T is 1 as long as CN0=SR0 (if SR=_TRIG=1) 1_B output on TOM[i]_OUT[x]_T is 1 for only one SYS_CLK period if CN0=SR0 (if SR=_TRIG=1)
UDMODE	19:18	rw	**Up/down counter mode** 00_B up/down counter mode disabled: CN0 counts always up 01_B up/down counter mode enabled: CN0 counts up and down, CM0,CM1 are updated if CN0 reaches 0 (i.e. changes from down to up) 10_B up/down counter mode enabled: CN0 counts up and down, CM0,CM1 are updated if CN0 reaches CM0 (i.e. changes from up to down) 11_B up/down counter mode enabled: CN0 counts up and down, CM0,CM1 are updated if CN0 reaches 0 or CM0 (i.e. changes direction) Note: This mode is only applicable in SOMP mode.
RST_CCU0	20	rw	**Reset source of CCU0** 0_B Reset counter register CN0 to 0 on matching comparison with CM0 1_B Reset counter register CN0 to 0 on trigger *TRIG_[x-1]* or *TIM_EXT_CAPTURE(x)*. Note: If RST_CCU0=1 and UPEN_CTRLx=1 are set, *TRIG_[x-1]* or TIM_*EXT_CAPTURE(x)* triggers also the update of work register (CM0, CM1 and CLK_SRC).
OSM_TRIG	21	rw	**Enable trigger of one-shot pulse by trigger signal OSM_TRIG** 0_B signal OSM_TRIG cannot trigger start of single pulse generation 1_B signal OSM_TRIG can trigger start of single pulse generation (if bit OSM = 1) Note: This bit should only be set if bit OSM=1 and bit RST_CCU0=0.
EXT_TRIG	22	rw	**Select TIM_EXT_CAPTURE(x) as trigger signal** 0_B signal *TIM_[x-1]* is selected as trigger to reset CN0 or to start single pulse generation. 1_B signal *TIM_EXT_CAPTURE(x)* is selected
EXTTRIGOUT	23	rw	**Select TIM_EXT_CAPTURE(x) as potential output signal TRIG_[x]** 0_B signal *TRIG_[x-1]* is selected as output on *TRIG_[x]* (if TRIGOUT=0) 1_B signal *TIM_EXT_CAPTURE(x)* is selected as output on *TRIG_[x]* (if TRIGOUT=0)
TRIGOUT	24	rw	**Trigger output selection (output signal TRIG_CHx) of module ATOM_CHx** 0_B *TRIG_[x]* is *TRIG_[x-1*] or *TIM_EXT_CAPTURE(x)*. 1_B *TRIG_[x]* is *TRIG_CCU0*
Not_used	25	rw	**Not used** Note: Not used in this mode.
OSM	26	rw	**One-shot mode** 0_B Continuous PWM generation after channel enable 1_B A single pulse is generated

Field	Bits	Type	Description
Not_used	27	rw	**Not used** Note: Not used in this mode.
Reserved	28	r	**Reserved** Read as zero, should be written as zero.
EXT_FUPD	29	rw	**External forced update** 0_B use FUPD(x) signal from AGC to force update 1_B use TIM_EXT_CAPTURE signal to force update This bit is only applicable in SOMP and SOMS mode.
Not_used	30	rw	**Not used** Note: Not used in this mode.
FREEZE	31	rw	**FREEZE** 0_B a channel disable/enable may change internal register and output register 1_B a channel enable/disable does not change an internal or output register but stops counter CN0 (in SOMP mode), comparison (in SOMC/SOMB mode) and shifting (in SOMS mode) *Note: If channel is disabled and output is enabled, in SOMP mode with UDMODE!=0b00 the output is depending directly on SL bit, independent on FREEZE mode.*

28.15.3.4 ATOM Signal Output Mode Serial (SOMS)

In ATOM Signal Output Mode Serial (SOMS) the ATOM channel acts as a serial output shift register where the content of the **CM1** register in the CCU1 unit is shifted out whenever the unit is triggered by the selected *CMU_CLK* input clock signal. The shift direction is configurable with the **ACB(0)** bit inside the **ATOM[i]_CH[x]_CTRL** register when ARU is disabled and the **ACBI(0)** bit inside the **ATOM[i]_CH[x]_STAT** register when ARU is enabled.

The data inside the **CM1** register has to be aligned according to the selected shift direction in the **ACB(0)**/**ACBI(0)** bit. This means that when a right shift is selected, that the data word has to be aligned to bit 0 of the **CM1** register and when a left shift is selected, that the data has to be aligned to bit 23 of the **CM1** register.

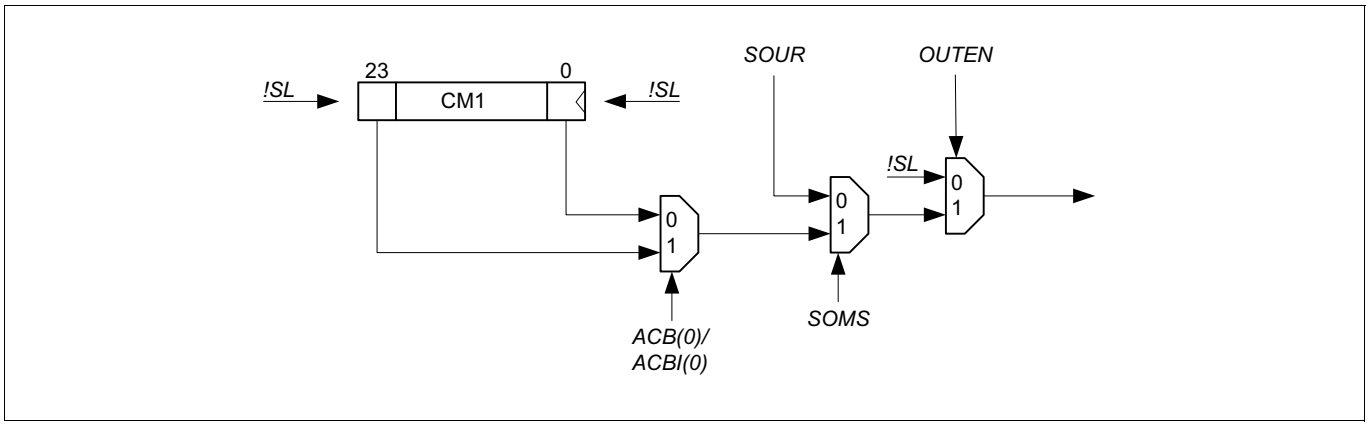


Figure 86 SOMS Mode output generation

Figure 86 shows the output generation in case of SOMS mode is selected.

In SOMS mode CCU0 runs in counter/compare mode and counts the number of bits shifted out so far. The total number of bits that should be shifted is defined as **CM0**. The total number of bits that are visible at *ATOM_OUT* is **CM0**+1.

When the output is disabled the *ATOM_OUT* is set to the inverse **SL** bit definition.

When the content of the **CM1** register is shifted out, the inverse signal level is shifted into the **CM1** register.

When the output is enabled while **UPEN_CTRL[x]** is disabled, the ATOM_OUT signal level is defined by **CM1** bit 0 or 23, dependent on the shift direction defined by **ACB(0)** or **ACBI(0)** register setting. **Figure 87** should clarify the ATOM channel startup behavior in this case for right shift. For left shift the **CM1** bit 0 in **Figure 87** has to be replaced by **CM1** bit 23.

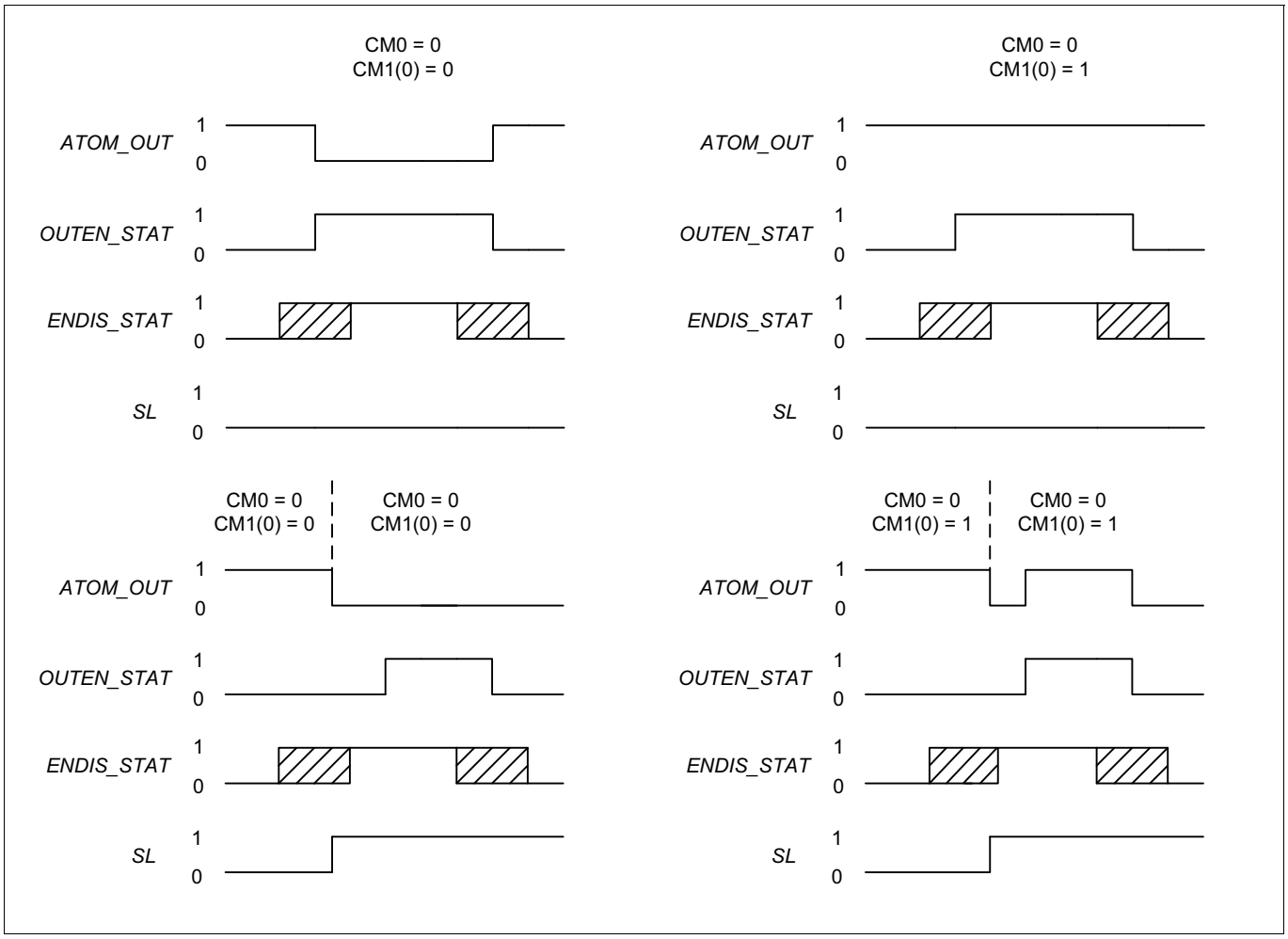


Figure 87 SOMS Output signal level at startup, UPEN_CTRL[x] disabled

If **UPEN_CTRL[x]** is set and the channel is enabled, the output level is defined by bit 0 or 23 of **CM1** register dependent on the shift direction. **Figure 88** shows the output behavior in that case.

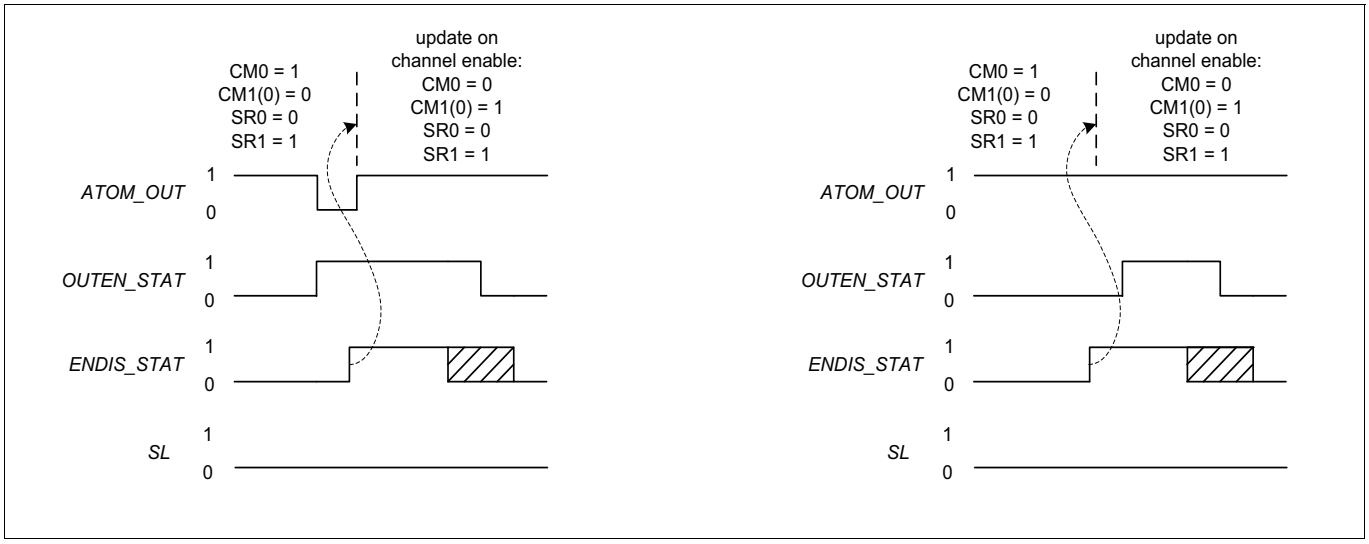


Figure 88 SOMS Output signal level at startup, UPEN_CTRL[x] enabled

When the serial data to be shifted is provided via ARU the number of bits that should be shifted has to be defined in the lower 24 bits of the ARU word (23 to 0) and the data that is to be shifted has to be defined in the ARU bits 47 to 24 aligned according to the shift direction. This shift direction has to be defined in the ARU word bit 48 (**ACB0** bit).

If bit **UPEN_CTRL[x]** of a channel x is set, after update of **CM0**/**CM1** register with the content of the **SR0**/**SR1** register, a new ARU read request is set up.

If bit **UPEN_CTRL[x]** of a channel x is not set, no (further) ARU read request is set up (because the **SR0**/**SR1** register are never used for update) and the ATOM may stop shifting after **CN0** has reached **CM0**. Note, that in this case also no automatic restart of shifting is possible.

If a channel is enabled with the settings SOMS mode and **ARU_EN** = 1, the first received values from ARU are stored in register **SR0** and **SR1**. If **CN0** and **CM0** are 0 (i.e. **CN0** is not counting) and the update of channel x is enabled (**UPEN_CTRL[x]**=1), an immediate update of the register **CM0** and **CM1** is also done. This update of **CM0** and **CM1** triggers the start of shifting.

It is recommended to configure the ATOM channel in One-shot mode when the **ARU_EN** bit is not set, since the ATOM channel would reload new values from the shadow registers when **CN0** reaches **CM0**.

28.15.3.4.1 SOMS mode with ARU_EN = 1 and OSM = 0, UPEN_CTRL[x] = 1

In case of bit **ARU_EN** is set and bit **OSM** is not set, the channel is running in the SOMS continuous mode. Then, if the content of the **CM0** register equals the counter **CN0**, the **CM0** and **CM1** registers are reloaded with the **SR0** and **SR1** content and new values are requested from the ARU. If the update of the shadow registers does not happen before **CN0** reaches **CM0** the old values of **SR0** and **SR1** are used to reload the operation registers.

In contrast to controlling the channel via AEI, the shift direction defined by ARU word bit 48 has only effect after the update of **CMx** operation registers from the **SRx** registers.

28.15.3.4.2 SOMS mode with ARU_EN = 1 and OSM = 1, UPEN_CTRL[x] = 1

In case of bit **ARU_EN** is set and bit **OSM** is set, the channel is running in the SOMS one-shot mode. Then, if the content of the **CM0** register equals the counter **CN0** and if new values are available in **SR0** and **SR1** (bit DV set), the **CM0** and **CM1** registers are reloaded with the **SR0** and **SR1** content and new values are requested from the ARU. If no new values are available in **SR0** and **SR1**, the register **CM0** and **CM1** will not be updated, the counter

CN0 stops and the ATOM channel continues to request new data from ARU. A later reception of new ARU data in **SR0** and **SR1** will immediately force the update of the register **CM0** and **CM1** and restart the counter **CN0**.

28.15.3.4.3 SOMS mode with ARU_EN = 0 and OSM = 0, UPEN_CTRL[x] = 1

In case of bit **ARU_EN** is not set and bit **OSM** is not set, the ATOM channel updates its CM0/CM1 register with the content of the SR0/SR1 register and restarts shifting immediately. The first bit of new CM1 register value will be applied at the output without any gap to the last bit of the previous CM1 register value.

28.15.3.4.4 SOMS mode with ARU_EN = 0 and OSM = 1, UPEN_CTRL[x] = 1:

In case of bit **ARU_EN** is not set and bit **OSM** is set, the ATOM channel stops shifting when **CN0** reaches **CM0** and no update of **CM0** and **CM1** is performed.

Then, the shifting of the channel can be restarted again by writing a zero to the **CN0** register again. Please note, that the **CN0** register should be written with a zero since the **CN0** register counts the number of bits shifted out by the ATOM channel.The writing of a zero to **CN0** causes also an immediate update of **CM0**/**CM1** register with the content of **SR0**/**SR1** register.

28.15.3.4.5 SOMS mode with double output

If in SOMS mode additionally the mode bit DSO is set (in register **ATOM[i]_CH[x]_CTRL**) two 12 bit data streams can be shifted out on the outputs *ATOM_OUT* and *ATOM_OUT_T* in parallel.This is reached by splitting the register **CM1** into two parts. The lower 12 bits are used as a shift register of output *ATOM_OUT* (i.e. bit 0 is assigned to output *ATOM_OUT*), the upper 12 bits are used as a shift register of output *ATOM_OUT_T* (i.e. bit 12 is assigned to output *ATOM_OUT_T*).On bit 23 and 11 of register **CM1** the value !**SL** is shifted in. Note: In this mode only shift right is possible. Bit **ACB0** is ignored.This behavior is depicted in the following figure:

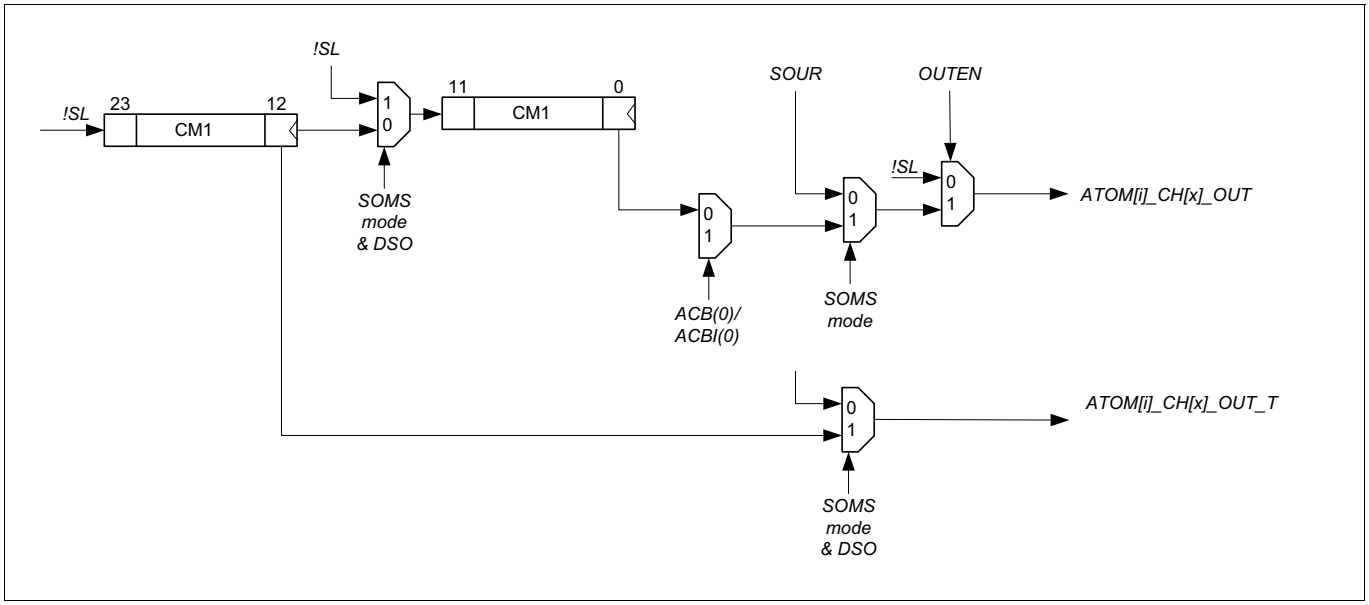


Figure 89 Double Output Shift Mode

28.15.3.4.6 Interrupts in SOMS mode

In ATOM Signal Output Mode Serial only the interrupt CCU0TC (**ATOM[i]_CH[x]_IRQ_NOTIFY**) in case of **CN0** >= **CM0** is generated. The interrupt **CCU1TC** has no meaning and is not generated.

28.15.3.4.7 Register ATOM[i]_CH[x]_CTRL in SOMS mode

Register ATOM[i]_CH[x]_CTRL in SOMS mode

GTM_ATOMi_CHx_SOMS (i=0-11; x=0-7)

ATOMi Channel x Control Register in SOMS Mode ($E8004_H$ + i*800_H+ x*80_H) **Reset Value: 00000800_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FREEZE	Not_used	EXT_FUPD	Reserved	Not_used	OSM	Not_used	Not_used	Not_used			Not_used	Not_used		Not_used	Not_used
rw	rw	rw	r	rw	rw	rw	rw	r			rw	rw		rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECLK_SRC	CLK_SRC_SR			SL	Not_used	Not_used	Not_used	DSO	Not_used		ACB0	ARU_EN	Not_used	MODE	
rw	rw			rw	rw	rw	rw	rw	rw		rw	rw	rw	rw	

Field	Bits	Type	Description
MODE	1:0	rw	**ATOM channel mode select** 11_B ATOM Signal Output Mode Serial (SOMS)
Not_used	2	rw	**Not used** Note: Not used in this mode.
ARU_EN	3	rw	**ARU Input stream enable** 0_B ARU Input stream disabled 1_B ARU Input stream enabled
ACB0	4	rw	**Shift direction for CM1 register** 0_B Right shift of data is started from bit 0 of CM1 1_B Left shift of data is started from bit 23 of CM1 Note: The data that has to be shifted out has to be aligned inside the CM1 register according to the defined shift direction. Note: This bit is only applicable if ARU_EN = 0. Note: If the direction (ACB0) is changed the output ATOM_OUT[x] switches immediately to the other 'first' bit of CM1 (bit 0 if ACB0 = 0, bit 23 if ACB0 = 1).
Not_used	6:5	rw	**Not used** Note: Not used in this mode.
DSO	7	rw	**Double Shift Output** 0_B CM1 is used as a 24 bit shift register 1_B CM1 is split into two 12 bit shift register Note: if DSO=1, only shift right is possible
Not_used	8	rw	**Not used** Note: Not used in this mode.
Not_used	9	rw	**Not used** Note: Not used in this mode.
Not_used	10	rw	**Not used** Note: Not used in this mode.

Field	Bits	Type	Description
SL	11	rw	**Defines signal level when channel and output is disabling** 0_B Low signal level 1_B High signal level Note: Reset value depends on the hardware configuration chosen by silicon vendor. Note: If the output is disabled, the output ATOM_OUT[x] is set to inverse value of SL. Note: If the output is enabled, the output ATOM_OUT[x] is set to bit 0 or 23 of CM1 register. Note: The inverse value of SL is shifted into the CM1 register. If FREEZE=0, the following note is valid: If the channel is disabled, the output register of SOU unit is set to inverse value of SL. If FREEZE=1, the following note is valid: If the channel is disabled, the output register of SOU unit is not changed and output ATOM_OUT[x] is not changed.
CLK_SRC_SR	14:12	rw	**Shift frequency select for channel** If ECLK_SRC=0 / ECLK_SRC=1: 000_B *CMU_CLK0* selected / *CMU_CLK0* selected 001_B *CMU_CLK1* selected / *CMU_CLK1* selected 010_B *CMU_CLK2* selected / *CMU_CLK2* selected 011_B *CMU_CLK3* selected / Reserved 100_B *CMU_CLK4* selected / clock stopped 101_B *CMU_CLK5* selected / *TRIG[x-1]* selected 110_B *CMU_CLK6* selected / *TIM_EXT_CAPTURE[x]* selected 111_B *CMU_CLK7* selected / *CMU_CLK7* selected Note: This register is a shadow register for the register CLK_SRC. Thus, if the CMU_CLK source for PWM generation should be changed during operation, the old CMU_CLK has to operate until the update of the ATOM channels internal CLK_SRC register by the CLK_SRC_SR content is done either by an end of a period or a FORCE_UPDATE. Note: After (channel) reset the selected CLK_SRC value is the SYS_CLK (input of Global Clock Divider). To use in SOMP mode one of the CMU_CLKx, it is recommended to perform a forced update of CLK_SRC with the value of CLK_SRC_SR value before/with enabling the channel.
ECLK_SRC	15	rw	**Extend CLK_SRC** 0_B CLK_SRC_SR set 1 selected 1_B CLK_SRC_SR set 2 selected See bit CLK_SRC_SR description for details.
Not_used	16	rw	**Not used** Note: Not used in this mode.
Not_used	17	rw	**Not used** Note: Not used in this mode.
Not_used	19:18	rw	**Not used** Note: Not used in this mode.
Not_used	20	rw	**Not used** Note: Not used in this mode.

Field	Bits	Type	Description
Not_used	23:21	r	**Not used** Note: Not used in this mode.
Not_used	24	rw	**Not used** Note: Not used in this mode.
Not_used	25	rw	**Not used** Note: Not used in this mode.
OSM	26	rw	**One-shot mode** 0_B Continuous shifting is enabled 1_B Channel stops, after number of bits defined in CM0 is shifted out
Not_used	27	rw	**Not used** Note: Not used in this mode.
Reserved	28	r	**Reserved** Read as zero, should be written as zero.
EXT_FUPD	29	rw	**External forced update** 0_B use FUPD(x) signal from AGC to force update 1_B use TIM_EXT_CAPTURE signal to force update Note: This bit is only applicable in SOMP and SOMS mode.
Not_used	30	rw	**Not used** Note: Not used in this mode.
FREEZE	31	rw	**FREEZE** 0_B a channel disable/enable may change internal register and output register 1_B a channel enable/disable does not change an internal or output register but stops counter CN0 (in SOMP mode), comparison (in SOMC/SOMB mode) and shifting (in SOMS mode)

28.15.3.5 ATOM Signal Output Mode Buffered Compare (SOMB)

28.15.3.5.1 Overview

In ATOM Signal Output Mode buffered Compare (SOMB) the output action is performed according to the comparison result of the input values located in **CM0** and/or **CM1** registers and the two (three) time base values *TBU_TS0* or *TBU_TS1* (or *TBU_TS2*) provided by the TBU. For a description of the time base generation please refer to the TBU specification in the chapter “Time Base Unite (TBU)”. It is configurable, which of the two (three) time bases is to be compared with one or both values in **CM0** and **CM1**.

The compare strategy of the two compare units CCU0 and CCU1 is controlled by the value of bit field ACBI of register **ATOM[i]_CH[x]_STAT**. This bit field is only readable by CPU. If ARU is disabled, the bit field ACBI can only be updated with the value of bit field **ACB** of register **ATOM[i]_CH[x]_CTRL**. If ARU is enabled, the **ACBI** bit field can be updated with the value of shadow register **ACB_SR** which contains a value received via ARU or the value of bit field **ACB** of register **ATOM[i]_CH[x]_CTRL**.

The table below lists all valid control configurations for bit field **ACBI** of register **ATOM[i]_CH[x]_STAT**.

Table 57 ATOM SOMB compare strategies

ACBI(4)	ACBI(3)	ACBI(2)	CCUx control
0	0	0	Reserved. Has no effect.
0	0	1	Reserved. Has no effect.
0	1	0	Compare in CCU0 only, use time base TBU_TS0. Output signal level is defined by combination of SL, ACB10/ACBI(1…0) bits.
0	1	1	Compare in CCU1 only, use time base TBU_TS1 or TBU_TS2. Output signal level is defined by combination of SL, ACBI[1:0] bits.
1	0	0	Serve Last: Compare in CCU0 and then in CCU1 using TBU_TS0. Output signal level when CCU0 matches is defined by combination of SL, ACBI[1:0]. On the CCU1 match the output level is toggled.
1	0	1	Serve Last: Compare in CCU0 and then in CCU1 using TBU_TS1 or TBU_TS2. Output signal level when CCU0 matches is defined by combination of SL, ACBI[1:0]. On the CCU1 match the output level is toggled.
1	1	0	Serve Last: Compare in CCU0 using TBU_TS0 and then in CCU1 using TBU_TS1 or TBU_TS2. Output signal level when CCU1 matches is defined by combination of SL, ACBI[1:0]
1	1	1	Cancels pending comparison independent on ARU_EN

The CCUx trigger signals *TRIG_CCU0* and *TRIG_CCU1* creates edges depending on the combination of the predefined signal level in **SL** bit and the two control bits **ACBI[1:0]**.

In SOMB mode, if ARU access is enabled, the new compare values received via ARU are always stored in the shadow register **SR0** and **SR1** and the **ACB** bits are stores in an internal register **ACB_SR**.

If the scheduled compare matches in CCU0 and/or CCU1 are occurred and the **SRx** register contain new valid values, the register **CM0** and **CM1** are updated automatically with the content of the corresponding **SRx** register, the **ACBI** bit field is updated with the content of internal **ACB_SR** register and the DV bit of register **ATOM[i]_CH[x]_STAT** is set. If the **SRx** register and the **CMx** register contain no valid value, the compare units are waiting in an idle state.

On a compare match of one of the compare units CCUx units the output ATOM_OUT is set according to combination of **ACBI** bit 1 down to 0 (in register **ATOM[i]_CH[x]_STAT**) and the **SL** bit of register **ATOM[i]_CH[x]_CTRL**.

Table 58 ATOM SOMB output control by ACBI[1:0] and SL

SL	ACBI(1)	ACBI(0)	Output Behavior
0	0	0	No signal level change at output.
0	0	1	Set output signal level to 1.
0	1	0	Set output signal level to 0.
0	1	1	Toggle output signal level.
1	0	0	No signal level change at output.
1	0	1	Set output signal level to 0.
1	1	0	Set output signal level to 1.
1	1	1	Toggle output signal level.

In opposite to SOMC mode no time stamp value of TBU is captured in **SRx** register.

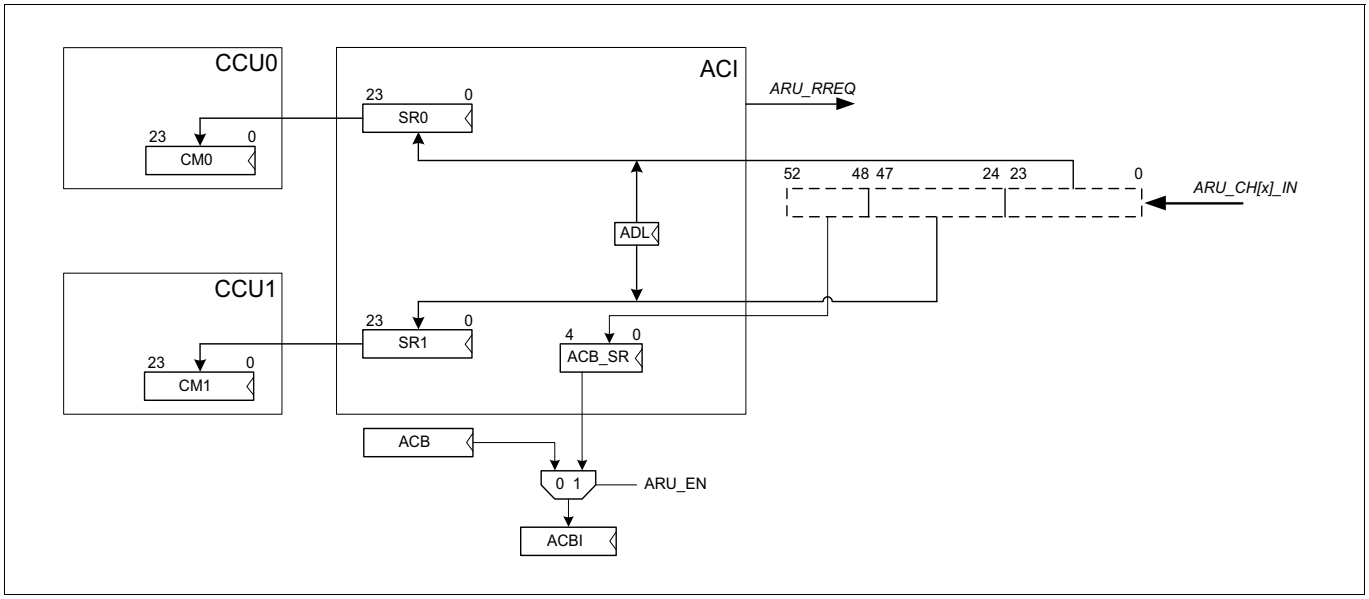


Figure 90 ARU interface behavior in SOMB mode

The flag **DV** of register **ATOM[i]_CH[x]_STAT** indicates that at least one of the **CMx** register contains valid data and a compare event may be pending (if channel is enabled).

The **DV** flag is reset if none of the **CMx** register contains valid data.

28.15.3.5.2 SOMB under CPU control

If bit **ARU_EN** of register **ATOM[i]_CH[x]_CTRL** is not set, the ATOM channel can only be controlled via CPU.

Writing to one of the **CMx** register sets automatically the **DV** bit to validate the new compare value. A comparison depending on value **ACBI** of register **ATOM[i]_CH[x]_STAT** is started immediately.Because only the **ACB** bit of register **ATOM[i]_CH[x]_CTRL** can be written and this bit field serves as a shadow register for the work register **ACBI** (bit field of register **ATOM[i]_CH[x]_STAT)**, it is recommended to first update the **ACB** bit field before updating **CMx**/**SRx** register.

The compare strategy is controlled by the value stored in bit field **ACBI** of register **ATOM[i]_CH[x]_STAT**. If ARU is disabled, this bit field can only be updated with the value of bit field **ACB** of register **ATOM[i]_CH[x]_CTRL**.

The update of bit field **ACBI** can be triggered by a forced update or the normal update mechanism controlled by bit **UPEN_CTRL[x]** in register **ATOM[i]_AGC_GLB_CTRL**.

Writing to one of the **SRx** register and triggering a forced update, updates the **CMx** register with the value of **SRx** register and the **ACBI** bit field with the content of **ACB** bit field of register **ATOM[i]_CH[x]_CTRL**. A new comparison is started.

Writing to one of the **SRx** register while update of **CMx** register is disabled (**UPEN_CTRL[x]** = 0 in **ATOM[i]_AGC_GLB_CTRL**) and enabling update afterwards, triggers the update of **CMx** register and the **ACBI** bit field and starts comparison if previous comparison is finished (**DV** bit was reset).

If ARU access is disabled (**ARU_EN**=0), a force update updates the **CMx** register with the content of **SRx** register and the **ACBI** bit field with the content of **ACB** bit field of register **ATOM[i]_CH[x]_CTRL**.

28.15.3.5.3 SOMB under ARU control

If both compare units CCU0/CCU1 are finished with previous job (depending on compare strategy) and the **SRx** register contain no new value, they are waiting until new data was received via ARU and stored in **SRx** register. Then, an immediately update takes place.

If both compare units are finished with previous job (depending on compare strategy) and there are new data available in **SRx** register, the update the **CMx** register with the value of the **SRx** register and the **ACBI** bit field with the value of internal **ACB_SR** register takes place and a new compare job is started immediately.

After an update of the **CMx** register, a new ARU read request is set.

New compare values received via the ARU are stored in shadow register **SRx**. The **ACB** bits received via ARU are stored in the internal register **ACB_SR**.

If ARU access is enabled (**ARU_EN**=1), a force update updates the **CMx** register with the content of **SRx** register and the **ACBI** bit field with the content of internal **ACB_SR** register.

For compare strategy 'serve last' the CCU0 and CCU1 compare match may occur sequentially. During different phases of compare match the CPU access rights to register **CM0** and **CM1** as well as to **WR_REQ** bit is different. These access rights by CPU to register **CM0** and **CM1** and the **WR_REQ** are depicted in the following figure for the case of **EUPM**=0 (register **ATOM[i]_CH[x]_CTRL**)

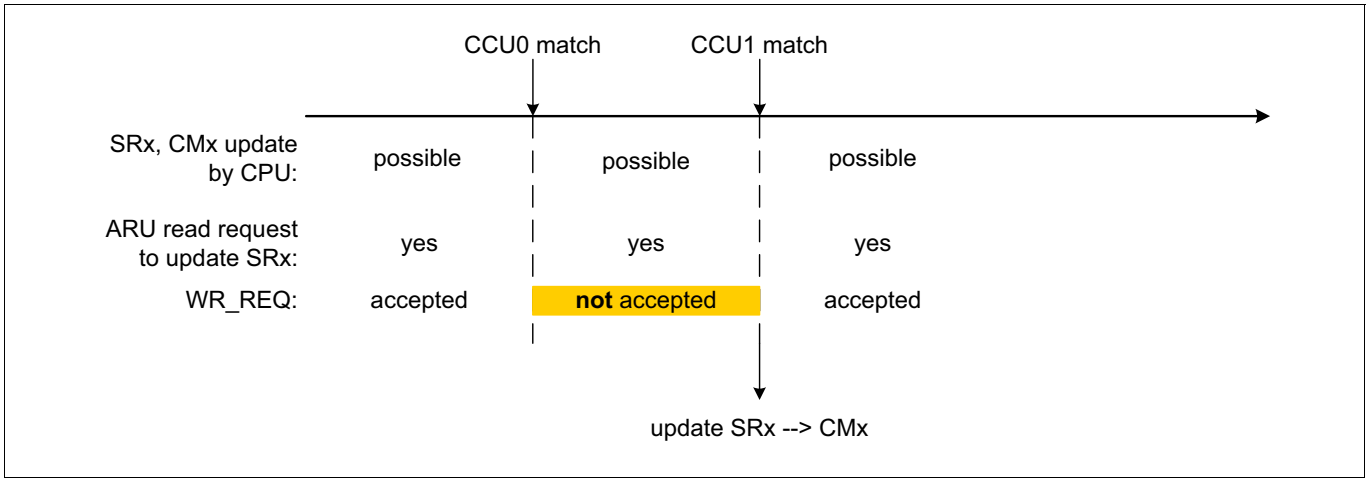


Figure 91 CPU access rights in case of compare strategy 'serve last' and EUPM=0

The access rights by CPU to register **CM0** and **CM1** and the WR_REQ are depicted in the following figure for the case of EUPM=1 (register **ATOM[i]_CH[x]_CTRL**)

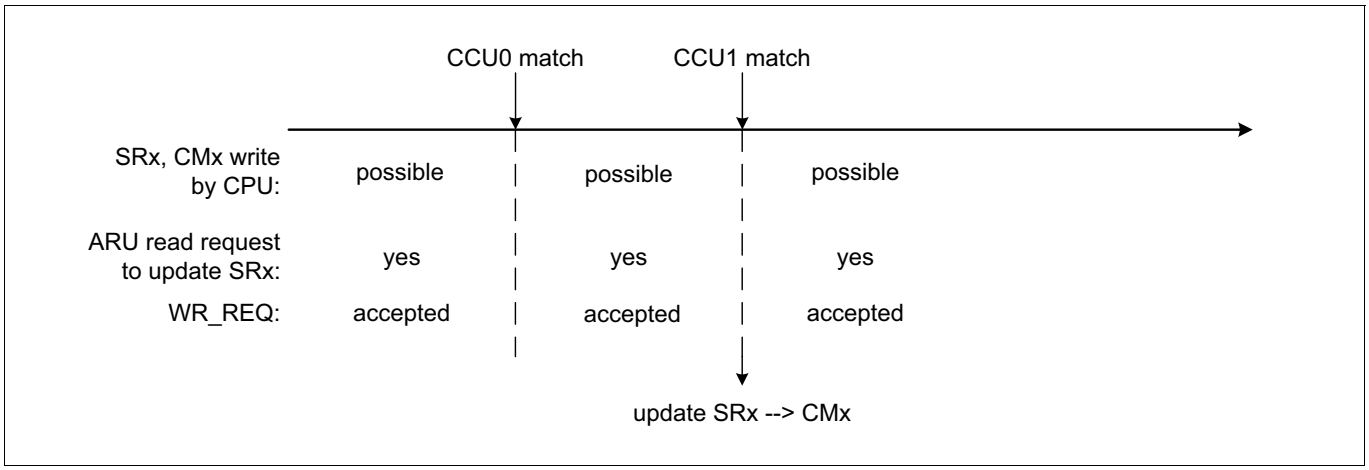


Figure 92 CPU access rights in case of compare strategy 'serve last' in case of EUPM=1

ARU Non-blocking mode

If bit **ABM** in register **ATOM[i]_CH[x]_CTRL** is not set, the ARU blocking mode is disabled. In this case the ATOM channel is continuously reading via ARU and storing new values in the **SRx** register and the ACB shadow register **ACB_SR**.

If **ARU_EN** is not set, the bit **ABM** has no meaning.

ARU Blocking mode

If bit **ABM** in register **ATOM[i]_CH[x]_CTRL** is set, the ARU blocking mode is enabled. In this case the ATOM channel stops requesting new **SRx** values via ARU after reception of a new **SRx** value and restarts requesting a new value via ARU after compare match on both compare units (depending on compare strategy) followed by the immediate update of the **CMx** register with content of **SRx** register and an update of **ACBI** with the content of **ACB_SR**.

If **ARU_EN** is not set, the bit **ABM** has no meaning.

Late Update by CPU

Although, the ATOM channel may be controlled by data received via the ARU, the CPU is able to request at any time a late update of the compare register. This can be initiated by setting the **WR_REQ** bit inside the **ATOM[i]_CH[x]_CTRL** register.

If none of the two compare match event happened, the ATOM channel accepts the setting of **WR_REQ** bit. In this case, the ATOM will request no further data from ARU (if ARU access was enabled) and will disable the update of **CMx** register with the content of **SRx** register on a compare match event.

If at least one of the requested compare match events happened (depending on strategy) the **WR_REQ** bit is not set and the **WRF** flag in register **ATOM[i]_CH[x]_STAT** is set to indicate that the late update was not successful.

The channel will in any case continue to compare against the values stored inside the compare registers (if bit **DV** was set). The CPU can now update the compare values by writing to the shadow registers and force the ATOM channel to update the compare registers by writing to the force update register bits in the AGC register.

With a force update the **WR_REQ** bit is reset automatically and the ARU read request is set up again (if ARU access was enabled).

28.15.3.5.4 Register ATOM[i]_CH[x]_CTRL in SOMB mode

Register ATOM[i]_CH[x]_CTRL in SOMB mode

GTM_ATOMi_CHx_SOMB (i=0-11; x=0-7)

ATOMi Channel x Control Register in SOMB Mode ($E8004_H$ + i*800_H+ x*80_H) **Reset Value: 00000800_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FREEZE	SOMB	Not_used	Reserved	ABM	Not_used	Not_used	TRIGOUT	EXTTRIGOUT	Not_used		Not_used	Not_used		Not_used	WR_REQ
rw	rw	rw	r	rw	rw	rw	rw	rw	r		rw	rw		rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Not_used	Not_used			SL	EUPM	CMP_CTRL	ACB[4:2]			ACB[1:0]		ARU_EN	TB12_SEL	MODE	
rw	rw			rw	rw	rw	rw			rw		rw	rw	rw	

Field	Bits	Type	Description
MODE	1:0	rw	**ATOM channel mode select** Not used in ATOM SOMB mode.
TB12_SEL	2	rw	**Select time base value TBU_TS1 or TBU_TS2** 0_B *TBU_TS1* selected for comparison 1_B *TBU_TS2* selected for comparison Note: This bit is only applicable if three time bases are present in the GTM. Otherwise, this bit is reserved.
ARU_EN	3	rw	**ARU Input stream enable** 0_B ARU Input stream disabled 1_B ARU Input stream enabled
ACB[1:0]	5:4	rw	**Signal level control bits** 00_B No signal level change at output. 01_B Set output signal level to 1 when SL bit = 0 else output signal level to 0. 10_B Set output signal level to 0 when SL bit = 0 else output signal level to 1. 11_B Toggle output signal level. Note: These bits are only applicable if ARU_EN = 0.
ACB[4:2]	8:6	rw	**ATOM SOMB compare strategy** 000_B Reserved. Has no effect. 001_B Reserved. Has no effect. 010_B Compare in CCU0 only against *TBU_TS0*. 011_B Compare in CCU1 only against *TBU_TS1* or *TBU_TS2*. 100_B Compare first in CCU0 and then in CCU1. Use *TBU_TS0*. 101_B Compare first in CCU0 and then in CCU1. Use *TBU_TS1* or *TBU_TS2*. 110_B Compare first in CCU0 and then in CCU1. Use *TBU_TS0* in CCU0 and *TBU_TS1* or *TBU_TS2* in CCU1. 111_B Cancel pending comparisons independent on ARU_EN. Note: These bits are only applicable if ARU_EN = 0.

Field	Bits	Type	Description
CMP_CTRL	9	rw	**CCUx compare strategy select** 0_B Greater-equal compare against TBU time base values (TBU_TS1/2 >= CM0/1) 1_B Less-equal compare against TBU time base values (TBU_TS1/2 <= CM0/1) Note: The compare unit CCU0 or CCU1 that compares against TBU_TS0 (depending on CCUx control mode defined by ACB_CM(4:2)) always performs a greater-equal comparison, independent on CMP_CTRL bit.
EUPM	10	rw	**Extended update mode** 0_B No extended update of CM0 and CM1 via CPU or ARU 1_B Extended update mode in case of compare strategy 'serve last': update of CM1 after CCU0 compare match possible via ARU or CPU. Note: If EUPM=1 write access to CM0 or CM1 never causes an AEI write status 0b10. Note: This bit is only applicable in SOMC and SOMB mode.
SL	11	rw	**Initial signal level after channel enable** 0_B Low signal level 1_B High signal level Note: Reset value depends on the hardware configuration chosen by silicon vendor. Note: If the output is disabled, the output ATOM_OUT[x] is set to inverse value of SL. If FREEZE=0, the following notes is valid: If the channel is disabled, the output register of SOU unit is set to value of SL. If FREEZE=1, the following note is valid: If the channel is disabled, the output register of SOU unit is not changed and output ATOM_OUT[x] is not changed.
Not_used	14:12	rw	**Not used** Note: Not used in this mode.
Not_used	15	rw	**Not used** Note: Not used in this mode.
WR_REQ	16	rw	**CPU Write request bit for late compare register update** 0_B No late update requested by CPU 1_B Late update requested by CPU Note: The CPU can disable subsequent ARU read requests by the channel and can update the shadow registers with new compare values, while the compare units operate on old compare values received by former ARU accesses, if occurred. Note: On a compare match event, the WR_REQ bit will be reset by hardware. Note: At the point of the force update only the shadow registers SR0 and SR1 are transferred into the CM0, CM1 registers. The output action is still defined by the ACBI bit field described by the ARU together with the old compare values for CM0/CM1.
Not_used	17	rw	**Not used** Note: Not used in this mode.

Field	Bits	Type	Description
Not_used	19:18	rw	**Not used** Note: Not used in this mode.
Not_used	20	rw	**Not used** Note: Not used in this mode.
Not_used	22:21	r	**Not used** Note: Not used in this mode.
EXTTRIGOUT	23	rw	**TIM_EXT_CAPTURE(x) as potential output signal TRIG_[x]** 0_B signal *TRIG_[x-1]* is selected as output on *TRIG_[x]* (if TRIGOUT=0) 1_B signal *TIM_EXT_CAPTURE(x)* is selected as output on *TRIG_[x]* (if TRIGOUT=0)
TRIGOUT	24	rw	**Trigger output selection (output signal TRIG_CHx) of module ATOM_CHx** 0_B *TRIG_[x]* is *TRIG_[x-1]* or TIM_*EXT_CAPTURE(x)*. 1_B *TRIG_[x]* is *TRIG_CCU0*
Not_used	25	rw	**Not used** Note: Not used in this mode.
Not_used	26	rw	**Not used** Note: Not used in this mode.
ABM	27	rw	**ARU blocking mode** 0_B ARU blocking mode disabled: ATOM reads continuously from ARU and updates SR0, SR1 and ACB bits independent of pending compare match event 1_B ARU blocking mode enabled: after updating SR0,SR1 and ACB bits via ARU, no new data is read via ARU until compare match event occurred.
Reserved	28	r	**Reserved** Read as zero, should be written as zero.
Not_used	29	rw	**Not used** Note: Not used in this mode.
SOMB	30	rw	**SOMB: SOMB mode** 0_B ATOM channel mode defined by bit filed MODE 1_B ATOM SOMB mode enabled
FREEZE	31	rw	**FREEZE** 0_B a channel disable/enable may change internal register and output register 1_B a channel enable/disable does not change an internal or output register but stops counter CN0 (in SOMP mode), comparison (in SOMC/SOMB mode) and shifting (in SOMS mode)

28.15.4 ATOM Interrupt Signals

Table 59 ATOM Interrupt Signals

Signal	Description
CCU0TCx_IRQ	CCU0 Trigger condition interrupt for channel x
CCU1TCx_IRQ	CCU1 Trigger condition interrupt for channel x

28.15.5 ATOM Register Overview

Table 60 ATOM Register Overview

Register name	Description	see Page
ATOM[i]_AGC_GLB_CTRL	ATOMi AGC global control register	297
ATOM[i]_AGC_ENDIS_CTRL	ATOMi AGC enable/disable control register	298
ATOM[i]_AGC_ENDIS_STAT	ATOMi AGC enable/disable status register	299
ATOM[i]_AGC_ACT_TB	ATOMi AGC action time base register	300
ATOM[i]_AGC_OUTEN_CTRL	ATOMi AGC output enable control register	301
ATOM[i]_AGC_OUTEN_STAT	ATOMi AGC output enable status register	301
ATOM[i]_AGC_FUPD_CTRL	ATOMi AGC force update control register	302
ATOM[i]_AGC_INT_TRIG	ATOMi AGC internal trigger control register	303
ATOM[i]_CH[x]_CTRL	ATOMi channel x control register	304
	ATOMi channel x control register in SOMI mode	248
	ATOMi channel x control register in SOMC mode	265
	ATOMi channel x control register in SOMP mode	279
	ATOMi channel x control register in SOMS mode	286
	ATOMi channel x control register in SOMB mode	293
ATOM[i]_CH[x]_STAT	ATOMi channel x status register	309
ATOM[i]_CH[x]_RDADDR	ATOMi channel x ARU read address register	311
ATOM[i]_CH[x]_CN0	ATOMi channel x CCU0 counter register	311
ATOM[i]_CH[x]_CM0	ATOMi channel x CCU0 compare register	312
ATOM[i]_CH[x]_SR0	ATOMi channel x CCU0 compare shadow register	312
ATOM[i]_CH[x]_CM1	ATOMi channel x CCU1 compare register	313
ATOM[i]_CH[x]_SR1	ATOMi channel x CCU1 compare shadow register	314
ATOM[i]_CH[x]_IRQ_NOTIFY	ATOMi channel x interrupt notification register	314
ATOM[i]_CH[x]_IRQ_EN	ATOMi channel x interrupt enable register	315
ATOM[i]_CH[x]_IRQ_FORCINT	ATOMi channel x software interrupt generation	316
ATOM[i]_CH[x]_IRQ_MODE	ATOMi channel x interrupt mode configuration register	316

28.15.6 ATOM Register Description

28.15.6.1 Register ATOM[i]_AGC_GLB_CTRL

ATOMi AGC Global Control Register

ATOMi_AGC_GLB_CTRL (i=0-11)
ATOMi AGC Global Control Register **($0E8040_H$+i*800_H)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
UPEN_CTRL7		UPEN_CTRL6		UPEN_CTRL5		UPEN_CTRL4		UPEN_CTRL3		UPEN_CTRL2		UPEN_CTRL1		UPEN_CTRL0	
rw		rw		rw		rw		rw		rw		rw		rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RST_CH7	RST_CH6	RST_CH5	RST_CH4	RST_CH3	RST_CH2	RST_CH1	RST_CH0	0							HOST_TRIG
w	w	w	w	w	w	w	w	r							w

Field	Bits	Type	Description
HOST_TRIG	0	w	**Trigger request signal (see AGC) to update the register ENDIS_STAT and OUTEN_STAT** Note: this flag is reset automatically after triggering the update 0_B No trigger request 1_B Set trigger request
RST_CHx (x=0-7)	x+8	w	**Software reset of channel x** *Note: This bit is cleared automatically after write by CPU. The channel registers are set to their reset values and channel operation is stopped immediately. The output register of SOU unit is reset to inverse reset value of SL bit.* 0_B No action 1_B Reset channel
UPEN_CTRLx (x=0-7)	2*x+17:2*x+16	rw	**ATOM channel x enable update of register CM0, CM1 and CLK_SRC from SR0, SR1 and CLK_SRC_SR** Write / Read: 00_B Don't care, bits 1:0 will not be change / update disabled 01_B Disable update / -- 10_B Enable update / -- 11_B Don't care, bits 1:0 will not be changed / update enabled
0	7:1	r	**Reserved** Read as zero, shall be written as zero.

28.15.6.2 Register ATOM[i]_AGC_ENDIS_CTRL

ATOMi AGC Enable/Disable Control Register

ATOMi_AGC_ENDIS_CTRL (i=0-11)

ATOMi AGC Enable/Disable Control Register($0E8044_H$+i*800_H) **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENDIS_CTRL7		ENDIS_CTRL6		ENDIS_CTRL5		ENDIS_CTRL4		ENDIS_CTRL3		ENDIS_CTRL2		ENDIS_CTRL1		ENDIS_CTRL0	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
ENDIS_CTRLx (x=0-7)	2*x+1:2*x	rw	**ATOM channel x enable/disable update value** If FREEZE=0 and an ATOM channel is disabled, the counter **CN0** is stopped and the output register of SOU unit is set to the inverse value of control bit SL. On an enable event, the counter **CN0** starts counting from its current value. If FREEZE=1 and an ATOM channel is disabled, the counter CN0 is stopped (SOMP, SOMS mode) and each comparison is stopped (SOMC, SOMB mode). On an enable event, the counter CN0 starts counting from its current value or a comparison is restarted. Write of following double bit values is possible: *Note: If the output is disabled (OUTEN[x]=0), the ATOM channel x output ATOM_OUT[x] is the inverted value of bit SL.* 00_B Don't care, bits 1:0 of register ENDIS_STAT will not be changed on an update trigger 01_B Disable channel on an update trigger 10_B Enable channel on an update trigger 11_B Don't change bits 1:0 of this register
0	31:16	r	**Reserved** Read as zero, shall be written as zero.

28.15.6.3 Register ATOM[i]_AGC_ENDIS_STAT

ATOMi AGC Enable/Disable Status Register

ATOMi_AGC_ENDIS_STAT (i=0-11)

ATOMi AGC Enable/Disable Status Register ($0E8048_H$+i*800_H) **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENDIS_STAT7		ENDIS_STAT6		ENDIS_STAT5		ENDIS_STAT4		ENDIS_STAT3		ENDIS_STAT2		ENDIS_STAT1		ENDIS_STAT0	
rw		rw		rw		rw		rw		rw		rw		rw	

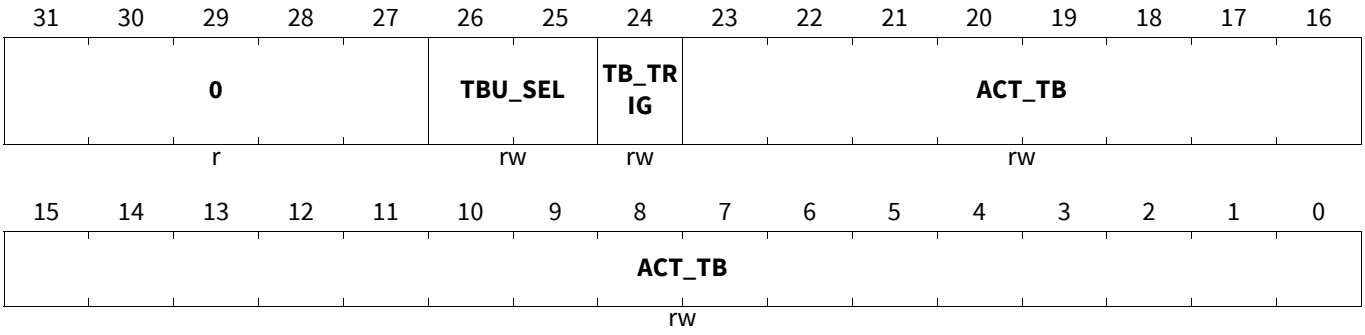
Field	Bits	Type	Description
ENDIS_STATx (x=0-7)	2*x+1:2*x	rw	**ATOM channel x enable/disable** If FREEZE=0 and an ATOM channel is disabled, the counter CN0 is stopped and the output register of SOU unit is set to the inverse value of control bit SL. On an enable event, the counter CN0 starts counting from its current value. If FREEZE=1 and an ATOM channel is disabled, the counter CN0 is stopped (SOMP, SOMS mode) and each comparison is stopped (SOMC, SOMB mode). On an enable event, the counter CN0 starts counting from its current value or a comparison is restarted. 00_B Write: Don't care bits, will not be changed; Read: Output disabled. 01_B Write: Disable channel on an update trigger; Read: Unused 10_B Write: Enable channel on an update trigger; Read: Unused 11_B Write: Don’t change bits 1:0 of this register; Read: Output enabled.
0	31:16	r	**Reserved** Read as zero, shall be written as zero.

28.15.6.4 Register ATOM[i]_AGC_ACT_TB

ATOMi AGC Action Time Base Register

ATOMi_AGC_ACT_TB (i=0-11)

ATOMi AGC Action Time Base Register **($0E804C_H$+i*800_H)** **Application Reset Value: 0000 0000_H**



Field	Bits	Type	Description
ACT_TB	23:0	rw	**Time base value** Specifies the signed compare value with selected signal TBU_TS[x], x=0..2. If selected TBU_TS[x] value is in the interval [ACT_TB-007FFFFFh,ACT_TB], the event is in the past, and the trigger is generated immediately. Otherwise, the event is in the future, and the trigger is generated if selected TBU_TS[x] is equal to ACT_TB.
TB_TRIG	24	rw	**Set trigger request** Note: This flag is reset automatically if the selected time base unit (*TBU_TS0*or *TBU_TS1*or *TBU_TS2,*if present) has reached the value **ACT_TB**, and the update of the register was triggered. 0_B No trigger request 1_B Set trigger request
TBU_SEL	26:25	rw	**Selection of time base used for comparison** *Note: The bit combination 0b10 is only applicable if the TBU of the device contains three time base channels. Otherwise, this bit combination is also reserved. Please refer to GTM Architecture block diagram on page 3 to determine the number of channels for TBU of this device.* 00_B TBU_TS0 selected 01_B TBU_TS1 selected 10_B TBU_TS2 selected 11_B Same as 0b00
0	31:27	r	**Reserved** Read as zero, shall be written as zero.

28.15.6.5 Register ATOM[i]_AGC_OUTEN_CTRL

ATOMi AGC Output Enable Control Register

ATOMi_AGC_OUTEN_CTRL (i=0-11)

ATOMi AGC Output Enable Control Register($0E8050_H$+i*800_H) **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTEN_CTRL 7		OUTEN_CTRL 6		OUTEN_CTRL 5		OUTEN_CTRL 4		OUTEN_CTRL 3		OUTEN_CTRL 2		OUTEN_CTRL 1		OUTEN_CTRL 0	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
OUTEN_CTRL x (x=0-7)	2*x+1:2*x	rw	**Output ATOM_OUTx enable/disable update value** Write of following double bit values is possible: *Note: If the channel is disabled (ENDIS[0]=0) or the output is disabled (OUTEN[0]=0), the TOM channel 0 output ATOM_OUT[0] is the inverted value of bit SL.* 00_B Don't care, bits 1:0 of register OUTEN_STAT will not be changed on an update trigger 01_B Disable channel output on an update trigger 10_B Enable channel output on an update trigger 11_B Don't change bits 1:0 of this register
0	31:16	r	**Reserved** Read as zero, shall be written as zero.

28.15.6.6 Register ATOM[i]_AGC_OUTEN_STAT

ATOMi AGC Output Enable Status Register

ATOMi_AGC_OUTEN_STAT (i=0-11)

ATOMi AGC Output Enable Status Register ($0E8054_H$+i*800_H) **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUTEN_STAT 7		OUTEN_STAT 6		OUTEN_STAT 5		OUTEN_STAT 4		OUTEN_STAT 3		OUTEN_STAT 2		OUTEN_STAT 1		OUTEN_STAT 0	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
OUTEN_STATx (x=0-7)	2*x+1:2*x	rw	**Control/status of output ATOM_OUTx** Write / Read : 00_B Don't care, bits 1:0 will not be changed / output disabled 01_B Disable output / -- 10_B Enable output / -- 11_B Don't care, bits 1:0 will not be changed / output enabled
0	31:16	r	**Reserved** Read as zero, shall be written as zero.

28.15.6.7 Register ATOM[i]_AGC_FUPD_CTRL

ATOMi AGC Force Update Control Register

ATOMi_AGC_FUPD_CTRL (i=0-11)

ATOMi AGC Force Update Control Register ($0E8058_H$+i*800_H) **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSTCN0_CH7		RSTCN0_CH6		RSTCN0_CH5		RSTCN0_CH4		RSTCN0_CH3		RSTCN0_CH2		RSTCN0_CH1		RSTCN0_CH0	
rw		rw		rw		rw		rw		rw		rw		rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FUPD_CTRL7		FUPD_CTRL6		FUPD_CTRL5		FUPD_CTRL4		FUPD_CTRL3		FUPD_CTRL2		FUPD_CTRL1		FUPD_CTRL0	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
FUPD_CTRLx (x=0-7)	2*x+1:2*x	rw	**Force update of ATOM channel x operation registers** If enabled, force update of register CM0, CM1 and CLK_SRC triggered by HOST_TRIG, ACT_TB compare match, or internal trigger. Write / Read : *Note: In SOMP mode, the force update request is stored and executed synchronized to the selected CMU_CLK. In all other modes, the force update request is executed immediately.* *Note: In SOMP mode, in case of ECLK_SRC=1 and CLK_SRC_SR = 0b011/0b100/0b101/0b110 a force update leads to an immediate update of CM0, CM1 and CLK_SRC.* 00_B Don't care, bits 1:0 will not be changed / force update disabled 01_B Disable force update / -- 10_B Enable force update / -- 11_B Don't care, bits 1:0 will not be changed / force update enabled

Field	Bits	Type	Description
RSTCN0_CHx (x=0-7)	2*x+17:2*x +16	rw	**Reset CN0 of channel x on force update event** If enabled, reset CN0 triggered by HOST_TRIG, ACT_TB compare match, or internal trigger. Write / Read : 00_B Don't care, bits 1:0 will not be changed / CN0 is not reset on forced update 01_B Do not reset CN0 on forced update / -- 10_B Reset CN0 on forced update / -- 11_B Don't care, bits 1:0 will not be changed / CN0 is reset on forced update

28.15.6.8 Register ATOM[i]_AGC_INT_TRIG

ATOMi AGC Internal Trigger Control Register

ATOMi_AGC_INT_TRIG (i=0-11)

ATOMi AGC Internal Trigger Control Register(0E805C$_H$+i*800$_H$) **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT_TRIG7		INT_TRIG6		INT_TRIG5		INT_TRIG4		INT_TRIG3		INT_TRIG2		INT_TRIG1		INT_TRIG0	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
INT_TRIGx (x=0-7)	2*x+1:2*x	rw	**Select input signal TRIG_x as a trigger source** Write / Read : 00_B Don't care, bits 1:0 will not be changed / internal trigger from channel 0 (TRIG_0) not used 01_B Do not use internal trigger from channel 0 (TRIG_0) / -- 10_B Use internal trigger from channel 0 (TRIG_0) / -- 11_B Don't care, bits 1:0 will not be changed / internal trigger from channel 0 (TRIG_0) used
0	31:16	r	**Reserved** Read as zero, shall be written as zero.

28.15.6.9 Register ATOM[i]_CH[x]_CTRL

ATOMi Channel x Control Register

ATOMi_CHx_CTRL (i=0-11;x=0-7)

ATOMi Channel x Control Register **($0E8004_H$+i*800_H+x*80_H)** **Application Reset Value: 0000 0800_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FREEZE	SOMB	EXT_FUPD	0	ABM	OSM	SLA	TRIGOUT	EXTTRIGOUT	EXT_TRIG	OSM_TRIG	RST_CCU0	UDMODE		TRIG_PULSE	WR_REQ
rw	rw	rw	r	rw	rw	rw	rw	rw	rw	rw	rw	rw		rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECLK_SRC	CLK_SRC_SR			SL	EUPM	CMP_CTRL	ACB					ARU_EN	TB12_SEL	MODE	
rw	rw			rw	rw	rw	rw					rw	rw	rw	

Field	Bits	Type	Description
MODE	1:0	rw	**ATOM channel mode select** 00_B ATOM Signal Output Mode Immediate (SOMI) 01_B ATOM Signal Output Mode Compare (SOMC) 10_B ATOM Signal Output Mode PWM (SOMP) 11_B ATOM Signal Output Mode Serial (SOMS)
TB12_SEL	2	rw	**Select time base value TBU_TS1 or TBU_TS2** *Note: This bit is only applicable in SOMC mode.* 0_B TBU_TS1 selected for comparison 1_B TBU_TS2 selected for comparison
ARU_EN	3	rw	**ARU input stream enable** 0_B ARU Input stream disabled 1_B ARU Input stream enabled
ACB	8:4	rw	**ATOM Mode control bits** These bits have different meaning in the different ATOM channel modes. Please refer to the mode description sections. SOMI : **Section 28.15.3.1** and **Register ATOM[i]_CH[x]_CTRL in SOMI mode** for register description. SOMC : **Section 28.15.3.2** and **Register ATOM[i]_CH[x]_CTRL in SOMC mode** for register description. SOMP : **Section 28.15.3.3** and **Register ATOM[i]_CH[x]_CTRL in SOMP mode** for register description. SOMS : **Section 28.15.3.4** and **Register ATOM[i]_CH[x]_CTRL in SOMS mode** for register description. SOMB : **Section 28.15.3.5** and **Register ATOM[i]_CH[x]_CTRL in SOMB mode** for register description.

Field	Bits	Type	Description
CMP_CTRL	9	rw	**CCUx compare strategy select** *Note: This bit is only applicable in SOMC mode.* 0_B Greater-equal compare against TBU time base values (TBU_TSx greater than or equal to CMx) 1_B Less-equal compare against TBU time base values (TBU_TSx less than or equal to CMx)
EUPM	10	rw	**Extended update mode** *Note: If EUPM=1, a write access to CM0 or CM1 never causes an AEI write status 10_B.* *Note: This bit is only applicable in SOMC and SOMB mode.* 0_B No extended update of CM0 and CM1 via CPU or ARU 1_B Extended update mode in case of compare strategy 'serve last': update of CM1 after CCU0 compare match possible via ARU or CPU.
SL	11	rw	**Initial signal level** *Note: Reset value depends on the hardware configuration chosen by silicon vendor.* *Note: If the output is disabled, the output ATOM_OUT[x] is set to inverse SL, independent of the ATOM channel mode.* If FREEZE=0, following notes are valid: In SOMP, SOMI, SOMS mode, if the channel is disabled, the internal register SOUR inside ATOM sub-unit SOU is set to inverse value of SL. By enabling the channel, the register SOUR is not changed. Thus, if the output is enabled afterwards, the output ATOM_OUT[x] is the inverse value of SL. In SOMC mode, if the channel is disabled, the internal register SOUR inside ATOM sub-unit SOU is set to value of SL. By enabling the channel, the register SOUR is not changed. Thus, if the output is enabled and the channel is disabled, the output ATOM_OUT[x] is the value of SL. If FREEZE=1, the following notes are valid: If the channel is disabled, the output register of SOU unit is not changed, and output ATOM_OUT[x] is not changed. 0_B Low signal level 1_B High signal level

Field	Bits	Type	Description
CLK_SRC_SR	14:12	rw	**Actual CMU clock source (SOMS)/ shadow register for CMU clock source (SOMP)** If ECLK_SRC=0 / ECLK_SRC=1: *Note: This register is a shadow register for the register CLK_SRC. Thus, if the CMU_CLK source for PWM generation should be changed during operation, the old CMU_CLK has to operate until the update of the ATOM channels internal CLK_SRC register by the CLK_SRC_SR content is done, either by an end of a period or a forced update.* *Note: After (channel) reset, the selected CLK_SRC value is the SYS_CLK (input of Global Clock Divider). To use in SOMP mode one of the CMU_CLKx, it is recommended to perform a forced update of CLK_SRC with the value of CLK_SRC_SR value before/with enabling the channel.* *Note: In case of ECLK_SRC=1 and CLK_SRC_SR = 011_B/100_B/101_B/110_B, a force update leads to an immediate update of CM0, CM1 and CLK_SRC.* 000_B CMU_CLK0 selected / CMU_CLK0 selected 001_B CMU_CLK1 selected / CMU_CLK1 selected 010_B CMU_CLK2 selected / CMU_CLK2 selected 011_B CMU_CLK3 selected / reserved 100_B CMU_CLK4 selected / clock stopped 101_B CMU_CLK5 selected / TRIG[x-1] selected 110_B CMU_CLK6 selected / TIM_EXT_CAPTURE[x] selected 111_B CMU_CLK7 selected / CMU_CLK7 selected
ECLK_SRC	15	rw	**Extend CLK_SRC** *Note: This bit is only applicable in SOMP and SOMS mode.* See bit CLK_SRC_SR description for details. 0_B CLK_SRC_SR set 1 selected 1_B CLK_SRC_SR set 2 selected
WR_REQ	16	rw	**CPU Write request bit for late compare register update** *Note: The CPU can disable subsequent ARU read requests by the channel and can update the shadow registers with new compare values, while the compare units operate on old compare values received by former ARU accesses, if occurred.* *Note: On a compare match event, the WR_REQ bit will be reset by hardware.* *Note: At the point of the force update, only the shadow registers SR0 and SR1 are transferred into the CM0, CM1 registers. The output action is still defined by the ACBI bit field described by the ARU together with the old compare values for CM0/CM1.* *Note: This bit is only applicable in SOMC and SOMB mode.* 0_B No late update requested by CPU 1_B Late update requested by CPU

Field	Bits	Type	Description
TRIG_PULSE	17	rw	**Trigger output pulse length of one SYS_CLK period** 0_B Output on TOM[i]_OUT[x]_T is '1' as long as CN0=SR0 (if SR=_TRIG=1) 1_B Output on TOM[i]_OUT[x]_T is '1' for only one SYS_CLK period if CN0=SR0 (if SR=_TRIG=1)
UDMODE	19:18	rw	**Up/down counter mode** *Note: This mode is only applicable in SOMP mode.* 00_B Up/down counter mode disabled: CN0 counts always up 01_B Up/down counter mode enabled: CN0 counts up and down, CM0,CM1 are updated if CN0 reaches 0 (i.e. changes from down to up) 10_B Up/down counter mode enabled: CN0 counts up and down, CM0,CM1 are updated if CN0 reaches CM0 (i.e. changes from up to down) 11_B Up/down counter mode enabled: CN0 counts up and down, CM0,CM1 are updated if CN0 reaches 0 or CM0 (i.e. changes direction)
RST_CCU0	20	rw	**Reset source of CCU0** *Note: If RST_CCU0=1 and UPEN_CTRLx=1 are set, TRIG_[x-1] or TIM_EXT_CAPTURE(x) triggers also the update of work register (CM0, CM1 and CLK_SRC).* *Note: This bit is only applicable in SOMP mode.* *Note: This bit should only be set if bit OSM=0 (i.e. in continuous mode).* 0_B Reset counter register CN0 to 0 on matching comparison with CM0 1_B Reset counter register CN0 to 0 on trigger TRIG_[x-1] or TIM_EXT_CAPTURE(x)
OSM_TRIG	21	rw	**Enable trigger of one-shot pulse by trigger signal OSM_TRIG** *Note: This bit should only be set if bit OSM=1 and bit RST_CCU0=0.* 0_B Signal OSM_TRIG cannot trigger start of single pulse generation 1_B Signal OSM_TRIG can trigger start of single pulse generation (only if bit OSM = 1)
EXT_TRIG	22	rw	**Select TIM_EXT_CAPTURE(x) as trigger signal** 0_B Signal TRIG_[x-1] is selected as trigger to reset CN0 or to start single pulse generation 1_B Signal TIM_EXT_CAPTURE(x) is selected
EXTTRIGOUT	23	rw	**Select TIM_EXT_CAPTURE(x) as potential output signal TRIG_[x]** 0_B Signal TRIG_[x-1] is selected as output on TRIG_[x] (if TRIGOUT=0) 1_B Signal TIM_EXT_CAPTURE(x) is selected as output on TRIG_[x] (if TRIGOUT=0)

Field	Bits	Type	Description
TRIGOUT	24	rw	**Trigger output selection (output signal TRIG_CHx) of module ATOM_CHx** 0_B TRIG_[x] is TRIG_[x-1] or TIM _EXT_CAPTURE(x) 1_B TRIG_[x] is TRIG_CCU0
SLA	25	rw	**Serve last ARU communication strategy** *Note: This bit is only applicable in SOMC mode.* *Note: Please note, that setting of this bit has only effect, when ACBI(4:2) is configured for serve last compare strategy (100_B, 101_B, or 110_B).* *Note: When this bit is not set, the captured time stamps in the shadow registers SRx are only provided after the CCU1 match occurred. The ACBO(4:3) bits always return 10_B in that case.* *Note: By setting this bit, the ATOM channel also provides the captured time stamps after the CCU0 match event to the ARU. The ACBO(4:3) bits are set to 01_B in that case. After the CCU1 match event, the time stamps are captured again in the SRx registers and provided to the ARU. The ACBO(4:3) bits are set to 10_B. When the data in the shadow registers after the CCU0 match was not consumed by an ARU destination and the CCU1 match occurs, the data in the shadow registers is overwritten by the new captured time stamps. The ATOM channel does not request new data from the ARU when the CCU0 match values are read from an ARU destination.* 0_B Capture SRx time stamps after CCU0 match event not provided to ARU 1_B Capture SRx time stamps after CCU0 match event provided to ARU
OSM	26	rw	**One-shot mode** *Note: This bit is only applicable in SOMP and SOMS modes.* 0_B Continuous PWM generation after channel enable 1_B A single pulse is generated
ABM	27	rw	**ARU blocking mode** *Note: This bit is only applicable in SOMC and SOMB mode.* 0_B ARU blocking mode disabled: ATOM reads continuously from ARU and updates CM0, CM1 and ACB bits in case of SOMC mode, or SR0, SR1 and ACB bits in case of SOMB mode, independent of pending compare match event 1_B ARU blocking mode enabled: After update of CM0, CM1 and ACB bit in case of SOMC mode, or SR0, SR1 and ACB bits in case of SOMB mode via ARU, no new data is read via ARU until compare match event occurred, and in case of SOMC mode, SR0 and/or SR1 are read

Field	Bits	Type	Description
EXT_FUPD	29	rw	**External forced update** *Note: This bit is only applicable in SOMP and SOMS mode.* 0_B Use FUPD(x) signal from AGC to force update 1_B Use TIM_EXT_CAPTURE signal to force update
SOMB	30	rw	**SOMB mode** 0_B ATOM channel mode defined by bit field MODE 1_B ATOM SOMB mode enabled
FREEZE	31	rw	**FREEZE** *Note: if channel is disabled and ouptut is enabled, in SOMP mode with UDMODE!=0b00 the output is dependng directly on SL bit, independent on FREEZE mode.* 0_B A channel disable/enable may change internal register and output register 1_B A channel enable/disable does not change an internal or output register but stops counter CN0 (in SOMP mode), comparison (in SOMC/SOMB mode) and shifting (in SOMS mode)
0	28	r	**Reserved** Read as zero, shall be written as zero.

28.15.6.10Register ATOM[i]_CH[x]_STAT

ATOMi Channel x Status Register

ATOMi_CHx_STAT (i=0-11;x=0-7)
ATOMi Channel x Status Register **($0E801C_H$+i*800_H+x*80_H)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0			**ACBO**					**DR**	**WRF**	**DV**	**ACBI**				
r			r					r	rw	r	r				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0															**OL**
r															r

Field	Bits	Type	Description
OL	0	r	**Actual output signal level of ATOM_CHx_OUT** *Note: Reset value is the inverted value of bit SL, which depends on the hardware configuration chosen by silicon vendor.* 0_B Actual output signal level is low 1_B Actual output signal level is high

Field	Bits	Type	Description
ACBI	20:16	r	**ATOM Mode control bits** *Note: For ATOM SOMI, SOMC, SOMP and SOMS mode, this register serves as a mirror for the five ARU control bits received through the ARU interface. The bits are valid when the DV bit is set.* *Note: For SOMB mode, this bit field serves as the work register of the compare strategy. It can be updated with the value of bit field ACB of register ATOM[i]_CH[x]_CTRL, or the value of internal shadow register ACB_SR.*
DV	21	r	**Valid ARU Data stored in compare registers** *Note: This bit is only applicable in SOMC and SOMB mode. The CPU can determine the status of the ARU transfers with this bit. After the compare event occurred, the bit is reset by hardware.* 0_B No valid data stored in register CM0 and/or CM1, no comparison is activated 1_B Valid data stored in CM0 and/or CM1, comparison activated
WRF	22	rw	**Write request of CPU failed for late update** *Note: This bit is only applicable in SOMC and SOMB mode.* Bit WRF can be reset by writing a 1 to it. 0_B Late update was successful, CCUx units wait for comparison 1_B Late update failed
DR	23	r	**ARU data rejected flag** *Note: The flag is cleared if valid data is received and stored via ARU.* 0_B Received ARU data stored 1_B Received ARU data rejected
ACBO	28:24	r	**ATOM Internal status bits** ACBO[3] = 1: CCU0 Compare match occurred. ACBO[4] = 1: CCU1 Compare match occurred. *Note: These bits are only set in SOMC mode.* *Note: ACBO is reset to 0b00000 on an update of register CM0 or CM1 (via ARU or CPU).* *Note: In SOMC mode, these bits are sent as ARU control bits 52..48.*
0	15:1, 31:29	r	**Reserved** Read as zero, shall be written as zero.

28.15.6.11Register ATOM[i]_CH[x]_RDADDR

ATOMi Channel x ARU read address Register

ATOMi_CHx_RDADDR (i=0-11;x=0-7)

ATOMi Channel x ARU read address Register($0E8000_H$+i*800_H+x*80_H) Application Reset Value: 01FE $01FE_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0							RDADDR1								
r							rw								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							RDADDR0								
r							rw								

Field	Bits	Type	Description
RDADDR0	8:0	rw	**ARU Read address 0** *Note: This read address is used by the ATOM channel to receive data from ARU immediately after the channel and ARU access is enabled (see ATOM[i]_CH[x]_CTRL register for details).* *Note: This bit field is only writable if channel is disabled.*
RDADDR1	24:16	rw	**ARU Read address 1** *Note: The ATOM channel switches to this read address, when requested in the ARU control bits 52 to 48 with the pattern "111--". The channel switches back to the RDADDR0 after one ARU data package was received on RDADDR1 and the compare match event is occurred.* *Note: This read address is only applicable in SOMC mode.* *Note: This bit field is only writable if channel is disabled.*
0	15:9, 31:25	r	**Reserved** Read as zero, shall be written as zero.

28.15.6.12Register ATOM[i]_CH[x]_CN0

ATOMi Channel x CCU0 Counter Register

ATOMi_CHx_CN0 (i=0-11;x=0-7)

ATOMi Channel x CCU0 Counter Register($0E8018_H$+i*800_H+x*80_H) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								CN0							
r								rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CN0															
rw															

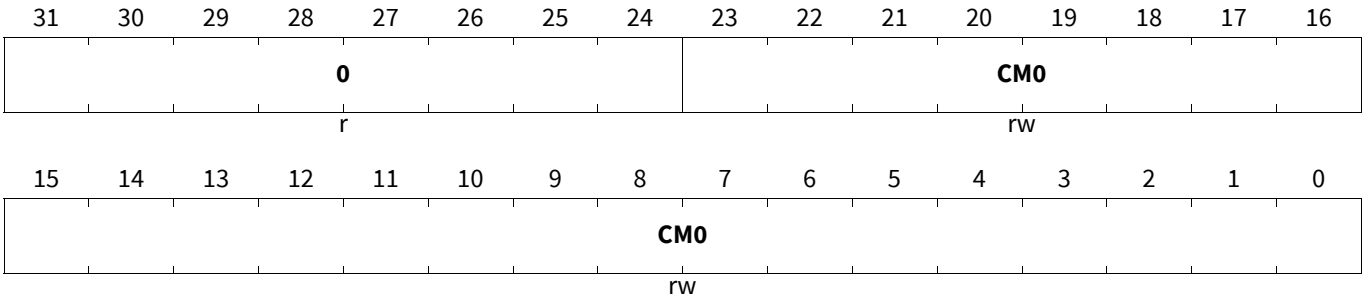
Field	Bits	Type	Description
CN0	23:0	rw	**ATOM CCU0 counter register**
0	31:24	r	**Reserved** Read as zero, shall be written as zero.

28.15.6.13Register ATOM[i]_CH[x]_CM0

ATOMi Channel x CCU0 Compare Register

Note: This register is write protected in SOMC mode and returns AEI_STATUS=0b10 on write access, when in serve last compare strategy the first match of CCU0 occurred.

ATOMi_CHx_CM0 (i=0-11;x=0-7)
ATOMi Channel x CCU0 Compare Register($0E8010_H$+i*800_H+x*80_H) Application Reset Value: 0000 0000_H

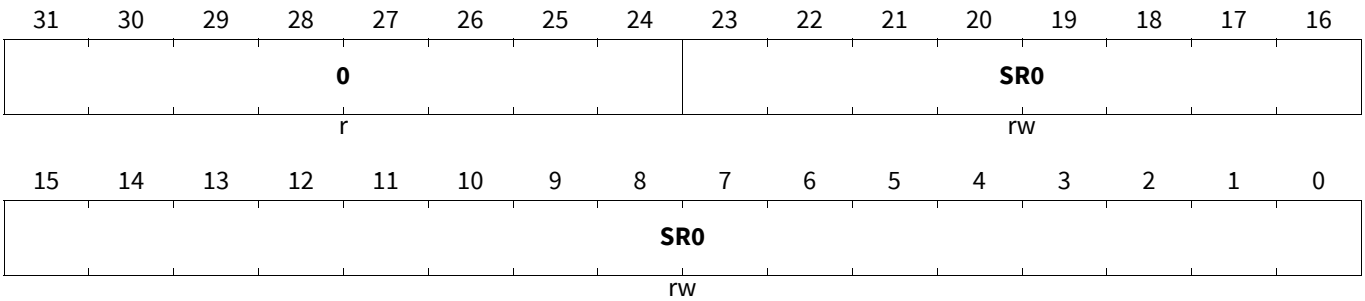


Field	Bits	Type	Description
CM0	23:0	rw	**ATOM CCU0 compare register**
0	31:24	r	**Reserved** Read as zero, shall be written as zero.

28.15.6.14Register ATOM[i]_CH[x]_SR0

ATOMi Channel x CCU0 Compare Shadow Register

ATOMi_CHx_SR0 (i=0-11;x=0-7)
ATOMi Channel x CCU0 Compare Shadow Register($0E8008_H$+i*800_H+x*80_H) Application Reset Value: 0000 0000_H



Field	Bits	Type	Description
SR0	23:0	rw	**ATOM channel x shadow register SR0** *Note: The SR0 register is used as shadow register for CM0 in SOMP and SOMS modes, and is used as capture register for time base TBU_TS0 in SOMC mode.*
0	31:24	r	**Reserved** Read as zero, shall be written as zero.

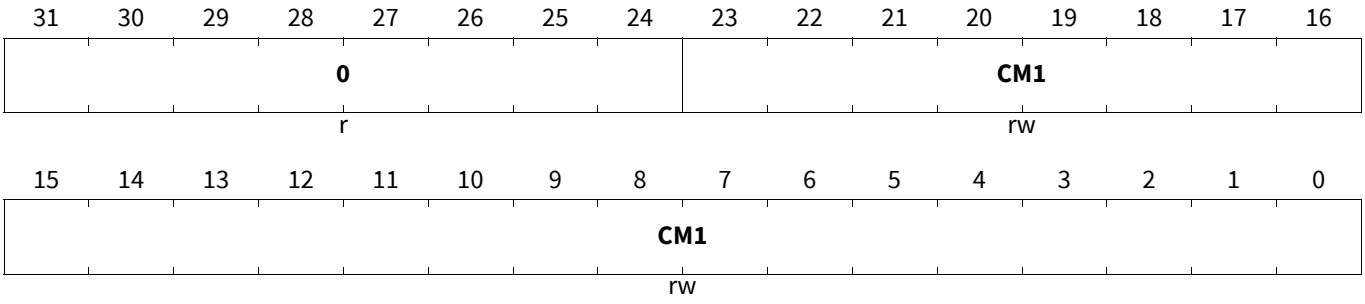
28.15.6.15Register ATOM[i]_CH[x]_CM1

ATOMi Channel x CCU1 Compare Register

Note: This register is write protected in SOMC mode and returns AEI_STATUS=0b10 on write access, when in serve last compare strategy the first match of CCU0 occurred.

ATOMi_CHx_CM1 (i=0-11;x=0-7)

ATOMi Channel x CCU1 Compare Register($0E8014_H$+i*800_H+x*80_H) **Application Reset Value: $0000\ 0000_H$**

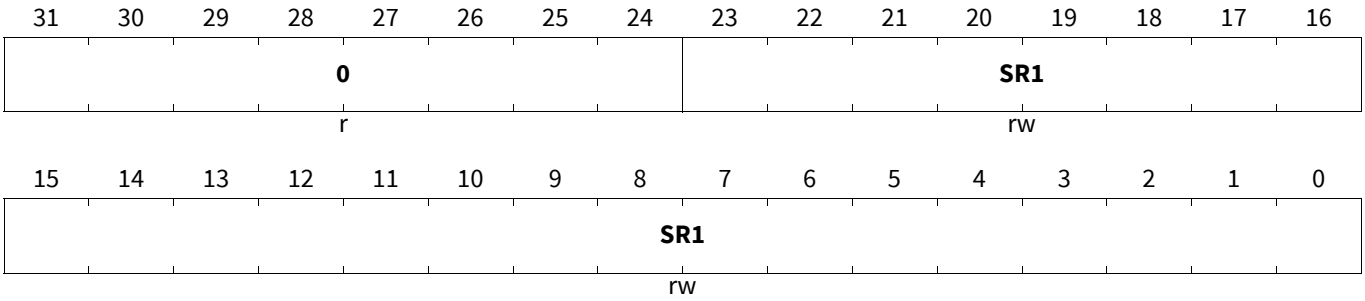


Field	Bits	Type	Description
CM1	23:0	rw	**ATOM CCU1 compare register**
0	31:24	r	**Reserved** Read as zero, shall be written as zero.

28.15.6.16Register ATOM[i]_CH[x]_SR1

ATOMi Channel x CCU1 Compare Shadow Register

ATOMi_CHx_SR1 (i=0-11;x=0-7)
ATOMi Channel x CCU1 Compare Shadow Register($0E800C_H$+i*800_H+x*80_H) Application Reset Value: 0000 0000_H

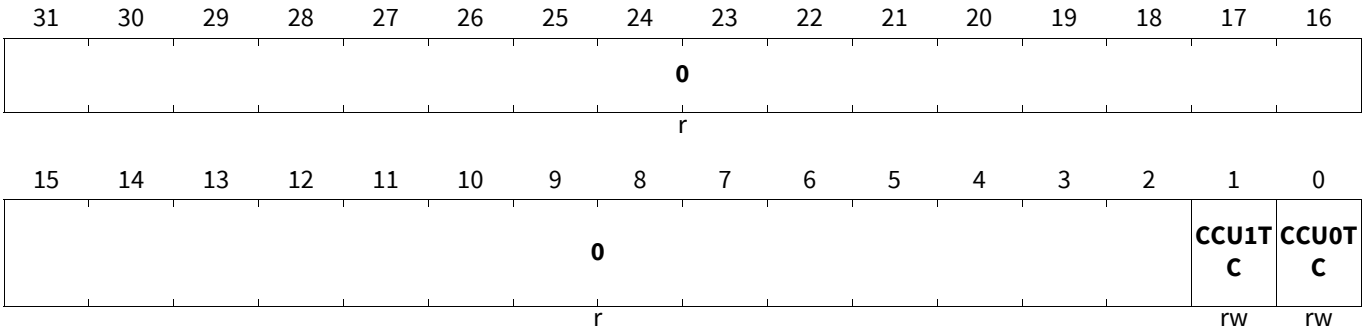


Field	Bits	Type	Description
SR1	23:0	rw	**ATOM channel x shadow register SR1** *Note: The SR1 register is used as shadow register for CM1 in SOMP and SOMS modes, and is used as capture register for time base TBU_TS1 or TBU_TS2 (when selected in ATOM[i]_CH[x]_CTRL register) in SOMC mode.*
0	31:24	r	**Reserved** Read as zero, shall be written as zero.

28.15.6.17Register ATOM[i]_CH[x]_IRQ_NOTIFY

ATOMi Channel x Interrupt Notification Register

ATOMi_CHx_IRQ_NOTIFY (i=0-11;x=0-7)
ATOMi Channel x Interrupt Notification Register($0E8020_H$+i*800_H+x*80_H) Application Reset Value: 0000 0000_H

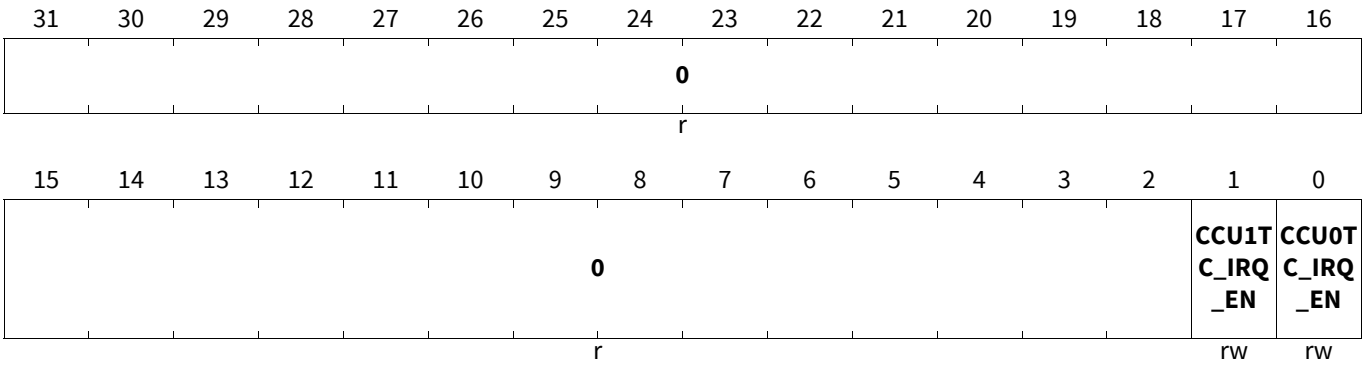


Field	Bits	Type	Description
CCU0TC	0	rw	**CCU0 Trigger condition interrupt for channel x** The notification of the interrupt is only triggered one time after reaching the condition CN0 >= CM0. To enable re-trigger of the notification, first the condition CN0 < CM1 has to be reached. *Note: This bit will be cleared on a CPU write access of value 1. A read access leaves the bit unchanged.* 0_B No interrupt occurred 1_B CCU0 Trigger condition interrupt was raised by ATOM channel x
CCU1TC	1	rw	**CCU1TC: CCU1 Trigger condition interrupt for channel x** The notification of the interrupt is only triggered one time after reaching the condition CN0 >= CM1. To enable re-trigger of the notification, first the condition CN0 < CM1 has to be reached. *Note: This bit will be cleared on a CPU write access of value 1. A read access leaves the bit unchanged.* *Note: If bit SR0_TRIG is set to 1 (only valid in SOMP mode), this interrupt notify flag is set in case of SR0 is equal to CN0 and not set in case of CM1 >=/<= CN0.*
0	31:2	r	**Reserved** Read as zero, shall be written as zero.

28.15.6.18Register ATOM[i]_CH[x]_IRQ_EN

ATOMi Channel x Interrupt Enable Register

ATOMi_CHx_IRQ_EN (i=0-11;x=0-7)
ATOMi Channel x Interrupt Enable Register($0E8024_H$+i*800_H+x*80_H) Application Reset Value: 0000 0000_H

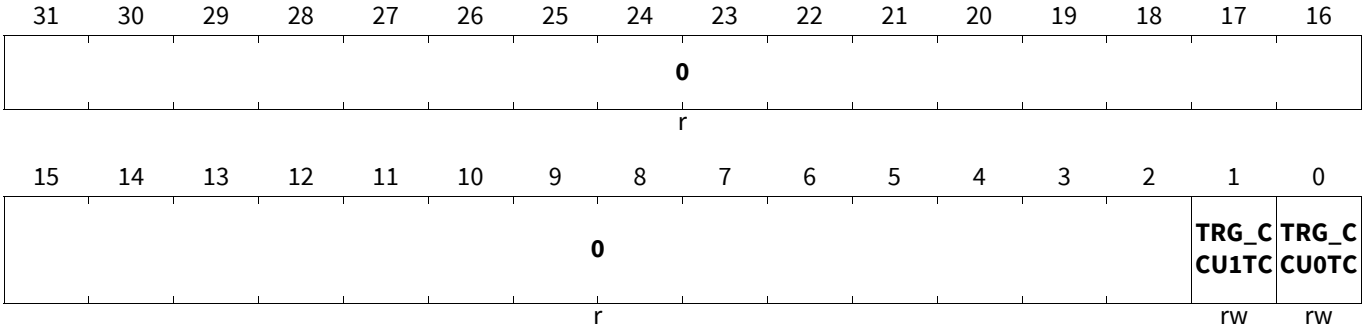


Field	Bits	Type	Description
CCU0TC_IRQ_EN	0	rw	**ATOM_CCU0TC_IRQ interrupt enable** 0_B Disable interrupt, interrupt is not visible outside GTM 1_B Enable interrupt, interrupt is visible outside GTM
CCU1TC_IRQ_EN	1	rw	**ATOM_CCU1TC_IRQ interrupt enable** See bit 0.
0	31:2	r	**Reserved** Read as zero, shall be written as zero.

28.15.6.19Register ATOM[i]_CH[x]_IRQ_FORCINT

ATOMi Channel x Software Interrupt Generation Register

ATOMi_CHx_IRQ_FORCINT (i=0-11;x=0-7)
ATOMi Channel x Software Interrupt Generation Register($0E8028_H$+i*800_H+x*80_H) Application Reset Value: $0000\ 0000_H$

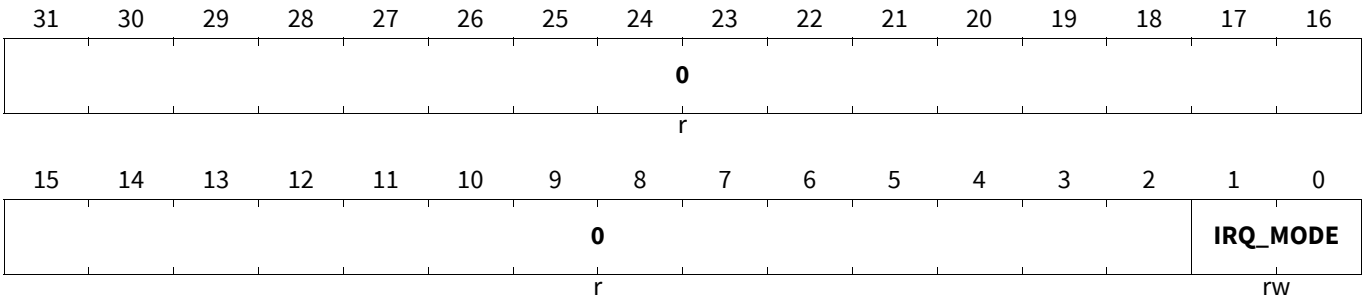


Field	Bits	Type	Description
TRG_CCU0TC	0	rw	**Trigger ATOM_CCU0TC_IRQ interrupt by software** *Note: This bit is cleared automatically after write.* *Note: This bit is write protected by bit RF_PROT of register GTM_CTRL* 0_B No interrupt triggering 1_B Assert CCU0TC_IRQ interrupt for one clock cycle
TRG_CCU1TC	1	rw	**Trigger ATOM_CCU1TC_IRQ interrupt by software** *Note: This bit is cleared automatically after write.* *Note: This bit is write protected by bit RF_PROT of register GTM_CTRL* 0_B No interrupt triggering 1_B Assert CCU1TC_IRQ interrupt for one clock cycle
0	31:2	r	**Reserved** Read as zero, shall be written as zero.

28.15.6.20Register ATOM[i]_CH[x]_IRQ_MODE

ATOMi Channel x Interrupt Mode Configuration Register

ATOMi_CHx_IRQ_MODE (i=0-11;x=0-7)
ATOMi Channel x Interrupt Mode Configuration Register($0E802C_H$+i*800_H+x*80_H) Application Reset Value: $0000\ 0000_H$



Field	Bits	Type	Description
IRQ_MODE	1:0	rw	**IRQ mode selection** *Note: The interrupt modes are described in **Section 28.4.5**.* 00_B Level mode 01_B Pulse mode 10_B Pulse-Notify mode 11_B Single-Pulse mode
0	31:2	r	**Reserved** Read as zero, shall be written as zero