Description

The HSSL module generates all necessary protocol formats in order to enable two devices to communicate to each other. Two basic modes are supported.
In register transfer mode the transmitter (“sending device”) provides an address and a data value by writing them into dedicated registers of the HSSL module. The HSSL module puts it into an envelop (called frame) and forwards it via physical layer to the target device. The target takes the information out of the frame and writes the received data into the address which came in the same frame as the data. If the sender wants to read the content of a register or a memory location, it simply sends only the address. The target device reads the value from the specified location and replies it to the sender by transferring it through an answer frame, which has a format of it’s own.

The transfer of register / memory contents is protected by several security levels. A 16 bit CRC value (called CRC16) is attached to the end of each frame. Each transfer process triggers a watchdog, which makes sure that the communication happens within a deterministic schedule. The target device itself offers the capability to define access windows, which allow reading or writing only from / into certain address ranges.

Each frame must be acknowledged by the target by sending an appropriate response frame. If the response frame does not come inside a predefined time window, the initiator module triggers a timeout interrupt.

In data stream mode data blocks of user defined size can moved from the memory of the sending device into the memory of the target device. A DMA master, which can be configured with any source address and source length, autonomously fetches data, breaks it into smaller blocks of programmable size, and puts it into a FIFO. The lower level companion module of the HSSL module empties the FIFO from the “other side” to the physical lines, which connect two devices. In the target device receives a structure, which is inverse to the sender system, the data blocks, puts them into a FIFO, which is in turn emptied by a DMA master into the target memory.

All streaming data transfers are subject to the protection features which are available for the register transfer mode.

After module reset, most registers are only released for read for remote access. They have to be unlocked by the local SW.

In order to ensure consistent initialization of the communication channel there is a possibility to determine the feature set of the module by using the JTAG ID of the device, which uniquely identifies the available HW options of the module. ASIC versions of the HSSL interface may only employ stripped down instances.

35.2 Overview

The following section gives an overview of the lower communication layers of the HSSL protocol.

35.2.1 Lower Communication Layers (HSCT, PLL, Pads)

The lower layer companion module and logic control the lower communication layers positioned between two devices, the data and the physical layer. They consist of High Speed Communication Tunnel (HSCT) module, a corresponding PLL and pads. For more information on the lower communication layers, see the HSCT chapter.

The chip to chip interface employs a digital interface for inter chip communication between a master IC and a slave IC. The interface is capable of running in a master or in a slave mode. During configuration phase the role of the Interface (master or slave) has to be defined. It is not intended to change the system role during an application.

The interface consists of a full-duplex RX and TX high-speed data interface based on double ended differential signals (in total 4 lines) and a master clock interface (SYS_CLK). The master IC owns the crystal and provides the clock to the slave. The interface reset is derived from the System reset and provided by chip internal reset signaling.

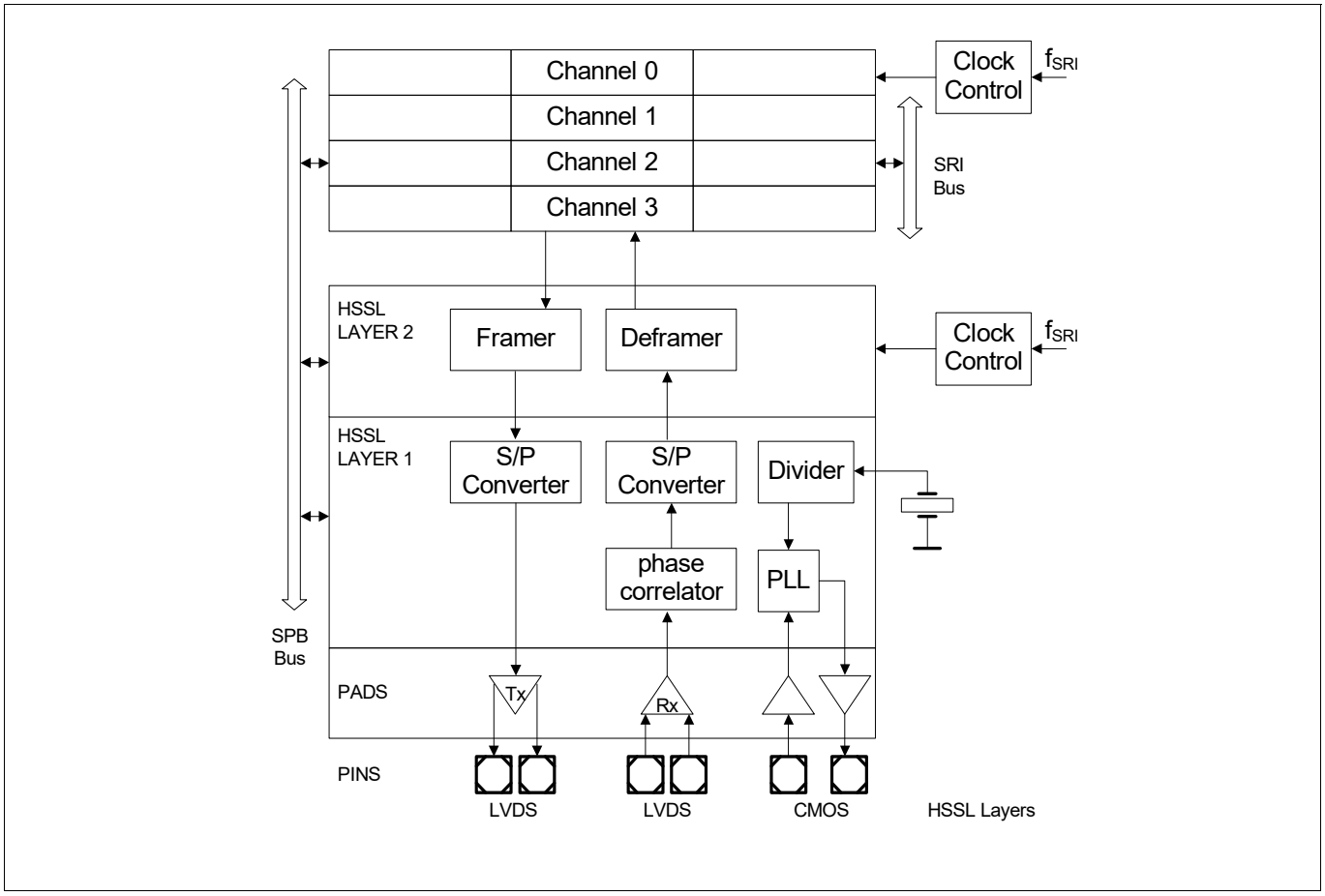

Figure 356 Physical Layer

Features:

- Transmission of symbol information from the master IC to the slave IC
- Receive symbol information sent from the slave IC to the master IC
- System Clock provided by the master IC (crystal owner) to the slave IC
- Exchange of control information in both directions
- Clear To Send indication in both directions
- Unsolicited status in both directions
- Regular data transfer in both directions based on data channels
- Master IC data transfer speed 5 MBaud and 320 MBaud
- Three slave IC data transfer speeds available based on 20 MHz SYS_Clk:
  5 MBaud (low speed)
  20 MBaud (medium speed)
  320 MBaud (high speed)
- Two slave IC data transfer speeds available based on 10 MHz SYS_Clk (lower EMI):
  5 MBaud (low speed)
  320 MBaud (high speed)
- The interface is based on IEEE 1596.3 LVDS input-output pads
- To reduce the voltage swing a configuration option is available