28.8 AEI to FIFO Data Interface (AFD)

28.8.1 Overview

The AFD sub-module implements a data interface between the AEI bus and the FIFO sub-module, which consists of eight logical FIFO channels.

The AFD sub-module provides one buffer registers that are dedicated to the logical channels of the FIFO. Access to the corresponding FIFO channel is given by reading or writing this buffer registers **AFD[i]_CH[x]_BUF_ACC**.

An AEI write access to the buffer register where the corresponding FIFO channel is full will be ignored. The data will be lost.

An AEI read access to the buffer register where the corresponding FIFO channel is empty will be served with zero data.

28.8.2 AFD Register overview

Table 23 AFD Register overview

Register Name	Description	see Page
AFD[i]_CH[z]_BUF_ACC	AFD i FIFO z buffer access register	95

28.8.3 AFD Register description

28.8.3.1 Register AFD[i]_CH[z]_BUF_ACC

AFD i FIFO x Buffer Access Register

AFDi_CHx_BUF_ACC (i=0-2;x=0-7)

AFD i FIFO x Buffer Access Register **(018080_H+i*4000_H+x*10_H)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0			DATA												
r			rw												

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA															
rw															

Field	Bits	Type	Description
DATA	28:0	rw	**Read/write data from/to FIFO**
0	31:29	r	**Reserved** Read as zero, shall be written as zero.