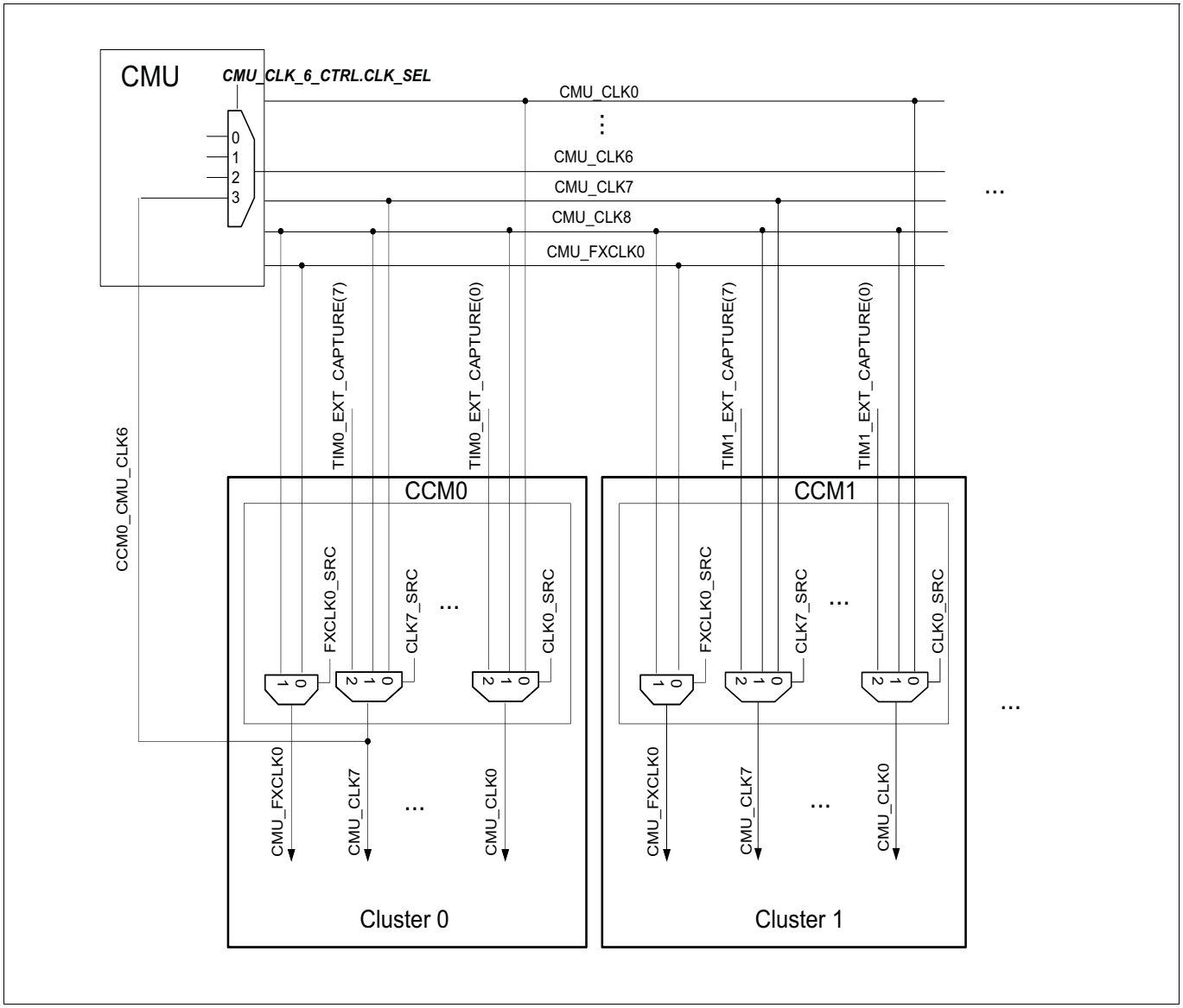

Figure 29 Cluster Clock Signal Wiring

The register **CCM[i]_AEIM_STA** captures the address and the reason of the first invalid AEIM bus master access of the cluster's MCS module.

The registers **CCM[i]_HW_CONF**, **CCM[i]_AUX_IN_SRC**, **CCM[i]_EXT_CAP_EN**, **CCM[i]_TOM_OUT**, and **CCM[i]_ATOM_OUT** are global status and configuration registers that are mirrored from the group of TOP-Level registers. The intention of these registers is to bring up cluster specific configuration registers into the address space of the bus master of the cluster's MCS module.

28.11.2 Address Range Protection

The CCM also provides up to NARP so called address range protectors (ARPs), where the number NARP depends on the actual device configuration (defined in device specific appendix). An ARP can be used to define a configurable write protected address range in order to support enhanced safety features. The address width of and ARP is also device dependent and it is determined by the parameter AAW as defined in device specific appendix.

The protected address range is mapped to the address range of the cluster's MCS RAM port.

Each ARP z (with z = 0…NARP-1) can be configured by the registers **CCM[i]_ARP[z]_CTRL** and **CCM[i]_ARP[z]_PROT**, where the register **CCM[i]_ARP[z]_CTRL** enables to configure the size and base address offset for an ARP and the register **CCM[i]_ARP[z]_PROT** configures, that an MCS channel x with a set bit field **WPROTx** cannot write to the corresponding z-th ARP. Whenever an MCS channel x is writing to an ARP that does not allow a write access from channel x by the configuration register **CCM[i]_ARP[z]_PROT**, the write access is discard. The bit field **WPROT_AEI** of register **CCM[i]_ARP[z]_CTRL** allows to configure if a CPU write access (via AEI slave interface) to the z-th ARP is protected. If the CPU wants to write to the z-th ARP while **WPROT_AEI** is set, the write access will be discard and the AEI status signal will signalize an invalid module access.

Considering the size and base address of an ARP, it should be noted that the configuration possibilities are limited. Details about the configuration can be found in the register description of **MCS[i]_ARP[z]_CTRL**.

The bit field **DIS_PROT** of register **CCM[i]_ARP[z]_CTRL** changes the meaning of an ARP configuration in a way that it explicitly allows an MCS channel x with a set bit field **WPROTx** to write to the z-th ARP. Accordingly, if the bit **DIS_PROT** is set while the bit **WPROT_AEI** is also set in the register **CCM[i]_ARP[z]_CTRL**, the z-th ARP explicitly allows a write access from the CPU to the z-th ARP. A meaningful application of an ARP z with a set bit field **DIS_PROT** for an MCS channel x has another ARP with a surrounding wider address range that is defining a write protection for MCS channel x and some other MCS channels.

Since the address range of an ARP can surround another ARP it is possible to configure contradictory conditions for MCS channels or the CPU within the overlapping area (e.g. if ARP y surrounds ARP z and ARP y allows a write access for an MCS channel x but ARP z prohibits a write access for MCS channel x). In order to resolve this ambiguity, the following rule is defined: A write protection for a specific address c concerning MCS channel x (the CPU) is active, if and only if, address c is covered by at least one ARP with a cleared bit **DIS_PROT** and a set bit **WPROTx** (**WPROT_AEI**) and there exists no ARP covering address c with a set bit field **DIS_PROT** and a set bit field **WPROTx** (**WPROT_AEI**).