33.14 Summary of Registers and Locations

The EDSADC is built from a series of channels that are controlled in an identical way. This makes programming versatile and scalable. The corresponding registers, therefore, have an individual offset assigned (see **Table 294**). The exact register location is obtained by adding the respective register offset to the base address (see product-specific appendix) of the corresponding channel.

Due to the regular structure, several registers appear within each channel. This is indicated in the register overview table by formulas.

Registers with write access mode "...,M" can additionally be protected from unintended write access by setting the corresponding protection bit in register ACCPROT. Refer to **"Register Access Control" on Page 14** for more details and an association table.

Table 294 Register Overview - EDSADC (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
CLC	Clock Control Register	0000_H	U,SV	SV,E,P	Application Reset	9
ID	Module Identification Register	0008_H	U,SV	BE	PowerOn Reset	7
OCS	OCDS Control and Status Register	0028_H	U,SV	SV,P,OEN	See page 9	9
KRSTCLR	Kernel Reset Status Clear Register	$002C_H$	U,SV	SV,E,P	Application Reset	13
KRST1	Kernel Reset Register 1	0030_H	U,SV	SV,E,P	Application Reset	13
KRST0	Kernel Reset Register 0	0034_H	U,SV	SV,E,P	Application Reset	12
ACCEN0	Access Enable Register 0	$003C_H$	U,SV	SV,SE	Application Reset	11
GLOBCFG	Global Configuration Register	0080_H	U,SV	U,SV,P,M	Application Reset	16
GLOBRC	Global Run Control Register	0088_H	U,SV	U,SV,P,M	Application Reset	17
ACCPROT	Access Protection Register	0090_H	U,SV	SV,SE,P	Application Reset	14
CGCFG	Carrier Generator Configuration Register	$00A0_H$	U,SV	U,SV,P,M	Application Reset	88
EVFLAG	Event Flag Register	$00E0_H$	U,SV	U,SV,P,M	Application Reset	83
EVFLAGCLR	Event Flag Clear Register	$00E4_H$	U,SV	U,SV,P,M	Application Reset	84
MODCFGx	Modulator Configuration Register x	0100_H+x *100_H	U,SV	U,SV,P,M	Application Reset	27
DICFGx	Demodulator Input Config. Register x	0108_H+x *100_H	U,SV	U,SV,P,M	Application Reset	30

Table 294 Register Overview - EDSADC (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
FCFGMx	Filter Configuration Register x, Main	0110_H+x *100_H	U,SV	U,SV,P,M	Application Reset	63
FCFGCx	Filter Configuration Register x, CIC Filter	0114_H+x *100_H	U,SV	U,SV,P,M	Application Reset	65
FCNTCx	Filter Counter Register x, CIC Filter	0118_H+x *100_H	U,SV	BE	Application Reset	66
OVSCFGx	Overshoot Compensation Cfg. Register x	$011C_H$+x *100_H	U,SV	U,SV,P,M	Application Reset	49
IWCTRx	Integration Window Control Register x	0120_H+x *100_H	U,SV	U,SV,P,M	Application Reset	57
IIVALx	Intermediate Integration Value	0124_H+x *100_H	U,SV	BE	Application Reset	59
ISTATx	Integrator Status Register x	0128_H+x *100_H	U,SV	BE	Application Reset	59
RFCx	Result FIFO Control Register x	$012C_H$+x *100_H	U,SV	U,SV,P,M	Application Reset	74
RESMx	Result Register x Main	0130_H+x *100_H	U,SV	BE	Application Reset	75
OFFCOMPx	Offset Compensation Register x	0138_H+x *100_H	U,SV	U,SV,P,M	Application Reset	54
GAINCALx	Gain Calibration Register x	$013C_H$+x *100_H	U,SV	U,SV,P,M	Application Reset	38
GAINCTRx	Gain Control Register x	0140_H+x *100_H	U,SV	U,SV,P,M	Application Reset	38
GAINCORRx	Gain Correction Register x	0144_H+x *100_H	U,SV	U,SV,P,M	Application Reset	47
TSTMPx	Time-Stamp Register x	0150_H+x *100_H	U,SV	BE	Application Reset	69
TSCNTx	Time-Stamp Counter x	0154_H+x *100_H	U,SV	U,SV,P,M	Application Reset	70
FCFGAx	Auxiliary Filter Configuration Register x	0170_H+x *100_H	U,SV	U,SV,P,M	Application Reset	68
BOUNDSELx	Boundary Select Register x	0178_H+x *100_H	U,SV	U,SV,P,M	Application Reset	80
RESAx	Result Register x Auxiliary	0180_H+x *100_H	U,SV	BE	Application Reset	67
CGSYNCx	Carrier Generator Synchronization Reg. x	$01A0_H$+x *100_H	U,SV	U,SV,P,M	Application Reset	90

Table 294 Register Overview - EDSADC (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
RECTCFGx	Rectification Configuration Register x	$01A8_H$+x *100_H	U,SV	U,SV,P,M	Application Reset	92
VCMx	Common Mode Voltage Register x	$01B0_H$+x *100_H	U,SV	U,SV,P,M	Application Reset	34