33.13 Application Considerations

The operation of the EDSADC and, hence, its behavior is programmable in a wide range. This makes it suitable for different applications while requiring a certain amount of initialization and/or handling during operation.

As far as possible the configuration options can be handled by initialization. Several functions, for example power control or calibration, have been automated so they require an absolute minimum of handling during operation.

Additional hints in section **"Changing the Configuration" on Page 7**.

33.13.1 Clock Synchronization

To eliminate the interference of concurrently operating ADC channels, the converters can operate in a synchronized way so each of them can reach its optimum performance. The Phase Synchronizer distributes a clock control signal which is used by the converters to generate a local clock signal. See **Section 33.4.1**.

After reset, the clock synchronization is active. Setting the Phase Synchronizer is mandatory for the EDSADC to deliver its documented performance.

33.13.2 Calibration Recommendation

The actual calibration algorithm is executed automatically by hardware, so only a few configurations need to be selected before starting the algorithm.

The automatic calibration algorithm is executed for gain factors of 1:1 and 1:2. If a factor of 1:4 is selected calibration is done for factor 1:2.

The optimum mode for offset calibration depends on the properties of the input signal. The high-pass filter can automatically remove the offset level of a differential input signal. For irregular input signals or for single-ended operation the filter must be disabled to receive an undisturbed signal.

Note: The calibration algorithm compensates manufacturing tolerances and adjusts the channel to the selected decimation rate. It is, therefore, recommended to execute the algorithm at least once after a reset.

Define the intended full-scale value for the calibration in bitfield CALTARGET in register **GAINCALx (x=0-13)** (default value 25 000). Trigger the calibration algorithm by setting bit CALIB in register **FCFGMx (x=0-13)**. The completion and status of the calibration algorithm is indicated by bitfield CAL in register **FCNTCx (x=0-13)**.

*Note: Set bit AUTOCAL in register **FCFGMx (x=0-13)** to enable automatically triggered calibration sequences.*

33.13.3 Examples for Operation

The digital filters provide a number of configuration options to control their operation. The automatic calibration algorithm normalizes the overall gain factor of the filter chain to 1.000, independent of their configuration. The full-scale value of the result is adapted to <CALTARGET> (25 000 after reset), representing the reference voltage.

Different full-scale values can be achieved by choosing a different value for CALTARGET (see **"Handling of Overload, Overdrive and Overflow Conditions" on Page 26**).

The usable passband is a fraction of the configured output data rate.
For passbands in the range of 10 … 100 kHz this fraction is 1/3rd,
for passbands in the range of 4 … <10 kHz this fraction is 1/6th.

The output data rate is determined by the modulator frequency divided by the total oversampling rate.

Example:
CIC filter active with oversampling rate of 64, FIR0/FIR1 active (both 2:1), integrator inactive, f_{MOD} = 26.67 MHz:
Total oversampling rate is 64 × 2 × 2 = 256, output data rate is 26.67 MHz/ 256 = 104.2 kHz.

33.13.4 Supported Operating Ranges

The EDSADC can be configured for various operating modes, depending on the application's requirements. The focus can be on the input impedance, on the power consumption, or on the signal-noise-ratio SNR.

The configured oversampling rate (or decimation rate) OSR defines the SNR within a wide range. The reachable SNR is limited by thermal noise within the on-chip modulator. The relation between OSR and SNR is, therefore, no more linear in the upper area.

The table below lists some properties of these operating modes. Shown SNR values are valid for the analog supply voltage range (VDDM) between 4.5 V and 5.5 V. For analog supply voltages higher than 2.97 V and lower than 4.5 V, the SNR values degrades by 6 dB.

Note: To achieve the passbands given in this table, both FIR filters must be enabled.

Table 292 Properties of Operating Ranges

Modulator Frequency f_{MOD}	Input Current I_{RMS} [1]	$f_{PB} \le 10$ kHz [2]		$f_{PB} \le 30$ kHz [3]		$f_{PB} \le 50$ kHz [3]		$f_{PB} \le 100$ kHz [3]	
		SNR [4]	OSR	SNR [4]	OSR	SNR [4]	OSR	SNR [4]	OSR
16 MHz (f_{ADC} / 10)	6 µA	≥78 dB	≥267	≥78 dB	≥178	≥74 dB	≥107	≥65 dB [5]	≥54
20 MHz (f_{ADC} / 8)	7.5 µA	≥80 dB	≥334	≥78 dB	≥223	≥74 dB	≥134	≥68 dB [5]	≥67
26.67 MHz (f_{ADC} / 6) [6]	10 µA	**≥80 dB**	≥445	**≥80 dB**	≥297	**≥78 dB**	≥178	**≥74 dB**	≥89
40 MHz (f_{ADC} / 4)	15 µA	≥80 dB	≥667	≥80 dB	≥445	≥78 dB	≥267	≥74 dB	≥134

1) These typical values refer to an input voltage of 5 V and the typical value of the switched capacitor: $I_{RMS} = 5\,V \times f_{MOD} \times 2 \times C_{SW}$. I_{RMS} defines the equivalent input impedance.
2) Passband = f_d / 6
3) Passband = f_d / 3
4) The reachable signal-noise-ratio is limited by thermal noise within the modulator.
5) With this configuration, the signal-noise-ratio is limited by quantization noise.
6) These OSRs reference the Datasheet values.

Note: Related to hardware characteristic for passband frequency ≤ 10 kHz the FIR1 has to be used with a decimation rate of 1:1.

The equivalent input impedance, which is seen by the external sensor, depends on the input current I_{RMS}. The input current is proportional to the effective switched input capacitance, which itself depends on the selected gain factor.

Table 293 Equivalent Input Impedance

Modulator Frequency	Input Current for Gain 1 / 2 / 4	Impedance for Gain factor = 1	Impedance for Gain factor = 2	Impedance for Gain factor = 4
16 MHz	6 µA / 12 µA / 24 µA	R_{IN} = 833 kΩ	R_{IN} = 416 kΩ	R_{IN} = 208 kΩ
20 MHz	7.5 µA / 15 µA / 30 µA	R_{IN} = 666 kΩ	R_{IN} = 333 kΩ	R_{IN} = 166 kΩ
26.67 MHz	10 µA / 20 µA / 40 µA	R_{IN} = 500 kΩ	R_{IN} = 250 kΩ	R_{IN} = 125 kΩ
40 MHz	15 µA / 30 µA / 60 µA	R_{IN} = 333 kΩ	R_{IN} = 166 kΩ	R_{IN} = 83 kΩ

Quasi-Differential Input Mode

When operating the EDSADC in single-ended mode, the smaller input voltage range reduces the achievable SNR by 6 dB. Quasi-differential input mode is realized by connecting the unused input line to the common mode voltage instead of to reference ground. This centers the result values around zero.

Using gain factor 2 doubles the result value range (-full-scale for input=ground, +full-scale for input=reference). In this case the achievable SNR is reduced by only 3 dB.

33.13.5 Basic Initialization Sequence

After reset, the EDSADC is disabled to minimize the initial power consumption. By executing the following steps the EDSADC can be prepared for operation and be started:

Enable and configure the phase synchronizer according to the overall system requirements.

This is described in section “Application Considerations” in chapter CONVCTRL.

Enable the EDSADC module and prepare it for operation

```
EDSADC_CLC      = 0x00000000 ;Enable module EDSADC
EDSADC_GLOBCFG  = 0x00000000 ;Use default: auto level, sync. operation, min. dithering
EDSADC_MODCFG0  = 0x80028000 ;Mod. frequency = 160 MHz / 8 = 20 MHz,
                             ;enable differential input on channel 0-A (example)
EDSADC_DICFG0   = 0x84000000 ;Single-word read mode, no timestamp, no FIFO
EDSADC_GAINCTR0= 0x061B1193  ;Calibrate with OSR 512, calibration factor 1.0984
EDSADC_GAINCORR0=0x0011126E  ;Set shifter for operation, operation factor 1.1519
EDSADC_FCFGC0   = 0x00310031 ;Select a data rate of 100 kHz (= 20 MHz / 200);200 =
50[CIC] * 4[FIR]
EDSADC_GLOBRC   = 0x00010001 ;Enable modulator and filter chain of channel 0 (example)
WAIT                         ;Pause for wakeup time (approx. 20 µs)
                             ;(other operations can be executed in the meantime)
EDSADC_FCFGM0   = 0x90038003 ;Enable service request and FIR filters,
                             ;start calibration
```

For applications where two or more DSADC channels have to provide synchronous results, all related channels shall be enabled synchronously using a single write access to register GLOBRC. To handle the EDSADC channel specific modulator settling time, the following sequence is proposed:

- Enable all modulators of the application specific synchronization group by a single write access to the corresponding MxRUN bits in the upper half-word of the Global Run Control Register:
  - GLOBRC = XXXX °°°°H, where XXXXH depends on the number of implemented modulators;
- Wait for modulator settling time tMSET (see Data Sheet);
- Enable all modulators and corresponding digital filter chains of the application specific synchronization group by a single write access to the corresponding MxRUN and CHxRUN bits in the Global Run Control Register:
  - GLOBRC = XXXX XXXXH, where XXXXH depends on the number of implemented modulators/demodulator channel

Retrieve Conversion Results

After the calibration has finished, the channel will begin to convert the input signal.Conversions results are indicated by service requests and can be read from RESM0.

33.13.6 Module Handling in Sleep Mode

The EDSADC does not change its operating mode in sleep mode. While sleep mode is evaluated (CLC.EDIS = 0, default after reset), the module clocks are stopped upon a sleep mode request. To achieve the power reduction that is usually intended during sleep mode, the application needs to disable the EDSADC, or parts of it as required, before entering sleep mode.

Note: If any activity is intended during sleep mode make sure that sleep mode requests are disregarded (CLC.EDIS = 1) and make sure the phase synchronizer is not disabled in this case.

33.13.7 Overlap of CH9 and CH12

In some products of the TC3XX family the inputs of channels CH9B and CH12A are connected to the same pair of pins. Both channels can be used to convert input signals from these pins. To avoid coupling effect from one channel to the other, it is recommended to enable only one input path at a given time.

Note: While CH12A is operating, CH9A may operate on another input.