If a data destination requests data from a data source over the ARU but the data source does not have any data yet, it has to wait until the data source provides new data. In this case the sub-module that owns the data destination may perform other tasks. When a data source produces new data faster than a data destination can consume the data the source raises an error interrupt and signals that the data could not be delivered in time. The new data is marked as valid for further transfers and the old data is overwritten.

In any case the round trip time for the ARU has a fixed reset value for a specific device configuration. The end value of the round-trip counter can be changed with a configuration register **ARU_CADDR_END** inside the ARU. For more details see the ARU specific chapter.

It is possible to reset the ARU round-trip counter **ARU_CADDR** manually synchronous to CMU clock enable from configuration register inside CMU module. Please refer to CMU specific chapter for more details.

One exception is the BRC sub-module when configured in Maximal Throughput Mode. Please refer to Broadcast Module chapter for a detailed description.

28.4.4 GTM Clock and Time Base Management (CTBM)

Inside the GTM several sub-units are involved in the clock and time base management of the whole GTM. **Section 28.4.4.1** shows the connections and sub blocks involved in these tasks. The sub blocks involved are called Clock and Time Base Management (CTBM) modules further on.

28.4.4.1 GTM Clock and time base management architecture

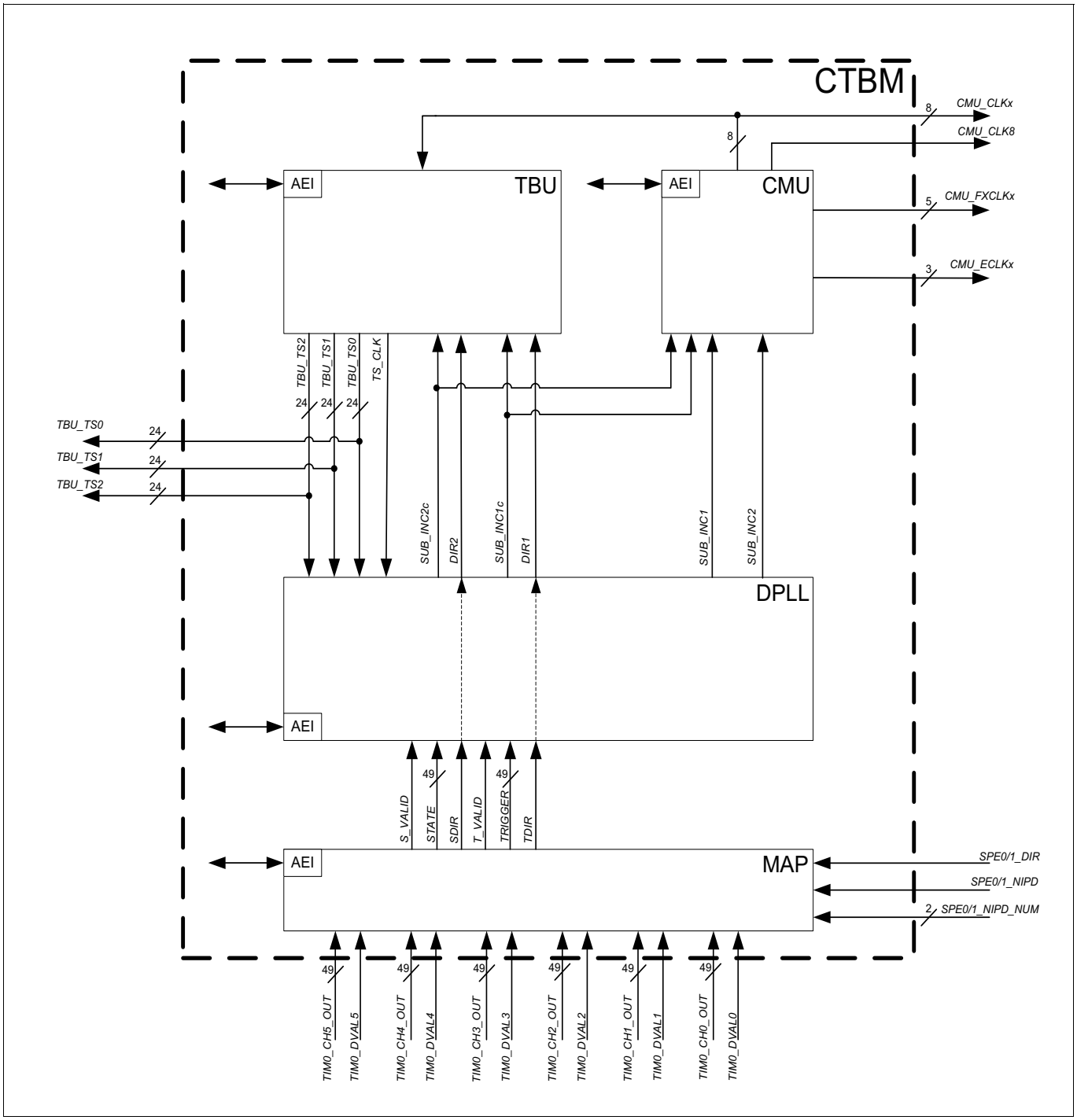

Figure 14 CTBM architecture

One important module of the CTBM is the Clock Management Unit (CMU) which generates up to 14 clocks for the sub-modules of the GTM and up to three GTM external clocks *CMU_ECLK[z]* (z: 0…2). For a detailed description of the CMU functionality and clocks please refer to Clock Management Unit chapter.

The five (5) *CMU_FXCLK[y]* (y: 0…4) clocks are used by the TOM sub-module for PWM generation.

A maximum of nine (9) *CMU_CLK[x]* (x: 0…8) clocks are used by other sub-modules of the GTM for signal generation.

Inside the Time Base Unit (TBU) one of *CMU_CLK[x]* (x: 0…7) clocks is used per channel to generate a common time base for the GTM. Besides the *CMU_CLK[x]* signals, the TBU can use the compensated *SUB_INC[i]c* (i: 1,2) signals coming from the DPLL sub-module for time base generation. This time base then typically represents an angle clock for an engine management system. For the meaning of compensated (*SUB_INC[i]c*) and uncompensated (*SUB_INC[i]*) DPLL signals please refer to the DPLL chapter. The *SUB_INC[i]c* signals in combination with the two direction signal lines *DIR[i]* the TBU time base can be controlled to run forwards or backwards. The TBU functionality is described in chapter “Time Base Unit (TBU)”.

The TBU sub-module generates the three time base signals *TBU_TS0*, *TBU_TS1* and *TBU_TS2* which are widely used inside the GTM as common time bases for signal characterization and generation.

Besides the time base 1 and 2 which may represent a relative angle clock for an engine management system it is helpful to have an absolute angle clock for CPU/MCS internal angle algorithm calculations. This absolute angle clock is represented by the TBU base 3. The TBU channel 0 up to 2 are widely used inside the GTM as common time (channel 0, 1 and/or 2) or angle (channel 1 and/or 2) bases for signal characterization and generation. The TBU channel 3 is only configurable and readable by MCS0 or CPU.

As stated before, the DPLL sub-module provides the four clock signals *SUB_INC[i]* and *SUB_INC[i]c* which can be seen as a clock multiplier generated out of the two input signal vectors *TRIGGER* and *STATE* coming from the MAP sub-module. For a detailed description of the DPLL functionality please refer to chapter “Digital PLL Module (DPLL)”.

The MAP sub-module is used to select the *TRIGGER* and *STATE* signals for the DPLL out of six input signals coming from TIM0 sub-module. Besides this, the MAP sub-module is able to generate a *TDIR* (TRIGGER Direction) and *SDIR* (STATE Direction) signal for the DPLL and TBU coming from the SPE0 and SPE1 signal lines. The direction signals are generated out of a defined input pattern. For a detailed description of the MAP sub-module please refer to chapter “TIM0 Input Mapping Module (MAP)”.

28.4.4.2 Cyclic Event Compare

With the time base module (TBU) the GTM provides three counters, where the counter of TBU_CH0 represents a time and the counter TBU_CH1 and TBU_CH2 may represent a time (if clock source is CMU_CLK generated inside CMU) or an angle (if clock source is a DPLL sub_inc signal provided via CMU).

From application point of view it is necessary to divide the cyclic event counter representing time or angle into two parts, the past and the future.The border of past/future is a moving border depending on current time or angle value.The cyclic event counting and the moving border of past/future is depicted in the figure below.