28.11 Cluster Configuration Module (CCM)

28.11.1 Overview

As already mentioned in the chapter “GTM architecture”, each submodule of the GTM is aligned explicitly to a cluster. The Cluster Configuration Module (CCM) enables the configuration of several cluster specific options namely

- cluster's clock frequency,
- module clock gating,
- Status observation of the cluster's MCS bus master (AEM),
- address range protection, and
- global architecture configuration.

The register **CCM[i]_CFG** allows disabling the system clock signal for unused sub modules of the i-th cluster. The registers **CCM[i]_CMU_CLK_CFG** and **CCM[i]_CMU_FXCLK_CFG** allows the configuration of various cluster clock frequencies.

Figure 29 shows important details about the wiring of the cluster's local clock signals.

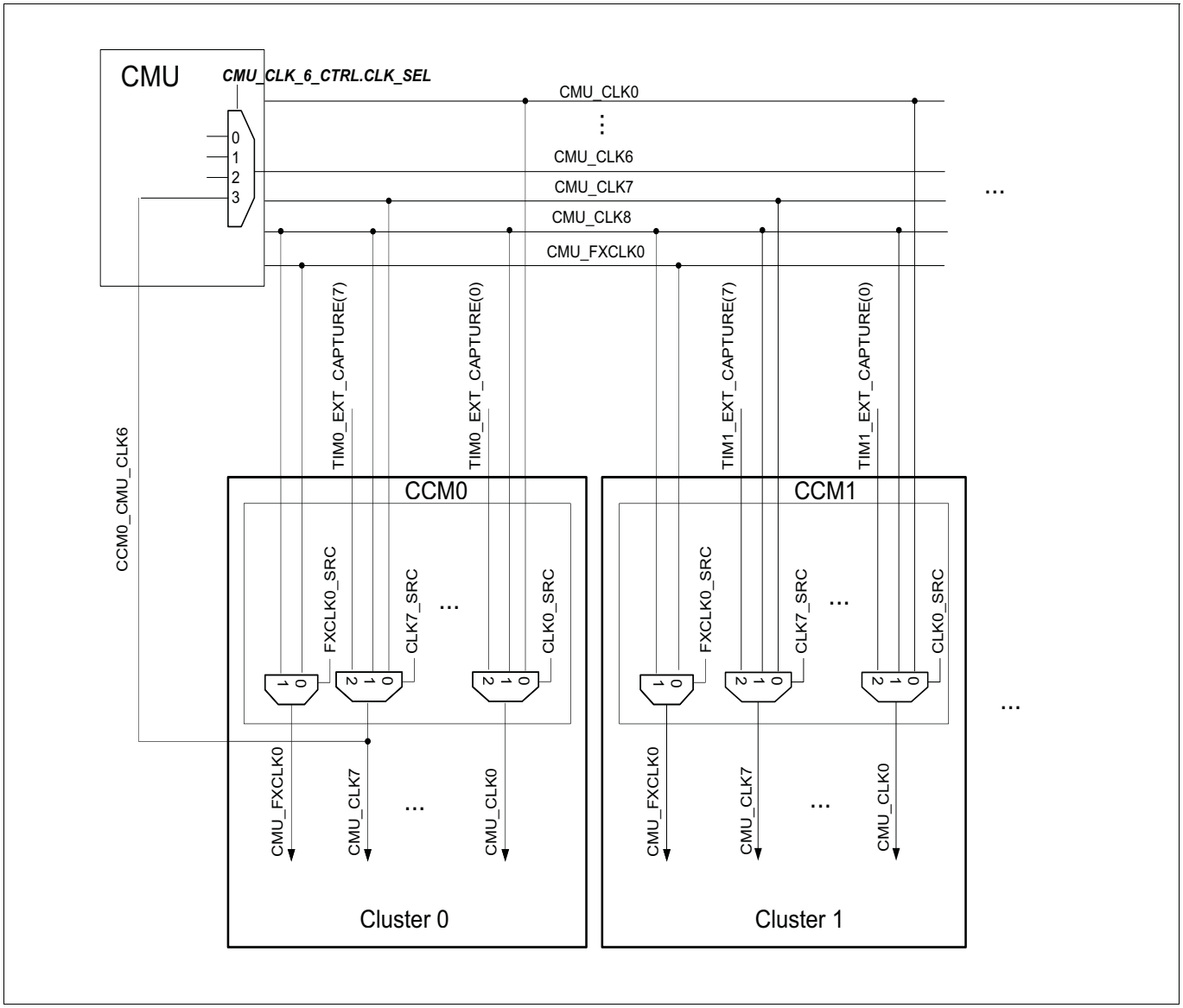


Figure 29 Cluster Clock Signal Wiring

The register **CCM[i]_AEIM_STA** captures the address and the reason of the first invalid AEIM bus master access of the cluster's MCS module.

The registers **CCM[i]_HW_CONF**, **CCM[i]_AUX_IN_SRC**, **CCM[i]_EXT_CAP_EN**, **CCM[i]_TOM_OUT**, and **CCM[i]_ATOM_OUT** are global status and configuration registers that are mirrored from the group of TOP-Level registers. The intention of these registers is to bring up cluster specific configuration registers into the address space of the bus master of the cluster's MCS module.

28.11.2 Address Range Protection

The CCM also provides up to NARP so called address range protectors (ARPs), where the number NARP depends on the actual device configuration (defined in device specific appendix). An ARP can be used to define a configurable write protected address range in order to support enhanced safety features. The address width of and ARP is also device dependent and it is determined by the parameter AAW as defined in device specific appendix.

The protected address range is mapped to the address range of the cluster's MCS RAM port.

Each ARP z (with z = 0…NARP-1) can be configured by the registers **CCM[i]_ARP[z]_CTRL** and **CCM[i]_ARP[z]_PROT**, where the register **CCM[i]_ARP[z]_CTRL** enables to configure the size and base address offset for an ARP and the register **CCM[i]_ARP[z]_PROT** configures, that an MCS channel x with a set bit field **WPROTx** cannot write to the corresponding z-th ARP. Whenever an MCS channel x is writing to an ARP that does not allow a write access from channel x by the configuration register **CCM[i]_ARP[z]_PROT**, the write access is discard. The bit field **WPROT_AEI** of register **CCM[i]_ARP[z]_CTRL** allows to configure if a CPU write access (via AEI slave interface) to the z-th ARP is protected. If the CPU wants to write to the z-th ARP while **WPROT_AEI** is set, the write access will be discard and the AEI status signal will signalize an invalid module access.

Considering the size and base address of an ARP, it should be noted that the configuration possibilities are limited. Details about the configuration can be found in the register description of **MCS[i]_ARP[z]_CTRL**.

The bit field **DIS_PROT** of register **CCM[i]_ARP[z]_CTRL** changes the meaning of an ARP configuration in a way that it explicitly allows an MCS channel x with a set bit field **WPROTx** to write to the z-th ARP. Accordingly, if the bit **DIS_PROT** is set while the bit **WPROT_AEI** is also set in the register **CCM[i]_ARP[z]_CTRL**, the z-th ARP explicitly allows a write access from the CPU to the z-th ARP. A meaningful application of an ARP z with a set bit field **DIS_PROT** for an MCS channel x has another ARP with a surrounding wider address range that is defining a write protection for MCS channel x and some other MCS channels.

Since the address range of an ARP can surround another ARP it is possible to configure contradictory conditions for MCS channels or the CPU within the overlapping area (e.g. if ARP y surrounds ARP z and ARP y allows a write access for an MCS channel x but ARP z prohibits a write access for MCS channel x). In order to resolve this ambiguity, the following rule is defined: A write protection for a specific address c concerning MCS channel x (the CPU) is active, if and only if, address c is covered by at least one ARP with a cleared bit **DIS_PROT** and a set bit **WPROTx** (**WPROT_AEI**) and there exists no ARP covering address c with a set bit field **DIS_PROT** and a set bit field **WPROTx** (**WPROT_AEI**).

28.11.3 CCM Configuration Register Overview

Table 26 CCM Configuration Register Overview

Register name	Description	see Page
CCM[i]_PROT	CCMi Protection Register	119
CCM[i]_CFG	CCMi Configuration Register	119
CCM[i]_CMU_CLK_CFG	CCMi CMU Clock Configuration Register	121
CCM[i]_CMU_FXCLK_CFG	CCMi CMU Fixed Clock Configuration Register	122
CCM[i]_AEIM_STA	CCMi MCS Bus Master Status Register	122
CCM[i]_ARP[z]_CTRL	CCMi Address Range Protector z Control Register	123
CCM[i]_ARP[z]_PROT	CCMi Address Range Protector z Protection Register	124
CCM[i]_HW_CONF	CCMi Hardware Configuration Register	125
CCM[i]_TIM_AUX_IN_SRC	CCMi TIM AUX input source Register.	128
CCM[i]_EXT_CAP_EN	CCMi External Capture Enable Register.	129
CCM[i]_TOM_OUT	CCMi TOM Output Register.	130
CCM[i]_ATOM_OUT	CCMi ATOM Output Register.	130

28.11.4 CCM Configuration Register description

28.11.4.1 Register CCM[i]_PROT

CCMi Protection Register

CCMi_PROT (i=0-11)
CCMi Protection Register **($0E21FC_H$+i*200_H)** **Application Reset Value: 0000 0001_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0															CLS_PROT
r															rw

Field	Bits	Type	Description
CLS_PROT	0	rw	**Cluster Protection** 0_B Write protection of cluster configuration registers is disabled 1_B Write protection of cluster configuration registers is enabled
0	31:1	r	**Reserved** Read as zero, shall be written as zero.

28.11.4.2 Register CCM[i]_CFG

CCMi Configuration Register

NOTE: The module specific clock enable registers (bit field **EN_***) are only implemented if the corresponding module is available in the i-th cluster.

NOTE: For the Clusters greater than 4, (only 100MHz capable), the only allowed settings for the CLS_CLK_DIV are 00 and 10 (clock divider 2).

CCMi_CFG (i=0-11)
CCMi Configuration Register **($0E21F8_H$+i*200_H)** **Application Reset Value: XXXX $XXXX_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TBU_DIR2	TBU_DIR1	0												CLS_CLK_DIV	
r	r	r												r	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								EN_CMP_MON	EN_PSM	EN_BRC	EN_DPLL_MAP	EN_MCS	EN_ATOM_ADTM	EN_TOM_SPE_TDTM	EN_TIM
r								rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
EN_TIM	0	rw	**Enable TIM** This bit is only writable if bit field **CLS_PROT** of register **CCM[i]_PROT** is cleared. 0_B Disable clock signal for sub module TIM 1_B Enable clock signal for sub module TIM
EN_TOM_SPE_TDTM	1	rw	**Enable TOM, SPE and TDTM** This bit is only writable if bit field **CLS_PROT** of register **CCM[i]_PROT** is cleared. 0_B Disable clock signal for modules TOM, SPE, and their related DTM modules 1_B Enable clock signal for modules TOM, SPE, and their related DTM modules.
EN_ATOM_ADTM	2	rw	**Enable ATOM and ADTM** This bit is only writable if bit field **CLS_PROT** of register **CCM[i]_PROT** is cleared. 0_B Disable clock signal for modules ATOM and their related DTM modules. 1_B Enable clock signal for modules ATOM and their related DTM modules.
EN_MCS	3	rw	**Enable MCS** This bit is only writable if bit field **CLS_PROT** of register **CCM[i]_PROT** is cleared. 0_B Disable clock signal for module MCS 1_B Enable clock signal for module MCS
EN_DPLL_MAP	4	rw	**Enable DPLL and MAP** This bit is only writable if bit field **CLS_PROT** of register **CCM[i]_PROT** is cleared. 0_B Disable clock signal for modules DPLL and MAP 1_B Enable clock signal for modules DPLL and MAP
EN_BRC	5	rw	**Enable BRC** This bit is only writable if bit field **CLS_PROT** of register **CCM[i]_PROT** is cleared. 0_B Disable clock signal for module BRC 1_B Enable clock signal for module BRC
EN_PSM	6	rw	**Enable PSM** This bit is only writable if bit field **CLS_PROT** of register **CCM[i]_PROT** is cleared. 0_B Disable clock signal for module PSM 1_B Enable clock signal for module PSM
EN_CMP_MON	7	rw	**Enable CMP and MON** This bit is only writable if bit field **CLS_PROT** of register **CCM[i]_PROT** is cleared. 0_B Disable clock signal for modules CMP and MON 1_B Enable clock signal for modules CMP and MON

Field	Bits	Type	Description
CLS_CLK_DIV	17:16	r	**Cluster Clock Divider** The value of this bit field mirrors the bit field **CLS[i]_CLK_DIV** of register **GTM_CLS_CLK_CFG**, whereas i equals the cluster index. 00_B Cluster is disabled 01_B Cluster is enabled without clock divider 10_B Cluster is enabled with clock divider 2 11_B Reserved, do not use.
TBU_DIR1	30	r	**DIR1 input signal of module TBU** 0_B Indicating forward direction 1_B Indicating backward direction
TBU_DIR2	31	r	**DIR2 input signal of module TBU** 0_B Indicating forward direction 1_B Indicating backward direction
0	15:8, 29:18	r	**Reserved** Read as zero, shall be written as zero.

28.11.4.3 Register CCM[i]_CMU_CLK_CFG

CCMi CMU Clock Configuration Register

The bit fields of this register are only writable if bit field **CLS_PROT** of register **CCM[i]_PROT** is cleared.

CCMi_CMU_CLK_CFG (i=0-11)
CCMi CMU Clock Configuration Register **($0E21F0_H$+i*200_H)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		**CLK7_SRC**		**0**		**CLK6_SRC**		**0**		**CLK5_SRC**		**0**		**CLK4_SRC**	
r		rw		r		rw		r		rw		r		rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		**CLK3_SRC**		**0**		**CLK2_SRC**		**0**		**CLK1_SRC**		**0**		**CLK0_SRC**	
r		rw		r		rw		r		rw		r		rw	

Field	Bits	Type	Description
CLKx_SRC (x=0-7)	4*x+1:4*x	rw	**Clock x source signal selector** 00_B Use CMU_CLKx signal of CMU as CMU_CLKx signal within cluster 01_B Use CMU_CLK8 signal of CMU as CMU_CLKx signal within cluster 10_B Use TIM[i]_EXT_CAPTURE(x) signal as CMU_CLKx signal within cluster 11_B Reserved

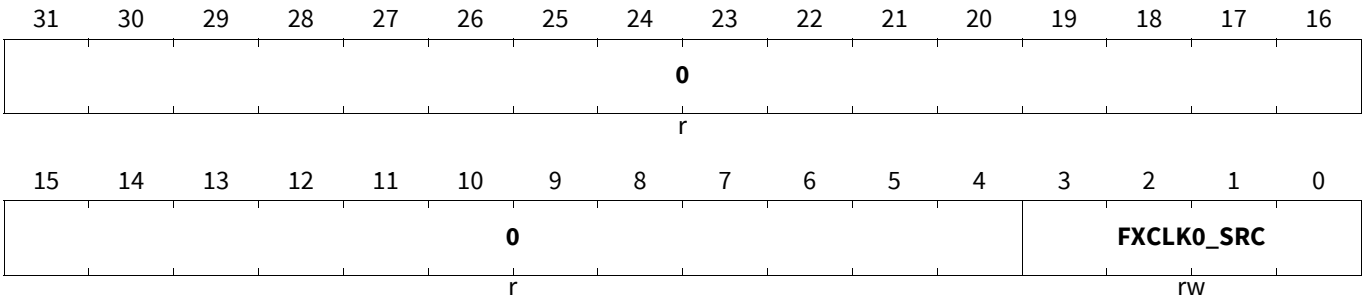
Field	Bits	Type	Description
0	31:30, 27:26, 23:22, 19:18, 15:14, 11:10, 7:6, 3:2	r	**Reserved** Read as zero, shall be written as zero.

28.11.4.4 Register CCM[i]_CMU_FXCLK_CFG

CCMi CMU Fixed Clock Configuration Register

CCMi_CMU_FXCLK_CFG (i=0-11)

CCMi CMU Fixed Clock Configuration Register(0E21F4$_H$+i*200$_H$) **Application Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
FXCLK0_SRC	3:0	rw	**Fixed clock 0 source signal selector** Bit field values that are not mentioned above are reserved. These bits are only writable if bit field **CLS_PROT** of register **CCM[i]_PROT** is cleared. 0_H Use CMU_FXCLK0 signal of CMU as CMU_FXCLK0 signal within cluster 1_H Use CMU_CLK8 signal of CMU as CMU_FXCLK0 signal within cluster
0	31:4	r	**Reserved** Read as zero, shall be written as zero.

28.11.4.5 Register CCM[i]_AEIM_STA

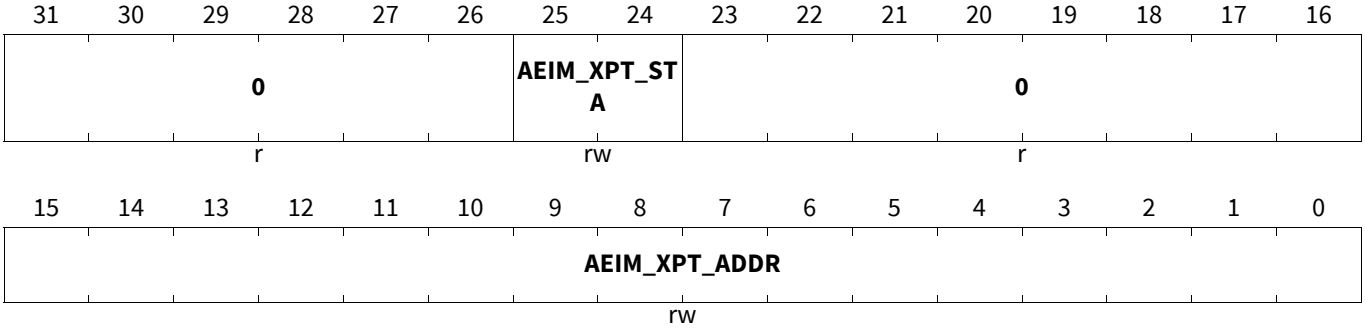
CCMi MCS Bus Master Status Register

Note: Only the first invalid AEIM bus master access of the MCS is updating this register with the invalid AEIM address (bit field AEIM_XPT_ADDR) and the reason of the invalid access (bit field AEIM_XPT_STA). A write access to this register (independent of the written data) always resets the bit fields AEIM_XPT_STA and AEIM_XPT_ADDR, and the next invalid AEIM access is captured by this register, again.

Note: If the i-th cluster does not provide an MCS module, this register is not available.

CCMi_AEIM_STA (i=0-11)

CCMi MCS Bus Master Status Register (0E21D8$_H$+i*200$_H$) Application Reset Value: 0000 0000$_H$



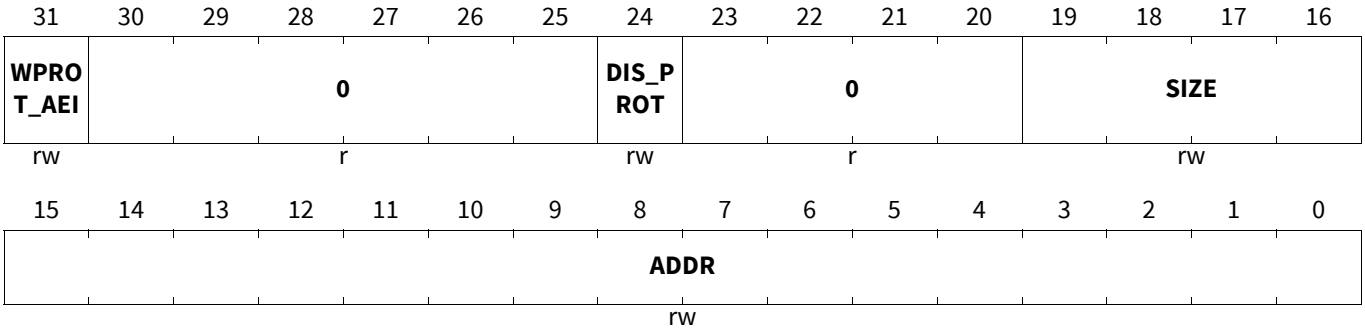
Field	Bits	Type	Description
AEIM_XPT_ADDR	15:0	rw	**Exception Address** Invalid bus master (AEIM) address of MCS module.
AEIM_XPT_STA	25:24	rw	**AEIM exception status** 00_B No invalid MCS bus master access occurred 01_B Invalid byte addressing of MCS bus master access 10_B Illegal module access of MCS bus master access 11_B Invalid MCS bus master access to an unsupported address
0	23:16, 31:26	r	**Reserved** Read as zero, shall be written as zero.

28.11.4.6 Register CCM[i]_ARP[z]_CTRL

CCM0 Address Range Protector z Control Register

CCMi_ARPz_CTRL (i=0-9;z=0-9)

CCMi Address Range Protector z Control Register(0E2000$_H$+i*200$_H$+z*8) Application Reset Value: 0003 0000$_H$



Field	Bits	Type	Description
ADDR	15:0	rw	**ARP base address** Base address for address range protector z. Only the bits 5 to AAW-1 of this bit field are implemented as registers. The bits AAW to 15 are reserved bits and always read and written as zeros. The bits 0 and 1 are functionally used for the definition of an ARP but they are always read and written as zeros. The actual base address for a protected address range is only defined by the upper AAW-(**SIZE**+2) bits (bit position 2+**SIZE** to bit position AAW-1) of bit field **ADDR**. The lower **SIZE**+2 bits (bit 0 to **SIZE**+1) are ignored for the address calculation and assumed as zeros. This bit field is only writable if bit field **CLS_PROT** of register **CCM[i]_PROT** is cleared.
SIZE	19:16	rw	**Size of ARP** Size of memory range protector z. The actual size of a protected memory range is defined as 2^{SIZE} address locations, whereas the bit field **SIZE** is interpreted as an unsigned integer number. This bit field is only writable if bit field **CLS_PROT** of register **CCM[i]_PROT** is cleared.
DIS_PROT	24	rw	**Disable ARP protection** This bit field is only writable if bit field **CLS_PROT** of register **CCM[i]_PROT** is cleared. 0_B Bit WPROTx (WPROT_AEI) defines write protection for selected address range 1_B Bit WPROTx (WPROT_AEI) explicitly allows write access to selected address range
WPROT_AEI	31	rw	**AEI slave write protection** The address range interval that is protected by this ARP can be calculated as [(**ADDR** AND NOT 4*(2^{SIZE}-1)); (**ADDR** AND NOT 4*(2^{SIZE}-1)) + 4*(2^{SIZE}-1)], assuming a byte-wise addressing, an unsigned integer representation for the bit fields **SIZE** and **ADDR**. NOT and AND are bitwise logical operators. The incrementation interval for neighboring memory locations is always 4. This bit field is only writable if bit field **CLS_PROT** of register **CCM[i]_PROT** is cleared. 0_B Write protection to address range from AEI slave is disabled 1_B Write protection to address range from AEI slave is enabled
0	23:20, 30:25	r	**Reserved** Read as zero, shall be written as zero.

28.11.4.7 Register CCM[i]_ARP[z]_PROT

CCM0 Address Range Protector z Protection Register

Only the first T bits of this register (bit 0 to T-1) are functionally implemented. The other bits (bit T to 31) are reserved bits. Parameter T reflects the number of available MCS channels in the cluster's MCS module.
These bit fields of this register are only writable if bit field **CLS_PROT** of register **CCM[i]_PROT** is cleared.

The meaning of the bit fields **WPROTx** can be changed by the bit field **DIS_PROT** of register **CCM[i]_ARP[z]_CTRL**.

CCMi_ARPz_PROT (i=0-9;z=0-9)
CCMi Address Range Protector z Protection Register($0E2004_H$+i*200_H+z*8) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								WPROT7	WPROT6	WPROT5	WPROT4	WPROT3	WPROT2	WPROT1	WPROT0
r								rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
WPROTy (y=0-7)	y	rw	**Write Protection MCS channel y** 0_B Write protection to ARP's address range for MCS channel y is disabled 1_B Write protection to ARP's address range for MCS channel y is enabled
0	31:8	r	**Reserved** Read as zero, shall be written as zero.

28.11.4.8 Register CCM[i]_HW_CONF

CCMi Hardware Configuration Register

CCMi_HW_CONF (i=0-11)
CCMi Hardware Configuration Register ($0E21DC_H$+i*200_H) Application Reset Value: 084F $022E_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		INT_CLK_EN_GEN	TOM_TRIG_INTCHAIN					ATOM_TRIG_INTCHAIN				IRQ_MODE_SINGLE_PULS	IRQ_MODE_PULSE_NOTIF	IRQ_MODE_PULSE	IRQ_MODE_LEVEL
r		r	r					r				r	r	r	r

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	ARU_CONNECT_CONFIG	ERM	RAM_INIT_RST	TOM_TRIG_CHAIN			TOM_OUT_RST	ATOM_TRIG_CHAIN			ATOM_OUT_RST	CFG_CLOCK_RATE	SYNC_INPUT_REG	BRIDGE_MODE_RST	GRSTEN
r	r	r	r	r			r	r			r	r	r	r	r

Field	Bits	Type	Description
GRSTEN	0	r	**Global Reset Enable** 0_B Global GTM reset register disabled 1_B Global GTM reset register enabled
BRIDGE_MODE_RST	1	r	**Bridge mode after reset** 0_B Bridge starts in synchronous mode after reset 1_B Bridge starts in asynchronous mode after reset
SYNC_INPUT_REG	2	r	**Additional pipelined stage in synchronous bridge mode** *Note: this register is only relevant (if existing) for synchronous bridge mode* 0_B No additional pipelined stage implemented. 1_B Additional pipelined stage implemented. All accesses in synchronous mode will be increased by one clock cycle.
CFG_CLOCK_RATE	3	r	**Clocks per ARU transfer** *Note: This value defines also the availability of configuration bits in register GTM_CLS_CLK_CFG.* If CFG_CLOCK_RATE=0, only the values 00_B and 01_B are valid for bit fields CLS[x]x_CLK_DIV. If CFG_CLOCK_RATE=1, only the values 00_B, 01_B and 10_B are valid for bit fields CLS[x]x_CLK_DIV. 0_B Each system clock an ARU transfer is scheduled 1_B Each second system clock an ARU transfer is scheduled. ARU transfer rate is half the system clock frequency.
ATOM_OUT_RST	4	r	**ATOM_OUT reset level** *Note: This value represents the ATOM output level after reset. The inverse value of this bit is the reset value of bit SL in all ATOM channels.* 0_B ATOM_OUT reset level is '0' 1_B ATOM_OUT reset level is '1'
ATOM_TRIG_CHAIN	7:5	r	**ATOM trigger chain length without synchronization register** It defines after which ATOM instance count a synchronization register is introduced into trigger chain (after ATOM_TRIG_<i> output if instance i and ATOM_TRIG_<i+1> input of instance i+1). Valid values are 1 to 7. 1 means that after each instance, a synchronization register is placed.
TOM_OUT_RST	8	r	**TOM_OUT reset level** *Note: This value represents the TOM output level after reset. The inverse value of this bit is the reset value of bit SL in all TOM channels.* 0_B TOM_OUT reset level is '0' 1_B TOM_OUT reset level is '1'

Field	Bits	Type	Description
TOM_TRIG_CHAIN	11:9	r	**TOM trigger chain length without synchronization register** It defines after which TOM instance count a synchronization register is introduced into trigger chain (after TOM_TRIG_<i> output if instance i and TOM_TRIG_<i+1> input of instance i+1). Valid values are 1 to 7. 1 means that after each instance, a synchronization register is placed.
RAM_INIT_RST	12	r	**RAM initialization from reset** 0_B RAM is not initialized after reset 1_B RAM is initialized after reset
ERM	13	r	**Enable RAM1 MSB for available MCS modules** *Note: The bit reflects the state of the configuration parameter ERM mentioned in the specification of MCFG.* 0_B MSB of MCS RAM1 address not used 1_B MSB of MCS RAM1 address used
ARU_CONNECT_CONFIG	14	r	**Defines number of parallel ARU ports** 0_B Two ARU ports available (two independent counter) 1_B One ARU port available
IRQ_MODE_LEVEL	16	r	**IRQ_MODE_LEVEL** 0_B Level mode not available 1_B Level mode available
IRQ_MODE_PULSE	17	r	**IRQ_MODE_PULSE** 0_B Pulse mode not available 1_B Pulse mode available
IRQ_MODE_PULSE_NOTIFY	18	r	**IRQ_MODE_PULSE_NOTIFY** 0_B Pulse notify mode not available 1_B Pulse notify mode available
IRQ_MODE_SINGLE_PULSE	19	r	**IRQ_MODE_SINGLE_PULSE** 0_B Single pulse mode not available 1_B Single pulse mode available
ATOM_TRIG_INTCHAIN	23:20	r	**ATOM internal trigger chain length without synchronization register** ATOM internal trigger chain length without synchronization register It defines after which ATOM channel count a synchronization register is introduced into trigger chain. Valid values are 1 to 8. 4 means that in channel 4 of the atom instances a synchronization register is placed.
TOM_TRIG_INTCHAIN	28:24	r	**TOM internal trigger chain length without synchronization register** It defines after which TOM channel count a synchronization register is introduced into trigger chain. Valid values are 1 to 16. 8 means that in channel 8 of the TOM instances, a synchronization register is placed.
INT_CLK_EN_GEN	29	r	**Internal clock enable generation** 0_B GTM external clock enable signals in use 1_B GTM internal clock enable signals in use

Field	Bits	Type	Description
0	15, 31:30	r	**Reserved** Read as zero, shall be written as zero.

28.11.4.9 Register CCM[i]_TIM_AUX_IN_SRC

CCMi TIM Module AUX_IN Source Selection Register

CCMi_TIM_AUX_IN_SRC (i=0-11)
CCMi TIM Module AUX_IN Source Selection Register($0E21E0_H$+i*200_H) Application Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								SEL_OUT_N_CH7	SEL_OUT_N_CH6	SEL_OUT_N_CH5	SEL_OUT_N_CH4	SEL_OUT_N_CH3	SEL_OUT_N_CH2	SEL_OUT_N_CH1	SEL_OUT_N_CH0
r								rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								SRC_CH7	SRC_CH6	SRC_CH5	SRC_CH4	SRC_CH3	SRC_CH2	SRC_CH1	SRC_CH0
r								rw	rw	rw	rw	rw	rw	rw	rw

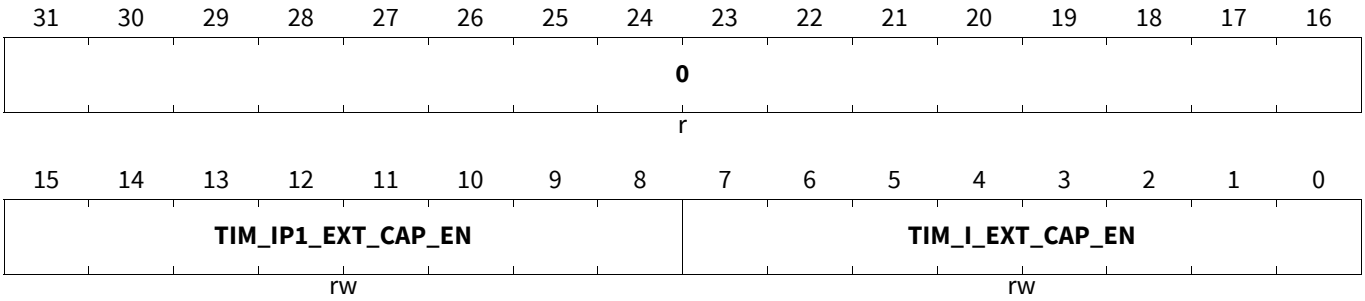
Field	Bits	Type	Description
SRC_CHz (z=0-7)	z	rw	**Defines AUX_IN source of TIM[i] channel z** SRC_CHz: Defines AUX_IN source of TIM[z] channel z SEL_OUT_N_CHz = 0 / SEL_OUT_N_CHz = 1: 0_B Defines AUX_IN source of TIM[i] channel (smaller number) CDTM[z].DTMz Output DTM_OUTz selected / CDTM[z].DTMzOutput 1_B Defines AUX_IN source of TIM[i] channel (higher number) CDTM[z].DTM4 Output DTM_OUT0 selected / CDTM[z].DTM4 Output DTM_OUT1_Nselected
SEL_OUT_N_CHz (z=0-7)	z+16	rw	**Use DTM_OUT or DTM_OUT_N signals as AUX_IN source of TIM[i] channel z** SEL_OUT_N_CHz: Use DTM_OUT or DTM_OUT_N signals as AUX_INsource of TIM[i] channel z 0_B Use DTM_OUT signal as AUX_IN source of TIM[0] 1_B Use DTM_OUT_N signal as AUX_IN source of TIM[0]
0	15:8, 31:24	r	**Reserved** Read as zero, shall be written as zero.

28.11.4.10Register CCM[i]_EXT_CAP_EN

CCMi External Capture Trigger Enable Register

CCMi_EXT_CAP_EN (i=0-11)

CCMi External Capture Trigger Enable Register(0E21E4$_H$+i*200$_H$) **Application Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
TIM_I_EXT_CAP_EN	7:0	rw	**TIM[i]_EXT_CAPTURE signal forwarding enable** Note: The trigger event forwarding is possible from TIM[i] and TIM[i+1] to MCS[i]. 00_H Disable forwarding of signal TIM[i]_EXT_CAPTURE to MCS[i] 01_H Enable forwarding of signal TIM[i]_EXT_CAPTURE to MCS[i]
TIM_IP1_EXT_CAP_EN	15:8	rw	**TIM[i+1]_EXT_CAPTURE signal forwarding enable** 00_H Disable forwarding of signal TIM[i+1]_EXT_CAPTURE to MCS[i] 01_H Enable forwarding of signal TIM[i+1]_EXT_CAPTURE to MCS[i]
0	31:16	r	**Reserved** Note: The trigger event forwarding is possible from TIM[i] and TIM[i+1] to MCS[i].

28.11.4.11Register CCM[i]_TOM_OUT

CCMi TOM Output Level Register

CCMi_TOM_OUT (i=0-11)
CCMi TOM Output Level Register **($0E21E8_H$+i*200_H)** **Application Reset Value: XXXX $XXXX_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TOM_OUT_N															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TOM_OUT															
r															

Field	Bits	Type	Description
TOM_OUT	15:0	r	Output level snapshot of TOM[i]_OUT all channels
TOM_OUT_N	31:16	r	Output level snapshot of TOM[i]_OUT_N all channels

28.11.4.12Register CCM[i]_ATOM_OUT

CCMi ATOM Output Level Register

*Note: Reset value depends on the hardware configuration chosen by silicon vendor. See **GTM_HW_CONF** for chosen value.*

CCMi_ATOM_OUT (i=0-11)
CCMi ATOM Output Level Register **($0E21EC_H$+i*200_H)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ATOM_IP1_OUT_N								ATOM_IP1_OUT							
r								r							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ATOM_I_OUT_N								ATOM_I_OUT							
r								r							

Field	Bits	Type	Description
ATOM_I_OUT	7:0	r	Output level snapshot of ATOM[i]_OUT all channels
ATOM_I_OUT_N	15:8	r	Output level snapshot of ATOM[i]_OUT_N all channels
ATOM_IP1_OUT	23:16	r	Output level snapshot of ATOM[i+1]_OUT all channels
ATOM_IP1_OUT_N	31:24	r	Output level snapshot of ATOM[i+1]_OUT_N all channels