28.16 Dead Time Module (DTM)

28.16.1 Overview

Figure 93 gives an overview of the structure of the Dead Time Module (DTM).

Note: In this paragraph, the following is used. Variable n is used for CDTMs, x for channels and i is used for DTMs. (An exception for TIM names.)

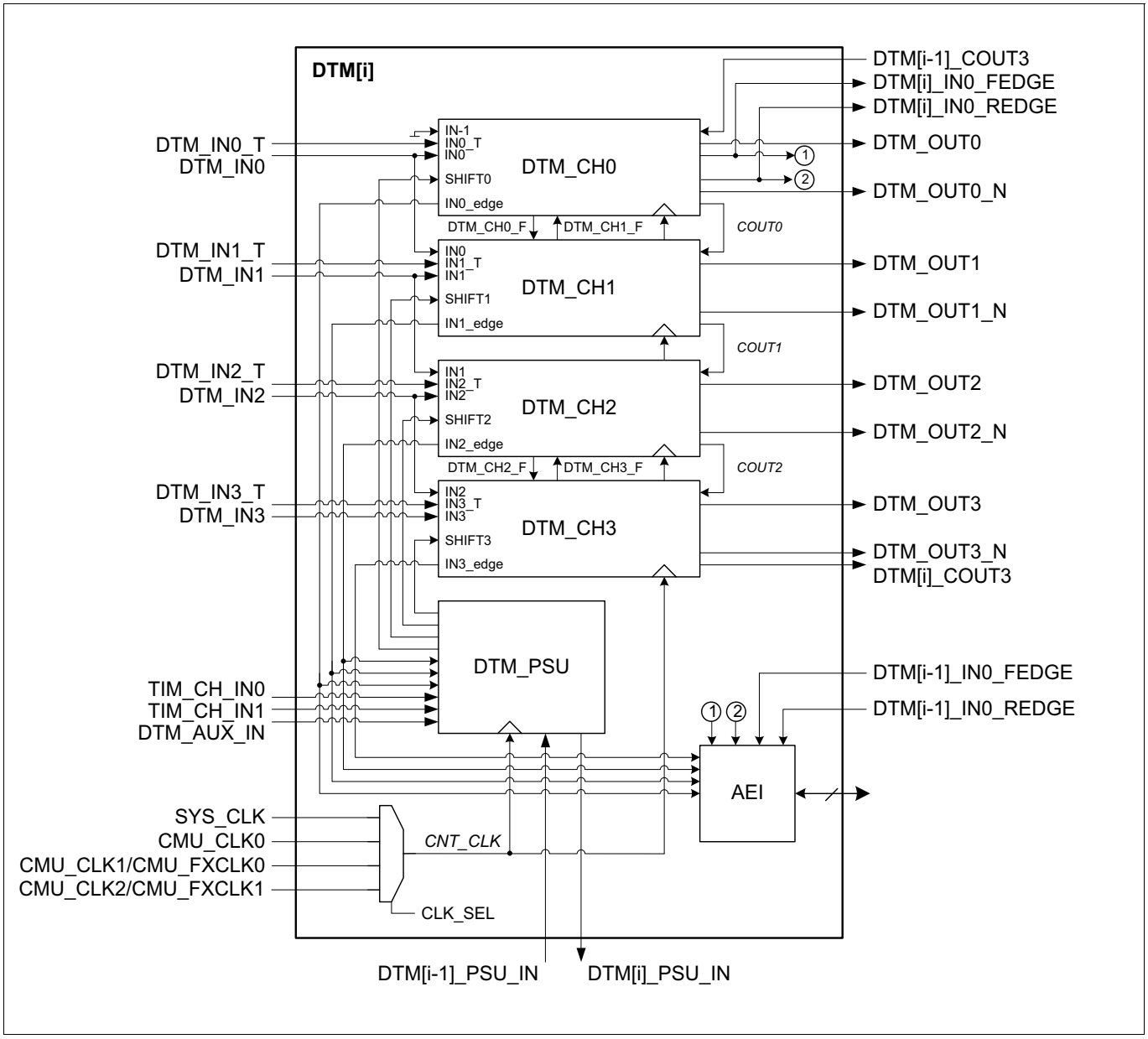


Figure 93 DTM overview

The main function of the DTM is to derive for each input *DTM_IN0* to *DTM_IN3* the individual inverse signal (*DTM[i]_OUT[x]_N*) and to apply an edge specific delay between the edge of the original signal and the edge of the derived inverted signal (i.e., the dead time). This function is mainly used for controlling of half bridges.

A second function provided by DTM is to set the outputs of one channel to the value of the preceding channel if requested by a trigger on input *TIM_CH_IN*0, *TIM_CH_IN1* or *DTM_AUX_IN*. This feature allows a phase shift on one PWM signal to the phase of the preceding PWM signal up to the next edge on this channel.

The third function provided by DTM is to (N)AND/(N)OR/X(N)OR combine the input *DTM_IN[x]* signal of one DTM channel with the signal on input *TIM_CH_IN0, TIM_CH_IN1* or *DTM_AUX_IN* (selected inside DTM_PSU and assigned to one of the signals *SHIFT[x]*) or with the combinational output (signal *COUT[x]*) of preceding channel.As a result *COUT2* may be the combined signal of *DTM_IN0* and *TIM_CH_IN0, TIM_CH_IN1* or *DTM_AUX_IN* and the signal *DTM_IN1*. For *COUT3* this chain can be combined again with signal *DTM_IN3*.

The outputs of each channel may be swapped individually to provide the function of combining signals on each output of a channel.

In general, the DTM instances are placed behind the TOM and the ATOM instances, i.e., the outputs *TOM_OUT[x] and TOM_OUT[x]_T* or *ATOM_OUT[x] and ATOM_OUT[x]_T* are each routed to the DTM instance inputs *DTM_IN[y]* and *DTM_IN[y]_T*.Four DTM instances behind a TOM instance i and two DTM instances behind an ATOM instance i are grouped together in a Cluster DTM hierarchy called CDTM[i]. The connections between DTM and the modules TOM and ATOM are depicted in **Figure 94**.

Note, depending on device configuration, not every DTM instance is available. E.g. a device may only have one DTM connected to the first four channels of ATOM. In this case, the other four channels (4 to 7) are connected directly to GTM outputs.For detailed information, which DTM instance is available, refer to corresponding device specific device specific appendix of this specification.

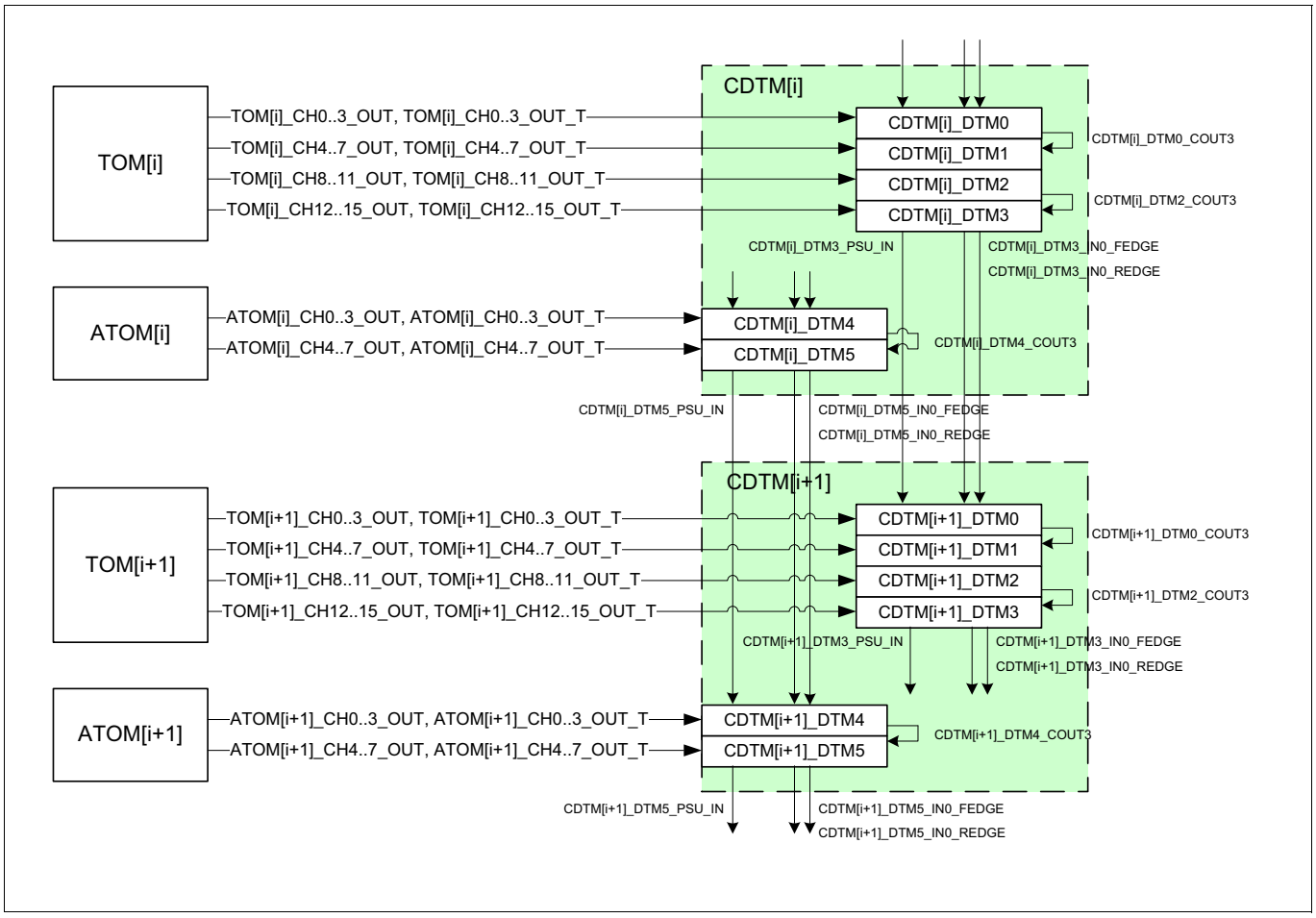


Figure 94 Connections of TOM and ATOM to DTM inputs DTM_IN[y]/DTM_IN[y]_T

Additionally, the DTM instances have inputs *TIM_CH_IN0*/*TIM_CH_IN1* which are driven by TIM output signals *TIM[i]_CH[x]_F_OUT*.

There are two configurations of TIM to DTM connections possible depending on the DTM channel specific configuration bit TIM_SEL.

In case of TIM_SEL=0 the connected TIM input may not be of the same cluster as the DTM.

In case of TIM_SEL=1 the TIM input is of the same cluster as the DTM.

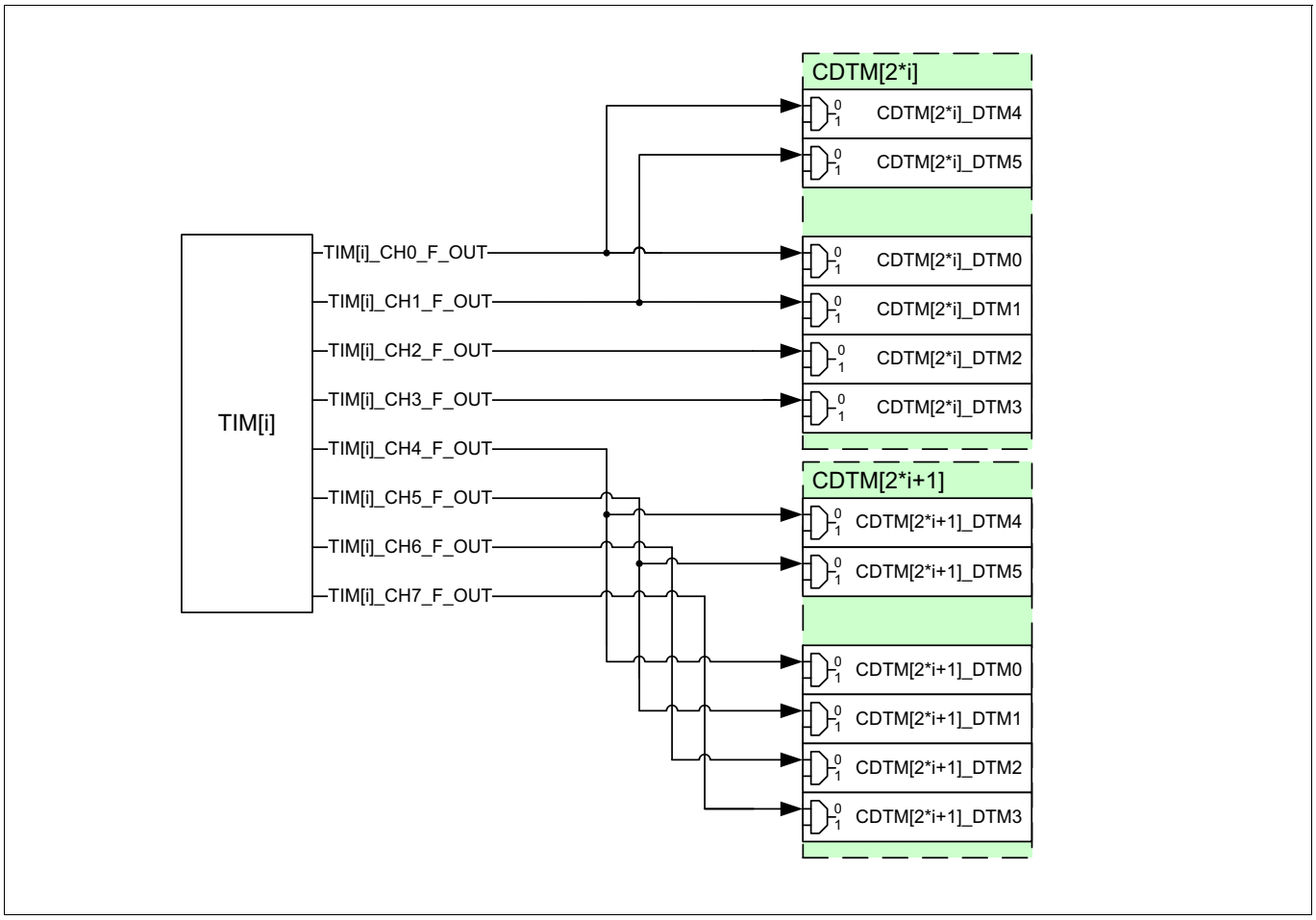


Figure 95 Connections of TIM to DTM inputs TIM_CH_IN0/TIM_CH_IN1 for TIM_SEL=0

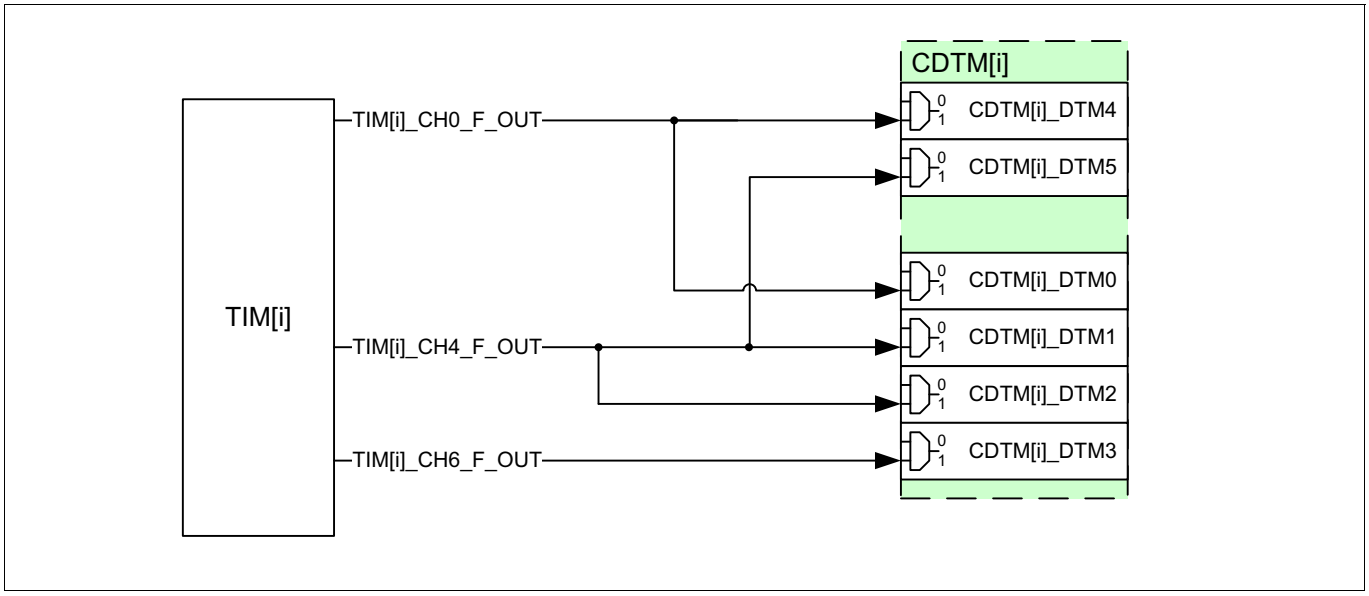


Figure 96 Connections of TIM to DTM inputs TIM_CH_IN0/TIM_CH_IN1 for TIM_SEL=1

There are also connections between DTM instances of same CDTM instance.For each pair of DTM instance 2i and 2i+1 the combinatorial output *COUT(3)* of DTM[2i] channel 3 is connected to DTM[2i+1] channel 0 *COUT(0-1)*.

With this a combinatorial chain over two neighbored DTM instances can be configured.

If one of the two neighbored DTM instances is not available (i.e. it is an empty instance) the inputs used for connections between two neighbored DTM instances are left open.

Note: For channel x=0 of DTM instance 2i input signals COUT[x-1] is unused and I1SEL[x] is defined as 0.

An additional link between DTM instances behind an ATOM is a forwarding of *DTM[i]_PSU_IN* signal to next available instance of DTM behind an ATOM (e.g. *DTM[i+1]_PSU_IN*).

The same link is available between all available DTM behind a TOM.

Note, for unavailable DTM[i] instances (i.e. the instance DTM[i] is called empty) the signal *DTM[i-1]_PSU_IN* is passed through empty instance DTM[i] to *DTM[i+1]_PSU_IN*, *DTM[i-1]_IN0_FEDGE* and *DTM[i-1]_IN0_REDGE* are passed through DTM[i] to *DTM[i+1]_IN0_FEDGE* and *DTM[i+1]_IN0_REDGE*.

Further connections between neighbored DTM instances are depicted in **Figure 97**:

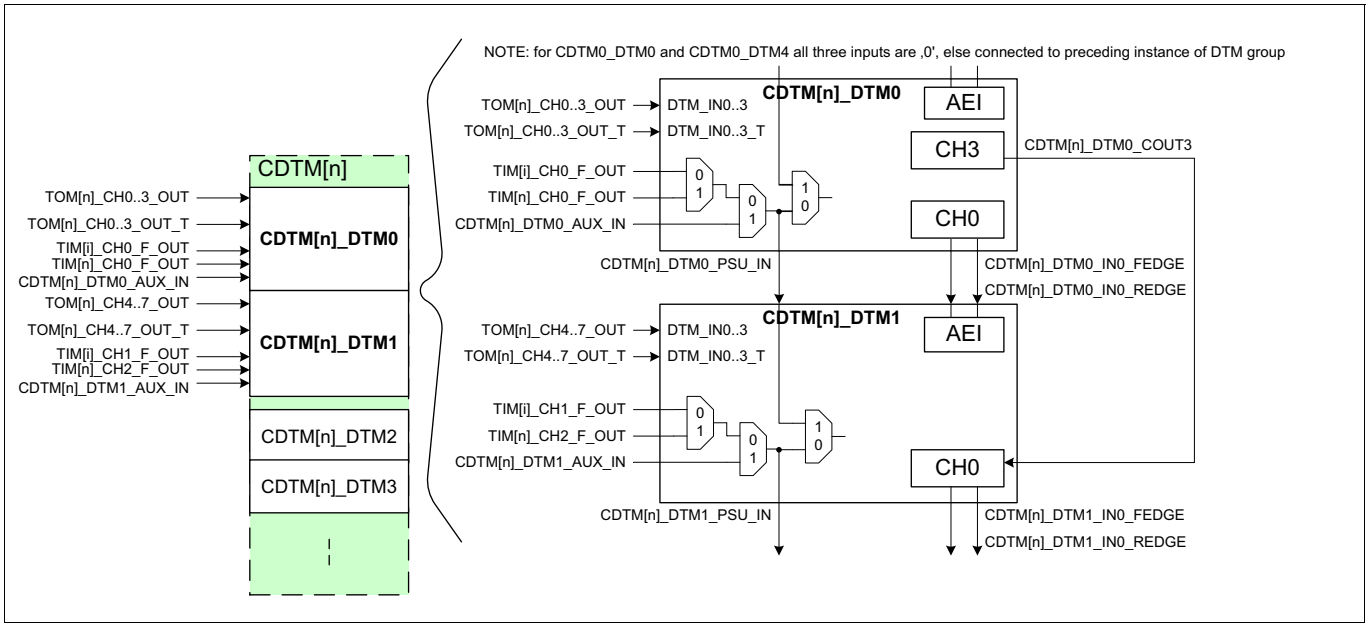


Figure 97 Connections between DTM instances

28.16.2 DTM Channel

Figure 98 depicts the functions of a DTM channel.

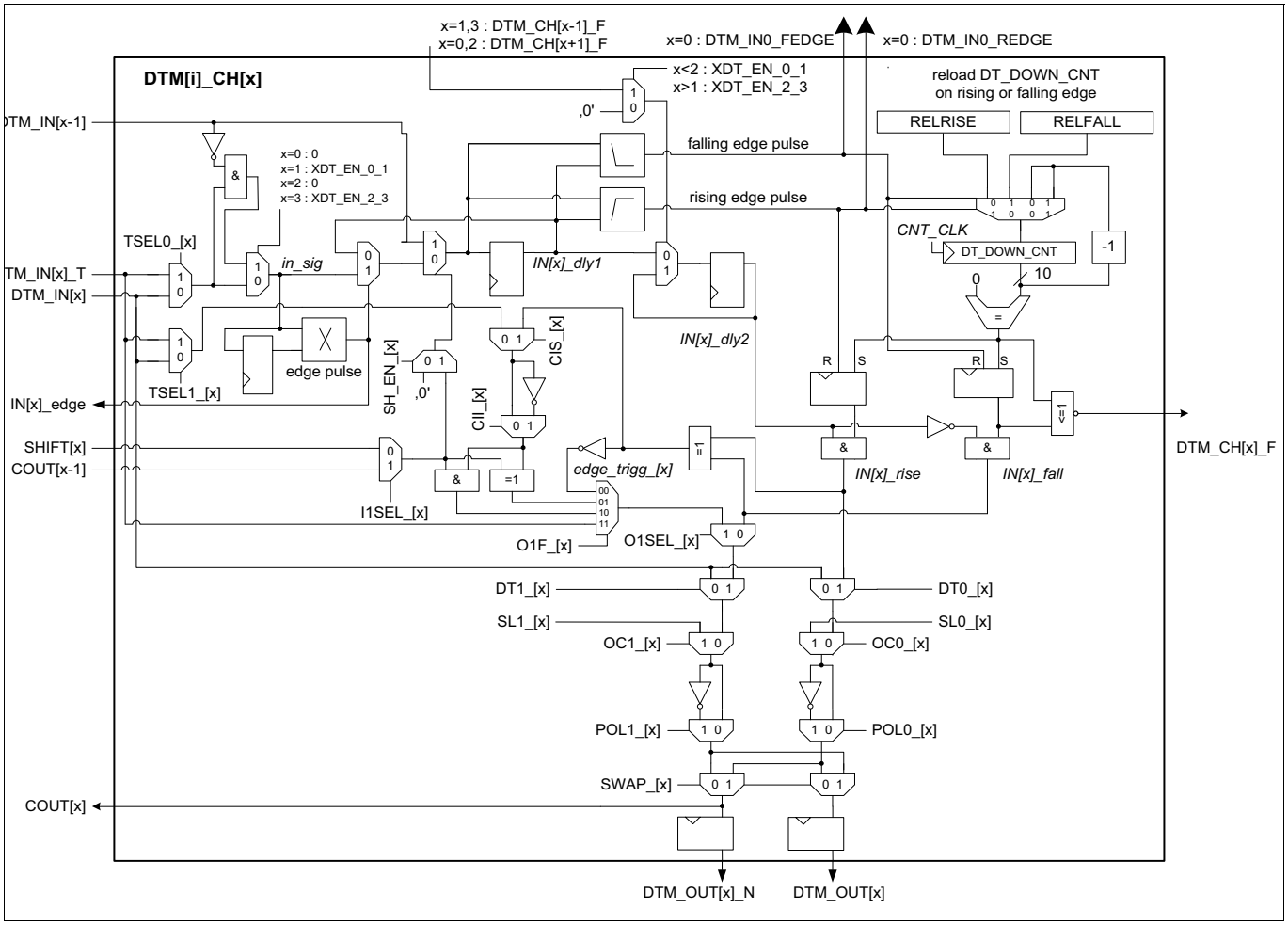


Figure 98 DTM channel overview

The main feature of each channel is to derive the inverse signal out of the input signal *DTM_IN[x]*, apply an edge dependent delay on the two resulting signal paths and provide these signals at the outputs *DTM[i]_OUT[x]* and *DTM[i]_OUT[x]_N*.

There are two possibilities to apply dead time on GTM output signals.One is to use one DTM channel per TOM/ATOM channel and generate inside the DTM the second inverse signal. This is called the standard dead time generation.The second way is to generate two signals out of two TOM/ATOM channel and to apply inside the DTM only the dead time by using two cross linked DTM channel. This is called the cross dead time generation.

28.16.2.1 Standard dead time generation

The dead time can be configured for each edge individually. The bit field **RELRISE** in register **DTM[i]_CH[x]_DTV** contains the reload value for the counter and defines the delay for rising edges in multiples of selected clock ticks.The bit field **RELFALL** in register **DTM[i]_CH[x]_DTV** contains the reload value for the counter and defines the delay for falling edges in multiples of selected clock ticks.

The counter is reloaded with the value of **RELRISE** on a rising edge and reloaded with the value of **RELFALL** on a falling edge on input *DTM_IN[x]* (or *DTM_IN[x-1]* in case of shift enable **SH_EN_[x]**).

On a reload of the counter the flip-flop following the counter output comparator is reset and stays reset until the counter has reached 0.After reload, the counter **DT_DOWN_CNT** counts down until it reaches 0 and stops at 0.

The signal flow for function of standard dead time signal generation is depicted in **Figure 99**.

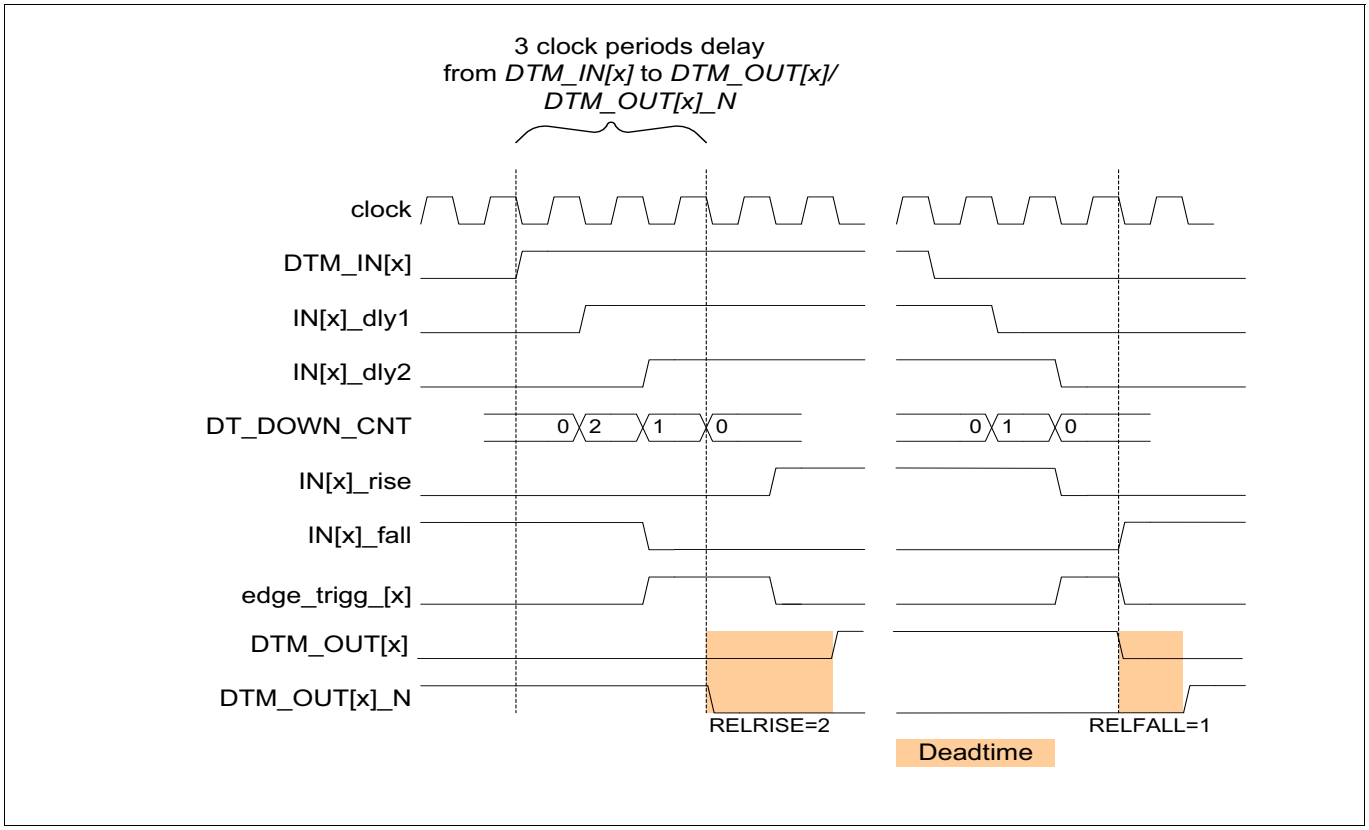


Figure 99 Wave signals for function of dead time generation

*Note: The delay from the input signal DTM_IN[x] to the output signals DTM[i]_OUT[x] and DTM[i]_OUT[x]_N is three system clock periods by disabled feed through (see **DT0/1_[x]** in **DTM[i]_CH_CTRL2**).*

*Note: The delay from the input signal DTM_IN[x] to the output signals DTM[i]_OUT[x] and DTM[i]_OUT[x]_N is one system clock periods by enabled feed through (see **DT0/1_[x]** in **DTM[i]_CH_CTRL2**).*

*Note: The delay from the input signal DTM_IN[x]_T to the output signals DTM[i]_OUT[x] and DTM[i]_OUT[x]_N is three system clock periods in case of disabled feed through (see **O1F_[x]** and **O1SEL_[x]** in **DTM[i]_CH_CTRL2**).*

*Note: The delay from the input signal DTM_IN[x]_T to the output signals DTM[i]_OUT[x] and DTM[i]_OUT[x]_N is one system clock periods in case of enabled feed through (see **O1F_[x]** and **O1SEL_[x]** in **DTM[i]_CH_CTRL2**).*

Note: The reset level of the output signals DTM[i]_OUT[x] connected from ATOM module depends on the hardware configuration value atom_out_reset_level_c chosen by silicon vendor.

Note: The reset level of the output signals DTM[i]_OUT[x]_N connected from ATOM module is defined by the inverse hardware configuration value atom_out_reset_level_c chosen by silicon vendor.

Note: The reset level of the output signals DTM[i]_OUT[x] connected from TOM module is defined by the hardware configuration value tom_out_reset_level_c chosen by silicon vendor.

Note: The reset level of the output signals DTM[i]_OUT[x]_N connected from TOM module is defined by the inverse hardware configuration value tom_out_reset_level_c chosen by silicon vendor.

28.16.2.2 Cross channel dead time

A second way to apply a dead time value on two output signals is the cross channel dead time.

In opposite to the dead time described in **Section 28.16.2.1** the cross channel dead time mode does not generate out of one signal the corresponding inverse signal but tries to apply the dead time on the input signals of two neighbored DTM channel.

To do this, two neighbored DTM input signals (on DTM channel (2k) and (2k+1) for k=0,1) are cross linked together in the way that a falling edge on one channel leads to a hold phase of current signal value on the cross linked channel.

This behavior is reached by the following:

A falling edge on e.g. channel (2k) reloads the **DT_DOWN_CNT** with the value of **RELFALL**. While this counter is counting down, the output signal of the cross linked channel (2k+1) keeps its value. If the counter **DT_DOWN_CNT** has reached 0 again, the channel (2k+1) output is released and can follow the value on its input.The timing of the cross channel dead time is depicted in the following figure:

Figure 100 shows the behavior in case of input edges at *DTM_IN[2k]* and *DTM_IN[2k+1]* occur at the same point in time.Then the falling edge is forwarded immediately (with only two clock cycles delay) and the rising edge is delayed additionally by the number of clock ticks specified by the **RELFALL** parameter of the cross linked channel.

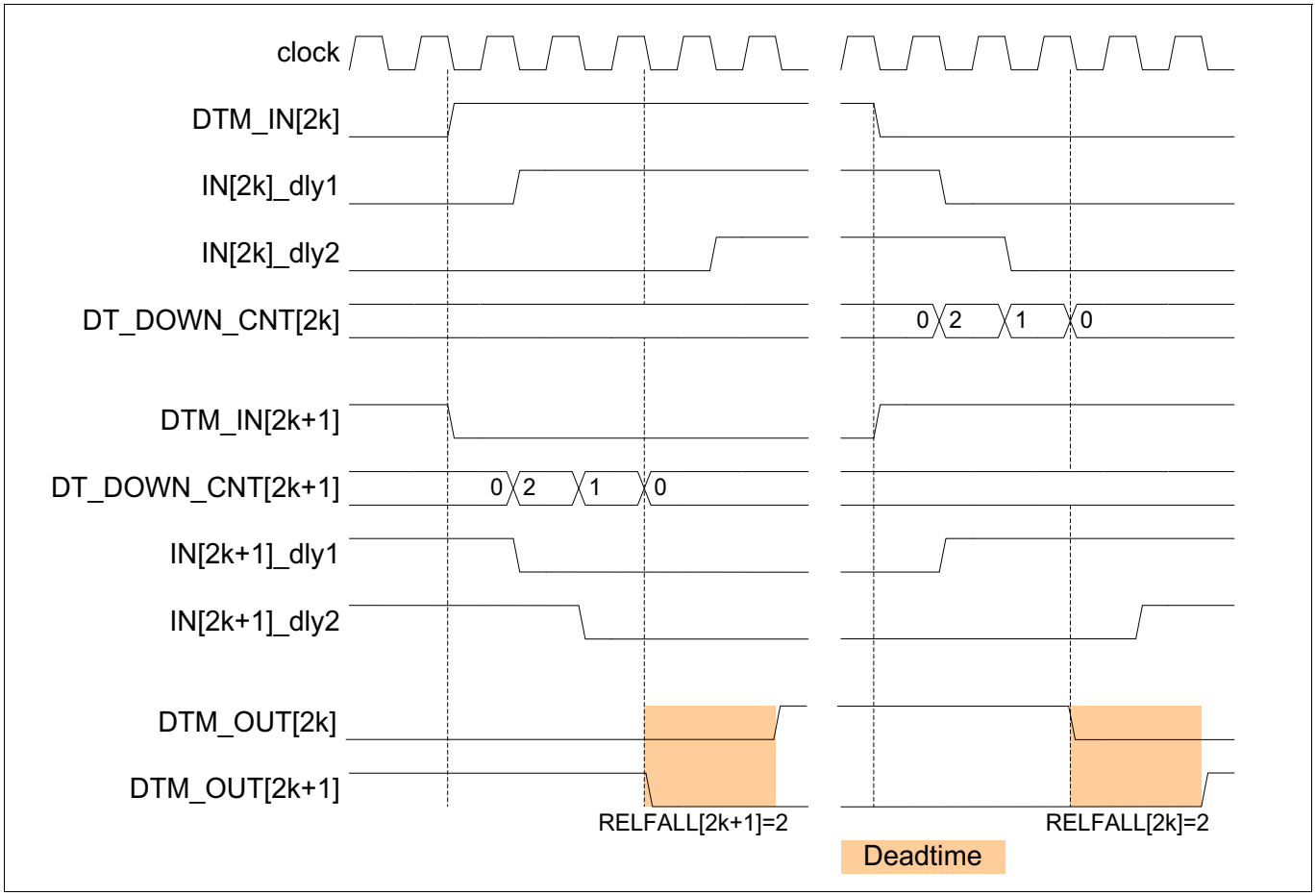


Figure 100 Cross channel dead time timing diagram

In case of high level (i.e. 1) at the DTM inputs *DTM_IN[2k]* and *DTM_IN[2k+1]* at the same point in time, the channel of (2k) has higher priority than the corresponding channel (2k+1). This means that in this case the input *DTM_IN[2k+1]* if forced immediately at channel input to low level (i.e. 0).

As a result the DTM output of channel *DTM_OUT[2k+1]* can never be high if the cross linked channel *DTM_OUT[2k]* is high.

28.16.3 Phase Shift Control Unit

The phase shift unit (DTM_PSU) is depicted in the following figure. It supports the second major function of the DTM module to allow phase shifting of PWM signal on one of the channels.

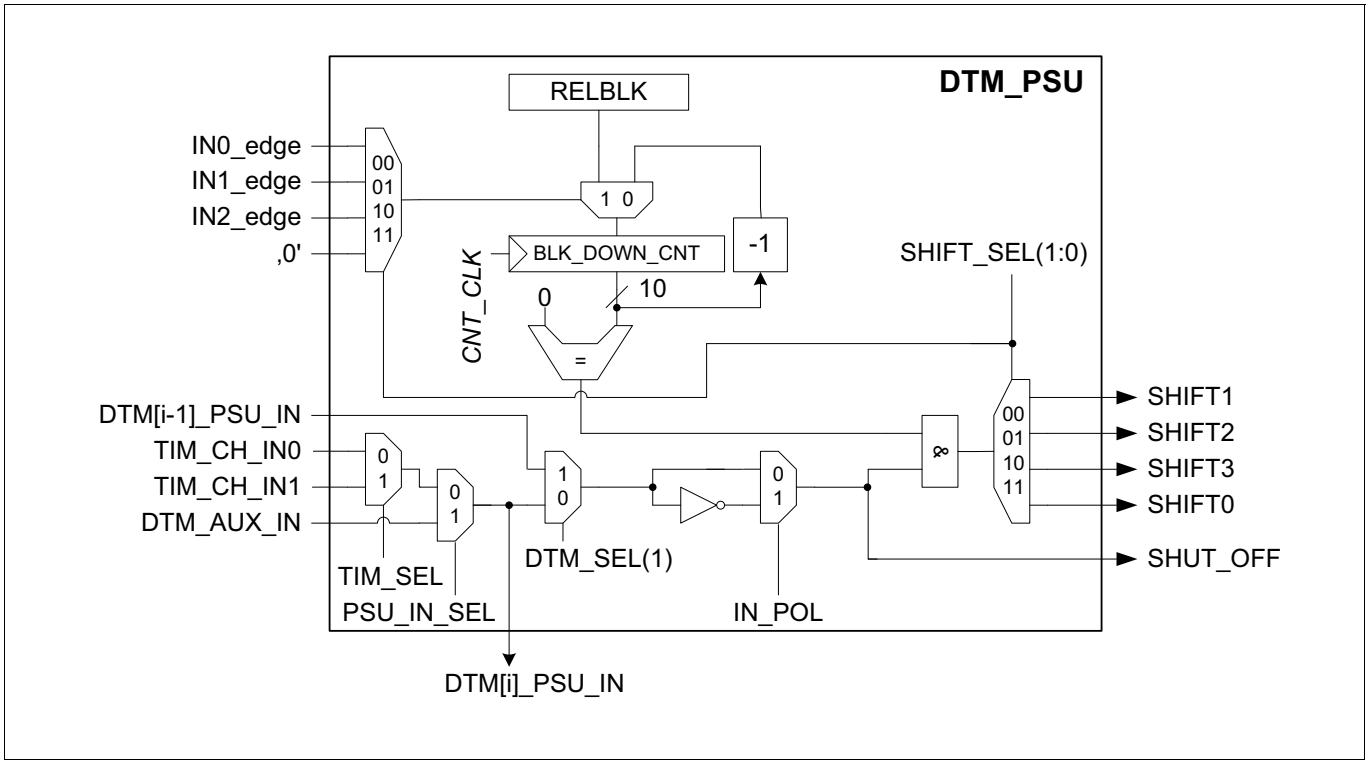


Figure 101 Phase Shift Unit overview

This sub-module provides an additional counter **BLK_DOWN_CNT** and reload register **RELBLK** (bit field of register **DTM[i]_PS_CTRL**). The counter is reloaded on an edge detected on one of the selected signals *IN0_edge* to *IN2_edge* (selected by bit field **SHIFT_SEL** in register **DTM[i]_PS_CTRL**). Then, the counter counts down until it reaches 0. While the counter is counting down, it blocks the trigger (i.e. the selected one of the signals *SHIFT[x]*) of one of the channels by one of the input signals *TIM_CH_IN0, TIM_CH_IN1* or *DTM_AUX_IN*.

If the counter **BLK_DOWN_CNT** is not counting, a pulse on the input *TIM_CH_IN*0, *TIM_CH_IN*1 or *DTM_AUX_IN* is forwarded to one of the selected DTM_PSU outputs *SHIFT[x]*. This signal triggers in the selected channel (if **SH_EN_x**=1) the update of the first flip-flop on channel x (i.e. representing *IN[x]_DLY*) to the input value *DTM_IN[x-1]* of the preceding channel. If this update leads to an edge, the succeeding part of DTM channel derives the inverse signal and applies the corresponding dead time (i.e. the edge delay) to the output signals of the channel.

*Note: For channel x=0 input signals DTM_IN[x-1] is unused and **SH_EN_[x]** is defined as 0.*

Figure 102 shows an example of phase shifting on channel 1.

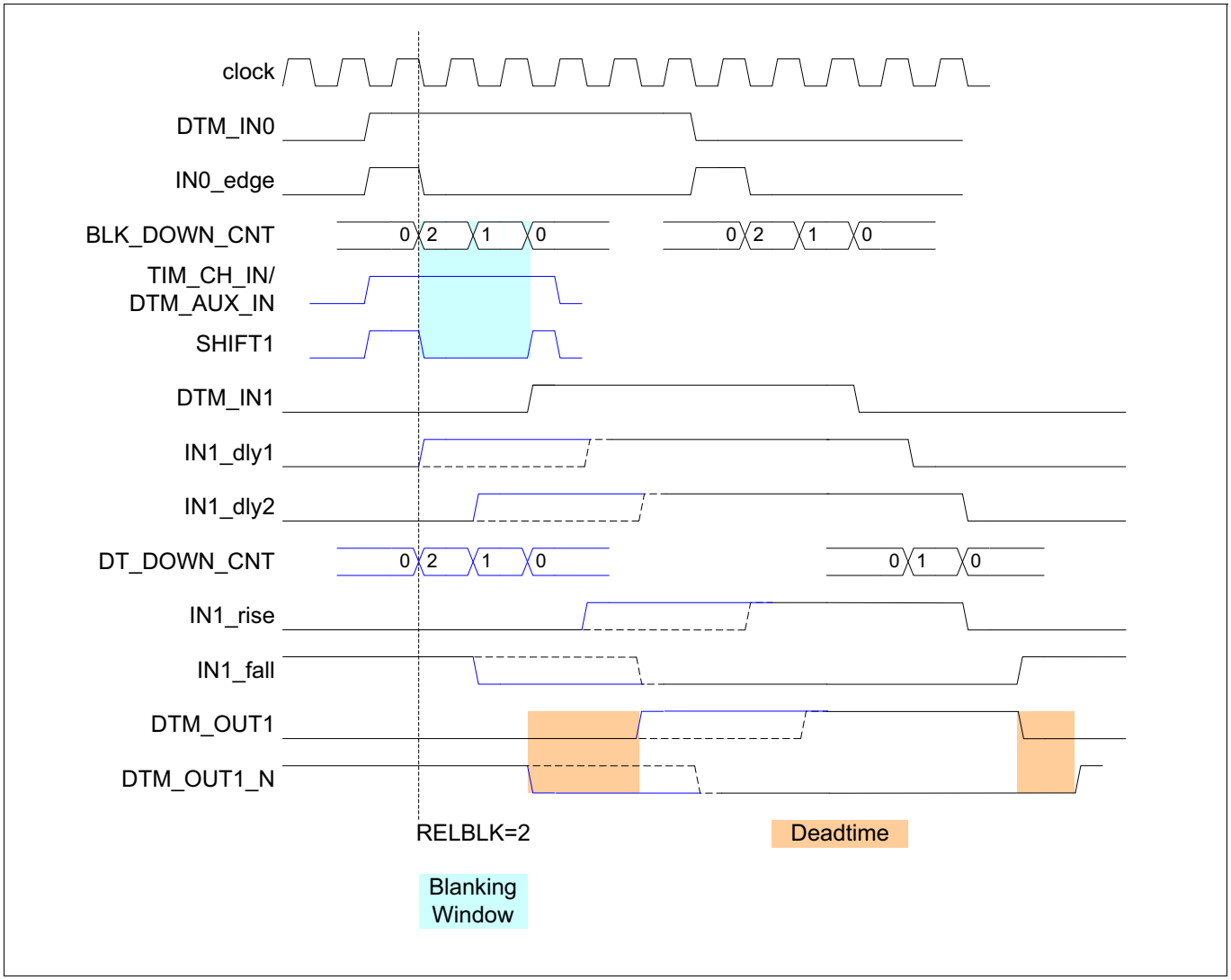


Figure 102 Example wave of phase shift on channel 1

28.16.4 Multiple output signal combination

Each channel provides additionally the possibility to combine the channel inputs *DTM_IN[x]* and *SHIFT[x]* or *COUT[x-1]* (selected by **I1SEL_[x]**) by an AND or an XOR gate (selected by **O1F_[x]**).

It is recommended to use the combination of signals only if bit field **RELBLK** of register **DTM[i]_PS_CTRL** is 0. Otherwise, the signal *TIM_CH_IN0, TIM_CH_IN1 or DTM_AUX_IN* may be disturbed by the blanking window counter.

Together with the inverter inside sub-module DTM_PSU (selected by **IN_POL**), the inverter on each output of a channel (selected by **POL0_[x]**/**POL1_[x]**) and the possibility to change polarity of *DTM_IN[x]* inside connected TOM/ATOM channel, a (N)AND, (N)OR or X(N)OR combination of the signals is possible.

28.16.4.1 Combination of input signal TIM_CH_IN/AUX_IN with TOM/ATOM signal

If the input selection **I1SEL_[x]** of a channel x is set to 0, the output selection **O1SEL_[x]** is set to 1 and **SWAP_[x]** is set to 0, depending on **PSU_IN_SEL** either *TIM_CH_IN0, TIM_CH_IN1* or *DTM_AUX_IN* can be combined with signal *DTM_IN[x]*.

The function of combination on DTM output *DTM[i]_OUT[x]_N* (and also *COUT[x]*) is defined by **O1F_[x]** in the following way:

Table 61 Function of combination on DTM channel x=0 output DTM[i]_OUT[x]_N (and also COUT[x])

	O1F_x	POL1_x	IN_POL	(A)TOM output inverted
XOR	01	0	0	no
AND	10	0	0	no
XNOR	01	1	0	no
NAND	10	1	0	no
XNOR	01	1	1	yes
OR	10	1	1	yes
XOR	01	0	1	yes
NOR	10	0	1	yes

*Note: The inversion of the (A)TOM output can be reached by switching the **SL** bit (for TOM and ATOM SOMP/SOMC mode).*

28.16.4.2 Combination of multiple TOM/ATOM output signals

If the input selection **I1SEL_[x]** of a channel x (with x=1…3) is set to 1, the output selection **O1SEL_[x]** is set to 1 and **SWAP_[x]** is set to 0, the output of the preceding DTM channel *COUT[x-1]* can be combined with signal *DTM_IN[x]*.

The function of combination on DTM output *DTM[i]_OUT[x]_N* (and also *COUT[x]*) is defined by **O1F_[x]** in the following way:

Table 62 Function of combination on DTM on channel x=1…3 output DTM[i]_OUT[x]_N (and also COUT[x])

	O1F_x	POL1_x	POL1_x-1	(A)TOM output inverted
XOR	01	0	0	no
AND	10	0	0	no
XNOR	01	1	0	no
NAND	10	1	0	no
XNOR	01	1	1	yes
OR	10	1	1	yes
XOR	01	0	1	yes
NOR	10	0	1	yes

By setting **I1SEL_[x]** to 1 on all four channel, a combination of all four signals *DTM_IN0* to *DTM_IN3* can be achieved (combinatorial chain).

To allow also combination of signals generated for output *DTM[i]_OUT[x]*, the outputs 0 and 1 can be swapped by setting bit **SWAP_ [x]** for channel x.

28.16.4.3 Pulse generation on edge

Another feature of the DTM is to generate on the second output *DTM[i]_OUT[x]_N* a pulse on every edge of corresponding input signal *DTM[i]_IN[x]*.

This can be reached by configuring **O1SEL_[x]** to 1, i.e. selecting signal *edge_trigg_[x]* as the output signal (**O1F_[x]** has to be 0b00). The signal *edge_trigg_[x]* is depicted in **Figure 99**.

The pulse length can be adjusted individually for each edge type by the configuration value **REL_RISE** and **REL_FALL** of register **DTM[i]_CH[x]_DV**.

The parameter **REL_RISE** defines the pulse length in case of a rising edge on input *DTM[i]_IN[x]*, the parameter **REL_FALL** define the pulse length in case of a falling edge on input *DTM[i]_IN[x]*.

The generated edge signal *edge_trigg_[x]* can be combined with the output signal of the preceding DTM channel x-1 at channel input *COUT[x-1]* (see **Figure 98**).

With the configuration of **CIS[x]**=1 and **I1SEL_[x]**=1, **CII[x]**=0 and **POL1_[x]**=1, the signal *edge_trigg_[x]* of channel x is ORed with the inverse signal at channel input *COUT[x-1]*. The signal at **COUT[x-1]** can be inverted by changing **POL1_[x-1]** of channel x-1.

As a result of this configuration one can generate at each edge on DTM input *DTM_IN[x]* a pulse signal and OR-combine these generated pulse signals with the generated signal of preceding DTM channel. If the combinatorial chain is configured over all four DTM channel the final signal is available at last DTM output *DTM_OUT3_N*.

28.16.5 Synchronous update of channel control register 2

It is possible to use the shadow register **DTM[i]_CH_CTRL2_SR** and a selected edge of one of the channel 0 to 3 to update the work register **DTM[i]_CH_CTRL2**.

The update mechanism and its configuration are depicted in **Figure 103**.

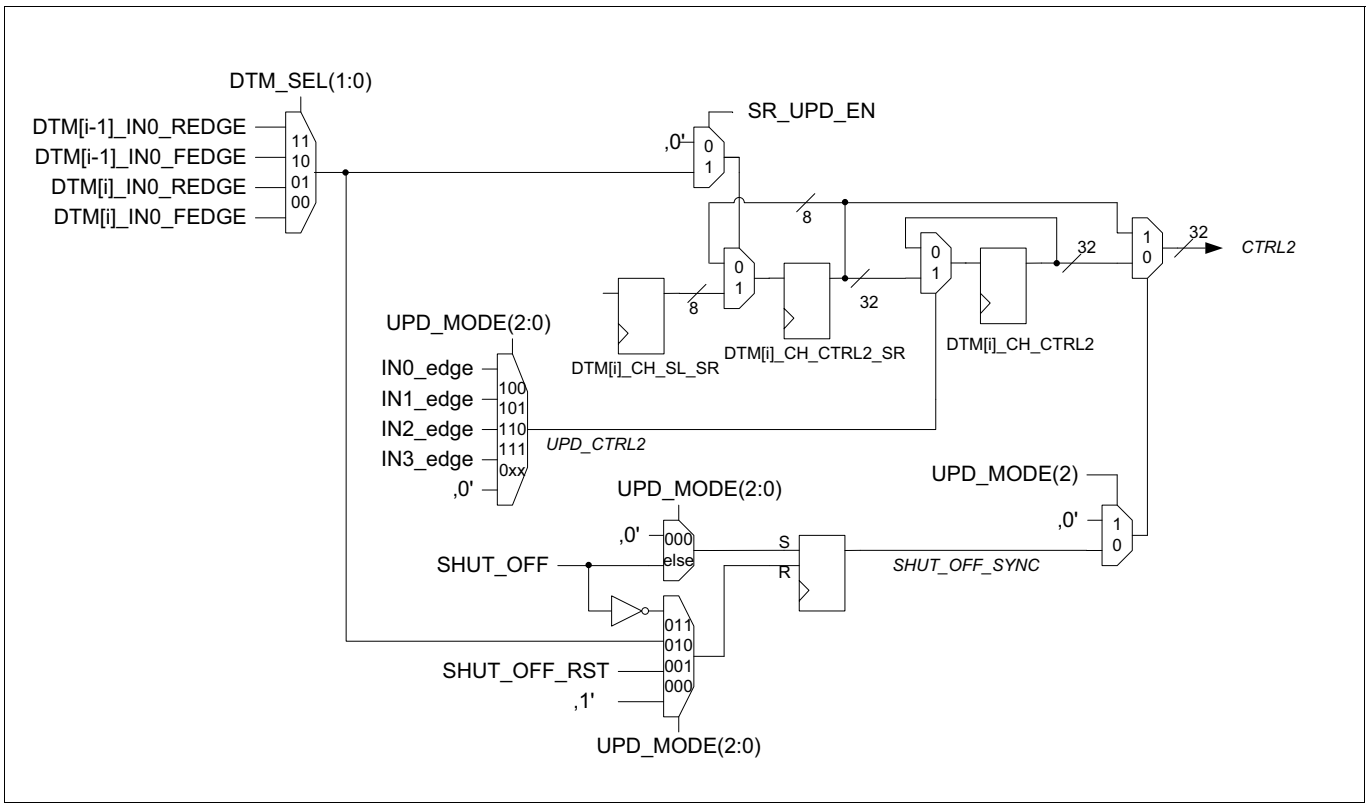


Figure 103 Synchronous update mechanism of register DTM[i]_CH_CTRL2

If enabled by the bit field **UPD_MODE** of register **DTM[i]_CTRL** (i.e. **UPD_MODE**=1xx), the register **DTM[i]_CH_CTRL2_SR** serves as a shadow register of register **DTM[i]_CH_CTRL2**. The update is then triggered by an edge on one of the selected inputs *DTM_IN0* to *DTM_IN3*.

The synchronous update allows the user to change output polarity, the selection of constant signal level, the constant signal level itself and the switch to/from feed through path on all four channels in parallel synchronized to one of the input edges on *DTM_IN0* to *DTM_IN3*.

28.16.6 DTM output shut off

A fast shut off for the eight outputs of DTM instance i can be triggered by one of the two assigned inputs TIM[n]_CH_IN or DTM[i]_AUX_IN or the two inputs TIM[m]_CH_IN or DTM[i-1]_AUX_IN of the previous DTM instance i-1. The selection of the trigger signal source is done by the bits **PSU_IN_SEL** and **DTM_SEL(1)** (see **Figure 101**). The selected trigger signal is named *SHUT_OFF*.

Enabling of the shut off feature is done by setting **UPD_MODE(2:0)** to one of the values 0b001, 0b010 or 0b011.

The shut off behavior of the DTM outputs is defined by the value of register **DTM[i]_CH_CTRL2_SR**.

If the shut off feature is enabled by **UPD_MODE**, as long as the signal *SHUT_OFF_SYNC* is 0, the register **DTM[i]_CH_CTRL2** defines the output signal behavior.

If the signal *SHUT_OFF_SYNC* is 1, the register **DTM[i]_CH_CTRL2_SR** defines the output signal behavior.

The signal *SHUT_OFF_SYNC* is set to 1 if signal *SHUT_OFF* switches to 1.The reset depends on value of **UPD_MODE(2:0)**.

There are three different ways to reset the signal *SHUT_OFF_SYNC* to 0:

- the CPU writes a 1 to bit **SHUT_OFF_RST** of register **DTM_CH_CTRL1**
- synchronous to an edge on DTM channel 0 input of this DTM instance i or on an edge on DTM channel 0 input of preceding DTM instance i-1.
- asynchronous if signal *SHUT_OFF* switches back to 0

Additionally, setting UPD_MODE(2:0) to value 0b000 or 0b1xx resets also the signal SHUT_OFF_SYNC.

Figure 103 depicts the shut off feature and the different shut off release possibilities.

Note: The reset of SHUT_OFF_SYNC has lower priority than the set of this signal.

A second shadow register **DTM[i]_CH_SR** exist for the eight **SL** bits (SLx_y_SR) of the shadow register **DTM[i]_CH_CTRL2_SR**.

If enabled by configuration bit **SR_UPD_EN** of register **DTM[i]_CTRL**, the update of **SL** bits of register **DTM[i]_CH_CTRL2_SR** can be triggered by one of the signals selected by bit field **DTM_SEL** of register **DTM[i]_CTRL**. This trigger signal is either the rising or the falling edge detected on *DTM[i]_IN0* of instance i or the rising or the falling edge on *DTM[i-1]_IN0* of preceding instance i-1.

As depicted in **Figure 95** the DTM input signal *TIM_CH_IN0, TIM_CH_IN1 or DTM_AUX_IN* can be forwarded to the succeeding instance. Thus, it can be used to trigger shut off in two consecutive DTM instances.

28.16.7 DTM connections on GTM top level

The DTM, if present, is placed behind the outputs of a TOM or ATOM. The outputs of the DTM are routed directly to the top level ports of GTM.If there is a DTM placed behind a TOM or ATOM depends on the GTM device configuration.

In case of a DTM behind a TOM or ATOM, the outputs (A)TOM_OUT and (A)TOM_OUT_T are connected to DTM inputs DTM_IN and DTM_IN_T. The outputs of the DTM are routed directly to the top level of GTM.The behavior of DTM after reset is shown in **Figure 104**.

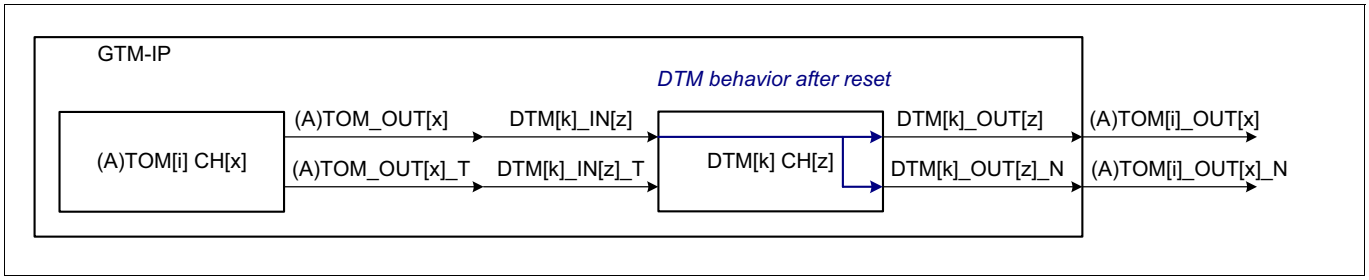


Figure 104 DTM behavior after reset

To route the signal *DTM[k]_IN[z]_T* to the DTM output DTM_[k]_OUT[z]_N, the following DTM channel configuration has to be chosen:

O1F_[x] = 11, **O1SEL_[x]**=1 and **DT1_[x]**=1.

The signals names and the signal routing in the case of no DTM instance is placed behind a TOM or ATOM is shown in **Figure 105**.

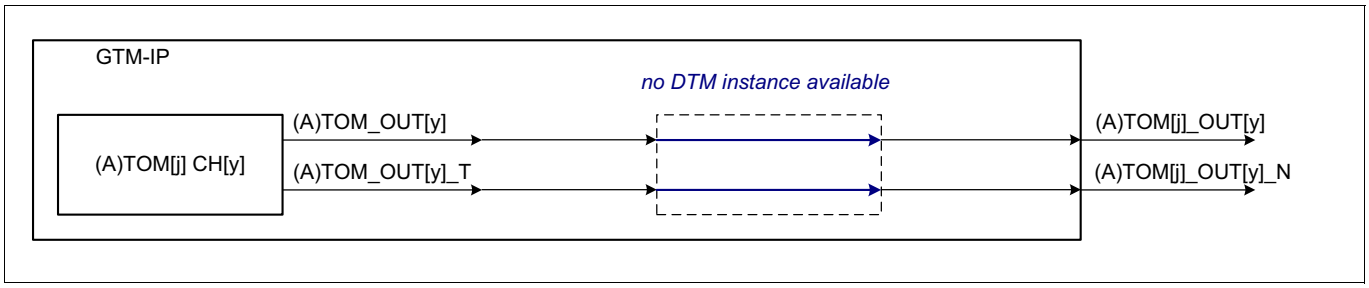


Figure 105 (A)TOM output signal routing in case of no DTM instance available

28.16.8 CDTM Configuration Register Overview

Table 63 Configuration Register Overview

Register name	Description	see Page
CDTM[i]_DTM[j]_CTRL	CDTMi DTMj global configuration and control register	332
CDTM[i]_DTM[j]_CH_CTRL1	CDTMi DTMj channel control register 1	334
CDTM[i]_DTM[j]_CH_CTRL2	CDTMi DTMj channel control register 2	337
CDTM[i]_DTM[j]_CH_CTRL2_SR	CDTMi DTMj channel control register 2 shadow	340
CDTM[i]_DTM[j]_CH_CTRL3	CDTMi DTMj channel control register 3	343
CDTM[i]_DTM[j]_PS_CTRL	CDTMi DTMj phase shift unit configuration and control register	345
CDTM[i]_DTM[j]_CH[z]_DTV	CDTMi DTMj dead time reload values	346
CDTM[i]_DTM[j]_CH_SR	CDTM DTMj channel shadow register	347

28.16.9 Configuration Register Description

28.16.9.1 Register CDTM[i]_DTM[j]_CTRL

CDTM0 DTM0 Global Configuration and Control Register

CDTMi_DTMj_CTRL (i=0-4;j=0-1,4-5)
CDTMi DTMj Global Configuration and Control Register($0E4000_H$+i*400_H+j*40_H) Application Reset Value: $0000\ 0000_H$
CDTMi_DTMj_CTRL (i=5-6;j=0-3)
CDTMi DTMj Global Configuration and Control Register($0E4000_H$+i*400_H+j*40_H) Application Reset Value: $0000\ 0000_H$
CDTMi_DTMj_CTRL (i=0-4;j=2-3)
CDTMi DTMj Global Configuration and Control Register($0E4000_H$+i*400_H+j*40_H) Application Reset Value: $0000\ 0000_H$
CDTMi_DTMj_CTRL (i=5-6;j=4-5)
CDTMi DTMj Global Configuration and Control Register($0E4000_H$+i*400_H+j*40_H) Application Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															SHUT_OFF_RST
r															rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							SR_UPD_EN	0	UPD_MODE			DTM_SEL		CLK_SEL	
r							rw	r	rw			rw		rw	

Field	Bits	Type	Description
CLK_SEL	1:0	rw	**Clock source select** 00_B SYS_CLK selected 01_B CMU_CLK0 selected 10_B CMU_CLK1 selected (if DTM is connected to an ATOM) / CMU_FXCLK0 selected (if DTM is connected to a TOM) 11_B CMU_CLK2 selected (if DTM is connected to an ATOM) / CMU_FXCLK1 selected (if DTM is connected to a TOM)
DTM_SEL	3:2	rw	**Select DTM update and SHUT_OFF reset signal** $0X_B$ Shut off by signal *TIM_CH_IN0*, *TIM_CH_IN1* or *DTM_AUX_IN* $1X_B$ Shut off by signal *DTM[i-1]_PSU_IN* 00_B Select falling edge on DTM[i] channel 0 input 01_B Select rising edge on DTM[i] channel 0 input 10_B Select falling edge on DTM[i-1] channel 0 input 11_B Select rising edge on DTM[i-1] channel 0 input 0b1 = shut off by signal DTM[i-1]_PSU_IN

Field	Bits	Type	Description
UPD_MODE	6:4	rw	**Update mode** *Note: If an INx_edge is not implemented, the value is unused. A write with this unused value returns 0b10 on status.* 000_B Asynchronous update - DTM[i]_CH_CTRL2_SR not used for update of DTM[i]_CH_CTRL2 001_B Shut off release by writing 1 to bit SHUT_OFF_RST of register DTM[i]_CTRL 010_B Shut off release by an edge on DTM[i]_IN0 or DTM[i-1]_IN0 (defined by bit field DTM_SEL of register DTM[i]_CTRL) 011_B Shut off release by shut off signal SHUT_OFF (defined by bits PSU_IN_SEL and IN_POL of register DTM[i]_PS_CTRL and DTM_SEL(2) of register DTM[i]_CTRL) 100_B Signal IN0_edge used to trigger update of DTM[i]_CH_CTRL2 with content of DTM[i]_CH_CTRL2_SR 101_B Signal IN1_edge used to trigger update of DTM[i]_CH_CTRL2 with content of DTM[i]_CH_CTRL2_SR 110_B Signal IN2_edge used to trigger update of DTM[i]_CH_CTRL2 with content of DTM[i]_CH_CTRL2_SR 111_B Signal IN3_edge used to trigger update of DTM[i]_CH_CTRL2 with content of DTM[i]_CH_CTRL2_SR
SR_UPD_EN	8	rw	**Shadow register update enable** 0_B No update of SLx_y_SR register bits in register DTM[i]_CH_CTRL2_SR 1_B Update of SLx_y_SR register bits in register DTM[i]_CH_CTRL2_SR on trigger
SHUT_OFF_RST	16	rw	**Shut off reset** Writing a 1 releases shut off (resets signal *SHUT_OFF_SYNC* if selected by UPD_MODE(2:0)=0b001)
0	7, 15:9, 31:17	r	**Reserved** Read as zero, shall be written as zero.

28.16.9.2 Register CDTM[i]_DTM[j]_CH_CTRL1

CDTM0 DTM0 Channel Control Register 1

CDTMi_DTMj_CH_CTRL1 (i=0-4;j=0-1,4-5)
CDTMi DTMj Channel Control Register 1 ($0E4004_H$+i*400_H+j*40_H) **Application Reset Value: 0000 0000_H**
CDTMi_DTMj_CH_CTRL1 (i=5-6;j=0-3)
CDTMi DTMj Channel Control Register 1 ($0E4004_H$+i*400_H+j*40_H) **Application Reset Value: 0000 0000_H**
CDTMi_DTMj_CH_CTRL1 (i=0-4;j=2-3)
CDTMi DTMj Channel Control Register 1 ($0E4004_H$+i*400_H+j*40_H) **Application Reset Value: 0000 0000_H**
CDTMi_DTMj_CH_CTRL1 (i=5-6;j=4-5)
CDTMi DTMj Channel Control Register 1 ($0E4004_H$+i*400_H+j*40_H) **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		O1F_3		SWAP_3	SH_EN_3	I1SEL_3	O1SEL_3	0	XDT_EN_2_3	O1F_2		SWAP_2	SH_EN_2	I1SEL_2	O1SEL_2
r		rw		rw	rw	rw	rw	r	rw	rw		rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		O1F_1		SWAP_1	SH_EN_1	I1SEL_1	O1SEL_1	0	XDT_EN_0_1	O1F_0		SWAP_0	0	I1SEL_0	O1SEL_0
r		rw		rw	rw	rw	rw	r	rw	rw		rw	r	rw	rw

Field	Bits	Type	Description
O1SEL_0	0	rw	**Output 1 select channel 0** 0_B Inverse dead time signal selected 1_B Special function on output 1 selected (defined by O1F_0)
I1SEL_0	1	rw	**Input 1 select channel 0** *Note: If i is even, I1SEL_0 is not implemented. Then the bit is read as zero and shall be written as zero.* 0_B Signal (PSU_)SHIFT0 selected 1_B Signal COUT3 from DTM[i-1] selected
SWAP_0	3	rw	**Swap outputs DTM[i]_CH[0]_OUT0 and DTM[i]_CH[0]_OUT1 (before final output register)** 0_B Outputs not swapped 1_B Swap outputs DTM[i]_OUT0 and DTM[i]_OUT0_N
O1F_0	5:4	rw	**Output 1 function channel 0** 00_B Signal edge_trigg is selected 01_B XOR of DTM[i]_IN0 and signal SHIFT0 10_B AND of DTM[i]_IN0 and signal SHIFT0 11_B DTM[i]_IN0_T selected

Field	Bits	Type	Description
XDT_EN_0_1	6	rw	**Cross dead time enable on channels 0 and 1** *Note: TSEL0_[x] and SH_EN_1 must be '0' for using cross dead time to avoid wrong input signals. (x:0,1)* 0_B Cross dead time disabled on channels 0 and 1 1_B Cross dead time enabled on channels 0 and 1 *Note: When a '1' is written to bit XDT_EN_0_1, the internal register IN[x]_dly1, IN[x]_dly2 and DT_DOWN_CNT is reset to '0' (x:0,1)*
O1SEL_1	8	rw	**Output 1 select channel 1** 0_B Inverse dead time signal selected 1_B Special function on output 1 selected (defined by O1F_1)
I1SEL_1	9	rw	**Input 1 select channel 1** 0_B Signal (PSU_)SHIFT1 selected 1_B Signal COUT1 selected
SH_EN_1	10	rw	**Shift enable channel 1** 0_B DTM[i]_IN0 is not used; no input signal shift 1_B Signal selected by I1SEL_1 triggers update of DTM[i]_IN1 with input of DTM[i]_IN0 -> input signal shift
SWAP_1	11	rw	**Swap outputs DTM[i]_CH[1]_OUT0 and DTM[i]_CH[1]_OUT1 (before final output register)** 0_B Outputs not swapped 1_B Swap outputs DTM[i]_OUT1 and DTM[i]_OUT1_N
O1F_1	13:12	rw	**Output 1 function channel 1** 00_B Signal edge_trigg is selected 01_B XOR of DTM[i]_IN1 and signal SHIFT1/OUT0 10_B AND of DTM[i]_IN1 and signal SHIFT1/OUT0 11_B DTM[i]_IN1_T selected
O1SEL_2	16	rw	**Output 1 select channel 2** 0_B Inverse dead time signal selected 1_B Special function on output 1 selected (defined by O1F_2)
I1SEL_2	17	rw	**Input 1 select channel 2** 0_B Signal (PSU_)SHIFT2 selected 1_B Signal COUT1 selected
SH_EN_2	18	rw	**Shift enable channel 2** 0_B DTM[i]_IN1 is not used; no input signal shift 1_B Signal selected by I1SEL_2 triggers update of DTM[i]_IN2 with input of DTM[i]_IN1 -> input signal shift
SWAP_2	19	rw	**Swap outputs DTM[i]_CH[2]_OUT0 and DTM[i]_CH[2]_OUT1 (before final output register)** 0_B Outputs not swapped 1_B Swap outputs DTM[i]_OUT2 and DTM[i]_OUT2_N
O1F_2	21:20	rw	**Output 1 function channel 2** 00_B Signal edge_trigg is selected 01_B XOR of DTM[i]_IN2 and signal SHIFT2/OUT1 10_B AND of DTM[i]_IN2 and signal SHIFT2/OUT1 11_B DTM[i]_IN2_T selected

Field	Bits	Type	Description
XDT_EN_2_3	22	rw	**Cross dead time enable on channels 0 and 1** *Note: TSEL0_[x] and SH_EN_[x] must be '0' for using cross dead time to avoid wrong input signals. (x:2,3)* 0_B Cross dead time disabled on channels 2 and 3 1_B Cross dead time enabled on channels 2 and 3 *Note: When a '1' is written to bit XDT_EN_2_3, the internal register IN[x]_dly1, IN[x]_dly2 and DT_DOWN_CNT is reset to '0' (x:2,3)*
O1SEL_3	24	rw	**Output 1 select channel 3** 0_B Inverse dead time signal selected 1_B Special function on output 1 selected (defined by O1F_3)
I1SEL_3	25	rw	**Input 1 select channel 3** 0_B Signal (PSU_)SHIFT3 selected 1_B Signal COUT2 selected
SH_EN_3	26	rw	**Shift enable channel 3** 0_B DTM[i]_IN2 is not used; no input signal shift 1_B Signal selected by I1SEL_3 triggers update of DTM[i]_IN3 with input of TM[i]_IN2-> input signal shift
SWAP_3	27	rw	**Swap outputs DTM[i]_CH[3]_OUT0 and DTM[i]_CH[3]_OUT1 (before final output register)** 0_B Outputs not swapped 1_B Swap outputs DTM[i]_OUT3 and DTM[i]_OUT3_N
O1F_3	29:28	rw	**Output 1 function channel 3** 00_B Signal edge_trigg is selected 01_B XOR of DTM[i]_IN3 and signal SHIFT3 / OUT2 10_B AND of DTM[i]_IN3 and signal SHIFT3 / OUT2 11_B DTM[i]_IN3_T selected
0	2, 7, 15:14, 23, 31:30	r	**Reserved** Read as zero, shall be written as zero.

28.16.9.3 Register CDTM[i]_DTM[j]_CH_CTRL2

CDTM0 DTM0 Channel Control Register 2

CDTMi_DTMj_CH_CTRL2 (i=0-4;j=0-1,4-5)
CDTMi DTMj Channel Control Register 2 ($0E4008_H$+i*400_H+j*40_H) **Application Reset Value: 0000 0000_H**
CDTMi_DTMj_CH_CTRL2 (i=5-6;j=0-3)
CDTMi DTMj Channel Control Register 2 ($0E4008_H$+i*400_H+j*40_H) **Application Reset Value: 0000 0000_H**
CDTMi_DTMj_CH_CTRL2 (i=0-4;j=2-3)
CDTMi DTMj Channel Control Register 2 ($0E4008_H$+i*400_H+j*40_H) **Application Reset Value: 0000 0000_H**
CDTMi_DTMj_CH_CTRL2 (i=5-6;j=4-5)
CDTMi DTMj Channel Control Register 2 ($0E4008_H$+i*400_H+j*40_H) **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DT1_3	**SL1_3**	**OC1_3**	**POL1_3**	**DT0_3**	**SL0_3**	**OC0_3**	**POL0_3**	**DT1_2**	**SL1_2**	**OC1_2**	**POL1_2**	**DT0_2**	**SL0_2**	**OC0_2**	**POL0_2**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DT1_1	**SL1_1**	**OC1_1**	**POL1_1**	**DT0_1**	**SL0_1**	**OC0_1**	**POL0_1**	**DT1_0**	**SL1_0**	**OC1_0**	**POL1_0**	**DT0_0**	**SL0_0**	**OC0_0**	**POL0_0**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
POL0_0	0	rw	**Polarity on output 0 channel 0** 0_B Output signal not inverted 1_B Output signal inverted
OC0_0	1	rw	**Output 0 control channel 0** 0_B Functional output 1_B Constant output defined by SL0_0
SL0_0	2	rw	**Signal level on output 0 channel 0** 0_B Signal Level is 0 on output if OC0_0=1 1_B Signal Level is 1 on output if OC0_0=1
DT0_0	3	rw	**Dead time path enable on output 0 channel 0** 0_B Feed through from DTM_IN0 to DTM[i]_OUT0 enabled 1_B Dead time path enabled
POL1_0	4	rw	**Polarity on output 1 channel 0** 0_B Output signal not inverted 1_B Output signal inverted
OC1_0	5	rw	**Output 1 control channel 0** 0_B Functional output 1_B Constant output defined by SL1_0
SL1_0	6	rw	**Signal level on output 1 channel 0** 0_B Signal Level is 0 on output if OC1_0=1 1_B Signal Level is 1 on output if OC1_0=1

Field	Bits	Type	Description
DT1_0	7	rw	**Dead time path enable on output 1 channel 0** 0_B Feed through from DTM_IN0 to DTM[i]_OUT0_N enabled 1_B Dead time path enabled
POL0_1	8	rw	**Polarity on output 0 channel 1** 0_B Output signal not inverted 1_B Output signal inverted
OC0_1	9	rw	**Output 0 control channel 1** 0_B Functional output 1_B Constant output defined by SL0_1
SL0_1	10	rw	**Signal level on output 0 channel 1** 0_B Signal Level is 0 on output if OC0_1=1 1_B Signal Level is 1 on output if OC0_1=1
DT0_1	11	rw	**Dead time path enable on output 0 channel 1** 0_B Feed through from DTM_IN1 to DTM[i]_OUT1 enabled 1_B Dead time path enabled
POL1_1	12	rw	**Polarity on output 1 channel 1** 0_B Output signal not inverted 1_B Output signal inverted
OC1_1	13	rw	**Output 1 control channel 1** 0_B Functional output 1_B Constant output defined by SL1_1
SL1_1	14	rw	**Signal level on output 1 channel 1** 0_B Signal Level is 0 on output if OC1_1=1 1_B Signal Level is 1 on output if OC1_1=1
DT1_1	15	rw	**Dead time path enable on output 1 channel 1** 0_B Feed through from DTM_IN1 to DTM[i]_OUT1_N enabled 1_B Dead time path enabled
POL0_2	16	rw	**Polarity on output 0 channel 2** 0_B Output signal not inverted 1_B Output signal inverted
OC0_2	17	rw	**Output 0 control channel 2** 0_B Functional output 1_B Constant output defined by SL0_2
SL0_2	18	rw	**Signal level on output 0 channel 2** 0_B Signal Level is 0 on output if OC0_2=1 1_B Signal Level is 1 on output if OC0_2=1
DT0_2	19	rw	**Dead time path enable on output 0 channel 2** 0_B Feed through from DTM_IN2 to DTM[i]_OUT2 enabled 1_B Dead time path enabled
POL1_2	20	rw	**Polarity on output 1 channel 2** 0_B Output signal not inverted 1_B Output signal inverted
OC1_2	21	rw	**Output 1 control channel 2** 0_B Functional output 1_B Constant output defined by SL1_2

Field	Bits	Type	Description
SL1_2	22	rw	**Signal level on output 1 channel 2** 0_B Signal Level is 0 on output if OC1_2=1 1_B Signal Level is 1 on output if OC1_2=1
DT1_2	23	rw	**Dead time path enable on output 1 channel 2** 0_B Feed through from DTM_IN2 to DTM[i]_OUT2_N enabled 1_B Dead time path enabled
POL0_3	24	rw	**Polarity on output 0 channel 3** 0_B Output signal not inverted 1_B Output signal inverted
OC0_3	25	rw	**Output 0 control channel 3** 0_B Functional output 1_B Constant output defined by SL0_3
SL0_3	26	rw	**Signal level on output 0 channel 3** 0_B Signal Level is 0 on output if OC0_3=1 1_B Signal Level is 1 on output if OC0_3=1
DT0_3	27	rw	**Dead time path enable on output 0 channel 3** 0_B Feed through from DTM_IN3 to DTM[i]_OUT3 enabled 1_B Dead time path enabled
POL1_3	28	rw	**Polarity on output 1 channel 3** 0_B Output signal not inverted 1_B Output signal inverted
OC1_3	29	rw	**Output 1 control channel 3** 0_B Functional output 1_B Constant output defined by SL1_3
SL1_3	30	rw	**Signal level on output 1 channel 3** 0_B Signal Level is 0 on output if OC1_3=1 1_B Signal Level is 1 on output if OC1_3=1
DT1_3	31	rw	**Dead time path enable on output 1 channel 3** 0_B Feed through from DTM_IN3 to DTM[i]_OUT3_N enabled 1_B Dead time path enabled

28.16.9.4 Register CDTM[i]_DTM[j]_CH_CTRL2_SR

CDTM0 DTM0 Channel Control Register 2 Shadow

CDTMi_DTMj_CH_CTRL2_SR (i=0-4;j=0-1,4-5)
CDTMi DTMj Channel Control Register 2 Shadow($0E400C_H$+i*400_H+j*40_H) Application Reset Value: $0000\ 0000_H$
CDTMi_DTMj_CH_CTRL2_SR (i=5-6;j=0-3)
CDTMi DTMj Channel Control Register 2 Shadow($0E400C_H$+i*400_H+j*40_H) Application Reset Value: $0000\ 0000_H$
CDTMi_DTMj_CH_CTRL2_SR (i=0-4;j=2-3)
CDTMi DTMj Channel Control Register 2 Shadow($0E400C_H$+i*400_H+j*40_H) Application Reset Value: $0000\ 0000_H$
CDTMi_DTMj_CH_CTRL2_SR (i=5-6;j=4-5)
CDTMi DTMj Channel Control Register 2 Shadow($0E400C_H$+i*400_H+j*40_H) Application Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DT1_3_SR	SL1_3_SR	OC1_3_SR	POL1_3_SR	DT0_3_SR	SL0_3_SR	OC0_3_SR	POL0_3_SR	DT1_2_SR	SL1_2_SR	OC1_2_SR	POL1_2_SR	DT0_2_SR	SL0_2_SR	OC0_2_SR	POL0_2_SR
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DT1_1_SR	SL1_1_SR	OC1_1_SR	POL1_1_SR	DT0_1_SR	SL0_1_SR	OC0_1_SR	POL0_1_SR	DT1_0_SR	SL1_0_SR	OC1_0_SR	POL1_0_SR	DT0_0_SR	SL0_0_SR	OC0_0_SR	POL0_0_SR
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
POL0_0_SR	0	rw	**Polarity on output 0 channel 0 shadow register** 0_B Output signal not inverted 1_B Output signal inverted
OC0_0_SR	1	rw	**Output 0 control channel 0 shadow register** 0_B Functional output 1_B Constant output defined by SL0_0
SL0_0_SR	2	rw	**Signal level on output 0 channel 0 shadow register** 0_B Signal Level is 0 on output if OC0_0=1 1_B Signal Level is 1 on output if OC0_0=1
DT0_0_SR	3	rw	**Dead time path enable on output 0 channel 0 shadow register** 0_B Feed through from DTM_IN0 to DTM[i]_OUT0 enabled 1_B Dead time path enabled
POL1_0_SR	4	rw	**Polarity on output 1 channel 0 shadow register** 0_B Output signal not inverted 1_B Output signal inverted

Field	Bits	Type	Description
OC1_0_SR	5	rw	**Output 1 control channel 0 shadow register** 0_B Functional output 1_B Constant output defined by SL1_0
SL1_0_SR	6	rw	**Signal level on output 1 channel 0 shadow register** 0_B Signal Level is 0 on output if OC1_0=1 1_B Signal Level is 1 on output if OC1_0=1
DT1_0_SR	7	rw	**Dead time path enable on output 1 channel 0 shadow register** 0_B Feed through from DTM_IN0 to DTM[i]_OUT0_N enabled 1_B Dead time path enabled
POL0_1_SR	8	rw	**Polarity on output 0 channel 1 shadow register** 0_B Output signal not inverted 1_B Output signal inverted
OC0_1_SR	9	rw	**Output 0 control channel 1 shadow register** 0_B Functional output 1_B Constant output defined by SL0_1
SL0_1_SR	10	rw	**Signal level on output 0 channel 1 shadow register** 0_B Signal Level is 0 on output if OC0_1=1 1_B Signal Level is 1 on output if OC0_1=1
DT0_1_SR	11	rw	**Dead time path enable on output 0 channel 1 shadow register** 0_B Feed through from DTM_IN1 to DTM[i]_OUT1 enabled 1_B Dead time path enabled
POL1_1_SR	12	rw	**Polarity on output 1 channel 1 shadow register** 0_B Output signal not inverted 1_B Output signal inverted
OC1_1_SR	13	rw	**Output 1 control channel 1 shadow register** 0_B Functional output 1_B Constant output defined by SL1_1
SL1_1_SR	14	rw	**Signal level on output 1 channel 1 shadow register** 0_B Signal Level is 0 on output if OC1_1=1 1_B Signal Level is 1 on output if OC1_1=1
DT1_1_SR	15	rw	**Dead time path enable on output 1 channel 1 shadow register** 0_B Feed through from DTM_IN1 to DTM[i]_OUT1_N 1_B Dead time path enabled

Field	Bits	Type	Description
POL0_2_SR	16	rw	**Polarity on output 0 channel 2 shadow register** 0_B Output signal not inverted 1_B Output signal inverted
OC0_2_SR	17	rw	**Output 0 control channel 2 shadow register** 0_B Functional output 1_B Constant output defined by SL0_2
SL0_2_SR	18	rw	**Signal level on output 0 channel 2 shadow register** 0_B Signal Level is 0 on output if OC0_2=1 1_B Signal Level is 1 on output if OC0_2=1
DT0_2_SR	19	rw	**Dead time path enable on output 0 channel 2 shadow register** 0_B Feed through from DTM_IN2 to DTM[i]_OUT2 1_B Dead time path enabled
POL1_2_SR	20	rw	**Polarity on output 1 channel 2 shadow register** 0_B Output signal not inverted 1_B Output signal inverted
OC1_2_SR	21	rw	**Output 1 control channel 2 shadow register** 0_B Functional output 1_B Constant output defined by SL1_2
SL1_2_SR	22	rw	**Signal level on output 1 channel 2 shadow register** 0_B Signal Level is 0 on output if OC1_2=1 1_B Signal Level is 1 on output if OC1_2=1
DT1_2_SR	23	rw	**Dead time path enable on output 1 channel 2 shadow register** 0_B Feed through from DTM_IN2 to DTM[i]_OUT2_N 1_B Dead time path enabled
POL0_3_SR	24	rw	**Polarity on output 0 channel 3 shadow register** 0_B Output signal not inverted 1_B Output signal inverted
OC0_3_SR	25	rw	**Output 0 control channel 3 shadow register** 0_B Functional output 1_B Constant output defined by SL0_3
SL0_3_SR	26	rw	**Signal level on output 0 channel 3 shadow register** 0_B Signal Level is 0 on output if OC0_3=1 1_B Signal Level is 1 on output if OC0_3=1

Field	Bits	Type	Description
DT0_3_SR	27	rw	**Dead time path enable on output 0 channel 3 shadow register** 0_B Feed through from DTM_IN3 to DTM[i]_OUT3 1_B Dead time path enabled
POL1_3_SR	28	rw	**Polarity on output 1 channel 3 shadow register** 0_B Output signal not inverted 1_B Output signal inverted
OC1_3_SR	29	rw	**Output 1 control channel 3 shadow register** 0_B Functional output 1_B Constant output defined by SL1_3
SL1_3_SR	30	rw	**Signal level on output 1 channel 3 shadow register** 0_B Signal Level is 0 on output if OC1_3=1 1_B Signal Level is 1 on output if OC1_3=1
DT1_3_SR	31	rw	**Dead time path enable on output 1 channel 3 shadow register** 0_B Feed through from DTM_IN3 to DTM[i]_OUT3_N 1_B Dead time path enabled

28.16.9.5 Register CDTM[i]_DTM[j]_CH_CTRL3

CDTM0 DTM0 Channel Control Register 3

CDTMi_DTMj_CH_CTRL3 (i=0-4;j=0-1,4-5)
CDTMi DTMj Channel Control Register 3 ($0E4028_H+i*400_H+j*40_H$) **Application Reset Value: 0000 0000_H**
CDTMi_DTMj_CH_CTRL3 (i=5-6;j=0-3)
CDTMi DTMj Channel Control Register 3 ($0E4028_H+i*400_H+j*40_H$) **Application Reset Value: 0000 0000_H**
CDTMi_DTMj_CH_CTRL3 (i=0-4;j=2-3)
CDTMi DTMj Channel Control Register 3 ($0E4028_H+i*400_H+j*40_H$) **Application Reset Value: 0000 0000_H**
CDTMi_DTMj_CH_CTRL3 (i=5-6;j=4-5)
CDTMi DTMj Channel Control Register 3 ($0E4028_H+i*400_H+j*40_H$) **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0				TSEL1_3	TSEL0_3	CIS3	CII3	0				TSEL1_2	TSEL0_2	CIS2	CII2
r				rw	rw	rw	rw	r				rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				TSEL1_1	TSEL0_1	CIS1	CII1	0				TSEL1_0	TSEL0_0	CIS0	CII0
r				rw	rw	rw	rw	r				rw	rw	rw	rw

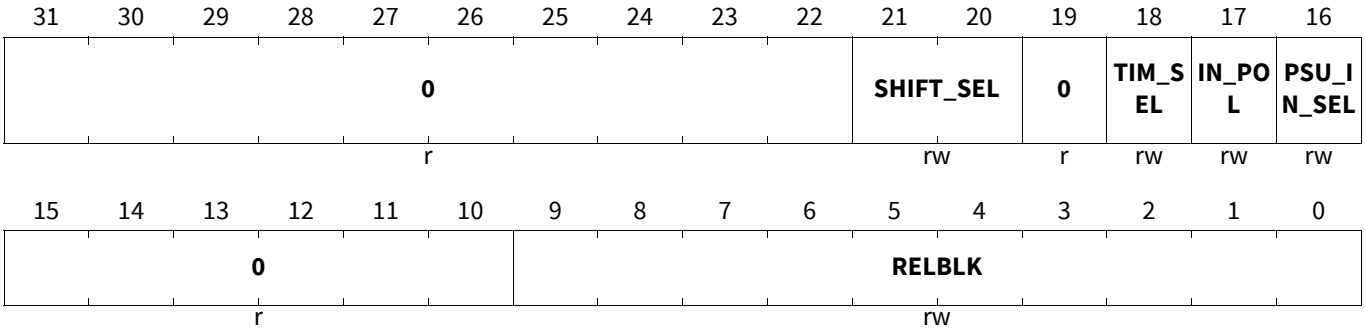
Field	Bits	Type	Description
CII0	0	rw	**Combinational input invert channel 0** 0_B Do not invert input 1_B Invert input
CIS0	1	rw	**Combinational input select channel 0** 0_B Select input DTM[i]_IN0 1_B Select internal signal edge_trigg_0
TSEL0_0	2	rw	**Input selection for dead time / edge trigger generation** 0_B Use DTM[i]_IN0 as input for dead time / edge trigger generation 1_B Use DTM[i]_IN0_T as input for dead time / edge trigger generation
TSEL1_0	3	rw	**Input selection combinational logic path** 0_B Use DTM[i]_IN0 as input for combinational logic path 1_B Use DTM[i]_IN0_T as input for combinational logic path
CII1	8	rw	**Combinational input invert channel 1** 0_B Do not invert input 1_B Invert input
CIS1	9	rw	**Combinational input select channel 1** 0_B Select input DTM[i]_IN1 1_B Select internal signal edge_trigg_1
TSEL0_1	10	rw	**Input selection for dead time / edge trigger generation** 0_B Use DTM[i]_IN1 as input for dead time / edge trigger generation 1_B Use DTM[i]_IN1_T as input for dead time / edge trigger generation
TSEL1_1	11	rw	**Input selection combinational logic path** 0_B Use DTM[i]_IN1 as input for combinational logic path 1_B Use DTM[i]_IN1_T as input for combinational logic path
CII2	16	rw	**Combinational input invert channel 2** 0_B Do not invert input 1_B Invert input
CIS2	17	rw	**Combinational input select channel 2** 0_B Select input DTM[i]_IN2 1_B Select internal signal edge_trigg_2
TSEL0_2	18	rw	**Input selection for dead time / edge trigger generation** 0_B Use DTM[i]_IN2 as input for dead time / edge trigger generation 1_B Use DTM[i]_IN2_T as input for dead time / edge trigger generation
TSEL1_2	19	rw	**Input selection combinational logic path** 0_B Use DTM[i]_IN2_T as input for dead time / edge trigger generation 1_B Use DTM[i]_IN2_T as input for combinational logic path
CII3	24	rw	**Combinational input invert channel 3** 0_B Do not invert input 1_B Invert input
CIS3	25	rw	**Combinational input select channel 3** 0_B Select input DTM[i]_IN3 1_B Select internal signal edge_trigg_3

Field	Bits	Type	Description
TSEL0_3	26	rw	**Input selection for dead time / edge trigger generation** 0_B Use DTM[i]_IN3 as input for dead time / edge trigger generation 1_B Use DTM[i]_IN3_T as input for dead time / edge trigger generation
TSEL1_3	27	rw	**Input selection combinational logic path** 0_B Use DTM[i]_IN3 as input for combinational logic path 1_B Use DTM[i]_IN3_T as input for combinational logic path
0	7:4, 15:12, 23:20, 31:28	r	**Reserved** Read as zero, shall be written as zero.

28.16.9.6 Register CDTM[i]_DTM[j]_PS_CTRL

CDTM0 DTM0 Phase Shift Unit Configuration and Control Register

CDTMi_DTMj_PS_CTRL (i=0-4;j=0-1,4-5)
CDTMi DTMj Phase Shift Unit Configuration and Control Register($0E4010_H$+i*400_H+j*40_H) Application Reset Value: 0000 0000_H
CDTMi_DTMj_PS_CTRL (i=5-6;j=0-3)
CDTMi DTMj Phase Shift Unit Configuration and Control Register($0E4010_H$+i*400_H+j*40_H) Application Reset Value: 0000 0000_H
CDTMi_DTMj_PS_CTRL (i=0-4;j=2-3)
CDTMi DTMj Phase Shift Unit Configuration and Control Register($0E4010_H$+i*400_H+j*40_H) Application Reset Value: 0000 0000_H
CDTMi_DTMj_PS_CTRL (i=5-6;j=4-5)
CDTMi DTMj Phase Shift Unit Configuration and Control Register($0E4010_H$+i*400_H+j*40_H) Application Reset Value: 0000 0000_H



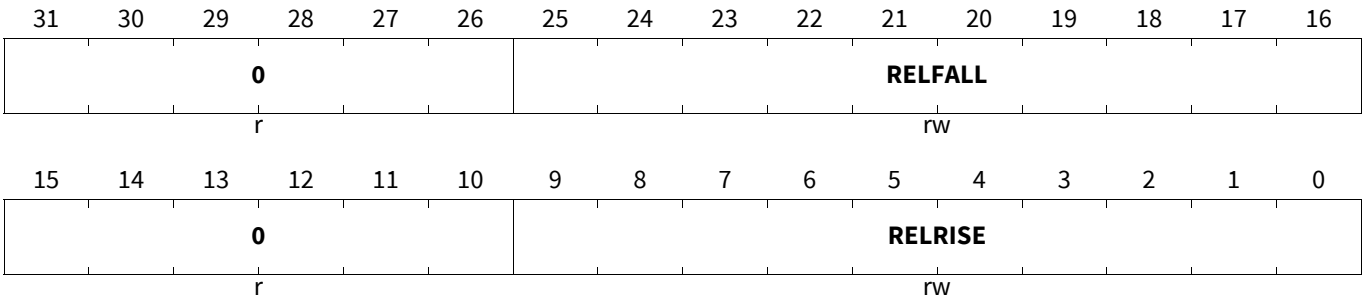
Field	Bits	Type	Description
RELBLK	9:0	rw	**Reload value blanking window** A value of 0x000 resets counter BLK_DOWN_CNT.
PSU_IN_SEL	16	rw	**PSU input selection** 0_B TIM_CH_IN0 or TIM_CH_IN1 selected 1_B DTM_AUX_IN selected
IN_POL	17	rw	**Input polarity** 0_B Input signal is not inverted 1_B Input signal is inverted

Field	Bits	Type	Description
TIM_SEL	18	rw	**TIM input selection** 0_B Select TIM_IN0 1_B Select TIM_IN1
SHIFT_SEL	21:20	rw	**Shift select** *Note: If a channel is not implemented, the value is unused. A write with this unused value returns 0b10 on status.* 00_B DTM channel 1 is connected via signal SHIFT1 with TIM_CH_IN0, TIM_CH_IN1, or DTM_AUX_IN 01_B DTM channel 2 is connected via signal SHIFT2 with TIM_CH_IN0, TIM_CH_IN1, or DTM_AUX_IN 10_B DTM channel 3 is connected via signal SHIFT3 with TIM_CH_IN0, TIM_CH_IN1, or DTM_AUX_IN 11_B DTM channel 0 is connected via signal SHIFT0 with TIM_CH_IN0, TIM_CH_IN1, or DTM_AUX_IN
0	15:10, 19, 31:22	r	**Reserved** Read as zero, shall be written as zero.

28.16.9.7 Register CDTM[i]_DTM[j]_CH[z]_DTV

CDTM0 DTM0 Channel z Dead Time Reload Values

CDTMi_DTMj_CHz_DTV (i=0-4;j=0-1,4-5;z=0-3)
CDTMi DTMj Channel z Dead Time Reload Values($0E4014_H$+i*400_H+j*40_H+z*4) Application Reset Value: $0000\ 0000_H$
CDTMi_DTMj_CHz_DTV (i=5-6;j=0-3;z=0-3)
CDTMi DTMj Channel z Dead Time Reload Values($0E4014_H$+i*400_H+j*40_H+z*4) Application Reset Value: $0000\ 0000_H$
CDTMi_DTMj_CHz_DTV (i=0-4;j=2-3;z=0-3)
CDTMi DTMj Channel z Dead Time Reload Values($0E4014_H$+i*400_H+j*40_H+z*4) Application Reset Value: $0000\ 0000_H$
CDTMi_DTMj_CHz_DTV (i=5-6;j=4-5;z=0-3)
CDTMi DTMj Channel z Dead Time Reload Values($0E4014_H$+i*400_H+j*40_H+z*4) Application Reset Value: $0000\ 0000_H$



Field	Bits	Type	Description
RELRISE	9:0	rw	**Reload value for rising edge dead time**
RELFALL	25:16	rw	**Reload value for falling edge dead time**

Field	Bits	Type	Description
0	15:10, 31:26	r	**Reserved** Read as zero, shall be written as zero.

28.16.9.8 Register CDTM[i]_DTM[j]_CH_SR

CDTM0 DTM0 Channel Shadow Register

CDTMi_DTMj_CH_SR (i=0-4;j=0-1,4-5)
CDTMi DTMj Channel Shadow Register (0E4024$_H$+i*400$_H$+j*40$_H$) Application Reset Value: 0000 0000$_H$
CDTMi_DTMj_CH_SR (i=5-6;j=0-3)
CDTMi DTMj Channel Shadow Register (0E4024$_H$+i*400$_H$+j*40$_H$) Application Reset Value: 0000 0000$_H$
CDTMi_DTMj_CH_SR (i=0-4;j=2-3)
CDTMi DTMj Channel Shadow Register (0E4024$_H$+i*400$_H$+j*40$_H$) Application Reset Value: 0000 0000$_H$
CDTMi_DTMj_CH_SR (i=5-6;j=4-5)
CDTMi DTMj Channel Shadow Register (0E4024$_H$+i*400$_H$+j*40$_H$) Application Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								SL1_3_SR_SR	SL0_3_SR_SR	SL1_2_SR_SR	SL0_2_SR_SR	SL1_1_SR_SR	SL0_1_SR_SR	SL1_0_SR_SR	SL0_0_SR_SR
r								rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
SL0_0_SR_SR	0	rw	**Shadow register for bit SL0_0_SR of register DTM[i]_CH_CTRL2_SR**
SL1_0_SR_SR	1	rw	**Shadow register for bit SL1_0_SR of register DTM[i]_CH_CTRL2_SR**
SL0_1_SR_SR	2	rw	**Shadow register for bit SL0_1_SR of register DTM[i]_CH_CTRL2_SR**
SL1_1_SR_SR	3	rw	**Shadow register for bit SL1_1_SR of register DTM[i]_CH_CTRL2_SR**
SL0_2_SR_SR	4	rw	**Shadow register for bit SL0_2_SR of register DTM[i]_CH_CTRL2_SR**
SL1_2_SR_SR	5	rw	**Shadow register for bit SL1_2_SR of register DTM[i]_CH_CTRL2_SR**
SL0_3_SR_SR	6	rw	**Shadow register for bit SL0_3_SR of register DTM[i]_CH_CTRL2_SR**
SL1_3_SR_SR	7	rw	**Shadow register for bit SL1_3_SR of register DTM[i]_CH_CTRL2_SR**
0	31:8	r	**Reserved** Read as zero, shall be written as zero.