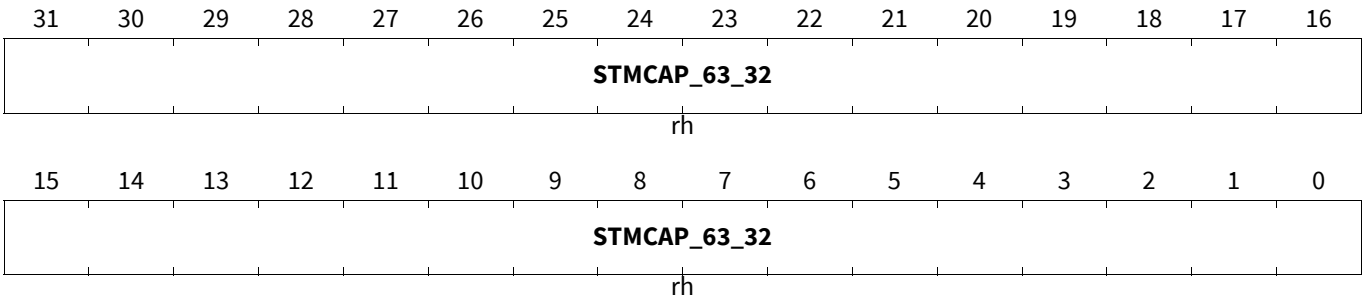
### Timer Capture Register Second View

**CAPSV**

**Timer Capture Register Second View** **($0054_H$)** **Application Reset Value: $0000\ 0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| **STMCAP_63_32** | 31:0 | rh | **Captured System Timer Bits [63:32] - STMCAP[63:32]**<br>The capture register STMCAP always captures the STM bits [63:32] when one of the registers TIM0 to TIM6 or TIM0SV is read. This capture operation is performed in order to enable software to operate with a coherent value of all the 64 STM bits at one time stamp.This bit field contains bits [63:32] of the 64-bit STM.<br>*Note: Reading register TIM0SV captures also the read value for register TIM6. In this way reading TIM0SV followed by CAPSV delivers the timer values for the first read request.* |

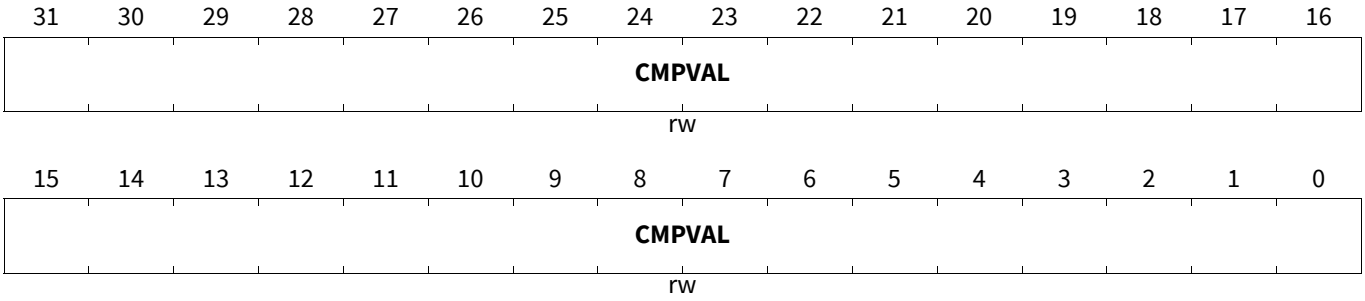
## 27.4.3 Compare Registers

The compare register CMPx holds up to 32-bits; its value is compared to the value of the STM.

### Compare Register x

**CMPx (x=0-1)**

**Compare Register x** **($0030_H$+x*4)** **Application Reset Value: $0000\ 0000_H$**




| Field | Bits | Type | Description |
|---|---|---|---|
| **CMPVAL** | 31:0 | rw | **Compare Value of Compare Register x**<br>This bit field holds up to 32 bits of the compare value (right-adjusted). |

### Compare Match Control Register

The STM Compare Match Control Register controls the parameters of the compare logic.

**CMCON**

**Compare Match Control Register** **($0038_H$)** **Application Reset Value: $0000\ 0000_H$**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **0** | | | **MSTART1** | | | | | **0** | | | **MSIZE1** | | | | |
| r | | | rw | | | | | r | | | rw | | | | |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **0** | | | **MSTART0** | | | | | **0** | | | **MSIZE0** | | | | |
| r | | | rw | | | | | r | | | rw | | | | |

| Field | Bits | Type | Description |
|---|---|---|---|
| **MSIZE0** | 4:0 | rw | **Compare Register Size for CMP0**<br>This bit field determines the number of bits in register CMP0 (starting from bit 0) that are used for the compare operation with the System Timer.<br>...<br>$00_H$ CMP0[0] used for compare operation<br>$01_H$ CMP0[1:0] used for compare operation<br>$1E_H$ CMP0[30:0] used for compare operation<br>$1F_H$ CMP0[31:0] used for compare operation |
| **MSTART0** | 12:8 | rw | **Start Bit Location for CMP0**<br>This bit field determines the lowest bit number of the 64-bit STM that is compared with the content of register CMP0 bit 0. The number of bits to be compared is defined by bit field MSIZE0.<br>...<br>$00_H$ STM[0] is the lowest bit number<br>$01_H$ STM[1] is the lowest bit number<br>$1E_H$ STM[30] is the lowest bit number<br>$1F_H$ STM[31] is the lowest bit number |
| **MSIZE1** | 20:16 | rw | **Compare Register Size for CMP1**<br>This bit field determines the number of bits in register CMP1 (starting from bit 0) that are used for the compare operation with the System Timer.<br>...<br>$00_H$ CMP1[0] used for compare operation<br>$01_H$ CMP1[1:0] used for compare operation<br>$1E_H$ CMP1[30:0] used for compare operation<br>$1F_H$ CMP1[31:0] used for compare operation |

| Field | Bits | Type | Description |
|---|---|---|---|
| **MSTART1** | 28:24 | rw | **Start Bit Location for CMP1**<br>This bit field determines the lowest bit number of the 64-bit STM that is compared with the content of register CMP1 bit 0. The number of bits to be compared is defined by bit field MSIZE1.<br>...<br>$00_H$ STM[0] is the lowest bit number<br>$01_H$ STM[1] is the lowest bit number<br>$1E_H$ STM[30] is the lowest bit number<br>$1F_H$ STM[31] is the lowest bit number |
| **0** | 7:5,<br>15:13,<br>23:21,<br>31:29 | r | **Reserved**<br>Read as 0; should be written with 0. |