Field	Bits	Type	Description
STR6_CONF	5:4	rw	**Reconfiguration of stream 6 to FIFO channel 2** Write of following double bit values is possible: The write protected bits of register **F2A[i]_CTRL** are only writable if the corresponding enable bit STR2_EN and STR6_EN of register **F2A_ENABLE** is cleared. 00_B Write: don't care, bits 1:0 will not be changed / Read: Stream 6 is mapped to FIFO buffer 6 01_B Stream 6 is mapped to FIFO buffer 6 10_B Stream 6 s mapped to FIFO buffer 2 11_B Write: don't care, bits 1:0 will not be changed / Read: Stream 6 is mapped to FIFO buffer 2
STR7_CONF	7:6	rw	**Reconfiguration of stream 7 to FIFO channel 3** Write of following double bit values is possible: The write protected bits of register **F2A[i]_CTRL** are only writable if the corresponding enable bit STR3_EN and STR7_EN of register **F2A_ENABLE** is cleared. 00_B Write: don't care, bits 1:0 will not be changed / Read: Stream 7 is mapped to FIFO buffer 7 01_B Stream 7 is mapped to FIFO buffer 7 10_B Stream 7 s mapped to FIFO buffer 3 11_B Write: don't care, bits 1:0 will not be changed / Read: Stream 7 is mapped to FIFO buffer 3
0	31:8	r	**Reserved** Read as zero, shall be written as zero.

28.10 Clock Management Unit (CMU)

28.10.1 Overview

The Clock Management Unit (CMU) is responsible for clock generation of the counters and of the GTM. The CMU consists of three sub-units that generate different clock sources for the whole GTM. The primary clock source for this sub-module is the cluster 0 clock signal cls0_clk which is defined by the value of bit field CLS0_CLK_DIV in the register GTM_CLS_CLK_CFG. **Figure 27** shows a block diagram of the CMU.

The Configurable Clock Generation (CFGU) sub-unit provides eight dedicated clock sources for the following GTM modules: TIM, ATOM, TBU, and MON. Each instance of such a module can choose an arbitrary clock source, in order to specify wide-ranging time bases.

The Fixed Clock Generation (FXU) sub-unit generates predefined non-configurable clocks *CMU_FXCLK[y]* (y: 0…4) for the TOM modules and the MON module. The *CMU_FXCLK[y]* signals are derived from the *CMU_GCLK_EN* signal generated by the Global Clock Divider. The dividing factors are defined as 2^0, 2^4, 2^8, 2^{12}, and 2^{16}.

The External Clock Generation (EGU) sub-unit is able to generate up to three chip external clock signals visible at *CMU_ECLK[z]* (z: 0…2) with a duty cycle of about 50%.

The External Clock Generation (EGU) sub-unit is able to generate clock *CMU_CLK8* for module CCM to manage 2 clock domains.

The clock source signals *CMU_CLK[x]* (x: 0…7) and *CMU_FXCLK[y]* are implemented in form of enable signals for the corresponding registers, which means that the actual clock signal of all registers always use the *CLS0_CLK* signal.

The four configurable clock signals *CMU_CLK0*, *CMU_CLK1*, *CMU_CLK6* and *CMU_CLK7* are used for the TIM filter counters.

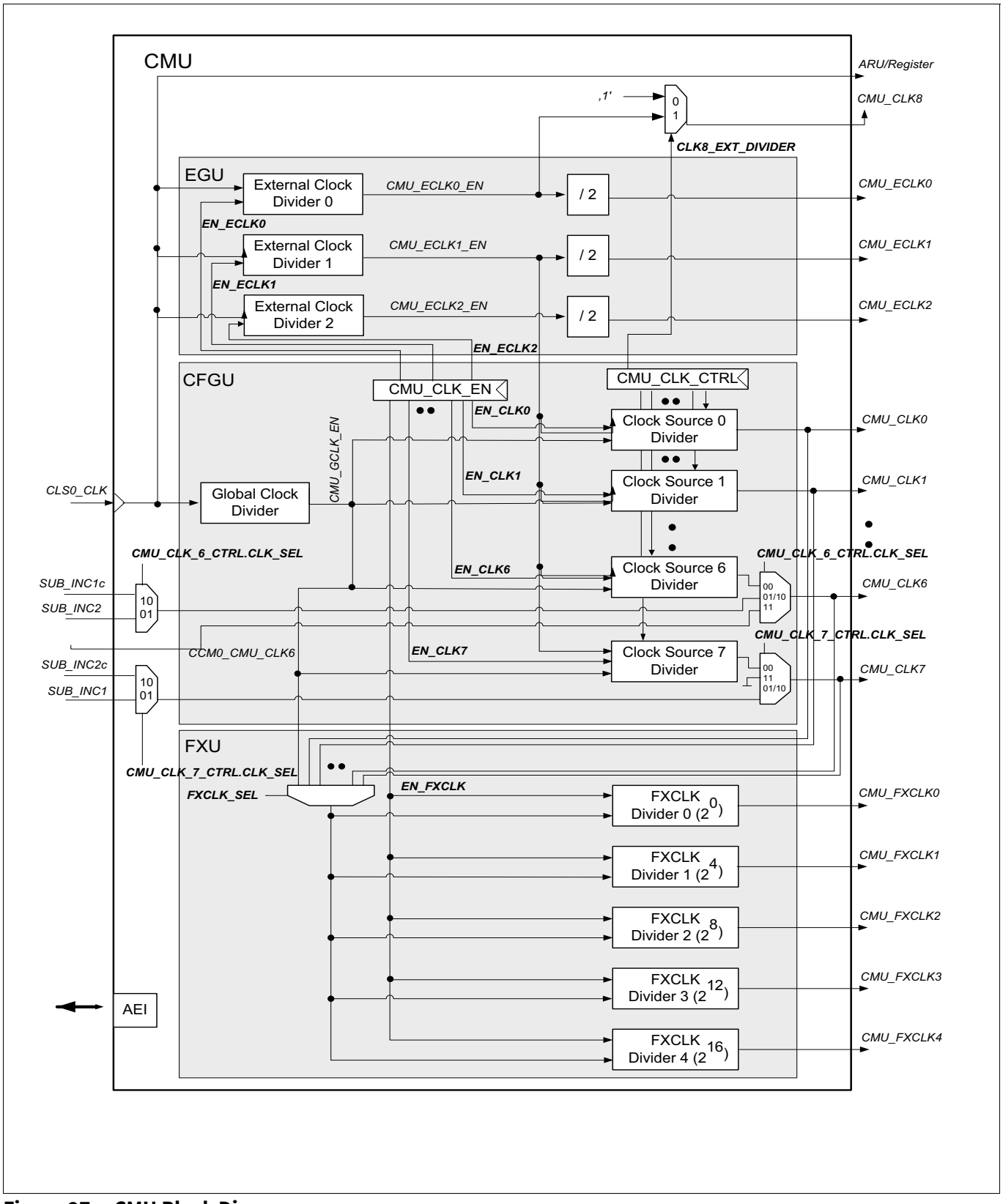


Figure 27 CMU Block Diagram

28.10.2 Global Clock Divider

The sub block Global Clock Divider can be used to divide the CMU primary source signal CLS0_CLK into a common subdivided clock signal.

The divided clock signal of the sub block Global Clock Divider is implemented as an enable signal that enables dedicated clocks from the *CLS0_CLK* signal to generate the user specified divided clock frequency.

The resulting fractional divider (Z/N) specified through equation:

$$T_{CMU\_GCLK\_EN}=(Z/N)*T_{CLS0\_CLK}$$

is implemented according the following algorithm

(*Z*: *CMU_GCLK_NUM(23:0)*; *N*: *CMU_GCLK_DEN(23:0)*; *Z,N* >0)

(1) Set remainder (*R*), operand1 (*OP1*) and operand2 (*OP2*) register during INIT-phase (with implicit conversion to signed):

R=Z, OP1=N, OP2=N-Z;

(2) After leaving INIT-phase (at least one *CMU_CLK[x]* has been enabled) the sign of remainder R for each CLS0_*CLK* cycle will be checked:

(3) If *R>0* keep updating remainder and keep *CMU_GCLK_EN='0'*:

R=R-OP1;

(4) If *R<0* update remainder and set *CMU_GCLK_EN='1'*:

R=R-OP2

After at most (*Z/N*+1) subtractions (3) there will be a negative *R* and an active phase of the generated clock enable (for one cycle) will be triggered (4). The remainder *R* is a measure for the distance to a real *Z/N* clock and will be regarded for the next generated clock enable cycle phase. The new *R* value will be *R=R+(Z-N)*. In the worst case the remainder *R* will sum up to an additional cycle in the generated clock enable period after *Z*-cycles. In the other cases equally distributed additional cycles will be inserted for the generated clock enable. If *Z* is an integer multiple of *N* no additional cycles will be included for the generated clock enable at all.

Note that for a better resource sharing all arithmetic has been reduced to subtractions and the initialization of the remainder *R* uses the complement of (*Z-N*).

28.10.3 Configurable Clock Generation sub-unit (CFGU)

The CMU sub-unit CFGU provides up to eight configurable clock divider blocks that divide the common C*MU_GCLK_EN* signal into dedicated enable signals for the GTM sub blocks.

The configuration of the eight different clock signals *CMU_CLK[x]* (x: 0…7) always depends on the configuration of the global clock enable signal *CMU_GCLK_EN*. Additionally, each clock source has its own configuration data, provided by the control register **CMU_CLK_[x]_CTRL (x=0..7)**.

According to the configuration of the Global Clock Divider, the configuration of the Clock Source x Divider is done by setting an appropriate value in the bit field **CLK_CNT[x]** of the register **CMU_CLK_[x]_CTRL**.

The frequency *fx = 1/Tx* of the corresponding clock enable signal *CMU_CLK[x]* can be determined by the unsigned representation of **CLK_CNT[x]** of the register **CMU_CLK_[x]_CTRL** in the following way:

$$T_{CMU\_CLK}[x]=(CLK\_CNT[x]+1)*T_{CMU\_GCLK\_EN}$$

The corresponding wave form is shown in **Figure 28**.

Each clock signal *CMU_CLK[x]* can be enabled individually by setting the appropriate bit field **EN_CLK[x]** in the register **CMU_CLK_EN**. Except for *CMU_CLK6* and *CMU_CLK7* individual enabling and disabling is active only if **CLK_SEL** is reset.

Alternatively, clock source six and seven (*CMU_CLK6* and *CMU_CLK7*) may provide the signal *SUB_INC1* and *SUB_INC2* coming from module DPLL as clock enable signal depending on the bit field **CLK_SEL(1:0)** of the register **CMU_CLK_6_CTRL** and on the bit field **CLK_SEL(1:0)** of the register **CMU_CLK_7_CTRL**.

CMU_CLK8 is switched by **CLK8_EXT_DIVIDER** of the register **CMU_CLK_CTRL** between *CLS0_CLK* and *CMU_ECLK0*.

To switch the clock reference CMU_GCLK_EN with *CMU_ECLK1*_EN an input selector are used in all Clock Source Divider. The *CMU_ECLK1*_EN source is enabled by setting the appropriate bit field **CMU[x]_EXT_DIVIDER** in the register **CMU_CLK_CTRL**.

To avoid unexpected behavior of the hardware, the configuration of register **CMU_CLK_[x]_CTRL** and **CMU_CLK_CTRL** can only be changed, when the corresponding clock signal *CMU_CLK[x]* and *CMU_ECLK[1]* is disabled.

Further, any changes to the registers **CMU_GCLK_NUM** and **CMU_GCLK_DEN** can only be performed, when all clock enable signals *CMU_CLK[x]* and the **EN_FXCLK** bit inside the **CMU_CLK_EN** register are disabled.

The clock source signals *CMU_CLK[x]* (x: 0…7) and *CMU_FXCLK[y]* are implemented in form of enable signals for the corresponding registers, which means that the actual clock signal of all registers always use the *CLS0_CLK* signal.

The hardware guarantees that all clock signals *CMU_CLK[x]* (x: 0…7), which were enabled simultaneous, are synchronized to each other. Simultaneous enabling does mean that the bits **EN_CLK[x]** in the register **CMU_CLK_EN** are set by the same write access.

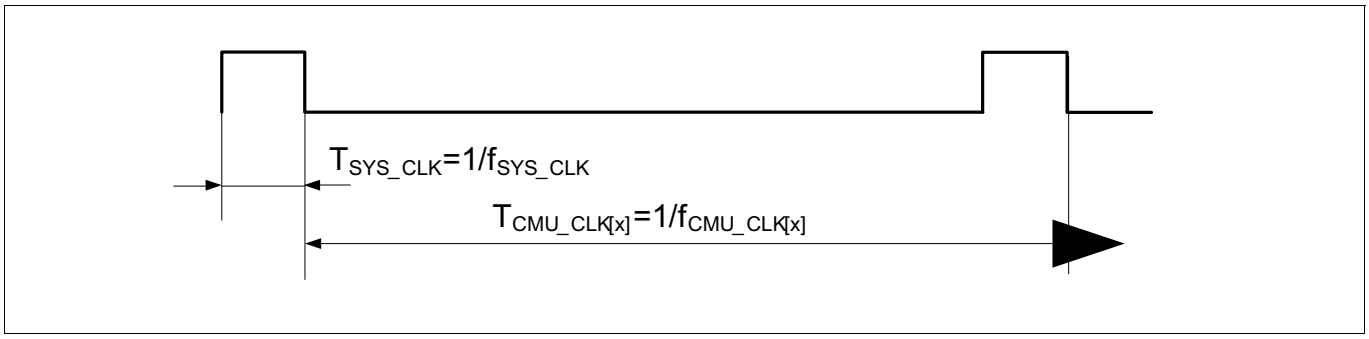


Figure 28 Wave Form of Generated Clock Signal CMU_CLK[x]

28.10.4 Fixed Clock Generation (FXU)

The FXU sub-unit generates fixed clock enables out of the *CMU_GCLK_EN* or one of the eight *CMU_CLK[x]* enable signal depending on the **FXCLK_SEL** bit field of the **CMU_FXCLK_CTRL** register. These clock enables are used for the PWM generation inside the TOM modules.

All clock enables *CMU_FXCLK[y]* can be enabled or disabled simultaneous by setting the appropriate bit field **EN_FXCLK** in the register **CMU_CLK_EN**.

The dividing factors are defined as 2^0, 2^4, 2^8, 2^{12}, and 2^{16}. The signals *CMU_FXCLK[y]* are implemented in form of enable signals for the corresponding registers (see also **Figure 28**)

28.10.5 External Generation Unit (EGU)

The EGU sub-unit generate up to three separate clock output signals *CMU_ECLK[z]* (z: 0…2).

Each of these clock signals is derived from the corresponding External Clock Divider z sub block, which generates a clock signal derived from the GTM input clock *CLS0_CLK*.

In contrast to the signals *CMU_CLK[x]* and *CMU_FXCLK[y]*, which are treated as simple enable signals for the registers, the signals *CMU_ECLK[z]* have a duty cycle of about 50% that is used as a true clock signal for external peripheral components.

To manage a second global frequency CMU_GCLK_EN could be replaced by ECLK[1]_EN for CMU_CLK[x](x:0..7). Also the all-time enabled CMU_CLK8 could be replaced by ECLK[0]_EN.

Each of the external clocks dividers are enabled and disabled by setting the appropriate bit field **EN_ECLK[z]** in the register **CMU_CLK_EN**.

The clock frequencies $f_{CMU\_ECLK[z]} = 1/T_{CMU\_ECLK[z]}$ of the external clocks are controlled with the registers **CMU_ECLK_[z]_NUM** and **CMU_ECLK_[z]_DEN** as follows:

$$T_{CMU\_ECLK}[z] = (ECLK[z]\_NUM / ECLK[z]\_DEN) * T_{CLS0\_CLK}$$

and is implemented according the following algorithm

(*Z:CMU_ECLK_[z]_NUM(23:0); N: CMU_ECLK_[z]_DEN(23:0*); *Z,N >0*; *Z>=N; CMU_ECLK[z]*='0'):

(1) Set remainder (*R*), operand1 (*OP1*) and operand2 (*OP2*) register during INIT-phase (with implicit conversion to signed): *R=Z, OP1=N, OP2=N-Z;*

(2) After leaving INIT-phase (*CMU_ECLK[z]* has been enabled) the sign of remainder R for each *CLS0_CLK* cycle will be checked:

(3) If *R>0* keep updating remainder and keep *CMU_ECLK[z]*: *R=R-OP1;*

(4) If *R<0* update remainder and toggle *CMU_ECLK[z]*: *R=R-OP2*;

After at most (*Z/N*+1) subtractions (3) there will be a negative *R* and an active phase of the generated clock enable (for one cycle) will be triggered (4). The remainder *R* is a measure for the distance to a real *Z/N* clock and will be regarded for the next generated clock toggle phase. The new *R* value will be *R=R+(Z-N)*. In the worst case the remainder *R* will sum up to an additional cycle in the generated clock toggle period after *Z*-cycles. In the other cases equally distributed additional cycles will be inserted for the generated clock toggle. If *Z* is an integer multiple of *N* no additional cycles will be included for the generated clock toggle at all. Note that for a better resource sharing all arithmetic has been reduced to subtractions and the initialization of the remainder *R* uses the complement of (*Z-N*).

The default value of the *CMU_ECLK[z]* output is low.

28.10.6 CMU Configuration Register Overview

Table 25 CMU Configuration Register Overview

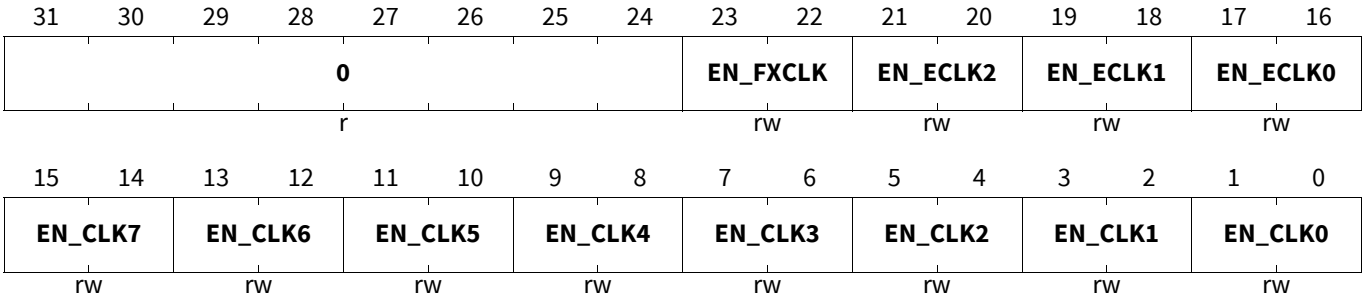
Register Name	Description	see Page
CMU_CLK_EN	CMU clock enable	107
CMU_GCLK_NUM	CMU global clock control numerator	108
CMU_GCLK_DEN	CMU global clock control denominator	108
CMU_CLK_[z]_CTRL	CMU control for clock source z	109
CMU_ECLK_[z]_NUM	CMU external clock z control numerator	110
CMU_ECLK_[z]_DEN	CMU external clock z control denominator	110
CMU_FXCLK_CTRL	CMU control FXCLK sub-unit input clock	111
CMU_GLB_CTRL	CMU synchronizing ARU and clock source	112
CMU_CLK_CTRL	CMU control for clock source selection	113

28.10.7 CMU Configuration Register Description

28.10.7.1 Register CMU_CLK_EN

CMU Clock Enable Register

CMU_CLK_EN
CMU Clock Enable Register **(000300_H)** **Application Reset Value: $0000\ 0000_H$**

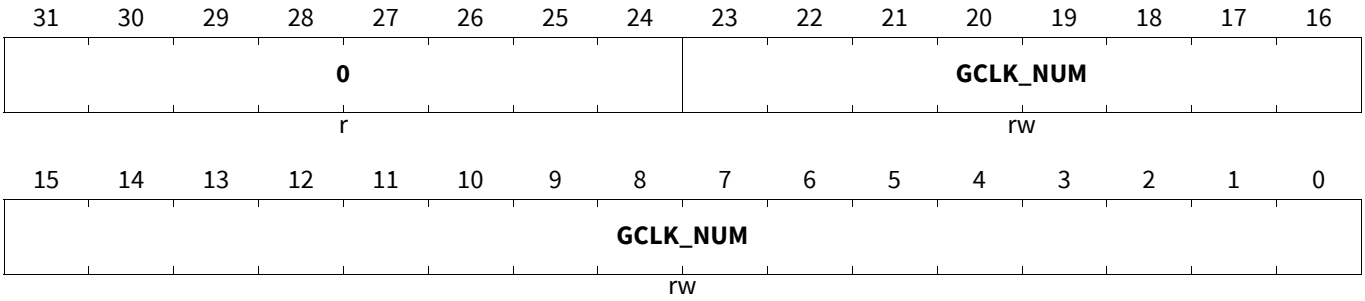


Field	Bits	Type	Description
EN_CLKx (x=0-7)	2*x+1:2*x	rw	**Enable clock source x** Any read access to an **EN_CLK[x]**, **EN_ECLK[z]** or **EN_FXCLK** bit field will always result in a value 00 or 11 indicating current state. A modification of the state is only performed with the values 01 and 10. Writing the values 00 and 11 is always ignored. Any disabling to **EN_CLK[x]** will be reset internal counters for configurable clocks. 00_B Clock source is disabled (ignore write access) 01_B Disable clock signal and reset internal states 10_B Enable clock signal 11_B Clock signal enabled (ignore write access)
EN_ECLKx (x=0-2)	2*x+17:2*x +16	rw	**Enable ECLK x generation sub-unit** Coding see bit EN_CLKx.
EN_FXCLK	23:22	rw	**Enable all CMU_FXCLK, see bits 1:0** An enable to **EN_FXCLK** from disable state will be reset internal fixed clock counters.
0	31:24	r	**Reserved** Read as zero, shall be written as zero

28.10.7.2 Register CMU_GCLK_NUM

CMU Global Clock Control Numerator

CMU_GCLK_NUM
CMU Global Clock Control Numerator **(000304_H)** **Application Reset Value: $0000\ 0001_H$**



Field	Bits	Type	Description
GCLK_NUM	23:0	rw	**GCLK_NUM** Value can only be modified when all clock enables **EN_CLK[x]** and the **EN_FXCLK** are disabled. The CMU hardware alters the content of **CMU_GCLK_NUM** and **CMU_GCLK_DEN** automatically to 0x1, if **CMU_GCLK_NUM** is specified less than **CMU_GCLK_DEN** or one of the values is specified with a value zero. Thus, a secure way for altering the values is writing twice to the register **CMU_GCLK_NUM** followed by a single write to register **CMU_GCLK_DEN**.
0	31:24	r	**Reserved** Read as zero, shall be written as zero

28.10.7.3 Register CMU_GCLK_DEN

CMU Global Clock Control Denominator

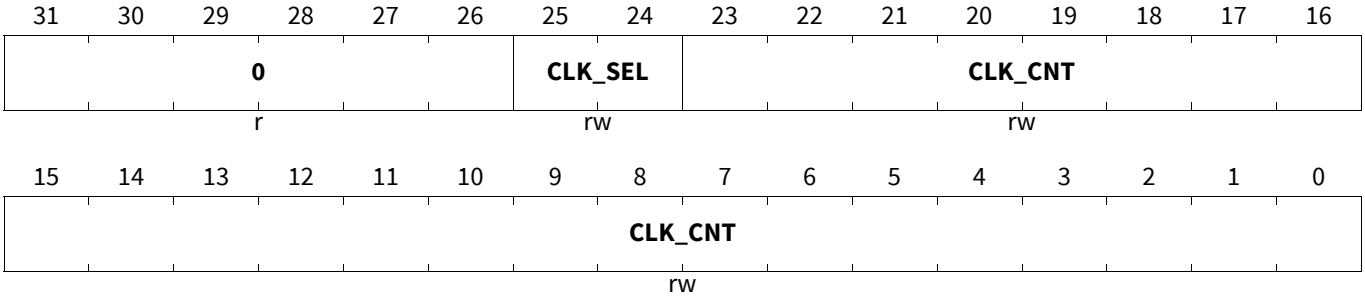
CMU_GCLK_DEN
CMU Global Clock Control Denominator **(000308_H)** **Application Reset Value: $0000\ 0001_H$**

Field	Bits	Type	Description
GCLK_DEN	23:0	rw	**GCLK_DEN** Value can only be modified when all clock enables **EN_CLK[x]** and the **EN_FXCLK** are disabled. The CMU hardware alters the content of **CMU_GCLK_NUM** and **CMU_GCLK_DEN** automatically to 0x1, if **CMU_GCLK_NUM** is specified less than **CMU_GCLK_DEN** or one of the values is specified with a value zero. Thus, a secure way for altering the values is writing twice to the register **CMU_GCLK_NUM** followed by a single write to register **CMU_GCLK_DEN**.
0	31:24	r	**Reserved** Read as zero, shall be written as zero

28.10.7.4 Register CMU_CLK_[z]_CTRL

CMU Control for Clock Source z

CMU_CLK_z_CTRL (z=0-7)
CMU Control for Clock Source z **($00030C_H$+z*4)** **Application Reset Value: 0000 0000_H**

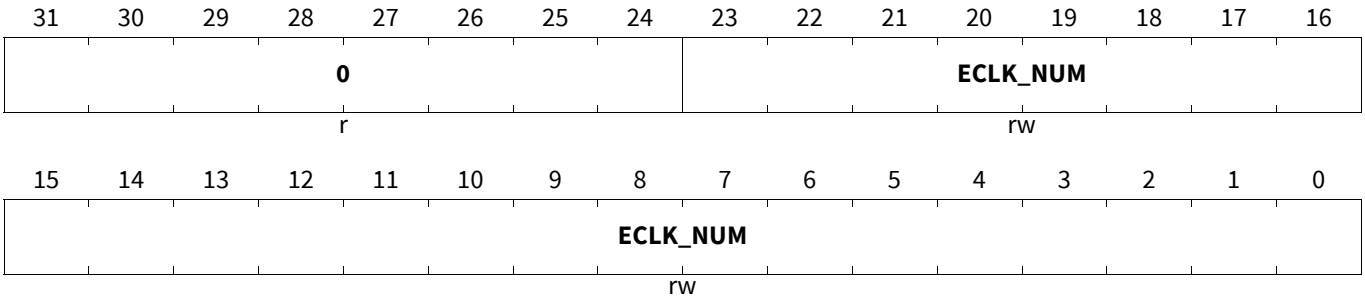


Field	Bits	Type	Description
CLK_CNT	23:0	rw	**Clock count** Defines count value for the clock divider. Value can only be modified when clock enable **EN_CLKz** and **EN_ECLK1** are disabled.
CLK_SEL	25:24	rw	**Clock source selection for CMU_CLKz** Value can only be modified when clock enable **EN_CLKz** and **EN_ECLK1** are disabled. *Note: The existence and interpretation of this bit field depends on z. z>5*
0	31:26	r	**Reserved** Read as zero, shall be written as zero.

28.10.7.5 Register CMU_ECLK_[z]_NUM

CMU External Clock z Control Numerator

CMU_ECLK_z_NUM (z=0-2)
CMU External Clock z Control Numerator (00032C$_H$+z*8) Application Reset Value: 0000 0001$_H$



Field	Bits	Type	Description
ECLK_NUM	23:0	rw	**ECLK_NUM** Numerator for external clock divider. Defines numerator of the fractional divider. *Note: Value can only be modified when clock enable **EN_ECLK[z]** disabled.* *Note: The CMU hardware alters the content of **CMU_ECLK_[z]_NUM** and **CMU_ECLK_[z]_DEN** automatically to 0x1, if **CMU_ECLK_[z]_NUM** is specified less than **CMU_ECLK_[z]_DEN** or one of the values is specified with a value zero. Thus, a secure way for altering the values is writing twice to the register **CMU_ECLK_[z]_NUM** followed by a single write to register **CMU_ECLK_[z]_DEN**.*
0	31:24	r	**Reserved** Read as zero, shall be written as zero

28.10.7.6 Register CMU_ECLK_[z]_DEN

CMU External Clock z Control Denominator

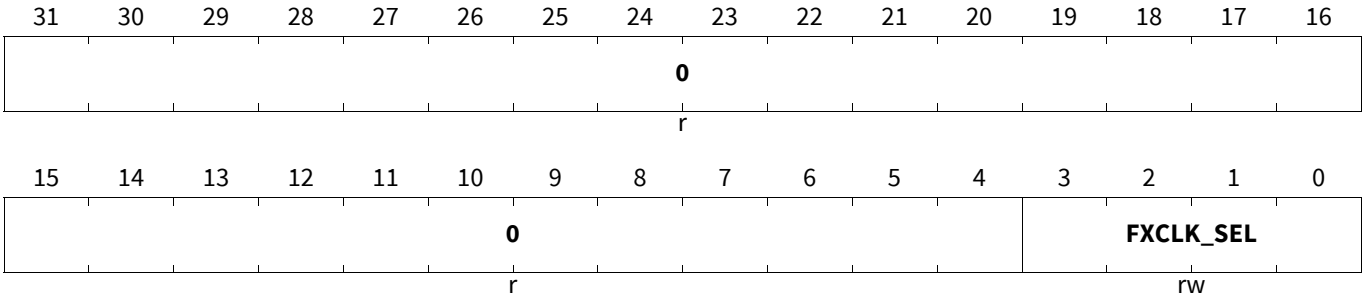
CMU_ECLK_z_DEN (z=0-2)
CMU External Clock z Control Denominator (000330$_H$+z*8) Application Reset Value: 0000 0001$_H$

Field	Bits	Type	Description
ECLK_DEN	23:0	rw	**ECLK_DEN** Denominator for external clock divider. Defines denominator of the fractional divider *Note: Value can only be modified when clock enable **EN_ECLK[z]** disabled.* *Note: The CMU hardware alters the content of **CMU_ECLK_[z]_NUM** and **CMU_ECLK_[z]_DEN** automatically to 0x1, if **CMU_ECLK_[z]_NUM** is specified less than **CMU_ECLK_[z]_DEN** or one of the values is specified with a value zero. Thus, a secure way for altering the values is writing twice to the register **CMU_ECLK_[z]_NUM** followed by a single write to register **CMU_ECLK_[z]_DEN**.*
0	31:24	r	**Reserved** Read as zero, shall be written as zero

28.10.7.7 Register CMU_FXCLK_CTRL

CMU Control FXCLK Sub-Unit Input Clock

CMU_FXCLK_CTRL
CMU Control FXCLK Sub-Unit Input Clock (000344$_H$) Application Reset Value: 0000 0000$_H$



Field	Bits	Type	Description
FXCLK_SEL	3:0	rw	**Input clock selection for EN_FXCLK line** This value can only be written when the CMU_FXCLK generation is disabled. See bits 23..22 in register **CMU_CLK_EN**. Other values for FXCLK_SEL are reserved and should not be used, but they behave like FXCLK_SEL = 0. 0_H CMU_GCLK_EN selected 1_H CMU_CLK0 selected 2_H CMU_CLK1 selected 3_H CMU_CLK2 selected 4_H CMU_CLK3 selected 5_H CMU_CLK4 selected 6_H CMU_CLK5 selected 7_H CMU_CLK6 selected 8_H CMU_CLK7 selected CMU_CLK7 selected
0	31:4	r	**Reserved** Read as zero, shall be written as zero.

28.10.7.8 Register CMU_GLB_CTRL

CMU Synchronizing ARU and Clock Source

CMU_GLB_CTRL
CMU Synchronizing ARU and Clock Source (000348$_H$) Application Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0															ARU_ADDR_RSTGLB
r															rw

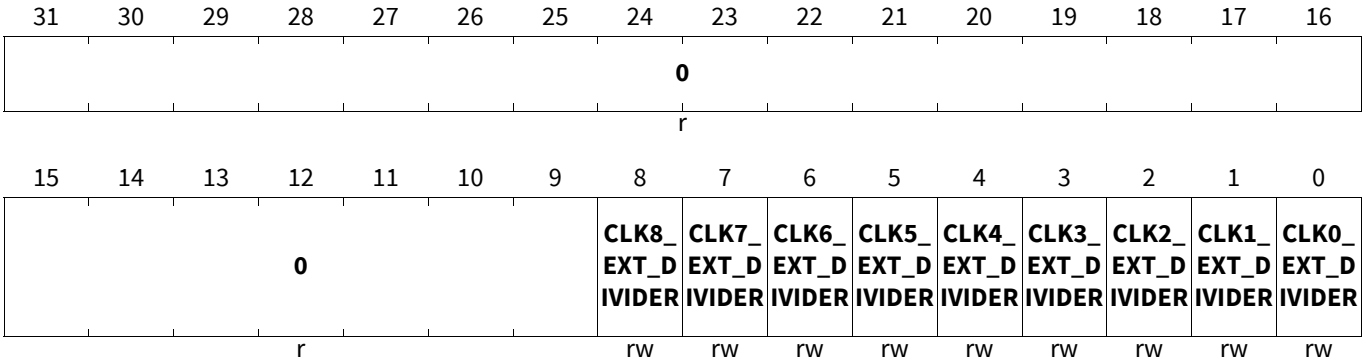
Field	Bits	Type	Description
ARU_ADDR_RSTGLB	0	rw	**Reset ARU caddr counter and ARU dynamic route counter** Writing value 1 to this bit field results in a request to reset the ARU caddr counter and ARU dynamic route counter. The next following write access to register **CMU_CLK_EN** applies the ARU caddr counter reset, ARU dynamic route counter reset and resets this bit. This feature can be used to synchronize the ARU round trip time to the CMU clocks. This bit is write protected. Before writing to this bit set bit RF_PROT of register **GTM_CTRL** to 0.

Field	Bits	Type	Description
0	31:1	r	**Reserved** Read as zero, shall be written as zero

28.10.7.9 Register CMU_CLK_CTRL

CMU Control for Clock Source Selection

CMU_CLK_CTRL
CMU Control for Clock Source Selection **(00034C$_H$)** **Application Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
CLK0_EXT_DIVIDER	0	rw	**Clock source selection for CMU_CLK_0_CTRL** Value can only be modified when clock enable **EN_CLK0** and **EN_ECLK1** are disabled. 0_B Use Clock Source CMU_GCLK_EN 1_B Use Clock Source CMU_ECLK1
CLK1_EXT_DIVIDER	1	rw	**Clock source selection for CMU_CLK_1_CTRL** Value can only be modified when clock enable **EN_CLK1** and **EN_ECLK1** are disabled.
CLK2_EXT_DIVIDER	2	rw	**Clock source selection for CMU_CLK_2_CTRL** Value can only be modified when clock enable **EN_CLK2** and **EN_ECLK1** are disabled.
CLK3_EXT_DIVIDER	3	rw	**Clock source selection for CMU_CLK_3_CTRL** Value can only be modified when clock enable **EN_CLK3** and **EN_ECLK1** are disabled.
CLK4_EXT_DIVIDER	4	rw	**Clock source selection for CMU_CLK_4_CTRL** Value can only be modified when clock enable **EN_CLK4** and **EN_ECLK1** are disabled.
CLK5_EXT_DIVIDER	5	rw	**Clock source selection for CMU_CLK_5_CTRL** Value can only be modified when clock enable **EN_CLK5** and **EN_ECLK1** are disabled.
CLK6_EXT_DIVIDER	6	rw	**Clock source selection for CMU_CLK_6_CTRL** Value can only be modified when clock enable **EN_CLK6** and **EN_ECLK1** are disabled.

Field	Bits	Type	Description
CLK7_EXT_DIVIDER	7	rw	**Clock source selection for CMU_CLK_7_CTRL** Value can only be modified when clock enable **EN_CLK7** and **EN_ECLK1** are disabled.
CLK8_EXT_DIVIDER	8	rw	**Clock source selection for CMU_CLK8** Value can only be modified when **EN_ECLK0** is disabled. 0_B Use Clock Source CLS0_CLK 1_B Use Clock Source CMU_ECLK0
0	31:9	r	**Reserved** Read as zero, shall be written as zero.