Table 10 Register behavior in case of Software Debugger accesses

Module	Register	Description
AFD	AFD[i]_CH[x]_BUFFACC	The FIFO read access pointers are not altered on behalf of a Debugger read access to this register.
TIM	TIM[i]_CH[x]_GPR0/1	The overflow bit is not altered in case of a Debugger read access to this registers.
ATOM	ATOM[i]_CH[x]_SR0/1	In SOMC mode a read access to this register by the Debugger does not release the channel for a new compare/match event.

Further on, some important states inside the GTM sub-module have to be signaled to the outside world, when reached and should for example trigger the software debugger to stop program execution. For this internal state signaling please refer to the GTM module integration guide.

The GTM provides an external signal *gtm_halt*, which disables clock signal *SYS_CLK* for debugging purposes. If *SYS_CLK* is disabled, a connected debugger can read any GTM related register and the GTM internal RAMs using AEI. Moreover, the debugger can also perform write accesses to the internal RAMs and to all GTM related registers in order to enable advanced debugging features (e.g. modifications of register contents in single step mode).

28.4.7 GTM Programming conventions

To serve different application domains the GTM is a highly configurable module with many configuration modes. In principle the sub-modules of the GTM are intended to be configured at system startup to fulfill certain functionality for the application domain the micro controller runs in.

For example, a TIM input channel can be used to monitor an application specific external signal, and this signal has to be filtered. Therefore, the configuration of the TIM channel filter mode will be specific to the external signal characteristic. While it can be necessary to adapt the filter thresholds during runtime an adaptation of the filter mode during runtime is not reasonable. Thus, the change of the filter mode during runtime can lead to an unexpected behavior.

In general, the programmer has to be careful when reprogramming configuration registers of the GTM sub-modules during runtime. It is recommended to disable the channels before reconfiguration takes place to avoid unexpected behavior of the GTM.

28.4.8 GTM TOP-Level Configuration Register Overview

Table 11 GTM TOP-Level Configuration Register Overview

Register name	Description	see Page
GTM_REV	GTM Version control register	30
GTM_RST	GTM Global reset register	31
GTM_CTRL	GTM Global control register	31
GTM_AEI_ADDR_XPT	GTM AEI Timeout exception address register	32
GTM_AEI_STA_XPT	GTM AEI Non zero status register	33
GTM_IRQ_NOTIFY	GTM Interrupt notification register	34
GTM_IRQ_EN	GTM Interrupt enable register	36
GTM_EIRQ_EN	GTM Error interrupt enable register	44

Table 11 GTM TOP-Level Configuration Register Overview (cont'd)

Register name	Description	see Page
GTM_IRQ_FORCINT	GTM Software interrupt generation register	37
GTM_IRQ_MODE	GTM top level interrupts mode selection	39
GTM_BRIDGE_MODE	GTM AEI bridge mode register	39
GTM_BRIDGE_PTR1	GTM AEI bridge pointer 1 register	41
GTM_BRIDGE_PTR2	GTM AEI bridge pointer 2 register	42
GTM_MCS_AEM_DIS	GTM MCS master port disable register	43
GTM_CLS_CLK_CFG	GTM Cluster Clock Configuration	45
GTM_CFG	GTM Configuration register	46