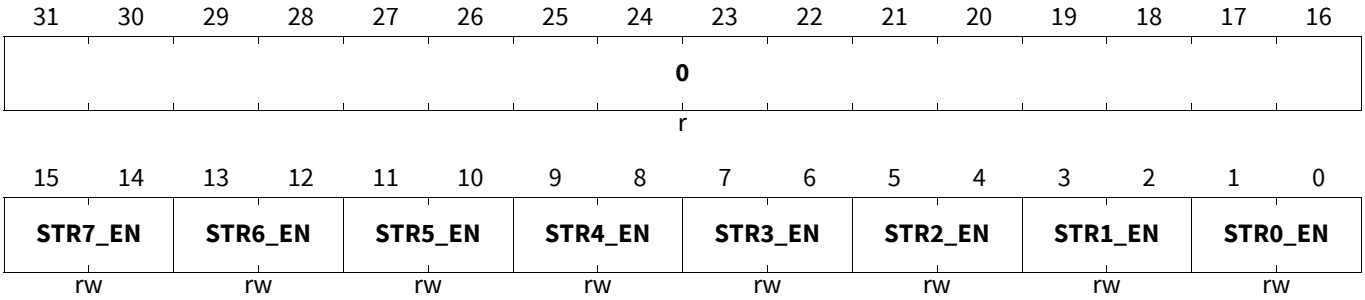
28.9.5 F2A Configuration Register description

28.9.5.1 Register F2A[i]_ENABLE

F2Ai Stream Activation Register

F2Ai_ENABLE (i=0-2)
F2Ai Stream Activation Register **(018040_H+i*4000_H)** **Application Reset Value: 0000 0000_H**

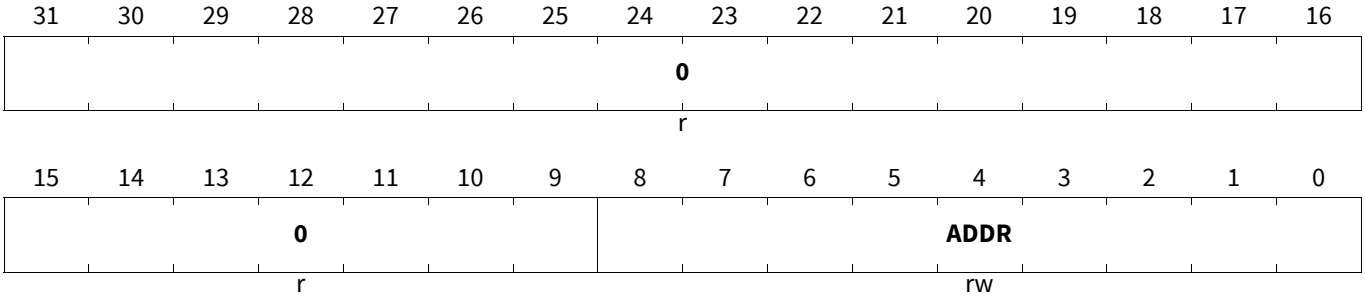


Field	Bits	Type	Description
STRx_EN (x=0-7)	2*x+1:2*x	rw	**Enable/disable stream x** Write of following double bit values is possible: 00_B Write: Don't care, bits 1:0 will not be changed / Read: Stream disabled 01_B Stream 0 is disabled and internal states are reset 10_B Stream 0 is enabled 11_B Write: Don't care, bits 1:0 will not be changed / Read: Stream enabled
0	31:16	r	**Reserved** Read as zero, shall be written as zero.

28.9.5.2 Register F2A[i]_CH[z]_ARU_RD_FIFO

F2Ai Stream z Read Address Register

F2Ai_CHz_ARU_RD_FIFO (i=0-2;z=0-7)
F2Ai Stream z Read Address Register **(018000_H+i*4000_H+z*4)** **Application Reset Value: 0000 $01FE_H$**



Field	Bits	Type	Description
ADDR	8:0	rw	**ARU Read address** This bit field is only writable if channel is disabled.
0	31:9	r	**Reserved** Read as zero, shall be written as zero

28.9.5.3 Register F2A[i]_CH[z]_STR_CFG

F2Ai Stream z Configuration Register

Note: The write protected bits of register **F2A_CH[z]_STR_CFG** are only writable if the corresponding enable bit STRx_EN of register **F2A_ENABLE** is cleared.

F2Ai_CHz_STR_CFG (i=0-2;z=0-7)
F2Ai Stream z Configuration Register **(018020_H+i*4000_H+z*4)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0													DIR	TMODE	
r													rw	rw	

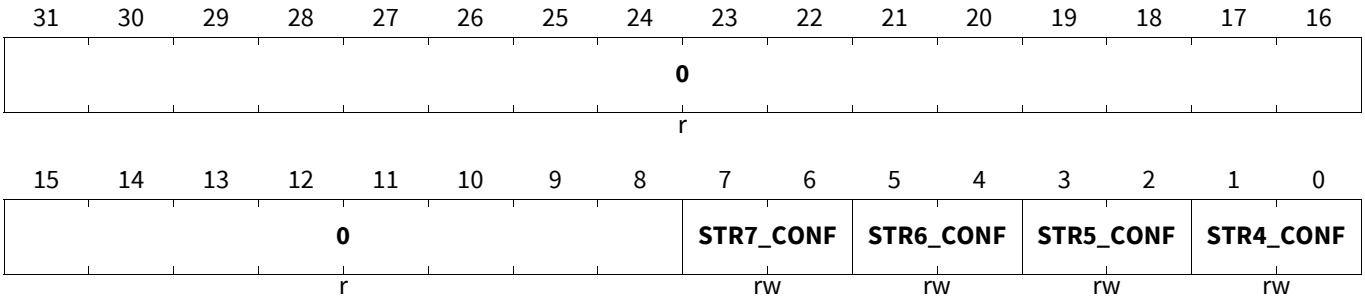
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0															
r															

Field	Bits	Type	Description
TMODE	17:16	rw	**Transfer mode for 53 bit ARU data from/to FIFO** 00_B Transfer low word (ARU bits 23:0) from/to FIFO 01_B Transfer high word (ARU bits 47:24) from/to FIFO 10_B Transfer both words from/to FIFO 11_B Reserved
DIR	18	rw	**Data transfer direction** 0_B Transport from ARU to FIFO 1_B Transport from FIFO to ARU
0	15:0, 31:19	r	**Reserved** Read as zero, shall be written as zero

28.9.5.4 Register F2A[i]_CTRL

F2Ai Stream Control Register

F2Ai_CTRL (i=0-2)
F2Ai Stream Control Register **(018044_H+i*4000_H)** **Application Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
STR4_CONF	1:0	rw	**Reconfiguration of stream 4 to FIFO channel 0** Write of following double bit values is possible: The write protected bits of register **F2A[i]_CTRL** are only writable if the corresponding enable bit STR0_EN and STR4_EN of register **F2A_ENABLE** is cleared. 00_B Write: don't care, bits 1:0 will not be changed / Read: Stream 4 is mapped to FIFO buffer 4 01_B Stream 4 is mapped to FIFO buffer 4 10_B Stream 4 is mapped to FIFO buffer 0 11_B Write: don't care, bits 1:0 will not be changed / Read: Stream 4 is mapped to FIFO buffer 0
STR5_CONF	3:2	rw	**Reconfiguration of stream 5 to FIFO channel 1** Write of following double bit values is possible: The write protected bits of register **F2A[i]_CTRL** are only writable if the corresponding enable bit STR1_EN and STR5_EN of register **F2A_ENABLE** is cleared. 00_B Write: don't care, bits 1:0 will not be changed / Read: Stream 5 is mapped to FIFO buffer 5 01_B Stream 5 is mapped to FIFO buffer 5 10_B Stream 5 is mapped to FIFO buffer 1 11_B Write: don't care, bits 1:0 will not be changed / Read: Stream 5 is mapped to FIFO buffer 1