28.7 First In First Out Module (FIFO)

28.7.1 Overview

The FIFO unit is the storage part of the FIFO sub-module. The F2A described in (FIFO to ARU Unit) and the AFD described in chapter “AEI to FIFO Data Interface” implement the interface part of the FIFO sub-module to the ARU and the AEI bus. Each FIFO unit embeds eight logical FIFOs. These logical FIFOs are configurable in the following manner:

- FIFO size (defines start and end address)
- FIFO operation modes (normal mode or ring buffer operation mode)
- Fill level control / memory region read protection

Each logical FIFO represents a data stream between the sub-modules of the GTM and the microcontroller connected to AFD sub-module (see chapter AEI to FIFO Data Interface). The FIFO RAM counts 1K words, where the word size is 29 bit. This gives the freedom to program or receive 24 bit of data together with the five control bits inside an ARU data word.

The FIFO unit provides three ports for accessing its content. One port is connected to the F2A interface, one port is connected to the AFD interface and one port has its own AEI bus interface.

The AFD interface has always the highest priority. Accesses to the FIFO from AFD interface and direct AEI interface in parallel - which means at the same time - is not possible, because both interfaces are driven from the same AEI bus interface of the GTM.

The priority between F2A and direct AEI interface can be defined by software. This can be done by using the register **FIFO[i]_CH[x]_CTRL** for all FIFO channels of the sub-module.

The FIFO is organized as a single RAM that is also accessible through the FIFO AEI interface connected to one of the FIFO ports. To provide the direct RAM access, the RAM is mapped into the address space of the microcontroller. The addresses for accessing the RAM via AEI can be found in [1].

After reset, the FIFO RAM isn't initialized by hardware.

The FIFO channels can be flushed individually. Each of the eight FIFO channels can be used whether in normal FIFO operation mode or in ring buffer operation mode.

Beside the possibility of flushing each FIFO channel directly, a write access to FIFO[i]_CH[x]_END_ADDR or to FIFO[i]_CH[x]_START_ADDR will also flush the regarding channel which means that the read and write pointer and also the fill level of the regarding channel will be reset. In consequence of this existing data in the concerned FIFO channel are not longer valid- thereafter the channel is empty.

28.7.2 Operation Modes

28.7.2.1 FIFO Operation Mode

In normal FIFO operation mode the content of the FIFO is written and read in first-in first-out order, where the data is destroyed after it is delivered to the system bus or the F2A sub-module (see chapter “FIFO to ARU Unit ”).

The upper and lower watermark registers (registers **FIFO[i]_CH[x]_UPPER_WM** and **FIFO[i]_CH[x]_LOWER_WM**) are used for controlling the FIFO’s fill level. If the fill level falls below the lower watermark or it exceeds the upper watermark, an interrupt signal is triggered by the FIFO sub-module if enabled inside the **FIFO[i]_IRQ_EN**.

The interrupt signals are sent to the Interrupt Concentrator Module (ICM) (see chapter “Interrupt Concentrator Module”). The ICM can also initiate specific DMA transfers.

28.7.2.2 Ring Buffer Operation Mode

The ring buffer mode can be used to provide a continuous data or configuration stream to the other GTM sub-modules without CPU interaction. In ring buffer mode the FIFO provides a continuous data stream to the F2A sub-module. The first word of the FIFO is delivered first and after the last word is provided by the FIFO to the ARU, the first word can be obtained again.

If in ring buffer mode the read pointer reaches the write pointer it will be set again to the configured start address. So the read pointer always rotates cyclic between the configured start address of the regarding FIFO channel (first written data) and the write pointer which points to the last written data of the channel.

It is possible to add data to the FIFO channel via the AEI to FIFO interface (AFD) using the register AFD[i]_CH[x]_BUF_ACC while running in ring buffer mode. The new written data will be added in the next ring buffer cycle.

However, the register AFD[i]_CH[x]_BUF_ACC should not be read in read buffer mode.

It is recommended to fill the FIFO channel first before enabling the data stream in the FIFO to ARU interface (F2A).

Modifications of the continuous data stream can be achieved by using direct memory access which is provided by the FIFO AEI interface.

28.7.2.3 DMA Hysteresis Mode

The DMA hysteresis mode can be enabled by setting bit DMA_HYSTERESIS=1 in the **FIFO[i]_CH[x]_IRQ_MODE** register.

In the DMA hysteresis mode the lower and upper watermark will be masked to generate the DMA request (=*fifo_irq*) in the following manner.

If a DMA is writing data to a FIFO (configured by setting bit DMA_HYST_DIR=1 in register **FIFO[i]_CH[x]_IRQ_MODE)**, the DMA request will be generated by the lower watermark. The upper watermark does not generate a DMA request. The next DMA request will be generated by the next lower watermark until the upper watermark was reached.

If a DMA is reading data from a FIFO (configured by setting bit DMA_HYST_DIR=0 in register **FIFO[i]_CH[x]_IRQ_MODE)**, the DMA request will be generated by the upper watermark. The lower watermark does not generate a DMA request. The next DMA request will be generated by the next upper watermark until the lower watermark was reached.

Note that the watermarks have to achieve the following condition depending on the irq mode

- IRQ_MODE = Level / Pulse / Pulse-Notify mode:
  - Upper watermark > Lower watermark
- IRQ_MODE = Single-Pulse mode:
  - Upper watermark > Lower watermark + 1

28.7.3 FIFO Interrupt

Table 17 FIFO Interrupt Signals

Signal	Description
FIFO[i]_CH[x]_EMPTY	Indicating empty FIFO x (x:0…7) was reached
FIFO[i]_CH[x]_FULL	Indicating full FIFO x (x:0…7) was reached

Table 17 FIFO Interrupt Signals (cont'd)

Signal	Description
FIFO[i]_CH[x]_LOWER_WM	Indicating FIFO x (x:0…7) reached lower watermark.
FIFO[i]_CH[x]_UPPER_WM	Indicating FIFO x (x:0…7) reached upper watermark.

28.7.4 FIFO Configuration Register Overview

Table 18 FIFO Configuration Register Overview

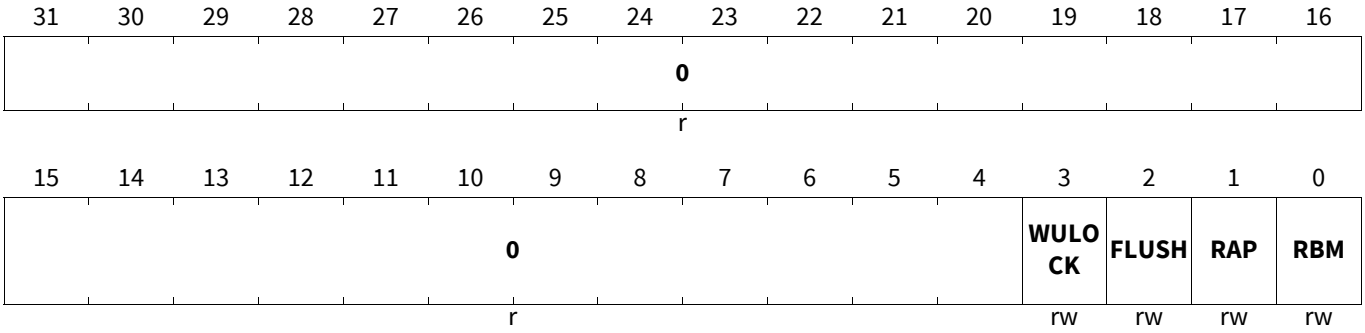
Register Name	Description	see Page
FIFO[i]_CH[z]_CTR	FIFOi channel z control register	84
FIFO[i]_CH[z]_END_ADDR	FIFOi channel z end address register	85
FIFO[i]_CH[z]_START_ADDR	FIFOi channel z start address register	85
FIFO[i]_CH[z]_UPPER_WM	FIFOi channel z upper watermark register	86
FIFO[i]_CH[z]_LOWER_WM	FIFOi channel z lower watermark register	86
FIFO[i]_CH[z]_STATUS	FIFOi channel z status register	87
FIFO[i]_CH[z]_FILL_LEVEL	FIFOi channel z fill level register	88
FIFO[i]_CH[z]_WR_PTR	FIFOi channel z write pointer register	88
FIFO[i]_CH[z]_RD_PTR	FIFOi channel z read pointer register	89
FIFO[i]_CH[z]_IRQ_NOTIFY	FIFOi channel z interrupt notification register	90
FIFO[i]_CH[z]_IRQ_EN	FIFOi channel z interrupt enable register	91
FIFO[i]_CH[z]_EIRQ_EN	FIFOi channel z error interrupt enable register	94
FIFO[i]_CH[z]_IRQ_FORCINT	FIFOi channel z force interrupt register	92
FIFO[i]_CH[z]_IRQ_MODE	FIFOi channel z interrupt mode control register	93

28.7.5 FIFO Configuration Registers Description

28.7.5.1 Register FIFO[i]_CH[z]_CTRL

FIFOi Channel z Control Register

FIFOi_CHz_CTRL (i=0-2;z=0-7)
FIFOi Channel z Control Register **(018400_H+i*4000_H+z*40_H)** **Application Reset Value: 0000 0000_H**



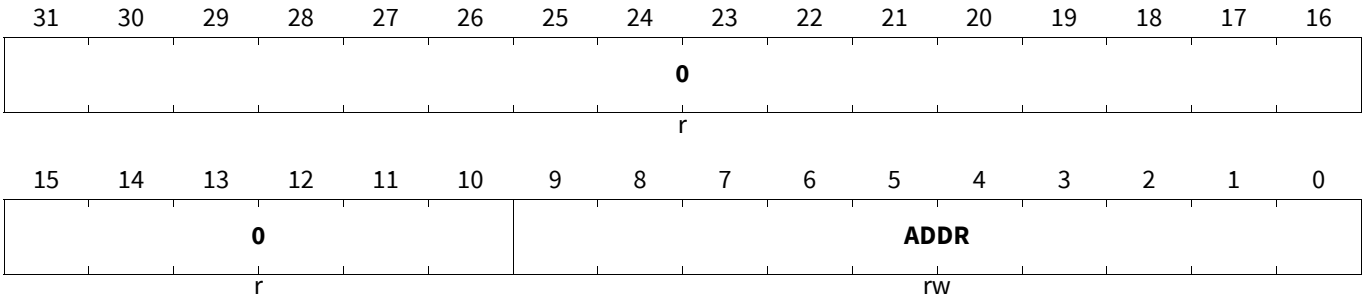
Field	Bits	Type	Description
RBM	0	rw	**Ring buffer mode enable** 0_B Normal FIFO operation mode 1_B Ring buffer mode
RAP	1	rw	**RAM access priority** RAP bit is only functional in register FIFO_0_CTRL. The priority is defined for all FIFO channels there. 0_B FIFO ports have higher access priority than AEI-IF 1_B AEI-IF has higher access priority than FIFO ports
FLUSH	2	rw	**FIFO Flush control** A FIFO Flush operation resets the **FIFO[i]_CH[z]_FILL_LEVEL**, **FIFO[i]_CH[z]_WR_PTR** and **FIFO[i]_CH[z]_RD_PTR** registers to their initial values. 0_B Normal operation 1_B Execute FIFO flush (bit is automatically cleared after flush)
WULOCK	3	rw	**RAM write unlock** Enable/disable direct RAM write access to the memory mapped FIFO region. Only the bit WULOCK of register FIFO[i]_CH0_CTRL enables/disables the direct RAM write access for all FIFO channel (whole FIFO RAM). The WULOCK bits of the other channels are writeable but have no effect. 0_B Direct RAM write access disabled 1_B Direct RAM write access enabled
0	31:4	r	**Reserved** Read as zero, shall be written as zero.

28.7.5.2 Register FIFO[i]_CH[z]_END_ADDR

FIFOi Channel z End Address Register

FIFOi_CHz_END_ADDR (i=0-2;z=0-7)

FIFOi Channel z End Address Register (018404_H+i*4000_H+z*40_H) **Reset Value: Table 19**



Field	Bits	Type	Description
ADDR	9:0	rw	**End address for FIFO channel z** value for ADDR is calculated as ADDR = 128*(x+1)-1 A write access will flush the regarding channel
0	31:10	r	**Reserved** Read as zero, shall be written as zero.

Table 19 Reset Values of FIFOi_CHz_END_ADDR (i=0-2;z=0-7)

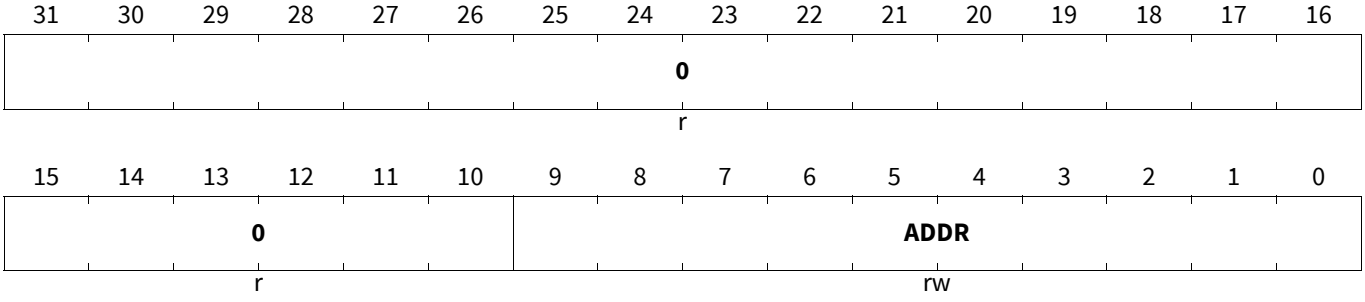
Reset Type	Reset Value	Note
Application Reset	0x80 * (z + 1) - 1	

28.7.5.3 Register FIFO[i]_CH[z]_START_ADDR

FIFOi Channel z Start Address Register

FIFOi_CHz_START_ADDR (i=0-2;z=0-7)

FIFOi Channel z Start Address Register (018408_H+i*4000_H+z*40_H) **Reset Value: Table 20**



Field	Bits	Type	Description
ADDR	9:0	rw	**Start address for FIFO channel z** Initial value for ADDR is calculated as ADDR = 128*z. A write access will flush the regarding channel.

Field	Bits	Type	Description
0	31:10	r	**Reserved** Read as zero, shall be written as zero.

Table 20 Reset Values of FIFOi_CHz_START_ADDR (i=0-2;z=0-7)

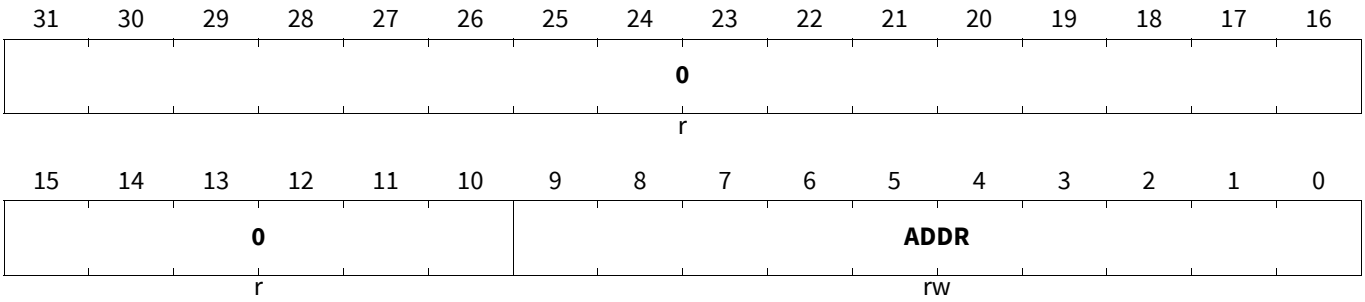
Reset Type	Reset Value	Note
Application Reset	0x80 * z	

28.7.5.4 Register FIFO[i]_CH[z]_UPPER_WM

FIFOi Channel z Upper Watermark Register

FIFOi_CHz_UPPER_WM (i=0-2;z=0-7)

FIFOi Channel z Upper Watermark Register($01840C_H$+i*4000_H+z*40_H) Application Reset Value: 0000 0060_H



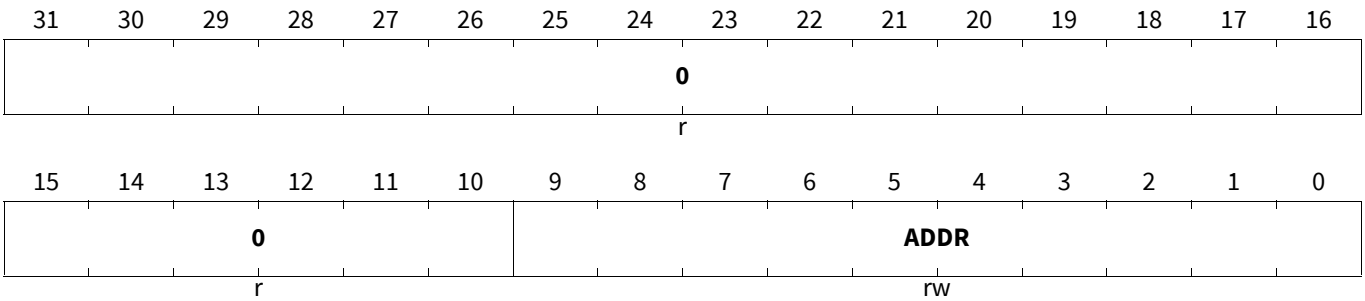
Field	Bits	Type	Description
ADDR	9:0	rw	**Upper watermark address for channel z** The upper watermark is configured as a relative fill level of the FIFO. ADDR must be in range: 0 <= ADDR <= **FIFO[i]_CH[x]_END_ADDR** - **FIFO[i]_CH[x]_START_ADDR**. Initial value for ADDR is defined as ADDR = 0x60.
0	31:10	r	**Reserved** Read as zero, shall be written as zero.

28.7.5.5 Register FIFO[i]_CH[z]_LOWER_WM

FIFOi Channel z Lower Watermark Register

FIFOi_CHz_LOWER_WM (i=0-2;z=0-7)

FIFOi Channel z Lower Watermark Register(018410_H+i*4000_H+z*40_H) Application Reset Value: 0000 0020_H



Field	Bits	Type	Description
ADDR	9:0	rw	**Lower watermark address for channel z** The lower watermark is configured as a relative fill level of the FIFO. ADDR must be in range: 0 <= ADDR <= **FIFO[i]_CH[z]_END_ADDR** - **FIFO[i]_CH[z]_START_ADDR**. Initial value for ADDR is defined as ADDR = 0x20.
0	31:10	r	**Reserved** Read as zero, shall be written as zero.

28.7.5.6 Register FIFO[i]_CH[z]_STATUS

FIFOi Channel z Status Register

FIFOi_CHz_STATUS (i=0-2;z=0-7)
FIFOi Channel z Status Register **(018414_H+i*4000_H+z*40_H)** **Application Reset Value: 0000 0005_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0												UP_WM	LOW_WM	FULL	EMPTY
r												r	r	r	r

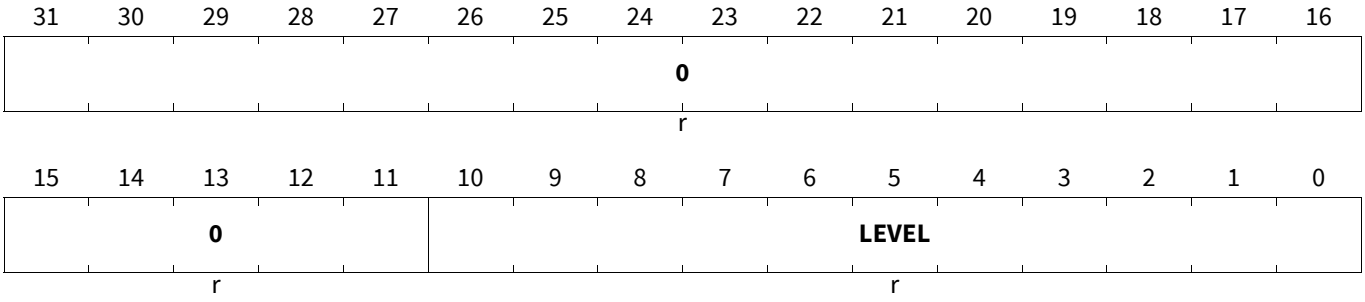
Field	Bits	Type	Description
EMPTY	0	r	**FIFO is empty** Bit only applicable in normal mode. 0_B Fill level greater then 0 1_B Fill level = 0
FULL	1	r	**FIFO is full** Bit only applicable in normal mode. 0_B Fill level less than FIFO[i]_CH[z]_END_ADDR − FIFO[i]_CH[z]_START_ADDR + 1 1_B Fill level = FIFO[i]_CH[z]_END_ADDR − FIFO[i]_CH[z]_START_ADDR + 1
LOW_WM	2	r	**Lower watermark reached** Bit only applicable in normal mode. 0_B Fill level greater than lower watermark 1_B Fill level less than or equal to lower watermark
UP_WM	3	r	**Upper watermark reached** Bit only applicable in normal mode. 0_B Fill level less than upper watermark 1_B Fill level greater than or equal to upper watermark

Field	Bits	Type	Description
0	31:4	r	**Reserved** Read as zero, shall be written as zero.

28.7.5.7 Register FIFO[i]_CH[z]_FILL_LEVEL

FIFOi Channel z Fill Level Register

FIFOi_CHz_FILL_LEVEL (i=0-2;z=0-7)
FIFOi Channel z Fill Level Register (018418_H+i*4000_H+z*40_H) Application Reset Value: 0000 0000_H

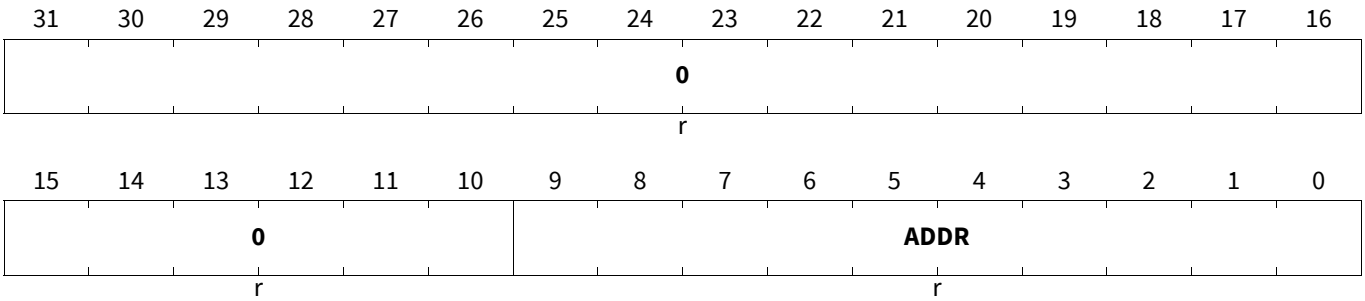


Field	Bits	Type	Description
LEVEL	10:0	r	**Fill level of the current FIFO** LEVEL is in range: 0 ≤ LEVEL ≤ FIFO[i]_CH[z]_END_ADDR − FIFO[i]_CH[z]_START_ADDR + 1 Register content is compared to the upper and lower watermark values for this channel to detect watermark over- and underflow.
0	31:11	r	**Reserved** Read as zero, shall be written as zero.

28.7.5.8 Register FIFO[i]_CH[z]_WR_PTR

FIFOi Channel z Write Pointer Register

FIFOi_CHz_WR_PTR (i=0-2;z=0-7)
FIFOi Channel z Write Pointer Register ($01841C_H$+i*4000_H+z*40_H) Reset Value: Table 21



Field	Bits	Type	Description
ADDR	9:0	r	**Position of the write pointer** ADDR must be in range 0 <= ADDR <= 1023. Initial value for ADDR is defined as ADDR = **FIFO[i]_CH[z]_START_ADDR**
0	31:10	r	**Reserved** Read as zero, shall be written as zero.

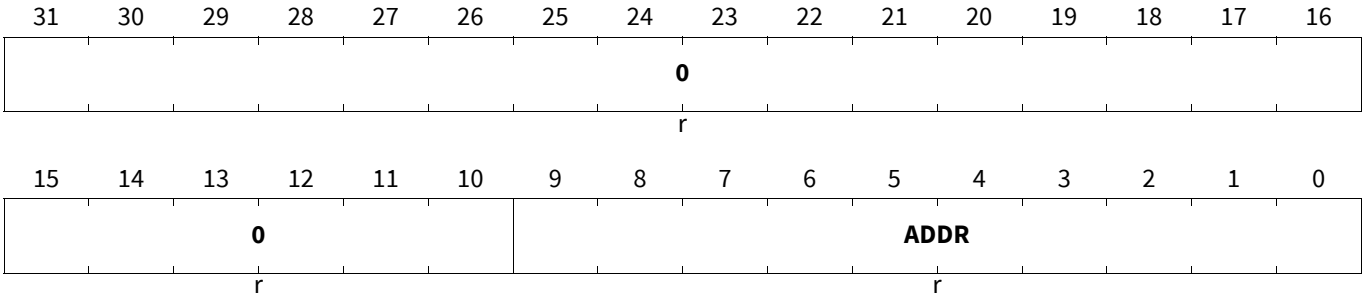
Table 21 Reset Values of FIFOi_CHz_WR_PTR (i=0-2;z=0-7)

Reset Type	Reset Value	Note
Application Reset	0x80 * z	

28.7.5.9 Register FIFO[i]_CH[z]_RD_PTR

FIFOi Channel z Read Pointer Register

FIFOi_CHz_RD_PTR (i=0-2;z=0-7)
FIFOi Channel z Read Pointer Register (018420_H+i*4000_H+z*40_H) **Reset Value: Table 22**



Field	Bits	Type	Description
ADDR	9:0	r	**Position of the read pointer** ADDR must be in range 0 ≤ ADDR ≤ 1023. Initial value for ADDR is defined as ADDR = FIFO[i]_CH[z]_START_ADDR
0	31:10	r	**Reserved** Read as zero, shall be written as zero.

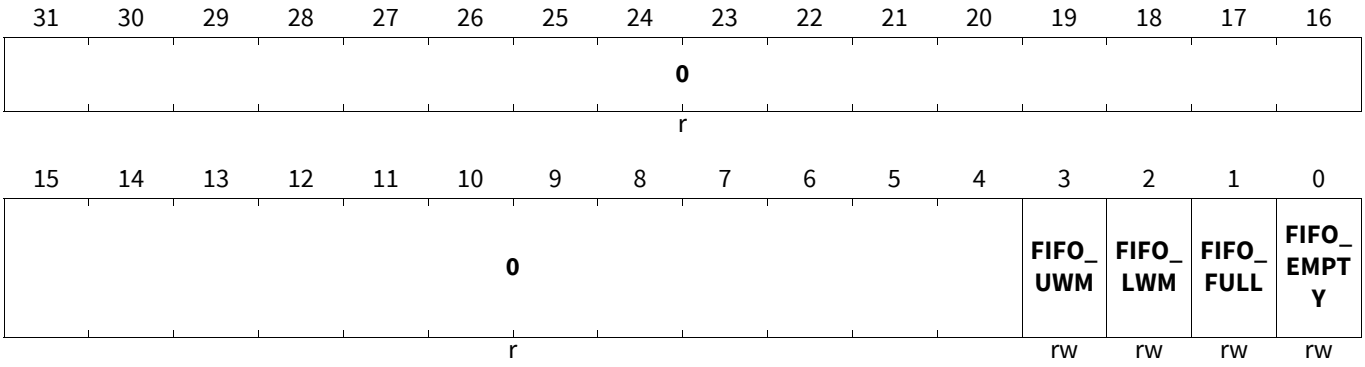
Table 22 Reset Values of FIFOi_CHz_RD_PTR (i=0-2;z=0-7)

Reset Type	Reset Value	Note
Application Reset	0x80 * z	

28.7.5.10 Register FIFO[i]_CH[z]_IRQ_NOTIFY

FIFOi Channel z Interrupt Notification Register

FIFOi_CHz_IRQ_NOTIFY (i=0-2;z=0-7)
FIFOi Channel z Interrupt Notification Register(018424_H+i*4000_H+z*40_H) Application Reset Value: $0000\ 0005_H$



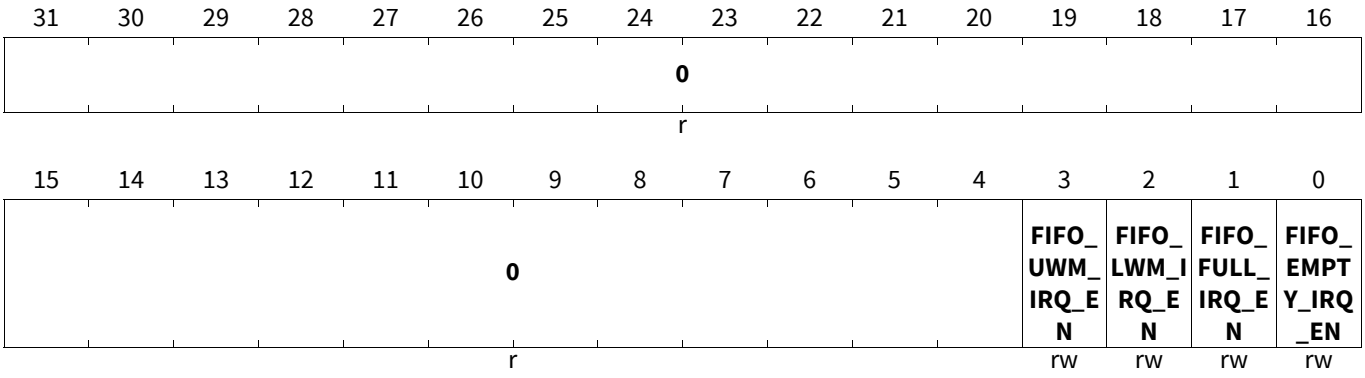
Field	Bits	Type	Description
FIFO_EMPTY	0	rw	**FIFO is empty** This bit will be cleared on a CPU write access of value '1'. A read access leaves the bit unchanged. 0_B No interrupt occurred 1_B FIFO Empty interrupt occurred
FIFO_FULL	1	rw	**FIFO is full** See bit 0.
FIFO_LWM	2	rw	**FIFO lower watermark was under-run** See bit 0.
FIFO_UWM	3	rw	**FIFO upper watermark was over-run** See bit 0.
0	31:4	r	**Reserved** Read as zero, shall be written as zero.

28.7.5.11 Register FIFO[i]_CH[z]_IRQ_EN

FIFOi Channel z Interrupt Enable Register

FIFOi_CHz_IRQ_EN (i=0-2;z=0-7)

FIFOi Channel z Interrupt Enable Register(018428_H+i*4000_H+z*40_H) Application Reset Value: 0000 0000_H



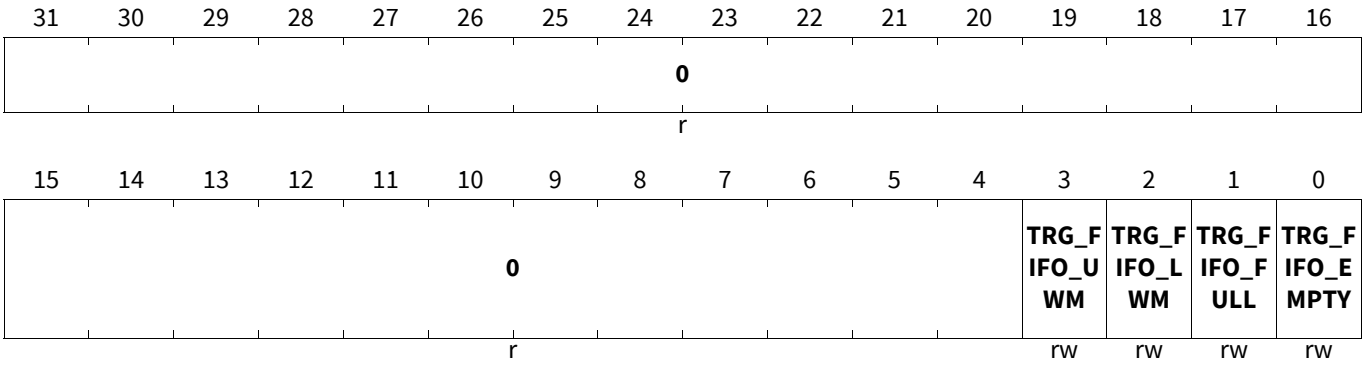
Field	Bits	Type	Description
FIFO_EMPTY_IRQ_EN	0	rw	**FIFO Empty interrupt enable** 0_B Disable interrupt, interrupt is not visible outside GTM 1_B Enable interrupt, interrupt is visible outside GTM
FIFO_FULL_IRQ_EN	1	rw	**FIFO Full interrupt enable** 0_B Disable interrupt, interrupt is not visible outside GTM 1_B Enable interrupt, interrupt is visible outside GTM
FIFO_LWM_IRQ_EN	2	rw	**FIFO Lower Watermark interrupt enable** 0_B Disable interrupt, interrupt is not visible outside GTM 1_B Enable interrupt, interrupt is visible outside GTM
FIFO_UWM_IRQ_EN	3	rw	**FIFO Upper Watermark interrupt enable** 0_B Disable interrupt, interrupt is not visible outside GTM 1_B Enable interrupt, interrupt is visible outside GTM
0	31:4	r	**Reserved** Read as zero, shall be written as zero.

28.7.5.12 Register FIFO[i]_CH[z]_IRQ_FORCINT

FIFOi Channel z Force Interrupt Register

FIFOi_CHz_IRQ_FORCINT (i=0-2;z=0-7)

FIFOi Channel z Force Interrupt Register($01842C_H$+i*4000_H+z*40_H) **Application Reset Value: 0000 0000_H**

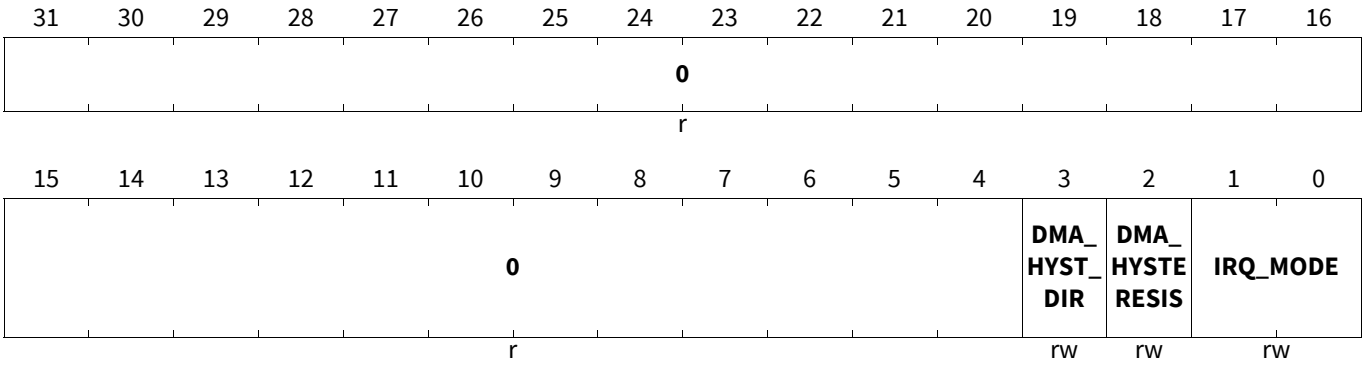


Field	Bits	Type	Description
TRG_FIFO_EMPTY	0	rw	**Force interrupt of FIFO Empty status** This bit is cleared automatically after write. This bit is write protected by bit RF_PROT of register GTM_CTRL 0_B Corresponding bit in status register will not be forced 1_B Assert corresponding field in FIFO[i]_CH[z]_IRQ_NOTIFY register
TRG_FIFO_FULL	1	rw	**Force interrupt of FIFO Full status** This bit is cleared automatically after write. This bit is write protected by bit RF_PROT of register GTM_CTRL. 0_B Corresponding bit in status register will not be forced 1_B Assert corresponding field in FIFO[i]_CH[z]_IRQ_NOTIFY register
TRG_FIFO_LWM	2	rw	**Force interrupt of Lower Watermark** This bit is cleared automatically after write. This bit is write protected by bit RF_PROT of register GTM_CTRL. 0_B Corresponding bit in status register will not be forced 1_B Assert corresponding field in FIFO[i]_CH[z]_IRQ_NOTIFY register
TRG_FIFO_UWM	3	rw	**Force interrupt of Upper Watermark** This bit is cleared automatically after write. This bit is write protected by bit RF_PROT of register GTM_CTRL. 0_B Corresponding bit in status register will not be forced 1_B Assert corresponding field in FIFO[i]_CH[z]_IRQ_NOTIFY register
0	31:4	r	**Reserved** Read as zero, shall be written as zero.

28.7.5.13 Register FIFO[i]_CH[z]_IRQ_MODE

FIFOi Channel z Interrupt Mode Control Register

FIFOi_CHz_IRQ_MODE (i=0-2;z=0-7)
FIFOi Channel z Interrupt Mode Control Register(018430_H+i*4000_H+z*40_H) Application Reset Value: $0000\ 0000_H$

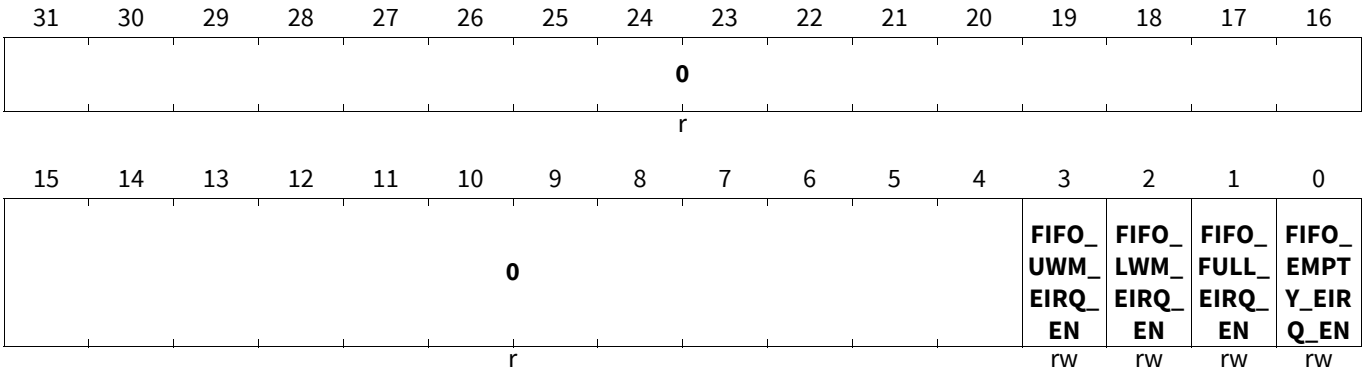


Field	Bits	Type	Description
IRQ_MODE	1:0	rw	**IRQ mode selection** The interrupt modes are described in **Section 28.4.5**. 00_B Level mode 01_B Pulse mode 10_B Pulse-Notify mode 11_B Single-Pulse mode
DMA_HYSTERESIS	2	rw	**Enable DMA hysteresis mode** 0_B Disable FIFO hysteresis for DMA access 1_B Enable FIFO hysteresis for DMA access
DMA_HYST_DIR	3	rw	**DMA direction in hysteresis mode** In the case of DMA writing data to a FIFO, the DMA requests must be generated by the lower watermark. If the DMA hysteresis is enabled, the FIFO does not generate a new DMA request until the upper watermark is reached. In the case of DMA reading data from FIFO, the DMA requests must be generated by the upper watermark. If the DMA hysteresis is enabled, the FIFO does not generate a new DMA request until the lower watermark is reached. 0_B DMA direction read in hysteresis mode 1_B DMA direction write in hysteresis mode
0	31:4	r	**Reserved** Read as zero, shall be written as zero.

28.7.5.14 Register FIFO[i]_CH[z]_EIRQ_EN

FIFOi Channel z Error Interrupt Enable Register

FIFOi_CHz_EIRQ_EN (i=0-2;z=0-7)
FIFOi Channel z Error Interrupt Enable Register(018434_H+i*4000_H+z*40_H) Application Reset Value: $0000\ 0000_H$



Field	Bits	Type	Description
FIFO_EMPTY_EIRQ_EN	0	rw	**FIFO Empty error interrupt enable** 0_B Disable error interrupt, error interrupt is not visible outside GTM 1_B Enable error interrupt, error interrupt is visible outside GTM
FIFO_FULL_EIRQ_EN	1	rw	**FIFO Full error interrupt enable** 0_B Disable error interrupt, error interrupt is not visible outside GTM 1_B Enable error interrupt, error interrupt is visible outside GTM
FIFO_LWM_EIRQ_EN	2	rw	**FIFO Lower Watermark error interrupt enable** 0_B Disable error interrupt, error interrupt is not visible outside GTM 1_B Enable error interrupt, error interrupt is visible outside GTM
FIFO_UWM_EIRQ_EN	3	rw	**FIFO Upper Watermark error interrupt enable** 0_B Disable error interrupt, error interrupt is not visible outside GTM 1_B Enable error interrupt, error interrupt is visible outside GTM
0	31:4	r	**Reserved** Read as zero, shall be written as zero.