28.19 TIM0 Input Mapping Module (MAP)

28.19.1 Overview

The MAP submodule generates the two input signals *TRIGGER* and *STATE* for the submodule DPLL by evaluating the output signals of the channel 0 up to channel 5 of submodule TIM0. By using the TIM as input submodule, the filtering of the input signals can be done inside the TIM channels themselves. The MAP submodule architecture is depicted in **Figure 119**.

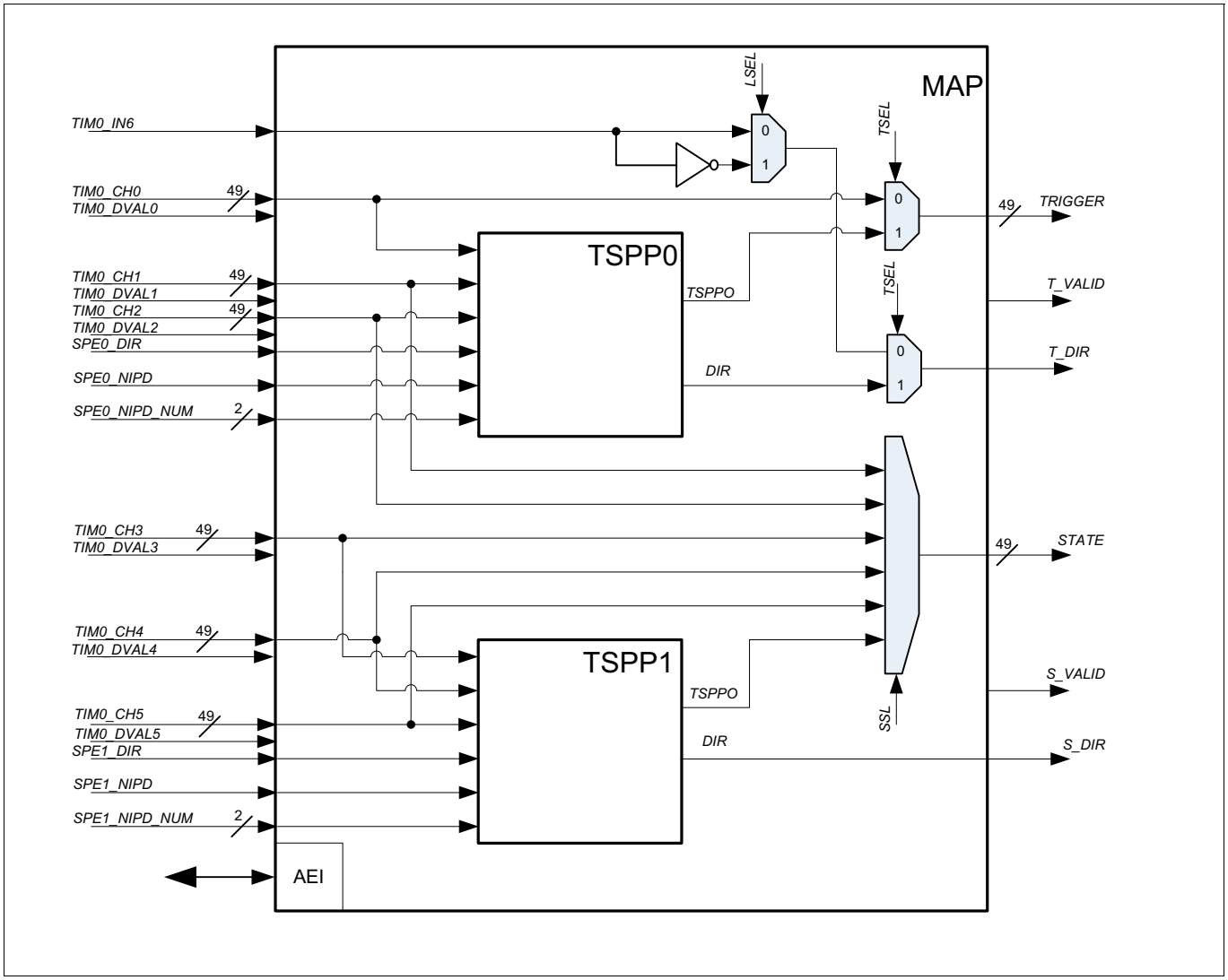

Figure 119 MAP Submodule architecture

Generally, the MAP submodule can route the channel signals coming from TIM0 in three ways. First, it is possible to route the whole 49 bits of data coming from channel 0 of module TIM0 (TIM0_CH0) to the *TRIGGER* signal which is then provided to the DPLL together with the *T_VALID* signal.

Second, the MAP module can route one of the five signals coming from the module TIM0 (i.e. the signals coming from channel 1 up to channel 5) to the output signal *STATE* which is then provided to the module DPLL together with the *S_VALID* signal.

Third, the *TRIGGER*, *T_VALID*, *STATE* and *S_VALID* signals can be generated out of the TIM Signal Preprocessing (TSPP) subunits. This is done in combination with the Sensor Pattern Evaluation (SPE) submodule described in chapter “Sensor Pattern Evaluation “.

There, the signal *TRIGGER* is generated in subunit TSPP0 out of the TIM0 signals coming from channel 0 up to 2.

The signal *STATE* is generated in subunit TSPP1 out of the TIM signals coming from channel 3 up to channel 5.

This is only be done, when the TSSPx subunits are enabled and when the *SPEx_NIPD* signal is raised by the SPE submodule. The *SPEx_NIPD_NUM* signal encodes, which of the 3 *TIMx_CHy* input signals has been changed. The *SPEx_DIR* signal is routed through the TSPPx subunit and implements the *T_DIR* or *S_DIR* signal.

A third method to provide a direction signal to DPLL is to use TIM0 channel 6 input (*TIM0_IN6*) and to route it instead of the *DIR* signal coming from TSSOP0 to the MAP output *T_DIR* (set TSEL=0)

28.19.2 TIM Signal Preprocessing (TSPP)

The TSPP combines the three 49 bit input streams coming from the TIM0 submodule and generates one combined 49 bit output stream *TSPPO*. The input stream combination is done in the unit Bit Stream Combination (BSC). The architecture of the TSPP is shown in **Figure 120**.

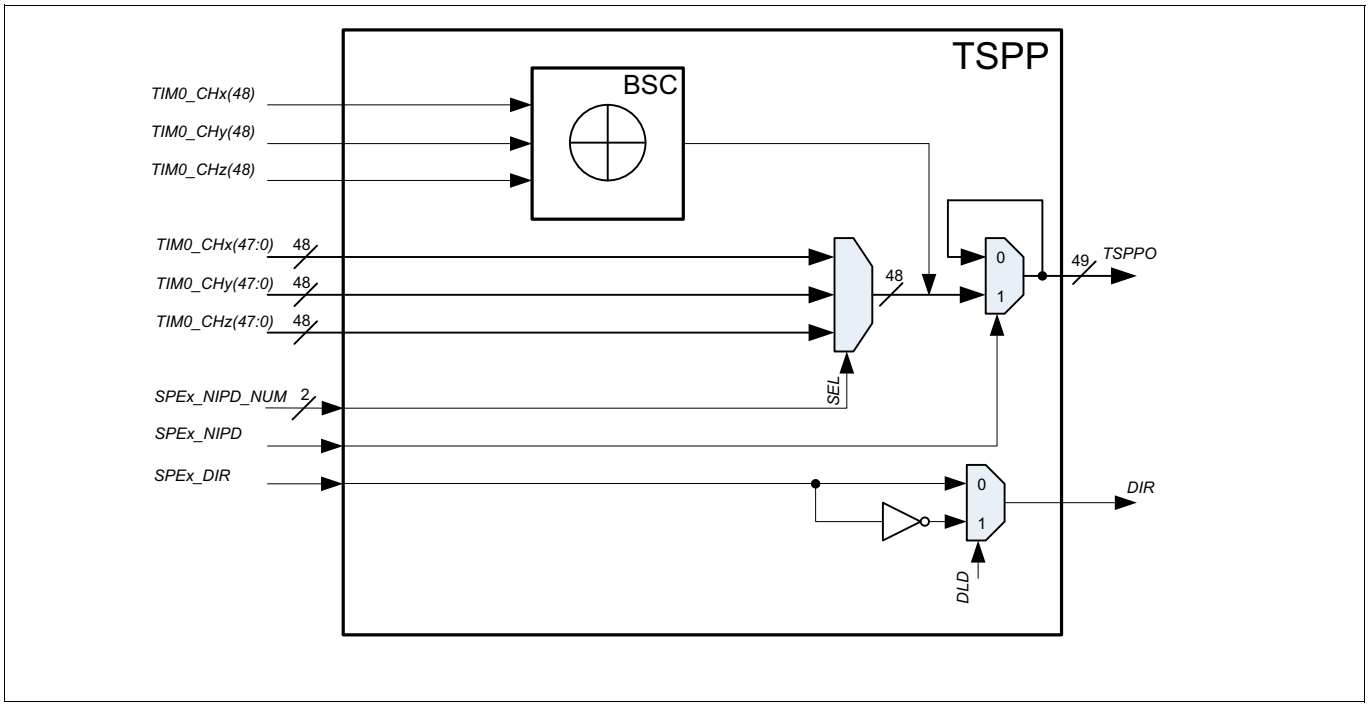

Figure 120 TIM Signal Preprocessing (TSPP) subunit architecture

28.19.2.1 Bit Stream Combination

The BSC subunit is used to XOR-combine the three most significant bits *TIM0_CHx(48)*, *TIM0_CHy(48)* and *TIM0_CHz(48)* of the TIM0 inputs. The XOR-combined signal is merged with the remaining 48 bits of one of the three input signals *TIM0_CHx(47…0)*, *TIM0_CHy(47…0)* or *TIM0_CHz(47…0)* the *TSPPO* signal. The selection is done with the *SPEx_NIPD_NUM* input signal coming from the SPE submodule. The action, when the 49 bits are transferred to the TSPPO and the T_VALID or S_VALID signal is raised is determined by the SPEx_NIPD signal coming from the SPE submodule. The *TSPPO* output signal generation is shown in the example in **Figure 121**.

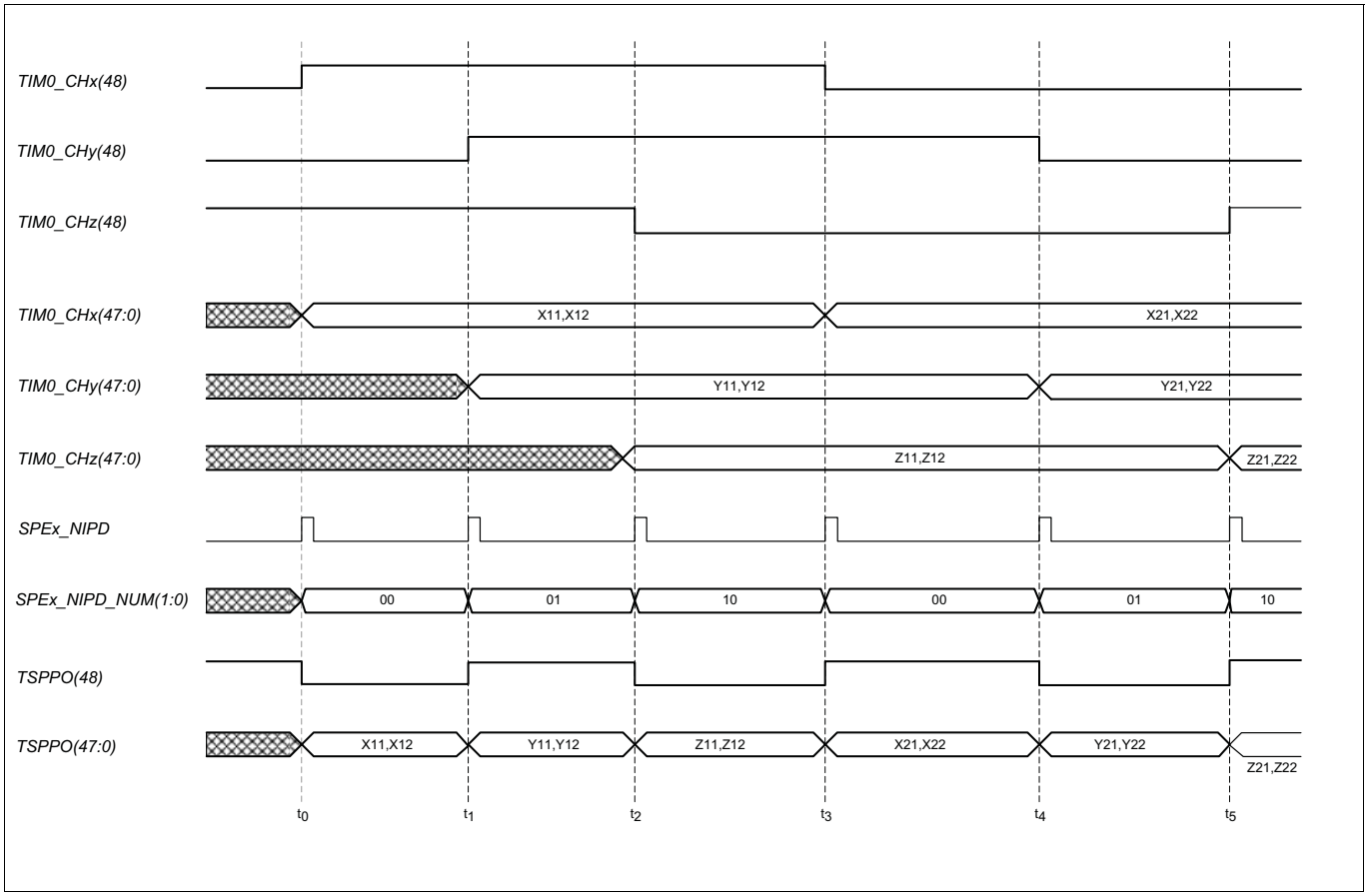

Figure 121 TSPP Signal generation for signal TSPPO

The *SPEx_NIPD_NUM* input signal determines, which data is routed to the *TSPPO* signal. At the first edge of *TIM0_CHx(48)* the new data X11 and X12 are routed to *TSPPO(47:0)*. The values X11 and X12 are the two 24 bit values coming from the TIM input channel TIM0_CHx. The next edge is at time t_1 on signal *TIM0_CHy(48)*. Therefore, at time t_1 the *TSPPO(48)* signal level changes and the *TSPPO(47:0)* is set to Y11 and Y12 and so forth.

28.19.3 MAP Register overview

Table 69 MAP Register overview

Register name	Description	see Page
MAP_CTRL	MAP Control register	434

28.19.4 MAP Register description

28.19.4.1 Register MAP_CTRL

MAP Control Register

MAP_CTRL
MAP Control Register **(000F00$_H$)** **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	TSPP1_I2V	TSPP1_I1V	TSPP1_I0V	0		TSPP1_DLD	TSPP1_EN	0	TSPP0_I2V	TSPP0_I1V	TSPP0_I0V	0		TSPP0_DLD	TSPP0_EN
r	rw	rw	rw	r		rw	rw	r	rw	rw	rw	r		rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0											LSEL	SSL			TSEL
r											rw	rw			rw

Field	Bits	Type	Description
TSEL	0	rw	**TRIGGER signal output select** 0_B TIM0_CH0 selected as TRIGGER output signal. TIM0_IN6 (TIM0 channel 6 input) is used as direction signal T_DIR. 1_B TSPP0_TSPPO selected as TRIGGER output signal
SSL	3:1	rw	**STATE signal output select** 000_B TIM0_CH1 selected as STATE output signal 001_B TIM0_CH2 selected as STATE output signal 010_B TIM0_CH3 selected as STATE output signal 011_B TIM0_CH4 selected as STATE output signal 100_B TIM0_CH5 selected as STATE output signal 101_B TSPP1_TSPPO selected as STATE output signal 110_B Same as 0b000 111_B Same as 0b000
LSEL	4	rw	**TIM0_IN6 input level selection** 0_B TIM0_IN6 input level '0' encodes TRIGGER in forward direction 1_B TIM0_IN6 input level '1' encodes TRIGGER in forward direction
TSPP0_EN	16	rw	**Enable of TSPP0 subunit** 0_B TSPP0 disabled 1_B TSPP0 enabled
TSPP0_DLD	17	rw	**DIR level definition bit** 0_B SPEx_DIR signal is routed through as is 1_B SPEx_DIR signal is inverted
TSPP0_I0V	20	rw	**Disable of TSPP0 TIM0_CHx(48) input line** 0_B Input line enabled 1_B Input line disabled; input for TSPP0 is set to zero (0)

Field	Bits	Type	Description
TSPP0_I1V	21	rw	**Disable of TSPP0 TIM0_CHy(48) input line** 0_B Input line enabled 1_B Input line disabled; input for TSPP0 is set to zero (0)
TSPP0_I2V	22	rw	**Disable of TSPP0 TIM0_CHz(48) input line** 0_B Input line enabled 1_B Input line disabled; input for TSPP0 is set to zero (0)
TSPP1_EN	24	rw	**Enable of TSPP1 subunit** 0_B TSPP1 disabled 1_B TSPP1 enabled
TSPP1_DLD	25	rw	**DIR level definition bit** 0_B SPEx_DIR signal is routed through as is 1_B SPEx_DIR signal is inverted
TSPP1_I0V	28	rw	**Disable of TSPP1 TIM0_CHx(48) input line** 0_B Input line enabled 1_B Input line disabled; input for TSPP1 is set to zero (0)
TSPP1_I1V	29	rw	**Disable of TSPP1 TIM0_CHy(48) input line** 0_B Input line enabled 1_B Input line disabled; input for TSPP1 is set to zero (0)
TSPP1_I2V	30	rw	**Disable of TSPP1 TIM0_CHz(48) input line** 0_B Input line enabled 1_B Input line disabled; input for TSPP1 is set to zero (0)
0	15:5, 19:18, 23, 27:26, 31	r	**Reserved** Read as zero, shall be written as zero.