To manage a second global frequency CMU_GCLK_EN could be replaced by ECLK[1]_EN for CMU_CLK[x](x:0..7). Also the all-time enabled CMU_CLK8 could be replaced by ECLK[0]_EN.

Each of the external clocks dividers are enabled and disabled by setting the appropriate bit field **EN_ECLK[z]** in the register **CMU_CLK_EN**.

The clock frequencies $f_{CMU\_ECLK[z]} = 1/T_{CMU\_ECLK[z]}$ of the external clocks are controlled with the registers **CMU_ECLK_[z]_NUM** and **CMU_ECLK_[z]_DEN** as follows:

$$T_{CMU\_ECLK}[z] = (ECLK[z]\_NUM / ECLK[z]\_DEN) * T_{CLS0\_CLK}$$

and is implemented according the following algorithm

(*Z:CMU_ECLK_[z]_NUM(23:0); N: CMU_ECLK_[z]_DEN(23:0*); *Z,N >0*; *Z>=N; CMU_ECLK[z]*='0'):

(1) Set remainder (*R*), operand1 (*OP1*) and operand2 (*OP2*) register during INIT-phase (with implicit conversion to signed): *R=Z, OP1=N, OP2=N-Z;*

(2) After leaving INIT-phase (*CMU_ECLK[z]* has been enabled) the sign of remainder R for each *CLS0_CLK* cycle will be checked:

(3) If *R>0* keep updating remainder and keep *CMU_ECLK[z]*: *R=R-OP1;*

(4) If *R<0* update remainder and toggle *CMU_ECLK[z]*: *R=R-OP2*;

After at most (*Z/N*+1) subtractions (3) there will be a negative *R* and an active phase of the generated clock enable (for one cycle) will be triggered (4). The remainder *R* is a measure for the distance to a real *Z/N* clock and will be regarded for the next generated clock toggle phase. The new *R* value will be *R=R+(Z-N)*. In the worst case the remainder *R* will sum up to an additional cycle in the generated clock toggle period after *Z*-cycles. In the other cases equally distributed additional cycles will be inserted for the generated clock toggle. If *Z* is an integer multiple of *N* no additional cycles will be included for the generated clock toggle at all. Note that for a better resource sharing all arithmetic has been reduced to subtractions and the initialization of the remainder *R* uses the complement of (*Z-N*).

The default value of the *CMU_ECLK[z]* output is low.

28.10.6 CMU Configuration Register Overview

Table 25 CMU Configuration Register Overview

Register Name	Description	see Page
CMU_CLK_EN	CMU clock enable	107
CMU_GCLK_NUM	CMU global clock control numerator	108
CMU_GCLK_DEN	CMU global clock control denominator	108
CMU_CLK_[z]_CTRL	CMU control for clock source z	109
CMU_ECLK_[z]_NUM	CMU external clock z control numerator	110
CMU_ECLK_[z]_DEN	CMU external clock z control denominator	110
CMU_FXCLK_CTRL	CMU control FXCLK sub-unit input clock	111
CMU_GLB_CTRL	CMU synchronizing ARU and clock source	112
CMU_CLK_CTRL	CMU control for clock source selection	113