

System Timer (STM)

Table 1 Register Overview - STM (ascending Offset Address) (cont'd)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
KRST0	Kernel Reset Register 0	00F4 _H	U,SV	SV,E,P	Application Reset	21
ACCEN1	Access Enable Register 1	00F8 _H	U,SV	SV,SE	Application Reset	20
ACCEN0	Access Enable Register 0	00FC _H	U,SV	SV,SE	Application Reset	20

27.4.1 Clock Control Register

Clock Control Register

The STM clock control register is used to switch the STM on or off and to control its input clock rate. After reset, the STM is always enabled and starts counting. The STM can be disabled by setting bit DISR to 1.

CLC

Clock Control Register (0000_H) **Application Reset Value: 0000 0000_H**

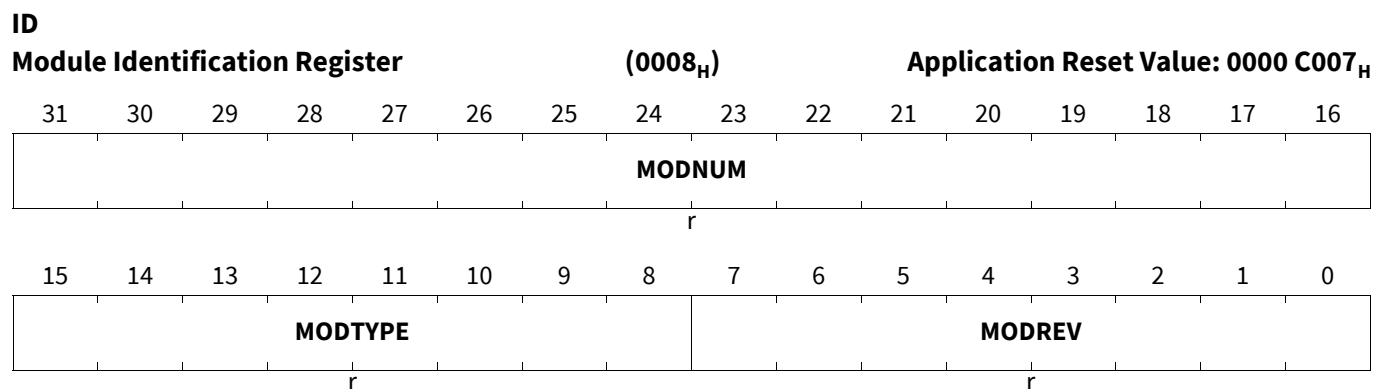
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0												EDIS	0	DISS	DISR
r												rw	rw	r	rw

Field	Bits	Type	Description
DISR	0	rw	Module Disable Request Bit Used for enable/disable control of the STM module. <i>Note:</i> f_{STM} is generated by the CCU. 0 _B No disable requested 1 _B Disable requested
DISS	1	r	Module Disable Status Bit Bit indicates the current status of the STM module. 0 _B STM module is enabled 1 _B STM module is disabled
EDIS	3	rw	Sleep Mode Enable Control Used for module sleep mode control.
0	2	rw	Reserved Read as 0; shall be written with 0.
0	31:4	r	Reserved Read as 0; should be written with 0.

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Module Identification Register

The STM Module Identification Register ID contains read-only information about the module version.



Field	Bits	Type	Description
MODREV	7:0	r	Module Revision Number MODREV defines the module revision number. The value of a module revision starts with 01 _H (first revision). Current revision is 0x7.
MODTYPE	15:8	r	Module Type This bit field defines the module as a 32-bit module: C0 _H
MODNUM	31:16	r	Module Number Value This bit field defines the module identification number for the STM: 0068 _H