## 28.18 Memory Configuration (MCFG)

### 28.18.1 Overview

The Memory Configuration submodule (MCFG) is an infrastructure module that organizes physical memory blocks and maps them to the RAM ports 0 and 1 of available Multi Channel Sequencer (MCS) modules.

The following parameters are design variables for the MCFG hardware structure that can vary in its range for different devices:

| Constant | Description | Value |
|---|---|---|
| MAW | Memory address width of a large physical memory block. | 11 |
| ERM | Enable RAM1 MSB (0 - RAM1 MSB disabled, 1 - RAM1 MSB enabled,) | 0 |

It should be noted that the actual value of the parameter ERM can be obtained by the bit **ERM** of the register **CCM[i]_HW_CONF**.

Depending on the value of parameter ERM, the MCFG module assumes externally connected physical RAM modules with different sizes. If ERM = 0, MCFG assumes that each MCS instance provides a large physical memory block with $2^{MAW}$ memory locations each 32 bit wide which leads to a RAM module with $2^{MAW+2}$ (byte wise) memory addresses. Further each MCS instance provides a small physical memory block with $2^{MAW-1}$ memory locations each 32 bit wide leading to a RAM module with $2^{MAW+1}$ (byte wise) memory addresses. If ERM = 1, MCFG assumes that each MCS instance provides two large physical memory block each with $2^{MAW}$ memory locations each 32-bit leading to a RAM module with $2^{MAW+2}$ (byte wise) memory addresses.

In order to support different memory sizes for different MCS instances, the MCFG module provides three layout configurations for reorganization of memory pages mapped to the RAM ports of neighboring MCS modules. Figure **Figure 115** shows all layout configurations for the case that ERM = 0 and **Figure 117** shows the layout configurations for the case that ERM = 1. Each box in these pictures represents a physical memory block.

The layout configuration DEFAULT is always assigning a memory block of size $2^{MAW}$x32 bits to MCS RAM port 0. Depending on ERM, RAM port 1 of each MCS is assigned to a memory block of size $2^{MAW-1}$x32 bits (ERM = 0) or a memory block of size $2^{MAW}$x32 bits (ERM = 1).

The layout configuration SWAP is swapping the memory block assigned to RAM port 1 of the current MCS instance with the memory block assigned to RAM port 0 of the successive MCS instance. If ERM = 0, this means that the memory of the current MCS instance is increased by $2^{MAW-1}$x32 bits but the memory of the successor is decreased by $2^{MAW-1}$x32 bits compared to the DEFAULT configuration. If ERM = 1, the SWAP configuration has no effect on the memory sizes of the individual MCS instances.

The layout configuration BORROW is borrowing the memory block assigned to RAM port 0 of the successive MCS instance for the current instance. This means, the memory of the current MCS module is increased by $2^{MAW}$x32 bits but the memory of the successor is decreased by $2^{MAW}$x32 bits compared to the DEFAULT configuration.

Considering the order the mentioned MCS modules, it should be noted that the successor of the last MCS instance is the first MCS instance MCS0.

The actual sizes of the memory pages mapped to the MCS RAM ports 0 and 1 depends on the layout configuration for of current instance MCS[i] and the layout configuration of the preceding memory instance MCS[i-1]. The sizes of these memory pages can be obtained by the layout parameters MP0 and MP1, as described in the specification of the MCS.

**Figure 116** and **Figure 118** summarize the layout parameters MP0 and MP1 of MCS instance MCS[i] for the case that ERM = 0 and ERM = 1. Note that the predecessor of instance MCS0 is last available MCS instance.

The addressing of memory port 0 ranges from 0 to MP0-4 and the addressing of memory page 1 ranges from MP0 to MP1-4.

This document assumes that the GTM implementation embeds 8 MCS instances. However, the actual number of implemented MCS instances is specified in device specific appendix.

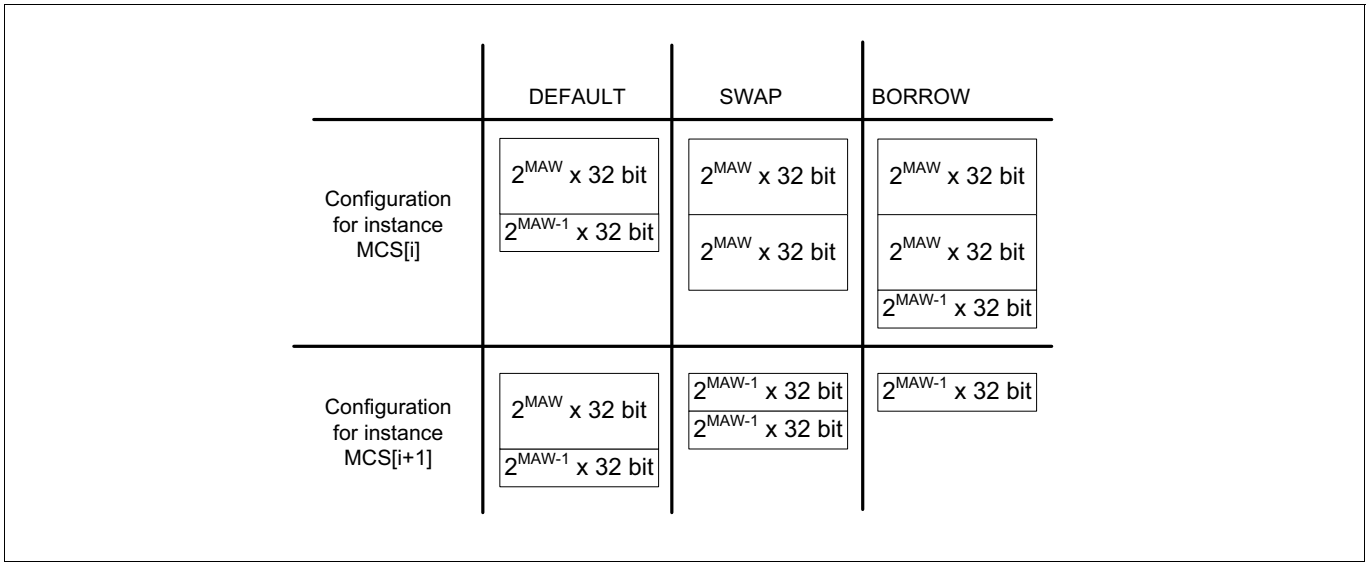


**Figure 115 Memory Layout Configurations (ERM = 0)**

| Memory Layout Option of current MCS instance MCS[i] | | | Memory Layout Option of preceding MCS instance MCS[i-1]: DEFAULT | SWAP | BORROW |
|---|---|---|---|---|---|
| DEFAULT | | MP0 | $2^{MAW+2}$ | $2^{MAW+1}$ | 0 |
| | | MP1 | $2^{MAW+2} + 2^{MAW+1}$ | $2^{MAW+2}$ | $2^{MAW+1}$ |
| SWAP | | MP0 | $2^{MAW+2}$ | $2^{MAW+1}$ | 0 |
| | | MP1 | $2^{MAW+3}$ | $2^{MAW+2} + 2^{MAW+1}$ | $2^{MAW+2}$ |
| BORROW | | MP0 | $2^{MAW+2}$ | $2^{MAW+1}$ | 0 |
| | | MP1 | $2^{MAW+3} + 2^{MAW+1}$ | $2^{MAW+3}$ | $2^{MAW+2} + 2^{MAW+1}$ |

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**Figure 116 Memory Layout Parameters (ERM = 0)**

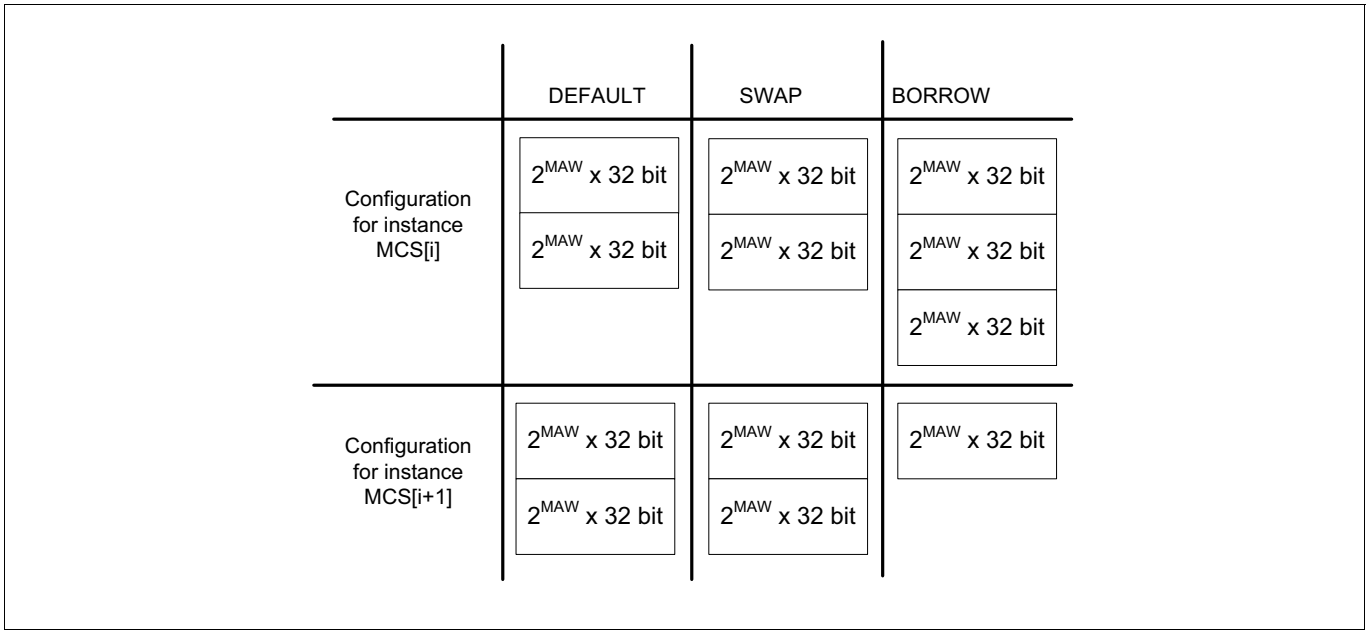


**Figure 117 Memory Layout Configurations (ERM = 1)**

| Memory Layout Option of current MCS instance MCS[i] | | | Memory Layout Option of preceding MCS instance MCS[i-1] | | |
|---|---|---|---|---|---|
| | | | DEFAULT | SWAP | BORROW |
| DEFAULT | | MP0 | $2^{MAW+2}$ | $2^{MAW+2}$ | 0 |
| | | MP1 | $2^{MAW+3}$ | $2^{MAW+3}$ | $2^{MAW+2}$ |
| SWAP | | MP0 | $2^{MAW+2}$ | $2^{MAW+2}$ | 0 |
| | | MP1 | $2^{MAW+3}$ | $2^{MAW+3}$ | $2^{MAW+2}$ |
| BORROW | | MP0 | $2^{MAW+2}$ | $2^{MAW+2}$ | 0 |
| | | MP1 | $2^{MAW+2} + 2^{MAW+3}$ | $2^{MAW+2} + 2^{MAW+3}$ | $2^{MAW+3}$ |

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**Figure 118 Memory Layout Parameters (ERM = 1)**

## 28.18.2 MCFG Register Overview

**Table 68 MCFG Configuration Registers Overview**

| Register Name | Description | see Page |
|---|---|---|
| MCFG_CTRL | MCFG Memory layout configuration. | 430 |

## 28.18.3 MCFG Register Description

### 28.18.3.1 Register MCFG_CTRL

**MCFG Memory Layout Configuration Register**

It should be noted that the actual GTM implementation may embed less MCS instances than mentioned in this register (see product specific appendix). In this case this register only implements the register bits for available MCS instances.

This register is only writable if the bit **RF_PROT** in register **GTM_CTRL** is cleared.

**MCFG_CTRL**

**MCFG Memory Layout Configuration Register (000F40$_H$)** **Application Reset Value: 0000 0000$_H$**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | | | | | | | | | | | | MEM9 | | MEM8 | |
| r | | | | | | | | | | | | rw | | rw | |

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| MEM7 | | MEM6 | | MEM5 | | MEM4 | | MEM3 | | MEM2 | | MEM1 | | MEM0 | |
| rw | | rw | | rw | | rw | | rw | | rw | | rw | | rw | |

| Field | Bits | Type | Description |
|---|---|---|---|
| **MEMx (x=0-9)** | 2*x+1:2*x | rw | **Configure Memory pages for MCS-instance MCSx**<br>$00_B$ DEFAULT configuration<br>$01_B$ SWAP configuration<br>$10_B$ BORROW configuration<br>$11_B$ Reserved, do not use. |
| **0** | 31:20 | r | **Reserved**<br>Read as zero, shall be written as zero. |