28.5.7 ARU Configuration Register Description

28.5.7.1 Register ARU_ACCESS

ARU Access Register

Note: The register ARU_ACCESS can be used either for reading or for writing at the same point in time.

ARU_ACCESS
ARU Access Register **(000280$_H$)** **Application Reset Value: 0000 01FE$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		WREQ	RREQ	0			ADDR								
r		rw	rw	r			rw								

Field	Bits	Type	Description
ADDR	8:0	rw	**ARU address** Define the ARU address used for transferring data. For an ARU write request, the preferred address 0x0 have to be used. A write request to the address 0x1FF (always full address) or 0x1FE (always empty address) are ignored and doesn't have any effect. ARU address bits ADDR are only writable if RREQ and WREQ bits are zero.
RREQ	12	rw	**Initiate read request** This bit is cleared automatically after transaction. Moreover, it can be cleared by software to cancel a read request. RREQ bit is only writable if WREQ bit is zero, so to switch from RREQ to WREQ a cancel request has to be performed before. Configuring both RREQ and WREQ bits results in a read request, so RREQ bit will be set if the WREQ bit of the register isn't already set. The ARU read request on address ADDR is served immediately when no other destination has actually a read request when the RREQ bit is set by CPU. In a worst case scenario, the read request is served after one round trip of the ARU, but this is only the case when every destination channel issues a read request at consecutive points in time. 0_B No read request is pending 1_B Set read request to source channel addressed by ADDR

Field	Bits	Type	Description
WREQ	13	rw	**Initiate write request** This bit is cleared automatically after transaction. Moreover, it can be cleared by software to cancel a write request. WREQ bit is only writable if RREQ bit is zero, so to switch from WREQ to RREQ a cancel request has to be performed before. Configuring both RREQ and WREQ bits results in a read request, so WREQ bit will not be set The data is provided at address ADDR. This address has to be programmed as the source address in the destination sub-module channel. In worst case, the data is provided after one full ARU round trip. 0_B No write request is pending 1_B Mark data in registers ARU_DATA_H and ARU_DATA_L as valid
0	11:9, 31:14	r	**Reserved** Read as zero, shall be written as zero.

28.5.7.2 Register ARU_DATA_H

ARU Access Register Upper Data Word

ARU_DATA_H
ARU Access Register Upper Data Word **(000284_H)** **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0			**DATA**												
r			rw												

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA															
rw															

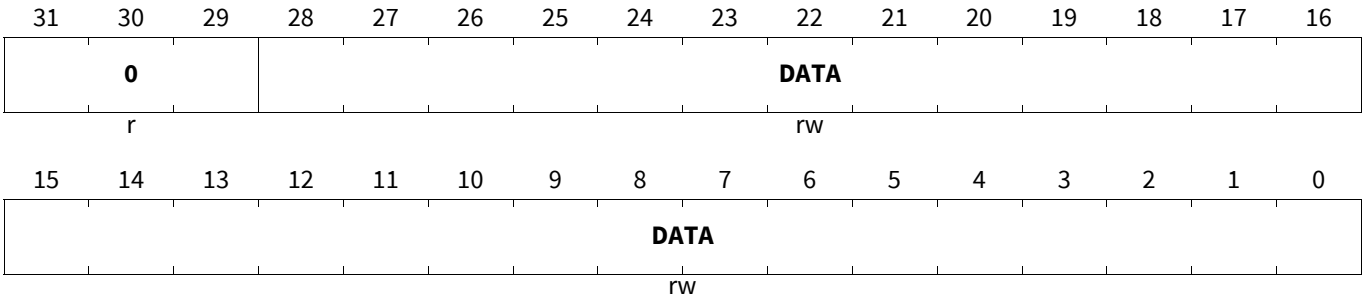
Field	Bits	Type	Description
DATA	28:0	rw	**Upper ARU data word** Transfer upper ARU data word addressed by ADDR. The data bits 24 to 52 of an ARU word are mapped to the data bits 0 to 28 of this register.
0	31:29	r	**Reserved** Read as zero, shall be written as zero.

28.5.7.3 Register ARU_DATA_L

ARU Access Register Lower Data Word

ARU_DATA_L

ARU Access Register Lower Data Word **(000288$_H$)** **Application Reset Value: 0000 0000$_H$**



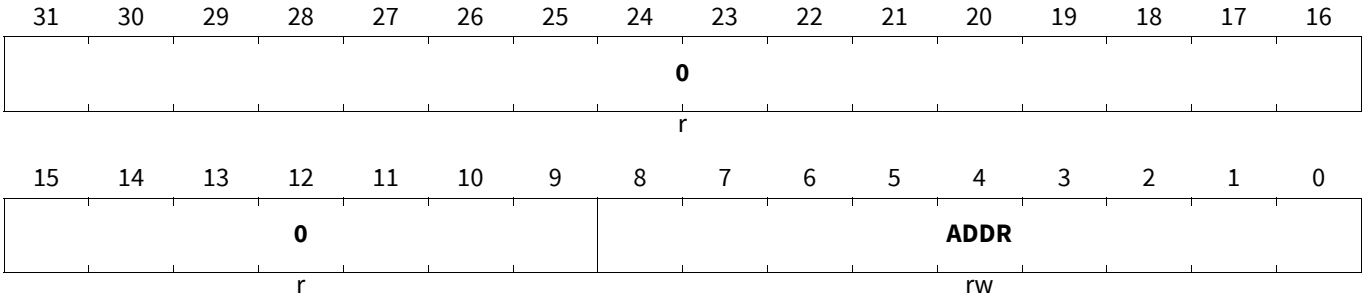
Field	Bits	Type	Description
DATA	28:0	rw	**Lower ARU data word** Transfer lower ARU data word addressed by ADDR. The data bits 0 to 23 of an ARU word are mapped to the data bits 0 to 23 of this register and the data bits 48 to 52 of an ARU word are mapped to the data bits 24 to 28 of this register when data is read by the CPU. For writing data into the ARU by the CPU the bits 24 to 28 are **not** transferred to bit 48 to 52 of the ARU word. Only bits 0 to 23 are written to bits 0 to 23 of the ARU word.
0	31:29	r	**Reserved** Read as zero, shall be written as zero.

28.5.7.4 Register ARU_DBG_ACCESS0

ARU Debug Access Channel 0

ARU_DBG_ACCESS0

ARU Debug Access Channel 0 **(00028C$_H$)** **Application Reset Value: 0000 01FE$_H$**



Field	Bits	Type	Description
ADDR	8:0	rw	**ARU debugging address** Define address of ARU debugging channel 0.

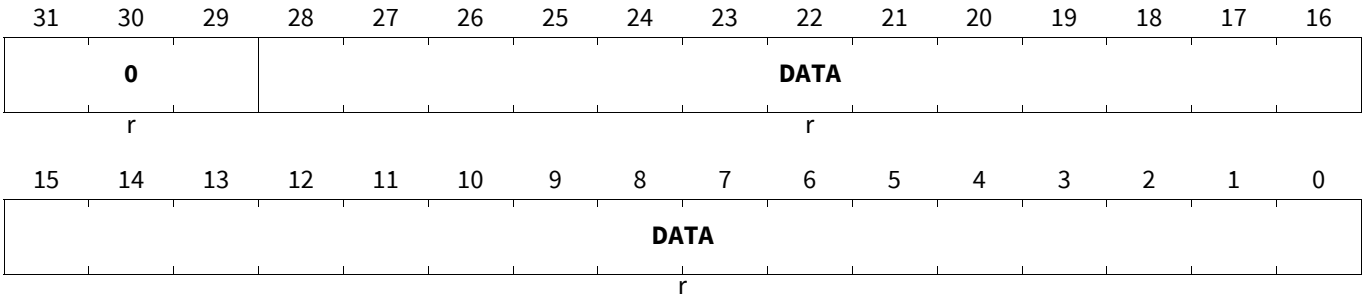
Field	Bits	Type	Description
0	31:9	r	**Reserved** Read as zero, shall be written as zero.

28.5.7.5 Register ARU_DBG_DATA0_H

ARU Debug Access 0 Transfer Register Upper Data Word

ARU_DBG_DATA0_H

ARU Debug Access 0 Transfer Register Upper Data Word(000290$_H$) **Application Reset Value: 0000 0000$_H$**



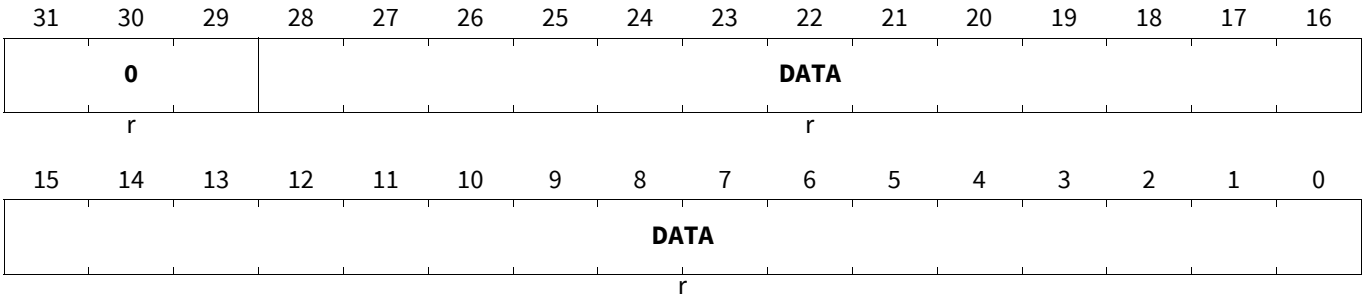
Field	Bits	Type	Description
DATA	28:0	r	**Upper debug data word** Transfer upper ARU data word addressed by register **DBG_ACCESS0**. The data bits 24 to 52 of an ARU word are mapped to the data bits 0 to 28 of this register The interrupt *ARU_NEW_DATA0_IRQ* is raised if a new data word is available.
0	31:29	r	**Reserved** Read as zero, shall be written as zero.

28.5.7.6 Register ARU_DBG_DATA0_L

ARU Debug Access 0 Transfer Register Lower Data Word

ARU_DBG_DATA0_L

ARU Debug Access 0 Transfer Register Lower Data Word(000294$_H$) **Application Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
DATA	28:0	r	**Lower debug data word** Transfer lower ARU data word addressed by register **DBG_ACCESS0**. The data bits 0 to 23 of an ARU word are mapped to the data bits 0 to 23 of this register and the data bits 48 to 52 of an ARU word is mapped to the data bits 24 to 28 of this register. The interrupt *ARU_NEW_DATA0_IRQ* is raised if a new data word is available.
0	31:29	r	**Reserved** Read as zero, shall be written as zero

28.5.7.7 Register ARU_DBG_ACCESS1

ARU Debug Access Channel 1

ARU_DBG_ACCESS1
ARU Debug Access Channel 1 **(000298_H)** **Application Reset Value: 0000 01FE$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							**ADDR**								
r							rw								

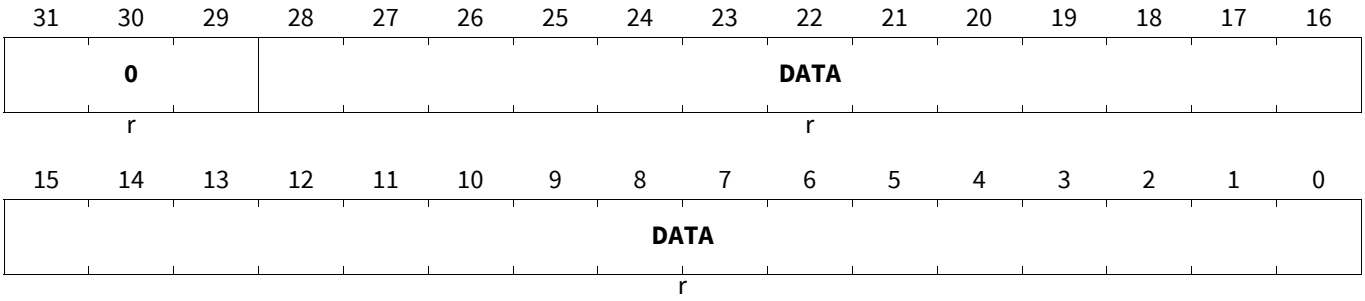
Field	Bits	Type	Description
ADDR	8:0	rw	**ARU debugging address** Define address of ARU debugging channel 1.
0	31:9	r	**Reserved** Read as zero, shall be written as zero

28.5.7.8 Register ARU_DBG_DATA1_H

ARU Debug Access 1 Transfer Register Upper Data Word

ARU_DBG_DATA1_H

ARU Debug Access 1 Transfer Register Upper Data Word(00029C$_H$) **Application Reset Value: 0000 0000$_H$**



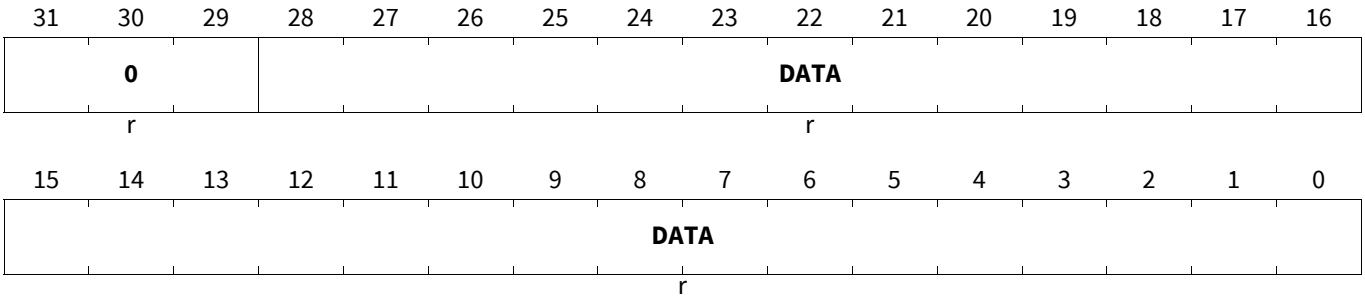
Field	Bits	Type	Description
DATA	28:0	r	**Upper debug data word** Transfer upper ARU data word addressed by register **DBG_ACCESS1**. The data bits 24 to 52 of an ARU word are mapped to the data bits 0 to 28 of this register. The interrupt *ARU_NEW_DATA1_IRQ* is raised if a new data word is available.
0	31:29	r	**Reserved** Read as zero, shall be written as zero.

28.5.7.9 Register ARU_DBG_DATA1_L

ARU Debug Access 1 Transfer Register Lower Data Word

ARU_DBG_DATA1_L

ARU Debug Access 1 Transfer Register Lower Data Word(0002A0$_H$) **Application Reset Value: 0000 0000$_H$**



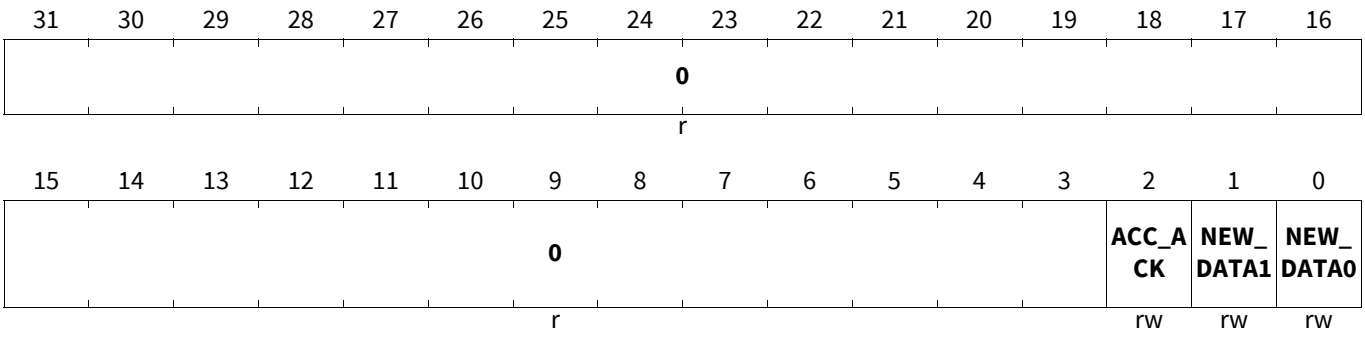
Field	Bits	Type	Description
DATA	28:0	r	**Lower debug data word** Transfer lower ARU data word addressed by register **DBG_ACCESS1**. The data bits 0 to 23 of an ARU word are mapped to the data bits 0 to 23 of this register and the data bits 48 to 52 of an ARU word is mapped to the data bits 24 to 28 of this register. The interrupt *ARU_NEW_DATA1_IRQ* is raised if a new data word is available.
0	31:29	r	**Reserved** Read as zero, shall be written as zero.

28.5.7.10 Register ARU_IRQ_NOTIFY

ARU Interrupt Notification Register

ARU_IRQ_NOTIFY

ARU Interrupt Notification Register **(0002A4$_H$)** **Application Reset Value: 0000 0000$_H$**

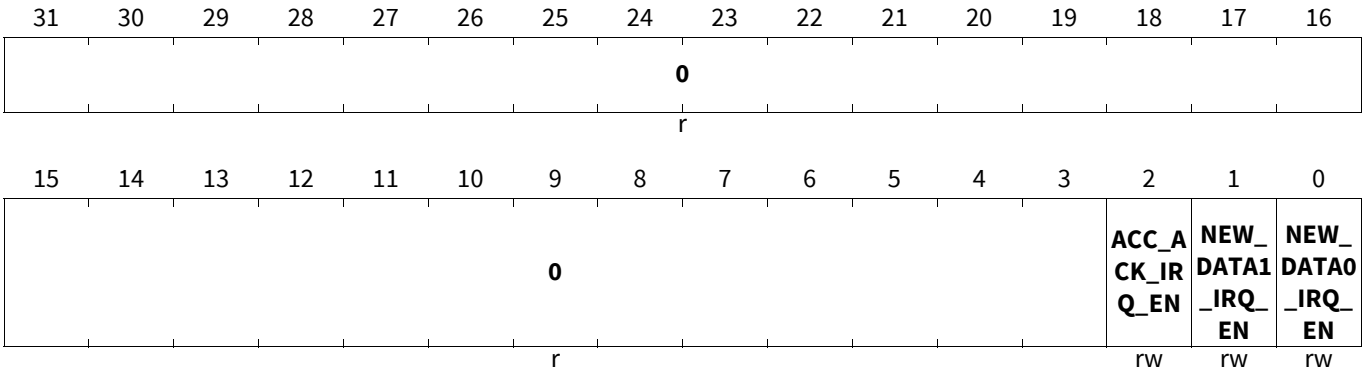


Field	Bits	Type	Description
NEW_DATA0	0	rw	**Data was transferred for addr ARU_DBG_ACCESS0** This bit will be cleared on a CPU write access of value '1'. (As the bit is rw, otherwise no clear.) A read access leaves the bit unchanged. 0_B No interrupt occurred 1_B ARU_NEW_DATA0_IRQ interrupt was raised by the ARU
NEW_DATA1	1	rw	**Data was transferred for addr ARU_DBG_ACCESS1** This bit will be cleared on a CPU write access of value '1'. (As the bit is rw, otherwise no clear.) A read access leaves the bit unchanged. 0_B No interrupt occurred 1_B ARU_NEW_DATA1_IRQ interrupt was raised by the ARU
ACC_ACK	2	rw	**AEI to ARU access finished, on read access data are valid** This bit will be cleared on a CPU write access of value '1'. (As the bit is rw, otherwise no clear.) A read access leaves the bit unchanged.
0	31:3	r	**Reserved** Read as zero, shall be written as zero.

28.5.7.11 Register ARU_IRQ_EN

ARU Interrupt Enable Register

ARU_IRQ_EN
ARU Interrupt Enable Register **($0002A8_H$)** **Application Reset Value: $0000\ 0000_H$**



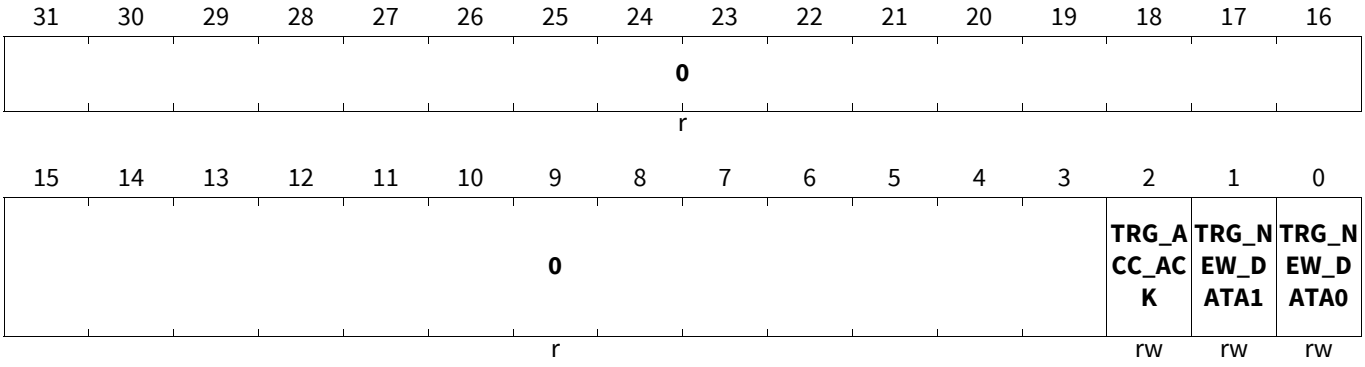
Field	Bits	Type	Description
NEW_DATA0_IRQ_EN	0	rw	**ARU_NEW_DATA0_IRQ interrupt enable** 0_B Disable interrupt, interrupt is not visible outside GTM 1_B Enable interrupt, interrupt is visible outside GTM
NEW_DATA1_IRQ_EN	1	rw	**ARU_NEW_DATA1_IRQ interrupt enable** 0_B Disable interrupt, interrupt is not visible outside GTM 1_B Enable interrupt, interrupt is visible outside GTM
ACC_ACK_IRQ_EN	2	rw	**ACC_ACK_IRQ interrupt enable** 0_B Disable interrupt, interrupt is not visible outside GTM 1_B Enable interrupt, interrupt is visible outside GTM

Field	Bits	Type	Description
0	31:3	r	**Reserved** Read as zero, shall be written as zero.

28.5.7.12 Register ARU_IRQ_FORCINT

ARU Force Interrupt Register

ARU_IRQ_FORCINT
ARU Force Interrupt Register **(0002AC$_H$)** **Application Reset Value: 0000 0000$_H$**

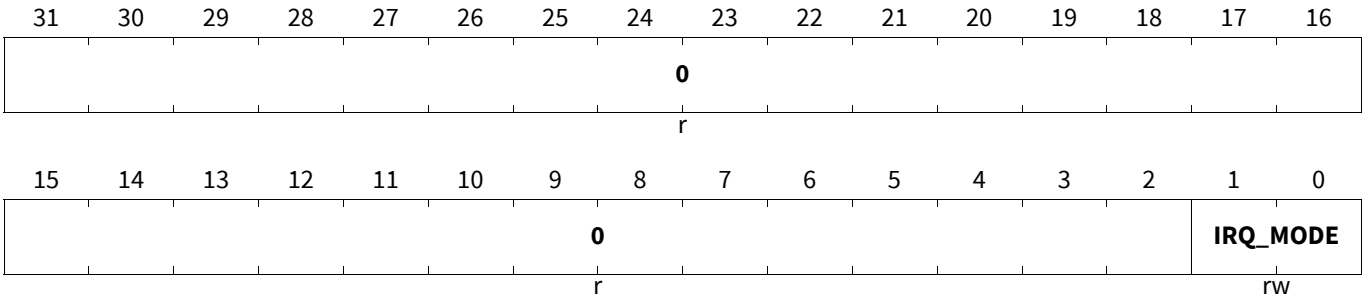


Field	Bits	Type	Description
TRG_NEW_DATA0	0	rw	**Trigger new data 0 interrupt** Note: This bit is cleared automatically after write. This bit is write protected by bit RF_PROT of register GTM_CTRL. 0_B Corresponding bit in status register will not be forced 1_B Assert corresponding field in ARU_IRQ_NOTIFY register
TRG_NEW_DATA1	1	rw	**Trigger new data 1 interrupt** Note: This bit is cleared automatically after write. This bit is write protected by bit RF_PROT of register GTM_CTRL. 0_B Corresponding bit in status register will not be forced 1_B Assert corresponding field in ARU_IRQ_NOTIFY register
TRG_ACC_ACK	2	rw	**Trigger ACC_ACK interrupt** Note: This bit is cleared automatically after write. This bit is write protected by bit RF_PROT of register GTM_CTRL. 0_B Corresponding bit in status register will not be forced 1_B Assert corresponding field in ARU_IRQ_NOTIFY register
0	31:3	r	**Reserved** Read as zero, shall be written as zero.

28.5.7.13 Register ARU_IRQ_MODE

ARU Interrupt Mode Register

ARU_IRQ_MODE
ARU Interrupt Mode Register **(0002B0$_H$)** **Application Reset Value: 0000 0000$_H$**

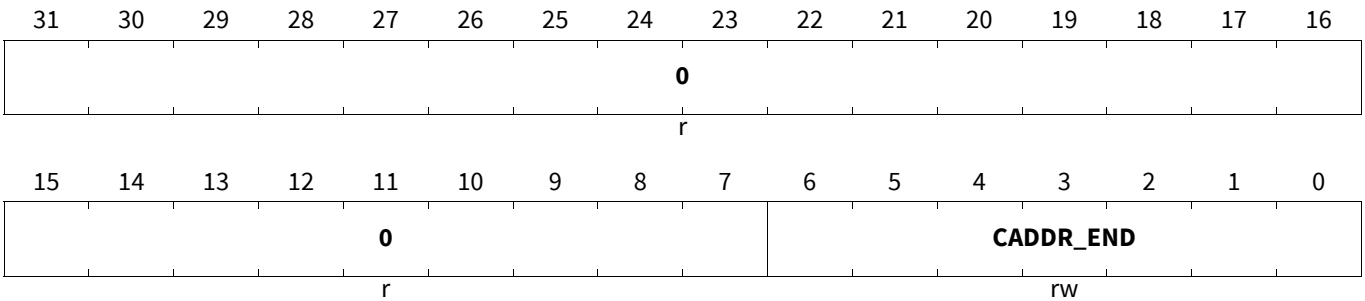


Field	Bits	Type	Description
IRQ_MODE	1:0	rw	**IRQ mode selection** The interrupt modes are described in **Section 28.4.5**. 00_B Level mode 01_B Pulse mode 10_B Pulse-Notify mode 11_B Single-Pulse mode
0	31:2	r	**Reserved** Read as zero, shall be written as zero.

28.5.7.14 Register ARU_CADDR_END

ARU caddr Counter End Value Register

ARU_CADDR_END
ARU caddr Counter End Value Register **(0002B4$_H$)** **Application Reset Value: 0000 007F$_H$**



Field	Bits	Type	Description
CADDR_END	6:0	rw	**Set end value of ARU caddr counter** The ARU roundtrip counter aru_caddr runs from zero to caddr_end value. Shorten the ARU roundtrip cycle by setting a smaller number than the defined reset value will cause that not all ARU-connected modules will be served. Making the roundtrip cycle longer than the reset value would cause longer ARU roundtrip time and as a result some ARU-connected modules will not be served as fast as possible for this device. This bit is write protected by bit RF_PROT of register GTM_CTRL
0	31:7	r	**Reserved** Read as zero, shall be written as zero.

28.5.7.15 Register ARU_CADDR

ARU caddr Counter Value

Note: The registers CADDR_0 and CADDR_1 start incrementing with each clock cycle just after reset. Due to this the initial reset value cannot be read back.

ARU_CADDR

ARU caddr Counter Value **(0002FC$_H$)** **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0									**CADDR_1**						
r									r						

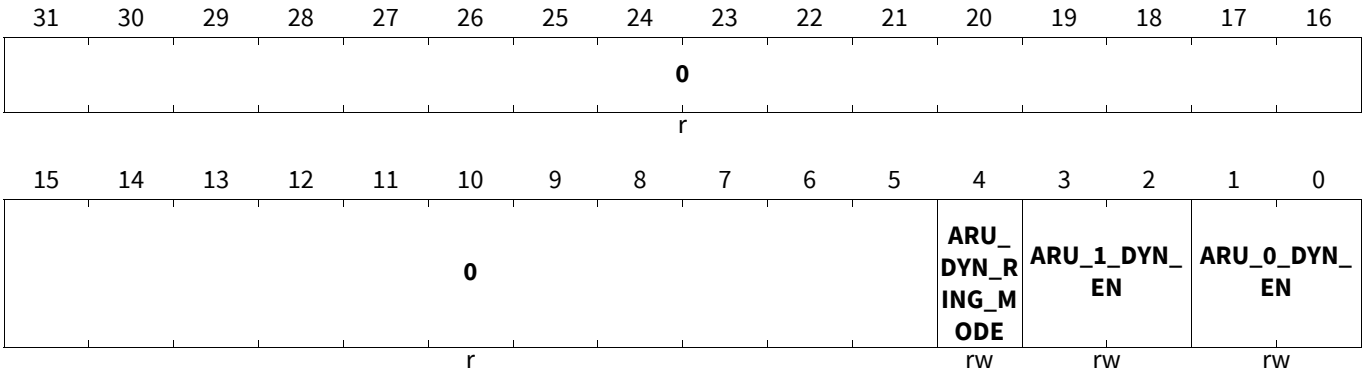
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0									**CADDR_0**						
r									r						

Field	Bits	Type	Description
CADDR_0	6:0	r	**Value of ARU-0 caddr counter**
CADDR_1	22:16	r	**Value of ARU-1 caddr counter**
0	15:7, 31:23	r	**Reserved** Read as zero, shall be written as zero.

28.5.7.16 Register ARU_CTRL

ARU Enable Dynamic Routing Register

ARU_CTRL
ARU Enable Dynamic Routing Register (0002BC$_H$) Application Reset Value: 0000 0000$_H$

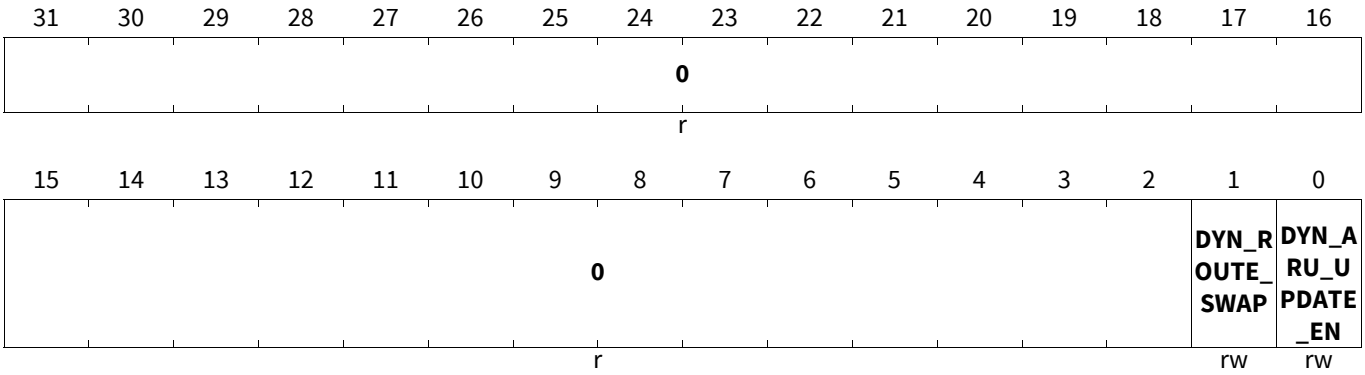


Field	Bits	Type	Description
ARU_0_DYN_EN	1:0	rw	**Enable dynamic routing for ARU-0** Dynamic routing enable of ARU-0. Write of following double bit values is possible: If dynamic routing is disabled, the normal ARU routing scheme for ARU-0 is executed. 00_B no change 01_B Disable dynamic routing 10_B Enable dynamic routing 11_B no change
ARU_1_DYN_EN	3:2	rw	**Enable dynamic routing for ARU-1** Dynamic routing enable of ARU-1. Write of following double bit values is possible: If dynamic routing is disabled, the normal ARU routing scheme for ARU-1 is executed. 00_B no change 01_B Disable dynamic routing 10_B Enable dynamic routing 11_B no change
ARU_DYN_RING_MODE	4	rw	**Enable dynamic routing ring mode** Dynamic routing ring mode for both ARU-0 and ARU-1. 0_B Different dynamic routing scheme for ARU-0 and ARU-11 1_B Same dynamic routing scheme for ARU-0 and ARU-1 with 24 possible read-ID's (dynamic routing ring mode)
0	31:5	r	**Reserved** Read as zero, shall be written as zero.

28.5.7.17 Register ARU_[z]_DYN_CTRL

ARU z Dynamic Routing Control Register

ARU_z_DYN_CTRL (z=0-1)
ARU z Dynamic Routing Control Register (0002C0$_H$+z*4) Application Reset Value: 0000 0000$_H$

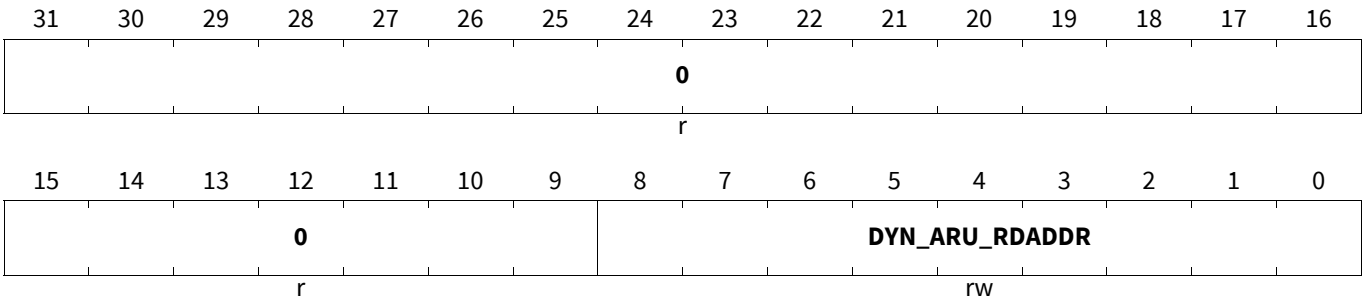


Field	Bits	Type	Description
DYN_ARU_UPDATE_EN	0	rw	**Enable reload of DYN_ROUTE register from ARU itself** Enable reload of DYN_ROUTE register from ARU itself.
DYN_ROUTE_SWAP	1	rw	**Enable swapping DYN_ROUTE_SR with DYN_ROUTE register** Enable swapping **DYN_ROUTE_SR** with **DYN_ROUTE** register.
0	31:2	r	**Reserved** Read as zero, shall be written as zero.

28.5.7.18 Register ARU_[z]_DYN_RDADDR

ARU z Read ID for Dynamic Routing

ARU_z_DYN_RDADDR (z=0-1)
ARU z Read ID for Dynamic Routing (0002E8$_H$+z*4) Application Reset Value: 0000 0000$_H$



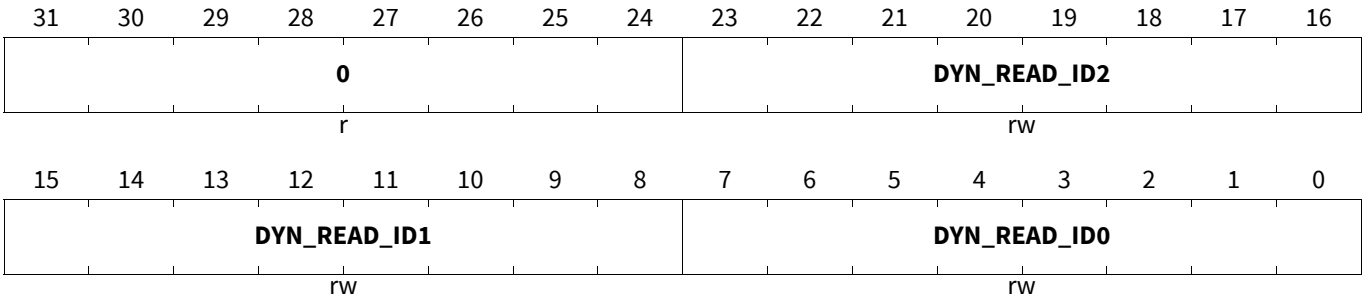
Field	Bits	Type	Description
DYN_ARU_RDADDR	8:0	rw	**ARU read address ID to reload the DYN_ROUTE register** ARU read address ID to reload the DYN_ROUTE register from ARU itself.
0	31:9	r	**Reserved** Read as zero, shall be written as zero.

28.5.7.19 Register ARU_[z]_DYN_ROUTE_LOW

ARU z Lower Bits of DYN_ROUTE Register

ARU_z_DYN_ROUTE_LOW (z=0-1)

ARU z Lower Bits of DYN_ROUTE Register (0002C8$_H$+z*4) Application Reset Value: 0000 0000$_H$



Field	Bits	Type	Description
DYN_READ_ID0	7:0	rw	**ARU read ID 0** ARU read ID 0 for dynamic routing.
DYN_READ_ID1	15:8	rw	**ARU read ID 2** ARU read ID 1 for dynamic routing.
DYN_READ_ID2	23:16	rw	**ARU read ID 2** ARU read ID 2 for dynamic routing.
0	31:24	r	**Reserved** Read as zero, shall be written as zero

28.5.7.20 Register ARU_[z]_DYN_ROUTE_HIGH

ARU z Higher Bits of DYN_ROUTE Register

ARU_z_DYN_ROUTE_HIGH (z=0-1)

ARU z Higher Bits of DYN_ROUTE Register (0002D0$_H$+z*4) Application Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0				DYN_CLK_WAIT				DYN_READ_ID5							
r				rw				rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DYN_READ_ID4								DYN_READ_ID3							
rw								rw							

Field	Bits	Type	Description
DYN_READ_ID3	7:0	rw	**ARU read ID 3** ARU read ID 3 for dynamic routing.
DYN_READ_ID4	15:8	rw	**ARU read ID 4** ARU read ID 4 for dynamic routing.
DYN_READ_ID5	23:16	rw	**ARU read ID 5** ARU read ID 5 for dynamic routing.
DYN_CLK_WAIT	27:24	rw	**Number of clk cycles for dynamic routing** Defines the number of clk cycles between each dynamic routing ID.
0	31:28	r	**Reserved** Read as zero, shall be written as zero.

28.5.7.21 Register ARU_[z]_DYN_ROUTE_SR_LOW

ARU z Shadow Register for ARU_z_DYN_ROUTE_LOW

NOTE : This is the shadow register for register **ARU_[z]_DYN_ROUTE_LOW**

ARU_z_DYN_ROUTE_SR_LOW (z=0-1)

ARU z Shadow Register for ARU_z_DYN_ROUTE_LOW(0002D8$_H$+z*4) Application Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								DYN_READ_ID8							
r								rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DYN_READ_ID7								DYN_READ_ID6							
rw								rw							

Field	Bits	Type	Description
DYN_READ_ID6	7:0	rw	**ARU read ID 6** ARU read ID 6 for dynamic routing. These bits are mapped to ARU data bits aru_data(7:0).
DYN_READ_ID7	15:8	rw	**ARU read ID 7** ARU read ID 7 for dynamic routing. These bits are mapped to ARU data bits aru_data(15:8).
DYN_READ_ID8	23:16	rw	**ARU read ID 8** ARU read ID 8 for dynamic routing. These bits are mapped to ARU data bits aru_data(23:16).
0	31:24	r	**Reserved** Read as zero, shall be written as zero.

28.5.7.22 Register ARU_[z]_DYN_ROUTE_SR_HIGH

ARU z Shadow Register for ARU_z_DYN_ROUTE_HIGH

NOTE : This is the shadow register for register **ARU_[z]_DYN_ROUTE_HIGH**

ARU_z_DYN_ROUTE_SR_HIGH (z=0-1)

ARU z Shadow Register for ARU_z_DYN_ROUTE_HIGH(0002E0$_H$+z*4) Application Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0			DYN_UPDATE_EN	DYN_CLK_WAIT				DYN_READ_ID11							
r			rw	rw				rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DYN_READ_ID10								DYN_READ_ID9							
rw								rw							

Field	Bits	Type	Description
DYN_READ_ID9	7:0	rw	**ARU read ID 9** ARU read ID 9 for dynamic routing. These bits are mapped to ARU data bits aru_data(31:24).
DYN_READ_ID10	15:8	rw	**ARU read ID 10** ARU read ID 10 for dynamic routing. These bits are mapped to ARU data bits aru_data(39:32).
DYN_READ_ID11	23:16	rw	**ARU read ID 11** ARU read ID 11 for dynamic routing. These bits are mapped to ARU data bits aru_data(47:40).
DYN_CLK_WAIT	27:24	rw	**Number of clk cycles for dynamic routing** Defines the number of clk cycles between each dynamic routing ID. These bits are mapped to ARU data bits aru_data(51:48).

Field	Bits	Type	Description
DYN_UPDATE_EN	28	rw	**Update enable from shadow register** Enable update **ARU_[z]_DYN_ROUTE_LOW/_HIGH** registers from shadow registers **ARU_[z]_DYN_ROUTE_SR_LOW/_HIGH**. This bit is mapped to ARU data bit aru_data(52).
0	31:29	r	**Reserved** Read as zero, shall be written as zero.