27.3.2 Compare Match Interrupt Control

The compare match interrupt control logic is shown in **Figure 3**. Each CMPx register has its compare match interrupt request flag (ICR.CMPxIR) that is set by hardware on a compare match event. The interrupt request flags can be set (ISCR.CMPxIRS) or cleared (ISCR.CMPxIRR) by software. Note that setting ICR.CMPxIR by writing a 1 into ISSR.CMPxIRS does not generate an interrupt at STMIRx. The compare match interrupts from CMP0 and CMP1 can be further directed by ICR.CMPxOS to either output signal STMIR0 or STMIR1.

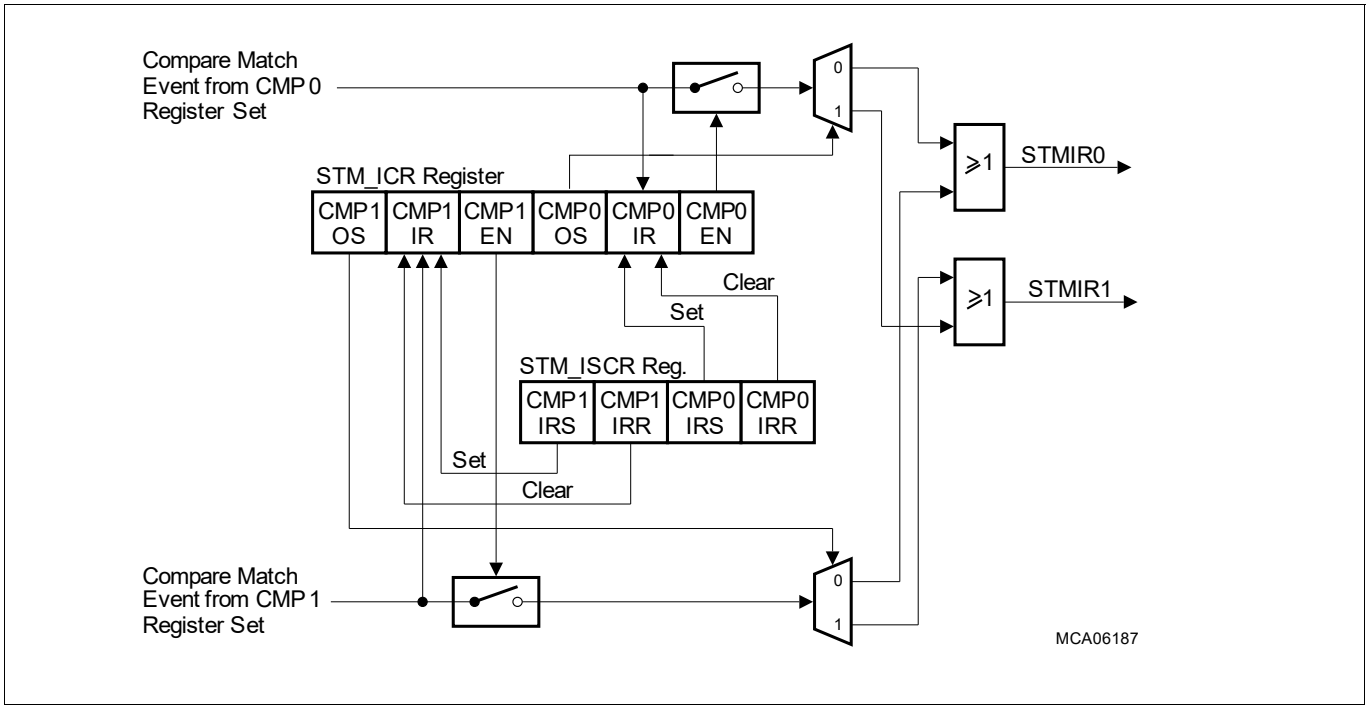

Figure 3 STM Interrupt Control

The compare match interrupt flags ICR.CMPxIR are immediately set after an STM reset operation, caused by a compare match event with the reset values of the STM and the compare registers CMPx. This does not directly generate compare match interrupts because the compare match interrupts are automatically disabled after an STM reset operation (ICR.CMPxEN = 0). Therefore, before enabling a compare match interrupt after an STM Application Reset, the software should configure the STM and modify the reset values of the compare registers. Otherwise, undesired compare match interrupt events are triggered. The CMPxIR flags which are set after an STM reset can be cleared by writing register ISCR with CMPxIRR set.

27.3.3 Using Multiple STMs

For systems that include multiple CPUs there are also multiple STMs available. Each STM is aimed to serve as time base for one individual CPU operating system main scheduler clock trigger. This is done by the usage of one compare register and the associated interrupt generating the trigger.

All STM modules are connected and controlled by f_{STM} and can therefore operate on the same frequency if desired.

27.3.4 STM as Reset Trigger

A compare match triggered by an CMP0 event can generate a reset in the system. The reset has to be enabled for each STM module individually in register SCU_RSTCON.

27.4 Registers

This section describes the registers of the STM.

Table 1 Register Overview - STM (ascending Offset Address)

Short Name	Long Name	Offset Address	Access Mode		Reset	Page Number
			Read	Write		
CLC	Clock Control Register	0000_H	U,SV	SV,E,P	Application Reset	7
ID	Module Identification Register	0008_H	U,SV	BE	Application Reset	8
TIM0	Timer Register 0	0010_H	U,SV	BE	Application Reset	9
TIM1	Timer Register 1	0014_H	U,SV	BE	Application Reset	10
TIM2	Timer Register 2	0018_H	U,SV	BE	Application Reset	10
TIM3	Timer Register 3	$001C_H$	U,SV	BE	Application Reset	10
TIM4	Timer Register 4	0020_H	U,SV	BE	Application Reset	11
TIM5	Timer Register 5	0024_H	U,SV	BE	Application Reset	11
TIM6	Timer Register 6	0028_H	U,SV	BE	Application Reset	12
CAP	Timer Capture Register	$002C_H$	U,SV	BE	Application Reset	12
CMPx	Compare Register x	0030_H+x *4	U,SV	U,SV,P	Application Reset	13
CMCON	Compare Match Control Register	0038_H	U,SV	U,SV,P	Application Reset	14
ICR	Interrupt Control Register	$003C_H$	U,SV	U,SV,P	Application Reset	16
ISCR	Interrupt Set/Clear Register	0040_H	U,SV	U,SV,P	Application Reset	17
TIM0SV	Timer Register 0 Second View	0050_H	U,SV	BE	Application Reset	9
CAPSV	Timer Capture Register Second View	0054_H	U,SV	BE	Application Reset	13
OCS	OCDS Control and Status Register	$00E8_H$	U,SV	SV,P,OEN	Debug Reset	19
KRSTCLR	Kernel Reset Status Clear Register	$00EC_H$	U,SV	SV,E,P	Application Reset	22
KRST1	Kernel Reset Register 1	$00F0_H$	U,SV	SV,E,P	Application Reset	21