28.10.2 Global Clock Divider

The sub block Global Clock Divider can be used to divide the CMU primary source signal CLS0_CLK into a common subdivided clock signal.

The divided clock signal of the sub block Global Clock Divider is implemented as an enable signal that enables dedicated clocks from the *CLS0_CLK* signal to generate the user specified divided clock frequency.

The resulting fractional divider (Z/N) specified through equation:

$$T_{CMU\_GCLK\_EN}=(Z/N)*T_{CLS0\_CLK}$$

is implemented according the following algorithm

(*Z*: *CMU_GCLK_NUM(23:0)*; *N*: *CMU_GCLK_DEN(23:0)*; *Z,N* >0)

(1) Set remainder (*R*), operand1 (*OP1*) and operand2 (*OP2*) register during INIT-phase (with implicit conversion to signed):

R=Z, OP1=N, OP2=N-Z;

(2) After leaving INIT-phase (at least one *CMU_CLK[x]* has been enabled) the sign of remainder R for each CLS0_*CLK* cycle will be checked:

(3) If *R>0* keep updating remainder and keep *CMU_GCLK_EN='0'*:

R=R-OP1;

(4) If *R<0* update remainder and set *CMU_GCLK_EN='1'*:

R=R-OP2

After at most (*Z/N*+1) subtractions (3) there will be a negative *R* and an active phase of the generated clock enable (for one cycle) will be triggered (4). The remainder *R* is a measure for the distance to a real *Z/N* clock and will be regarded for the next generated clock enable cycle phase. The new *R* value will be *R=R+(Z-N)*. In the worst case the remainder *R* will sum up to an additional cycle in the generated clock enable period after *Z*-cycles. In the other cases equally distributed additional cycles will be inserted for the generated clock enable. If *Z* is an integer multiple of *N* no additional cycles will be included for the generated clock enable at all.

Note that for a better resource sharing all arithmetic has been reduced to subtractions and the initialization of the remainder *R* uses the complement of (*Z-N*).

28.10.3 Configurable Clock Generation sub-unit (CFGU)

The CMU sub-unit CFGU provides up to eight configurable clock divider blocks that divide the common C*MU_GCLK_EN* signal into dedicated enable signals for the GTM sub blocks.

The configuration of the eight different clock signals *CMU_CLK[x]* (x: 0…7) always depends on the configuration of the global clock enable signal *CMU_GCLK_EN*. Additionally, each clock source has its own configuration data, provided by the control register **CMU_CLK_[x]_CTRL (x=0..7)**.

According to the configuration of the Global Clock Divider, the configuration of the Clock Source x Divider is done by setting an appropriate value in the bit field **CLK_CNT[x]** of the register **CMU_CLK_[x]_CTRL**.

The frequency *fx = 1/Tx* of the corresponding clock enable signal *CMU_CLK[x]* can be determined by the unsigned representation of **CLK_CNT[x]** of the register **CMU_CLK_[x]_CTRL** in the following way:

$$T_{CMU\_CLK}[x]=(CLK\_CNT[x]+1)*T_{CMU\_GCLK\_EN}$$

The corresponding wave form is shown in **Figure 28**.

Each clock signal *CMU_CLK[x]* can be enabled individually by setting the appropriate bit field **EN_CLK[x]** in the register **CMU_CLK_EN**. Except for *CMU_CLK6* and *CMU_CLK7* individual enabling and disabling is active only if **CLK_SEL** is reset.