33.8 Conversion Result Handling

The EDSADC preprocesses the conversions result data before storing them for retrieval by the CPU or a DMA channel.

Conversion result handling comprises the following functions:

- **Filtering and Post-Processing**
- **Storage of Conversion Results** to FIFO and result register
- **Result Service Request Generation and Read Sequencing**
- **Hardware Data Interface** provides result values to other modules

33.8.1 Filtering and Post-Processing

The result data words are generated by feeding the input data stream through a chain of filter elements and decimating it by a selectable ratio. The selectable integrator can further reduce the output data rate while executing accumulation and averaging.

Several elements of the filter chain can be bypassed, i.e. the filter chain is configurable and its behavior can be adapted to the requirements of the actual application.

The result values are multiplied by a factor that serves for gain calibration and data format normation. An offset can be subtracted automatically from each result value before being fed to the integrator or being written to the result register.

For differential mode applications, the offset can alternatively be removed automatically by the high-pass filter.

Due to the differential input stage, the results are signed values. Usually, these results are stored in a 16-bit two's-complement format. For the specific quasi-differential operating modes (single-ended input using common mode voltage) the results can be stored as 16-bit unsigned integer values (see **DICFGx (x=0-13)**).

The CIC filter's output value depends on the selected filter parameters and decimation factor. A data shifter extracts the most significant bits from this filter result. A multiplier adjusts the magnitude of the result values to the result range required by the application.

33.8.2 Storage of Conversion Results

The conversion result values are stored in a FIFO-structure which is accessible via the result register RESMx.

This enables the following features:

- Buffering increases the allowable latency for retrieving result values
- Two result values can be retrieved by one single read access
- Two subsequent read accesses enable the efficient transfer of up to 4 result values[1)]
- The previous result value is still available to calculate interpolation values for timestamp operation

Also timestamp information can be accessed through the result register (either directly or via the FIFO). This enables access to all relevant data using a single DMA channel.

To optimize access to result values, the result register can be read in several modes:

Table 290 Result Register Read Modes

Read Mode[1)]	RESMx[31:16] (high)	RESMx[15:0] (low)	Notes
Single-word read mode, sign-extended ($DRM = 00_B$) (SSSS'RRRR)	Extended sign value (only valid for result values)	Next result value (from FIFO stage 1)	TSM = 0, 16-bit read access[2)] ($SRLVL = 00_B, 01_B, 10_B, 11_B$)
		Timestamp[3)], then initial result value, then next result value (from FIFO stage 1)	TSM = 1, gate-controlled timestamp mode, 16-bit read access[2)] ($SRLVL = 10_B, 11_B$)
Single-word read mode ($DRM = 01_B$) (0000'RRRR, TTTT'RRRR)	0000_H	Recent result value (FIFO not used, overwrite RESULTLO)	TSM = 0, 16-bit read access
	Timestamp	Recent result value (FIFO not used, overwrite RESULTLO)	TSM = 1, 32-bit read access
Double-word read mode ($DRM = 10_B$) (NNNN'RRRR)	Subsequent res. value (from FIFO stage 2)	Next result value (from FIFO stage 1)	TSM = 0 32-bit read access[4)], (low bus load) ($SRLVL = 01_B, 11_B$)
	Initial result value, then subsequent value (from FIFO stage 2)	Timestamp[3)], then next result value (from FIFO stage 1)	TSM = 1, gate-controlled timestamp mode, 32-bit read access[4)] ($SRLVL = 11_B$)

1) Selected by bitfields DRM and TSM in register **DICFGx (x=0-13)**.
2) Due to the sign extension, result values can also be read as signed 32-bit values.
3) The timestamp is inserted once when the selected gate opens. The FIFO is flushed when the selected gate closes.
4) In double-word read mode, a service request shall only be generated when the result double buffer holds 2 values.

FIFO Control

Result values are only written to the FIFO ($DRM = X0_B$) while service requests are enabled. This enables the application e.g. to read stored values after the service request gate has closed.The FIFO is flushed when the service request gate opens, so it provides an actual set of result values.

In gate-controlled timestamp mode, the FIFO is flushed when the gate closes, so it can store the current result value in stage 2.

1) Also refer to **"Result Service Request Generation and Read Sequencing" on Page 76**.

Result Handling Without FIFO

In a special single-word read mode (DRM = 01_B) the result values are stored in RESMx directly.

The low word returns the latest result value, the high word either is cleared or returns the current timestamp counter value.

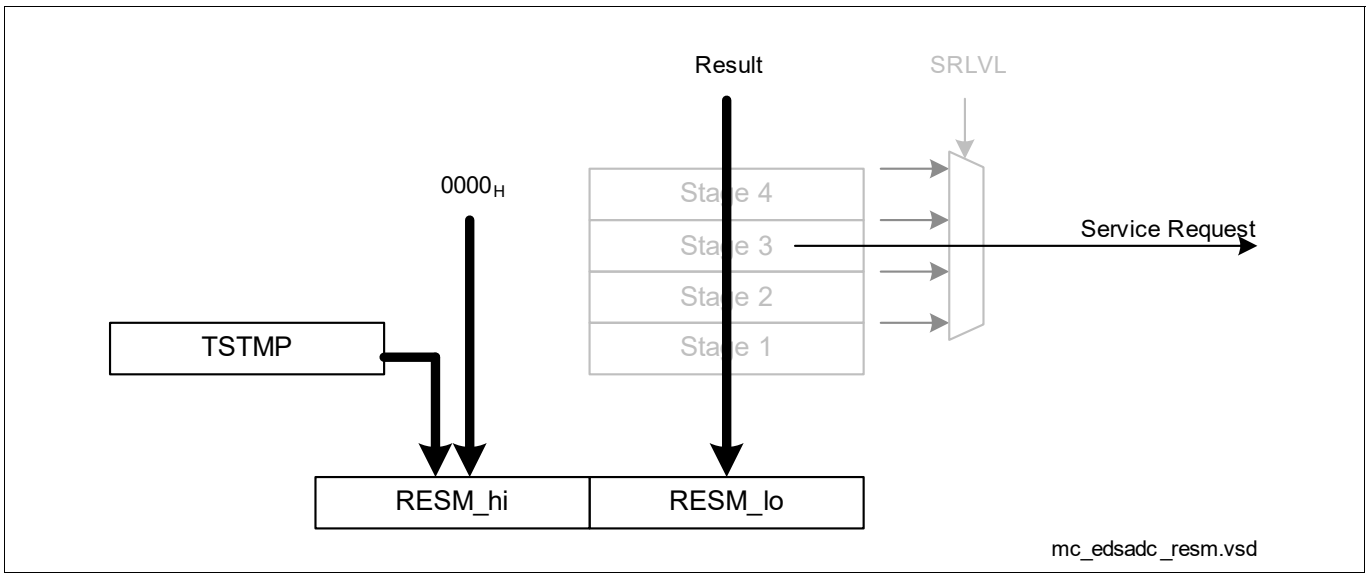

Figure 312 Direct Result Storage

Result Handling Via FIFO

The result values are not directly written to RESMx but are stored in a FIFO structure. From there they are retrieved when RESMx is read. In timestamp mode, the FIFO is transparent while the gate signal is inactive, i.e. all input values are directly forwarded to stage 2 of the FIFO. When the gate opens (this is the trigger event) a timestamp is generated and inserted to stage 1 of the FIFO. Subsequent input values are then piled into the FIFO.

A service request is generated when a certain number of values has been stored in the FIFO. The respective FIFO fill level is selected in bitfield SRLVL.

FIFO control and status bitfields are available in register **RFCx (x=0-13)**.

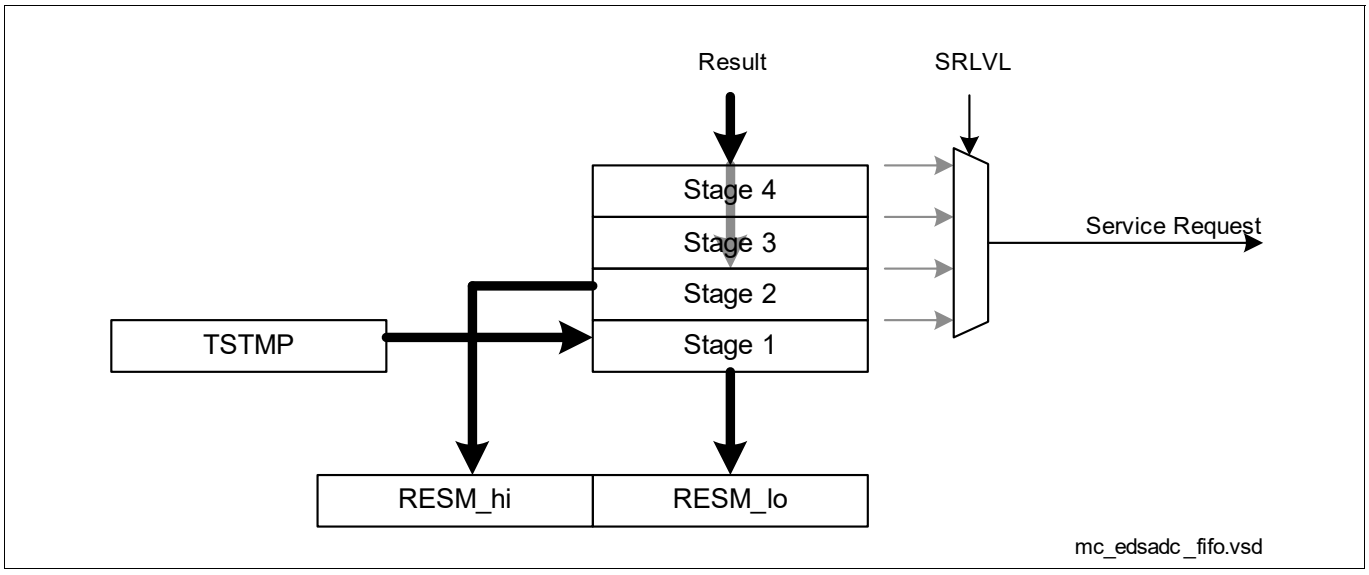

Figure 313 Result FIFO Structure

Result FIFO Control Register x

RFCx (x=0-13)

Result FIFO Control Register x **($012C_H$+x*100_H)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0										WRERR	RDERR	0	FILL		
r										rh	rh	r	rh		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0									FIFL	WREC	RDEC	0		SRLVL	
r									w	w	w	r		rw	

Field	Bits	Type	Description
SRLVL	1:0	rw	**Service Request FIFO Level** 00_B Generate service request when FIFO fill level reaches 1 value 01_B Generate service request when FIFO fill level reaches 2 values 10_B Generate service request when FIFO fill level reaches 3 values 11_B Generate service request when FIFO fill level reaches 4 values
RDEC	4	w	**Read Error Flag Clear** 0_B No action 1_B Clear flag RDERR
WREC	5	w	**Write Error Flag Clear** 0_B No action 1_B Clear flag WRERR
FIFL	6	w	**FIFO Flush** 0_B No action 1_B Remove all entries from result FIFO
FILL	18:16	rh	**FIFO Fill Level** Not listed combinations are reserved. 000_B Result FIFO is empty 001_B Result FIFO contains 1 valid value 010_B Result FIFO contains 2 valid values 011_B Result FIFO contains 3 valid values 100_B Result FIFO contains 4 valid values
RDERR	20	rh	**Read Error Flag** 0_B No problem encountered 1_B A read access occurred while the FIFO was empty A read error is also indicated when a read access occurs during the FIFO's synchronization stall phase (4 clock cycles after a read access). Clear this sticky flag by writing 1 to bit RDEC.
WRERR	21	rh	**Write Error Flag** 0_B No problem encountered 1_B A write access occurred while the FIFO was full Clear this sticky flag by writing 1 to bit WREC.

Field	Bits	Type	Description
0	3:2, 15:7, 19, 31:22	r	**Reserved, write 0, read as 0**

Result Register x Main

RESMx (x=0-13)

Result Register x Main **(0130_H+x*100_H)** **Application Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RESULTHI															
rh															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESULTLO															
rh															

Field	Bits	Type	Description
RESULTLO	15:0	rh	**Result Value Lower Part** Returns the next value from the result FIFO (Result or timestamp, see **Table 290**)
RESULTHI	31:16	rh	**Result Value Higher Part** Returns an additional value (Sign extension, result from FIFO, timestamp, or zero, see **Table 290**)

33.8.3 Result Service Request Generation and Read Sequencing

The generated result values (including timestamp values, if enabled) are retrieved in a defined sequence. This sequence depends on the selected result register read mode, the availability of result/timestamp values, and the system's response to service requests.

Result events are generated for each available result value. Result service requests are generated depending on the configured read mode and the FIFO fill level. Each data transfer (result data values or timestamp information) is initiated by a service request. This service request is issued when a defined number of values becomes available.

Figure 314 shows different situations for standard data transfers:

- Single Read:
  The service request is generated when one result value is available
  and is serviced by 16-bit read access (D0, D1)
- Double Read:
  The service request is generated when two result values are available
  and is serviced by 32-bit read access (D3/D2, D5/D4)
- Single Transfer Mode:
  The service request is answered with a single transfer.
  This transfer either transfers 16 or 32 bits.
- Double Transfer Mode:
  The service request is answered with two subsequent transfers[1].
  These transfers either transfer 16 or 32 bits.

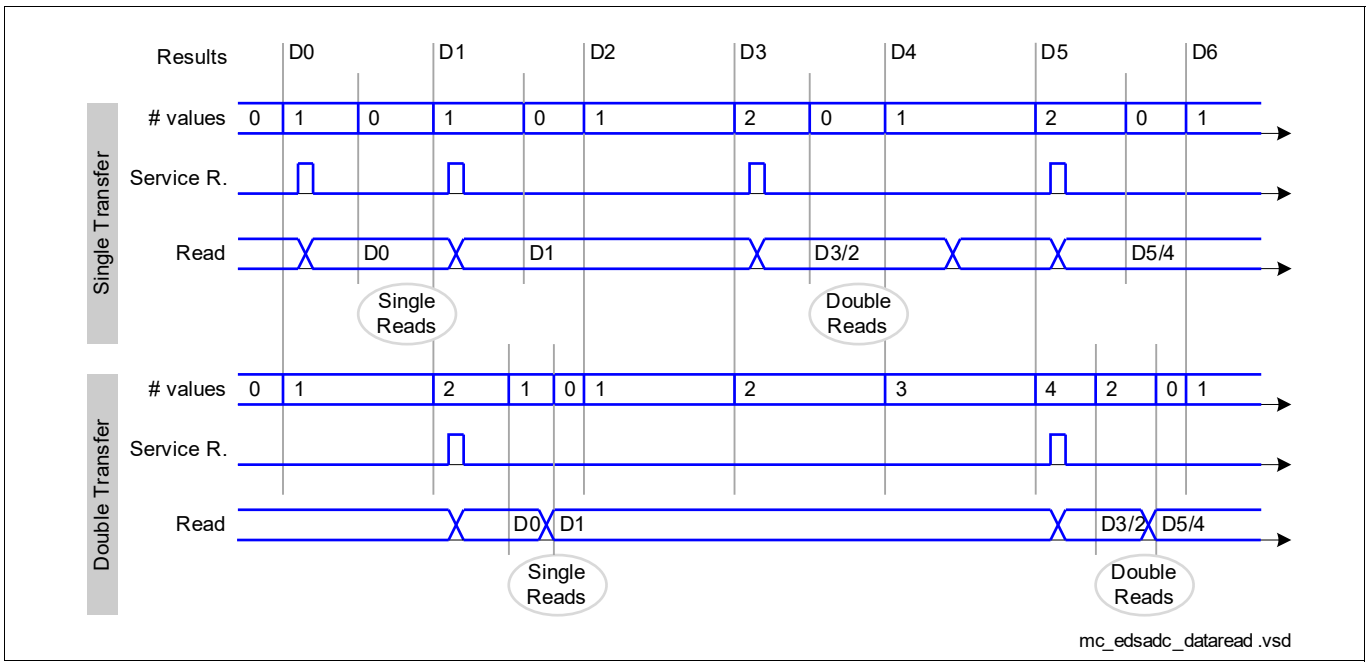

Figure 314 Standard Read Sequences

1) Synchronizing the result values between the two clock domains and controlling the result FIFO takes up to 8 cycles of f_{SPB}. Read accesses, therefore, must have at least 8 cycles of f_{SPB} in between them.

Timestamp mode supports applications using service request gating. A timestamp is generated when the gate opens (defined timestamp trigger). When the configured number of values (including the timestamp) is available, a service request is generated.

Figure 315 shows different situations for timestamp usage:

- Single Read:
  A timestamp trigger is generated when the service request gate opens. Read accesses return the timestamp value, the result before the timestamp (D0), and then subsequent result values. Note that D1 may be generated shortly after the timestamp event.
- Double Read:
  A timestamp trigger is generated when the service request gate opens. Read accesses return the result before the timestamp (D0) and the timestamp value, and then subsequent result value pairs. Accumulating 4 values and transferring them with two subsequent transfers provides the most efficient way to store data.

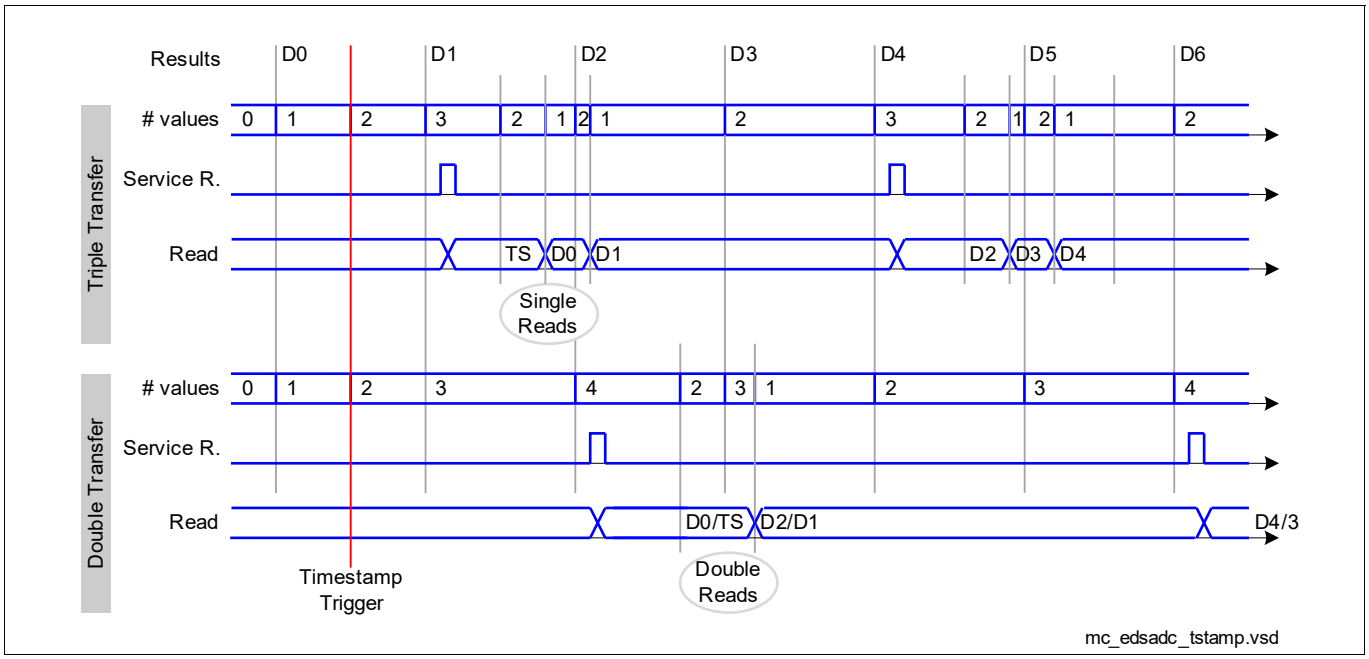

Figure 315 Read Sequences With Timestamp

Note: When setting up the service request level and e.g. DMA functionality, note that timestamp value and subsequent data value (D1) may be generated within a short timeframe, i.e. there are then 3 values in the FIFO.

33.8.4 Hardware Data Interface

The digital conversion results are directly available to other modules via the hardware data interface (HDI). Each value that is written to the result FIFO structure is also output to this interface. Each time a result event is generated, the HDI updates the data vector and generates a write strobe indicating the availability of a new result value.

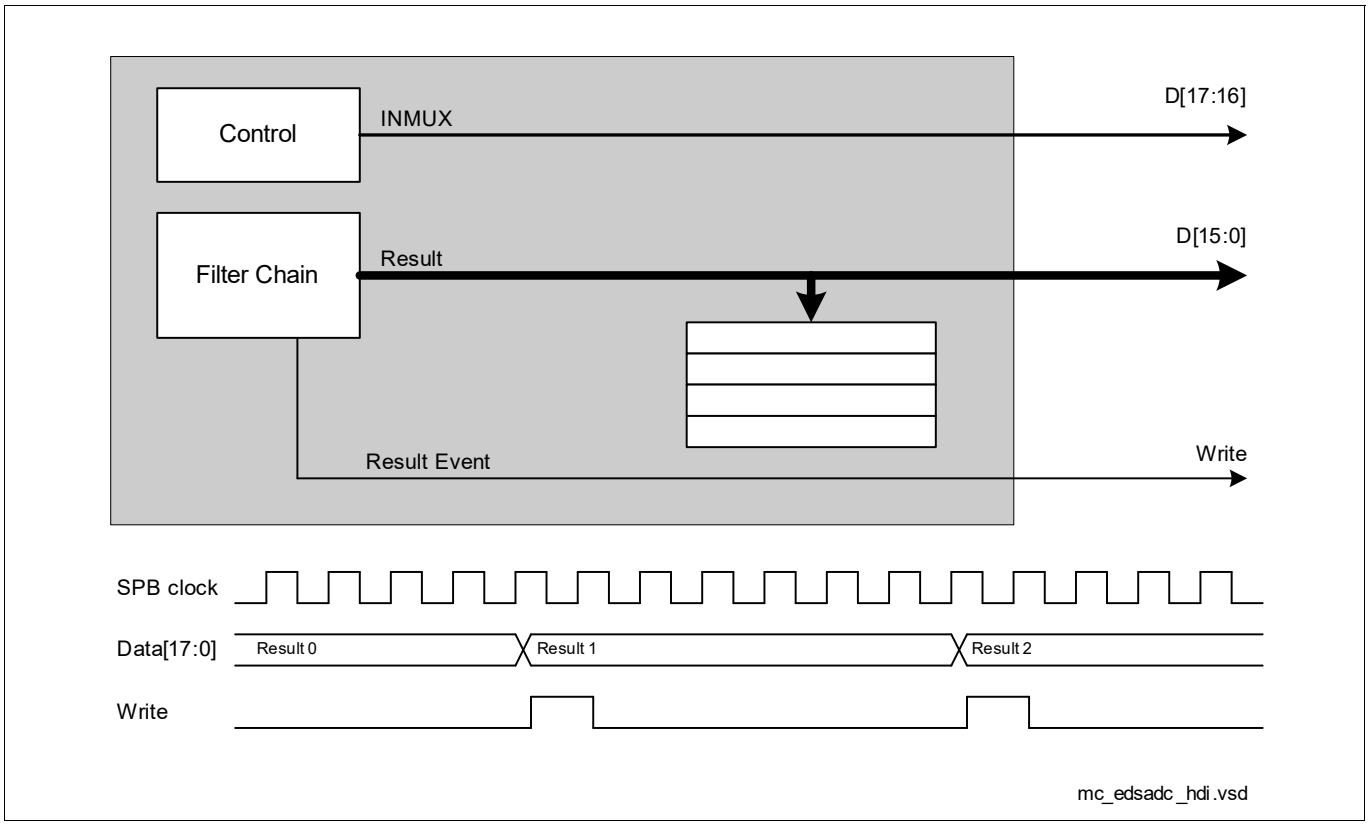

Figure 316 Hardware Data Interface

This interface writes results to the GTM to make them available for the MCSs equipped with an analog data interface (ADI).

The following data elements are available through the HDI:

Table 291 HDI Data Assignment

Bit Position	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data Content							MUX		Conversion Result															

Note: The availability of the MUX indicator bits depends on the respective channel. Unused bits are 0.