Alternatively, clock source six and seven (*CMU_CLK6* and *CMU_CLK7*) may provide the signal *SUB_INC1* and *SUB_INC2* coming from module DPLL as clock enable signal depending on the bit field **CLK_SEL(1:0)** of the register **CMU_CLK_6_CTRL** and on the bit field **CLK_SEL(1:0)** of the register **CMU_CLK_7_CTRL**.

CMU_CLK8 is switched by **CLK8_EXT_DIVIDER** of the register **CMU_CLK_CTRL** between *CLS0_CLK* and *CMU_ECLK0*.

To switch the clock reference CMU_GCLK_EN with *CMU_ECLK1*_EN an input selector are used in all Clock Source Divider. The *CMU_ECLK1*_EN source is enabled by setting the appropriate bit field **CMU[x]_EXT_DIVIDER** in the register **CMU_CLK_CTRL**.

To avoid unexpected behavior of the hardware, the configuration of register **CMU_CLK_[x]_CTRL** and **CMU_CLK_CTRL** can only be changed, when the corresponding clock signal *CMU_CLK[x]* and *CMU_ECLK[1]* is disabled.

Further, any changes to the registers **CMU_GCLK_NUM** and **CMU_GCLK_DEN** can only be performed, when all clock enable signals *CMU_CLK[x]* and the **EN_FXCLK** bit inside the **CMU_CLK_EN** register are disabled.

The clock source signals *CMU_CLK[x]* (x: 0…7) and *CMU_FXCLK[y]* are implemented in form of enable signals for the corresponding registers, which means that the actual clock signal of all registers always use the *CLS0_CLK* signal.

The hardware guarantees that all clock signals *CMU_CLK[x]* (x: 0…7), which were enabled simultaneous, are synchronized to each other. Simultaneous enabling does mean that the bits **EN_CLK[x]** in the register **CMU_CLK_EN** are set by the same write access.

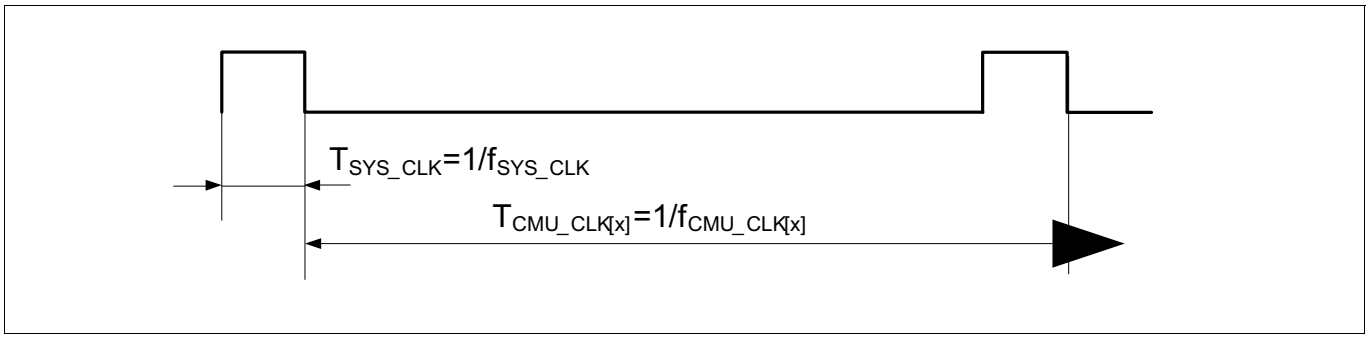

Figure 28 Wave Form of Generated Clock Signal CMU_CLK[x]

28.10.4 Fixed Clock Generation (FXU)

The FXU sub-unit generates fixed clock enables out of the *CMU_GCLK_EN* or one of the eight *CMU_CLK[x]* enable signal depending on the **FXCLK_SEL** bit field of the **CMU_FXCLK_CTRL** register. These clock enables are used for the PWM generation inside the TOM modules.

All clock enables *CMU_FXCLK[y]* can be enabled or disabled simultaneous by setting the appropriate bit field **EN_FXCLK** in the register **CMU_CLK_EN**.

The dividing factors are defined as 2^0, 2^4, 2^8, 2^{12}, and 2^{16}. The signals *CMU_FXCLK[y]* are implemented in form of enable signals for the corresponding registers (see also **Figure 28**)

28.10.5 External Generation Unit (EGU)

The EGU sub-unit generate up to three separate clock output signals *CMU_ECLK[z]* (z: 0…2).

Each of these clock signals is derived from the corresponding External Clock Divider z sub block, which generates a clock signal derived from the GTM input clock *CLS0_CLK*.

In contrast to the signals *CMU_CLK[x]* and *CMU_FXCLK[y]*, which are treated as simple enable signals for the registers, the signals *CMU_ECLK[z]* have a duty cycle of about 50% that is used as a true clock signal for external peripheral components.