28.12 Time Base Unit (TBU)

28.12.1 Overview

The Time Base Unit TBU provides common time bases for the GTM. The TBU sub-module is organized in channels, where the number of channels is device dependent. There are up to four channels implemented inside the TBU. The time base register **TBU_CH0_BASE** of TBU channel 0 is 27 bits wide and it is configurable whether the lower 24 bit or the upper 24 bit are provided to the GTM as signal *TBU_TS0*. The two TBU channels 1 and 2 have a time base register **TBU_CH[y]_BASE** (y: 1, 2) of 24 bit length. The time base register value *TBU_TS[y]* is provided to subsequent sub-modules of the GTM.

The time base register of TBU channel 3 **TBU_CH3_BASE** is 24 bit wide. It used as a modulo counter by **TBU_CH3_BASE_MARK** to get a relative angle clock to **TBU_CH[y]_BASE**. The absolute angle clock value for the current **TBU_CH3_BASE** is captured in **TBU_CH3_BASE_CAPTURE**.

TBU_CH[y]_BASE = TBU_CH3_BASE_CAPTURE + **... + TBU_CH3_BASE*TBU_CH3_BASE_MARK**

DIRy: direction value for time base y (y:1…2)

0 up counter

1 down counter

Note: The right-hand sum is limited to 24 bit.

The *TBU_UP[y]* (y: 1…2) signals are set to high for a single SYS_CLK period, whenever the corresponding signal *TBU_TS[y]* (y: 1…2) is getting updated. The signal *TBU_UP0_L* is set to high for a single SYS_CLK period if the signal TBU_TS0 and TBU_TS0x is getting updated and *TBU_UP0_H* is set to high for a single SYS_CLK period, whenever the upper 24 bit of TBU_TS0 are updated.

The time base channels can run independently of each other and can be enabled and disabled synchronously by control bits in a global TBU channel enable register **TBU_CHEN**. **Figure 30** shows a block diagram of the Time Base Unit.

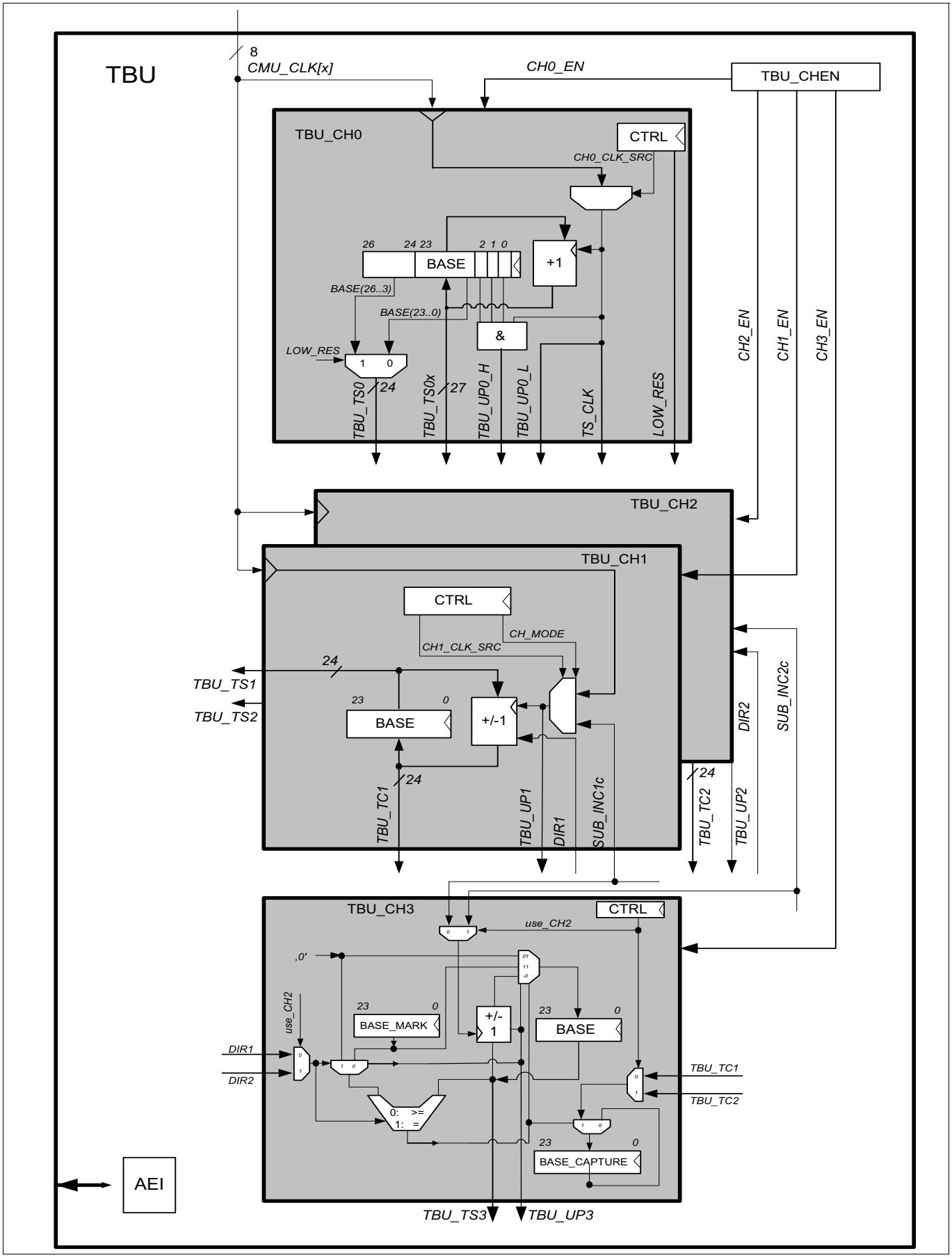


Figure 30 TBU Block Diagram

Dependent on the device a third TBU channel exists which offers the same functionality as time base channel 1.

The configuration of the independent time base channels TBU_CH[z]_BASE is done via the AEI interface. The TBU channel 0 to 2 may select one of the eight *CMU_CLK[x]* (x: 0…7) signals coming from the CMU sub-module.

For TBU channels 1 and 2 an additional clock signal *SUB_INC[y]c* (y: 1, 2) coming from the DPLL can be selected as input clock for the TBU_CH[y]_BASE. This clock in combination with the *DIR[y]* signals determines the counter direction of the TBU_CH[y]_BASE.

The selected time stamp clock signal for the TBU_CH0 sub-unit is served via the *TS_CLK* signal line to the DPLL sub-module. The *TS_CLK* signal equals the signal *TBU_UP0*.

28.12.2 TBU Channels

The time base values are generated within the TBU time base channels in two independent and one dependent operation modes.

In all modes, the time base register **TBU_CH[z]_BASE** (z: 0…3) can be initialized with a start value just before enabling the corresponding TBU channel.

Moreover, the time base register **TBU_CH[z]_BASE** (z: 0…3) can always be read in order to determine the actual value of the counter.

28.12.2.1 Independent Modes

28.12.2.1.1 Free Running Counter Mode

TBU channel 0 provides a 27 bit counter in a free running counter mode. Dependent on the bit field **LOW_RES** of register **TBU_CH0_CTRL,** the lower 24 bits (bit 0 to 23) or the upper 24 bits (bits 3 to 26) are provided to the GTM sub-modules.

TBU channel 1 and 2 provides a 24 bit counter in a free running counter mode enabled by reset CH_MODE of register **TBU_CH[y]_CTRL** (y:1…2).

In TBU Free running counter mode, the time base register **TBU_CH[v]_BASE** (v:0…2) is updated on every specified incoming clock event by the selected signal *CMU_CLK[x]* (x: 0…8) (dependent on **TBU_CH[v]_CTRL** (v:0…2) register). In general the time base register **TBU_CH[v]_BASE** is incremented on every *CMU_CLK[x]* clock tick.

28.12.2.1.2 Forward/Backward Counter Mode

TBU channel 1 and 2 provides a 24 bit forward/backward counter enabled by set CH_MODE of register **TBU_CH[y]_CTRL** (y:1…2). In this mode the *DIR[y]* signal provided by the DPLL is taken into account.

The value of the time base register **TBU_CH[y]_BASE** is incremented in case when the *DIR[y]* signal equals ‘0’ and decremented in case when the *DIR[y]* signal is ‘1’.

28.12.2.2 Dependent Mode

28.12.2.2.1 Modulo Counter Mode

TBU channel 3 provides a 24 bit forward/backward modulo counter. The clock SUB_INC[y]c and counter direction DIR[y] provided by DPLL is selected by use_CH2 of register TBU_CH3_CTRL.

The modulo value is defined in TBU_CH3_BASE_MARK. In forward counter mode if TBU_CH3_BASE value is reaching TBU_CH3_BASE_MARK TBU_CH3_BASE is reset and TBU_TS[y] is captured in TBU_CH3_BASE_CAPTURE. In backward counter mode if TBU_CH3_BASE value is reaching '0' TBU_CH3_BASE is set to TBU_CH3_BASE_MARK and TBU_TS[y] is captured in TBU_CH3_BASE_CAPTURE.

28.12.3 TBU Configuration Register Overview

Table 27 TBU Configuration Register Overview

Register Name	Description	see Page
TBU_CHEN	TBU global channel enable	135
TBU_CH0_CTRL	TBU channel 0 control	135
TBU_CH0_BASE	TBU channel 0 base	136
TBU_CH1_CTRL	TBU channel 1 control	137
TBU_CH[y]_BASE	TBU channel y base	139
TBU_CH2_CTRL	TBU channel 2 control	138
TBU_CH3_CTRL	TBU channel 3 control	140
TBU_CH3_BASE	TBU channel 3 base	140
TBU_CH3_BASE_MARK	TBU channel 3 modulo value	141
TBU_CH3_BASE_CAPTURE	TBU channel 3 base captured	141

In a typical application the Time Base Unit (TBU) considers channels 0, 1 and 3 only. In this case register addresses 0x20…0x2C are reserved and shall be read as zero. Channel 2 can be additionally implemented on special high-end application requirements.

28.12.4 TBU Register description

28.12.4.1 Register TBU_CHEN

TBU Global Channel Enable

TBU_CHEN
TBU Global Channel Enable **(000100_H)** **Application Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								ENDIS_CH3		ENDIS_CH2		ENDIS_CH1		ENDIS_CH0	
r								rw		rw		rw		rw	

Field	Bits	Type	Description
ENDIS_CHx (x=0-3)	2*x+1:2*x	rw	**TBU channel x enable/disable control** Write / Read : 00_B Don't care, bits 1:0 will not be changed / channel disabled 01_B Channel disabled: is read as 00 (see below) / -- 10_B Channel enabled: is read as 11 (see below) / -- 11_B Don't care, bits 1:0 will not be changed / channel enabled
0	31:8	r	**Reserved** Read as zero, shall be written as zero.

28.12.4.2 Register TBU_CH0_CTRL

TBU Channel 0 Control Register

TBU_CH0_CTRL
TBU Channel 0 Control Register **(000104_H)** **Application Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0												CH_CLK_SRC			LOW_RES
r												rw			rw

Field	Bits	Type	Description
LOW_RES	0	rw	**TBU_CH0_BASE register resolution** The two resolutions for the TBU channel 0 can be used in the TIM channel 0 and the DPLL sub-modules. This value can only be modified if channel 0 is disabled. 0_B TBU channel uses lower counter bits (bit 0 to 23) 1_B TBU channel uses upper counter bits (bit 3 to 26)
CH_CLK_SRC	3:1	rw	**Clock source for channel x (x:0...2) time base counter** This value can only be modified if channel 0 is disabled. 000_B CMU_CLK0 selected 001_B CMU_CLK1 selected 010_B CMU_CLK2 selected 011_B CMU_CLK3 selected 100_B CMU_CLK4 selected 101_B CMU_CLK5 selected 110_B CMU_CLK6 selected 111_B CMU_CLK7 selected
0	31:4	r	**Reserved** Read as zero, shall be written as zero.

28.12.4.3 Register TBU_CH0_BASE

TBU Channel 0 Base Register

TBU_CH0_BASE
TBU Channel 0 Base Register **(000108_H)** **Application Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0					**BASE**										
r					rw										

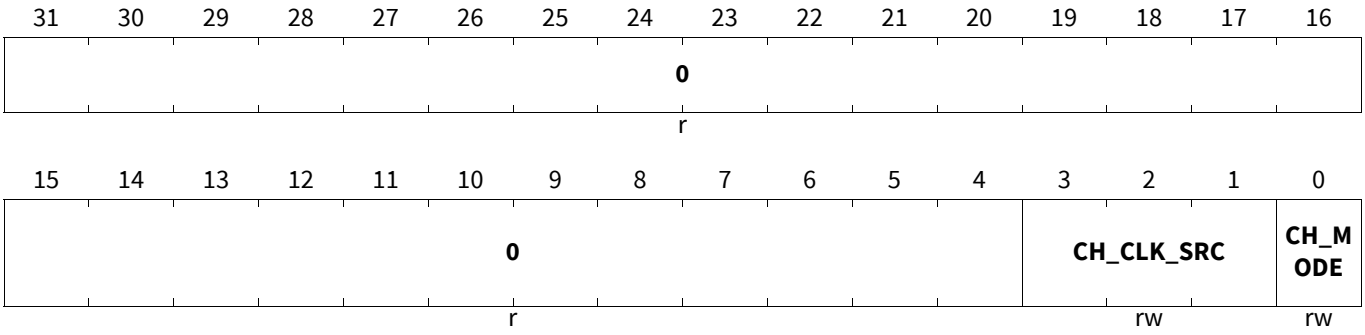
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE															
rw															

Field	Bits	Type	Description
BASE	26:0	rw	**Time base value for channel 0** The value of **BASE** can only be written if the TBU channel 0 is disabled. If channel 0 is enabled, a read access to this register provides the current value of the underlying 27 bit counter.
0	31:27	r	**Reserved** Read as zero, shall be written as zero

28.12.4.4 Register TBU_CH1_CTRL

TBU Channel 1 Control Register

TBU_CH1_CTRL
TBU Channel 1 Control Register **(00010C$_H$)** **Application Reset Value: 0000 0000$_H$**

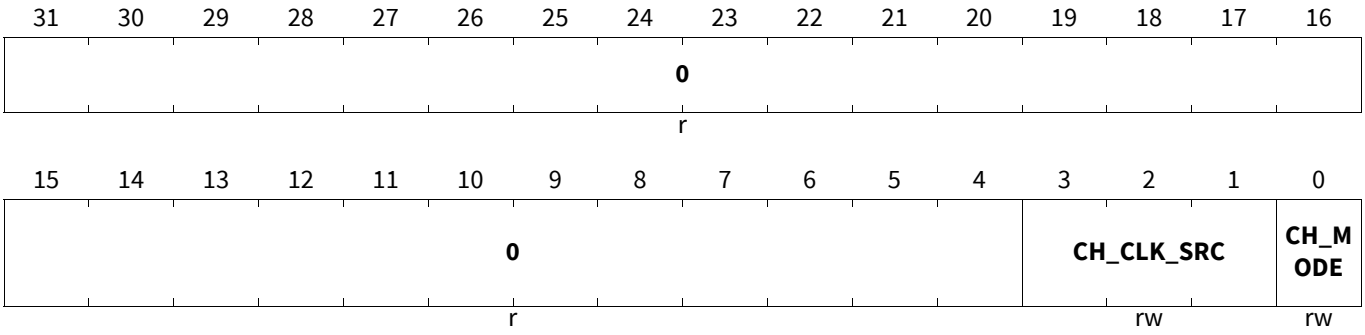


Field	Bits	Type	Description
CH_MODE	0	rw	**Channel mode** This value can only be modified if channel 1 is disabled. In Free running counter mode the CMU clock source specified by **CH_CLK_SRC** is used for the counter. In Forward/Backward counter mode the *SUB_INC1c* clock signal in combination with the *DIR1* input signal is used to determine the counter direction and clock frequency. 0_B Free running counter mode 1_B Forward/backward counter mode
CH_CLK_SRC	3:1	rw	**Clock source for channel 1 time base counter** This value can only be modified if channel 1 was disabled 000_B CMU_CLK0 selected 001_B CMU_CLK1 selected 010_B CMU_CLK2 selected 011_B CMU_CLK3 selected 100_B CMU_CLK4 selected 101_B CMU_CLK5 selected 110_B CMU_CLK6 selected 111_B CMU_CLK7 selected
0	31:4	r	**Reserved** Read as zero, shall be written as zero.

28.12.4.5 Register TBU_CH2_CTRL

TBU Channel 2 Control Register

TBU_CH2_CTRL
TBU Channel 2 Control Register **(000114_H)** **Application Reset Value: $0000\ 0000_H$**



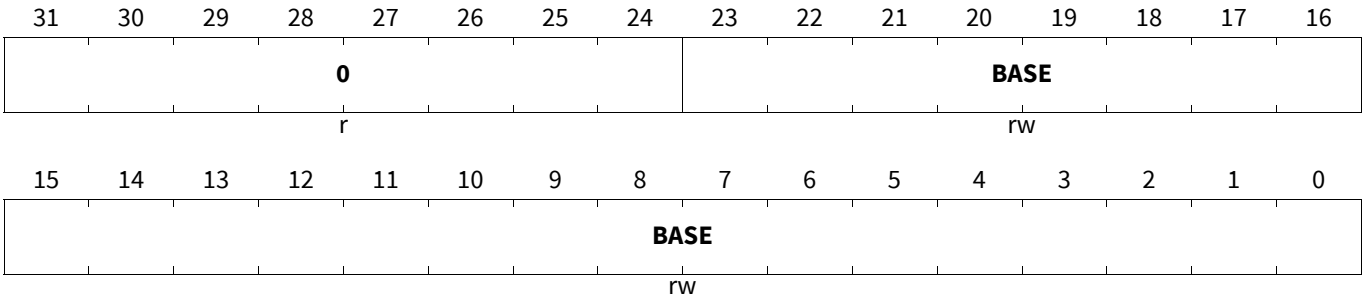
Field	Bits	Type	Description
CH_MODE	0	rw	**Channel mode** This value can only be modified if channel 2 is disabled. In Free running counter mode the CMU clock source specified by **CH_CLK_SRC** is used for the counter. In Forward/Backward counter mode the *SUB_INC2c* clock signal in combination with the *DIR2* input signal is used to determine the counter direction and clock frequency. 0_B Free running counter mode 1_B Forward/backward counter mode
CH_CLK_SRC	3:1	rw	**Clock source for channel 2 time base counter** This value can only be modified if channel 2 was disabled 000_B CMU_CLK0 selected 001_B CMU_CLK1 selected 010_B CMU_CLK2 selected 011_B CMU_CLK3 selected 100_B CMU_CLK4 selected 101_B CMU_CLK5 selected 110_B CMU_CLK6 selected 111_B CMU_CLK7 selected
0	31:4	r	**Reserved** Read as zero, shall be written as zero.

28.12.4.6 Register TBU_CH[y]_BASE

TBU Channel 1 Base Register

TBU_CH1_BASE

TBU Channel 1 Base Register **(000110_H)** **Application Reset Value: $0000\ 0000_H$**

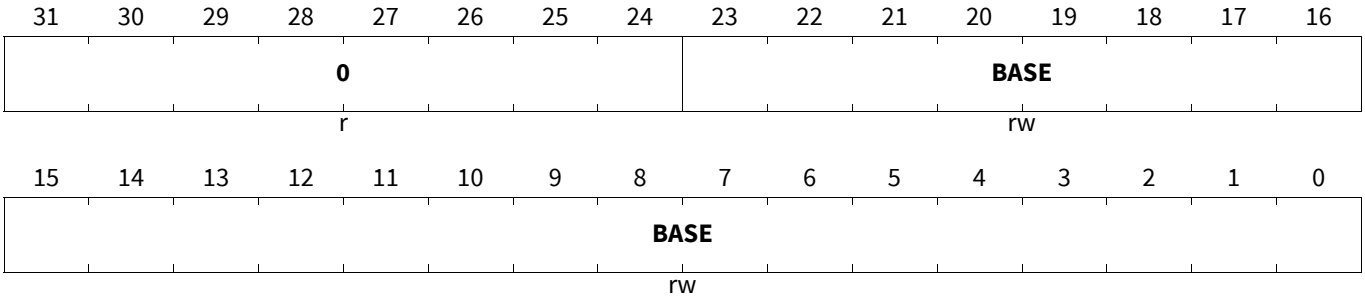


Field	Bits	Type	Description
BASE	23:0	rw	**Time base value for channel y (y: 1, 2)** The value of **BASE** can only be written if the corresponding TBU channel y is disabled. If the corresponding channel y is enabled, a read access to this register provides the current value of the underlying counter.
0	31:24	r	**Reserved** Read as zero, shall be written as zero

TBU Channel 2 Base Register

TBU_CH2_BASE

TBU Channel 2 Base Register **(000118_H)** **Application Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
BASE	23:0	rw	**Time base value for channel y (y: 1, 2)** The value of **BASE** can only be written if the corresponding TBU channel y is disabled. If the corresponding channel y is enabled, a read access to this register provides the current value of the underlying counter.
0	31:24	r	**Reserved** Read as zero, shall be written as zero

28.12.4.7 Register TBU_CH3_CTRL

TBU Channel 3 Control Register

TBU_CH3_CTRL
TBU Channel 3 Control Register **(00011C$_H$)** **Application Reset Value: 0000 0001$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0											USE_CH2	0			CH_MODE
r											rw	r			r

Field	Bits	Type	Description
CH_MODE	0	r	**Channel mode** 1 = Forward/backward counter mode
USE_CH2	4	rw	**Channel selector for modulo counter** This value can only be modified if channel 3 was disabled 0_B TBU_CH1 values used (SUB_INC1c for clock, DIR1 for counter direction, TBU_TS1 for capturing) 1_B TBU_CH2 values used (SUB_INC2c for clock, DIR2 for counter direction, TBU_TS2 for capturing)
0	3:1, 31:5	r	**Reserved** Read as zero, shall be written as zero.

28.12.4.8 Register TBU_CH3_BASE

TBU Channel 3 Base Register

TBU_CH3_BASE
TBU Channel 3 Base Register **(000120$_H$)** **Application Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								BASE							
r								rw							

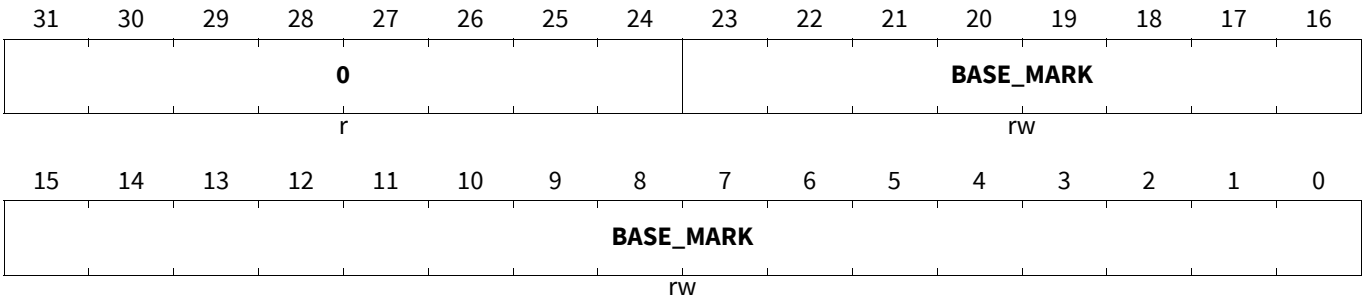
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE															
rw															

Field	Bits	Type	Description
BASE	23:0	rw	**Time base value for channel 3** The value of **BASE** can only be written if the corresponding TBU channel 3 is disabled. If the corresponding channel 3 is enabled, a read access to this register provides the current value of the underlying counter.
0	31:24	r	**Reserved** Read as zero, shall be written as zero

28.12.4.9 Register TBU_CH3_BASE_MARK

TBU Channel 3 Modulo Value Register

TBU_CH3_BASE_MARK
TBU Channel 3 Modulo Value Register **(000124_H)** **Application Reset Value: 0000 0000$_H$**

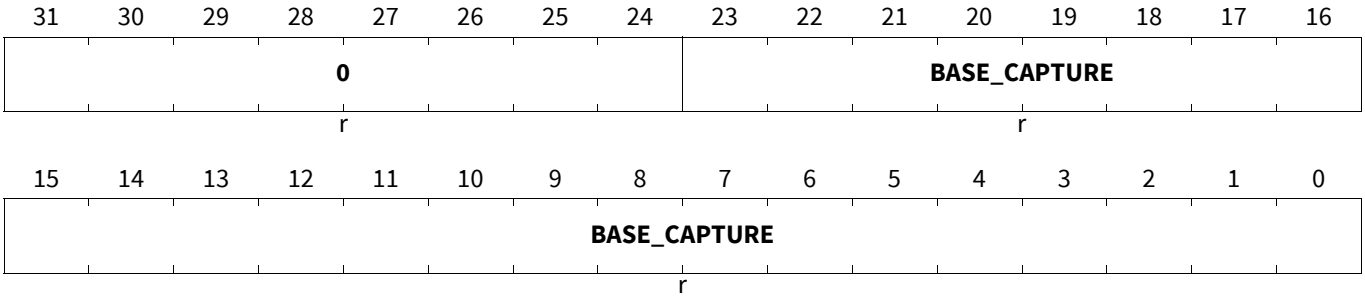


Field	Bits	Type	Description
BASE_MARK	23:0	rw	**Modulo value for channel 3** The value of **BASE_MARK** can only be written if the corresponding TBU channel 3 is disabled.
0	31:24	r	**Reserved** Read as zero, shall be written as zero.

28.12.4.10Register TBU_CH3_BASE_CAPTURE

TBU Channel 3 Base Captured Register

TBU_CH3_BASE_CAPTURE
TBU Channel 3 Base Captured Register **(000128_H)** **Application Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
BASE_CAPTURE	23:0	r	**Captured value of time base channel 1 or 2** When USE_CH2=0, TBU_TS1 is captured, and if USE_CH2 is set TBU_TS2 is captured.
0	31:24	r	**Reserved** Read as zero, shall be written as zero.