34 Inter-Integrated Circuit (I2C)

This chapter describes the Inter-Integrated Circuit (short I2C) Module. The I2C module is not available in some variants. In these variants registers are still accessible but functionality cannot be guaranteed. The I2C module contains the following sections:

Note: The I2C module register names described in this chapter are referenced in the User's Manual by the module name prefix "I2Cm_" with m being the number of the module.

34.1 Feature List

- Compatible with I2C-bus specification version 2.1 **[1]**. See module functional restrictions in **Section 34.3.1.3**
- Master mode supported
- Multi-master mode supported (See restriction in **Section 34.3.1.3**)
- Slave mode supported
- Different speed ranges available for data transfer:
  - Standard mode up to 100 kbit/s (20kbit/s - 100kbit/s)
  - Fast mode up to 400 kbit/s (100kbit/s - 400kbit/s)
  - High-speed mode up to 3.4 Mbit/s (500kbit/s - 3.4Mbit/s)
- 7-bit and 10-bit I2C-bus addressing supported
- Automatic execution of low-level tasks like:
  - (De)Serialization of the bus data
  - Generation/detection of start and stop signal
  - Generation/detection of acknowledge signal
  - Bus state detection
  - Bus access arbitration in multi-master mode (See restriction in **Section 34.3.1.3**)
  - Recognition of device address in slave mode
  - Configurable detection of general call address
  - Configurable repeated start in master mode
- Flexible clock and timing control:
  - Prescaler for I2C kernel clock (from 0 to 255)
  - Bit rate generation via fractional divider
  - I2C-bus signal timing adjustment