EECS 170D

Project #2: Static CMOS Logic Gate

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Introduction

A fundamental purpose of transistors is to create logic gates. CMOS logic gates have many advantages in modern chip design. In this project, a logic gate will be designed for the following binary equation (eq1).

$$F = \big((A + B) * C * (D + E)\big)' \quad \text{(eq1)}$$

Logic Gate Design

Starting with the pulldown network using NMOS, inputs that are ‘or’ can be put in parallel while inputs that are ‘and’ can be put in series. For the pull up network using PMOS, replacing all series with parallel and parallel with series will result in the following CMOS logic gate as shown in Figure 1. The drawn schematic is turned into a stick diagram in Figure 2. The drawn schematic and stick diagram will later aid in the computer aided design in Cadence Virtuoso.

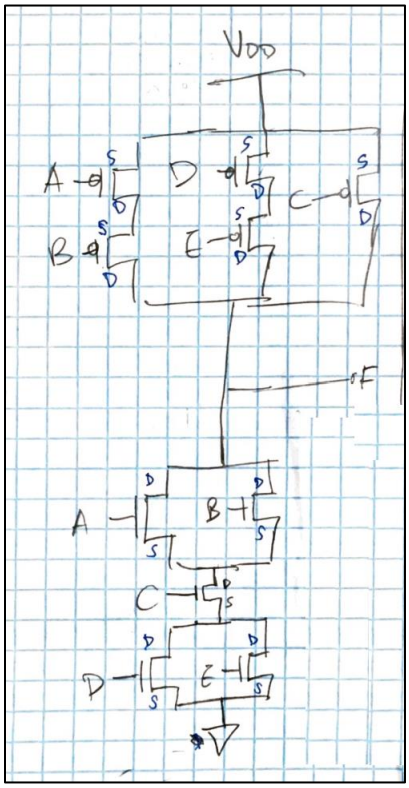

Figure 1: Drawn Schematic

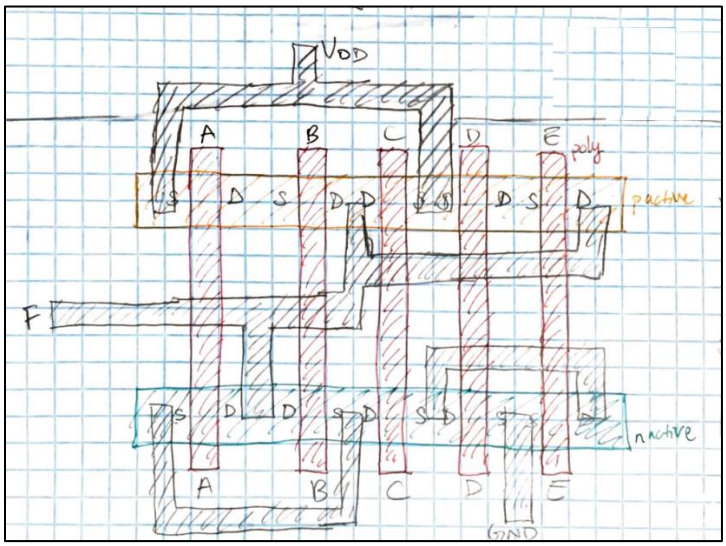

Figure 2: Stick Diagram

Transistor sizes were also calculated. PMOS were designed to be three times as large as NMOS. Transistors in series were increased in size to maintain a consistent propagation delay. Calculations for transistor sizing is shown in Figure 3.

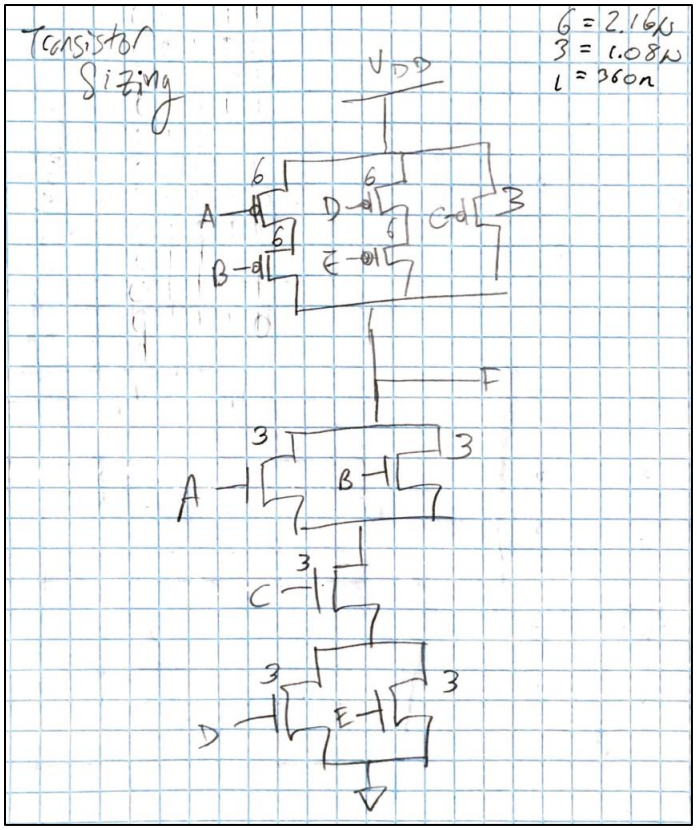

Figure 3: Transistor Sizing

Logic Gate Layout

Using Cadence Virtuoso, a schematic was created for the CMOS logic gate as shown in Figure 4. This schematic was turned into a symbol as shown in Figure 5.

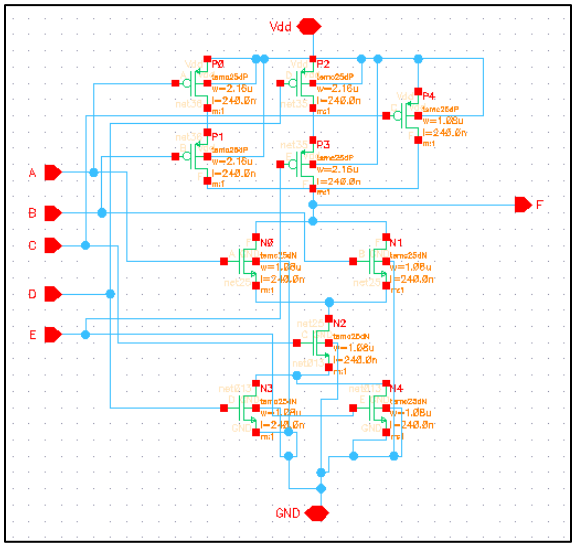

Figure 4: CMOS Logic Gate Schematic

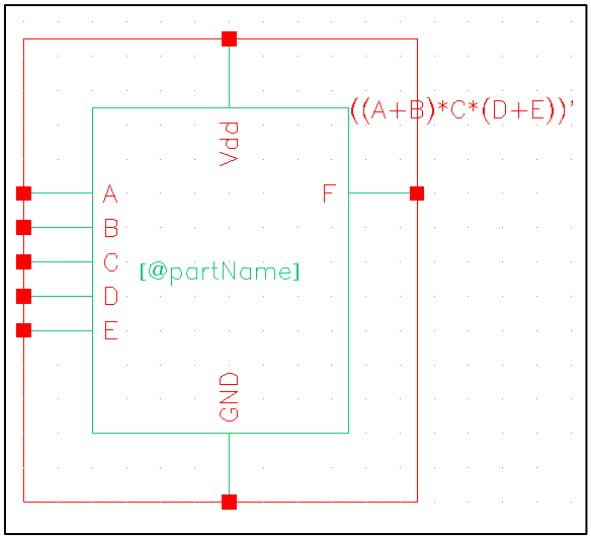

Figure 5: Symbolic CMOS Logic Gate

A layout was created for the CMOS logic gate as shown in Figure 6. The layout was based on the stick diagram from Figure 2. The transistors in the layout were sized according to the sizing in Figure 3. It is clear that the PMOS at gate C has a slightly smaller gate width compared to the other PMOS in the layout. Analog extraction with parasitic capacitance was performed on the layout.

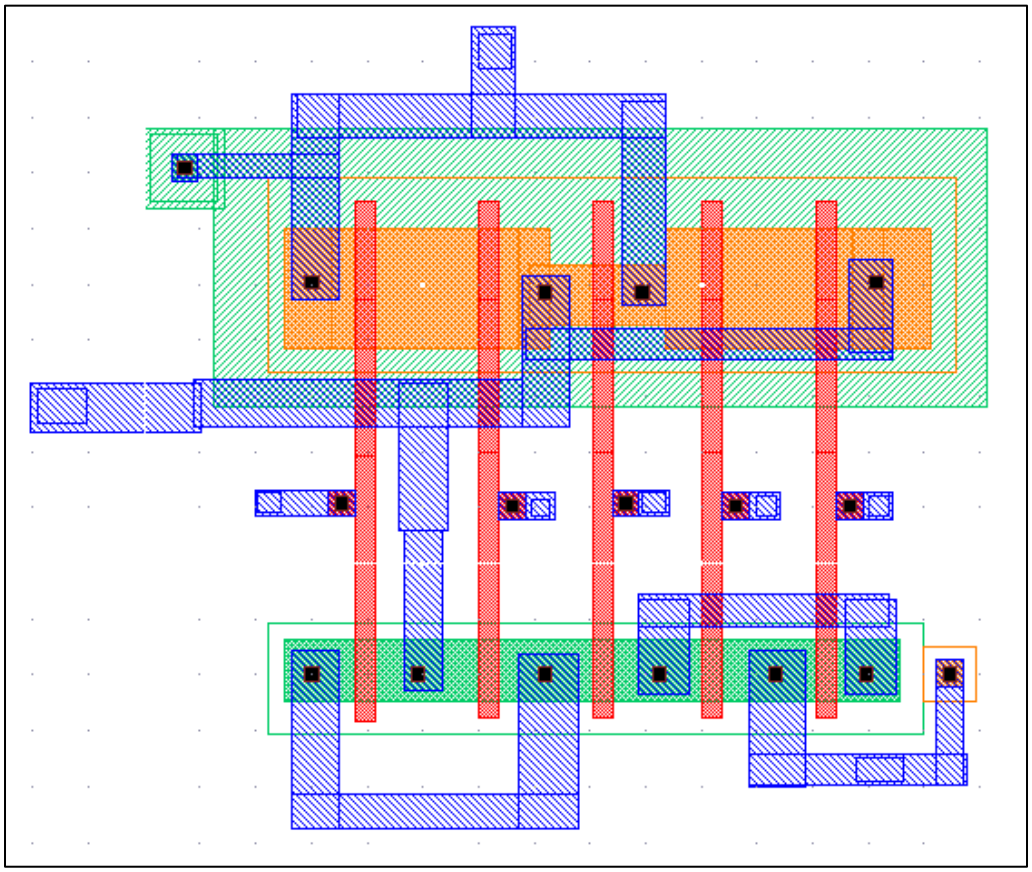

Figure 6: CMOS Logic Gate Layout

Logic Gate Verification

Using a configuration that included parasitic capacitance, the logic gate was simulated using five pulse sources with varying delays as shown in Figure 7. Each pulse source had a rise and fall time of 50 psec. Each pulse source was set to a different delay based on timings derived from the truth table in Figure 8. For input A, an input delay of 16ns was used after which was a pulse width of 16ns with period of 35ns. For input B, an input delay of 8ns was used after which was a pulse width of 8ns with period of 16ns. For input C, an input delay of 4ns was used after which was a pulse width of 4ns with a period of 8ns. For input D, an input delay of 2ns was used after which was a pulse width of 2ns with a period of 4ns. For input E, an input delay of 1ns was used after which was a pulse width of 1ns with a period of 2ns. In this way, every output of the original Boolean equation (eq1) could be plotted on a waveform.

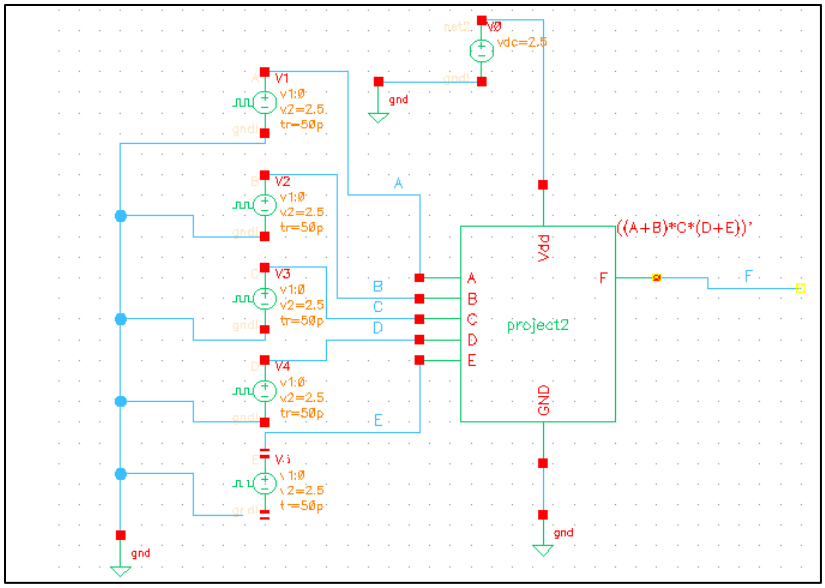

Figure 7: CMOS Logic Gate Simulation Configuration

Timing Number	A	B	C	D	E	F
1.	0	0	0	0	0	**1**
2.	0	0	0	0	1	**1**
3.	0	0	0	1	0	**1**
4.	0	0	0	1	1	**1**
5.	0	0	1	0	0	**1**
6.	0	0	1	0	1	**1**
7.	0	0	1	1	0	**1**
8.	0	0	1	1	1	**1**
9.	0	1	0	0	0	**1**
10.	0	1	0	0	1	**1**
11.	0	1	0	1	0	**1**
12.	0	1	0	1	1	**1**
13.	0	1	1	0	0	**1**
14.	0	1	1	0	1	**0**
15.	0	1	1	1	0	**0**
16.	0	1	1	1	1	**0**
17.	1	0	0	0	0	**1**
18.	1	0	0	0	1	**1**
19.	1	0	0	1	0	**1**
20.	1	0	0	1	1	**1**
21.	1	0	1	0	0	**1**

22.	1	0	1	0	1	**0**
23.	1	0	1	1	0	**0**
24.	1	0	1	1	1	**0**
25.	1	1	0	0	0	**1**
26.	1	1	0	0	1	**1**
27.	1	1	0	1	0	**1**
28.	1	1	0	1	1	**1**
29.	1	1	1	0	0	**1**
30.	1	1	1	0	1	**0**
31.	1	1	1	1	0	**0**
32.	1	1	1	1	1	**0**

Figure 7: CMOS Logic Truth Table

Examining the timings in relation to the truth table in Figure 7, we should see an output of zero from 13ns to 16ns. 22ns to 24ns, and 30ns to 32ns. All other times should be Vdd. This is verified in the simulation waveform shown in Figure 8. There is a fair amount of propagation delay when going from low to high and high to low, nevertheless, the binary logic components align with the truth table values. Other perturbations in the output signal can also be attributed to parasitic capacitances as well variances due to rise and fall time of the input signals.

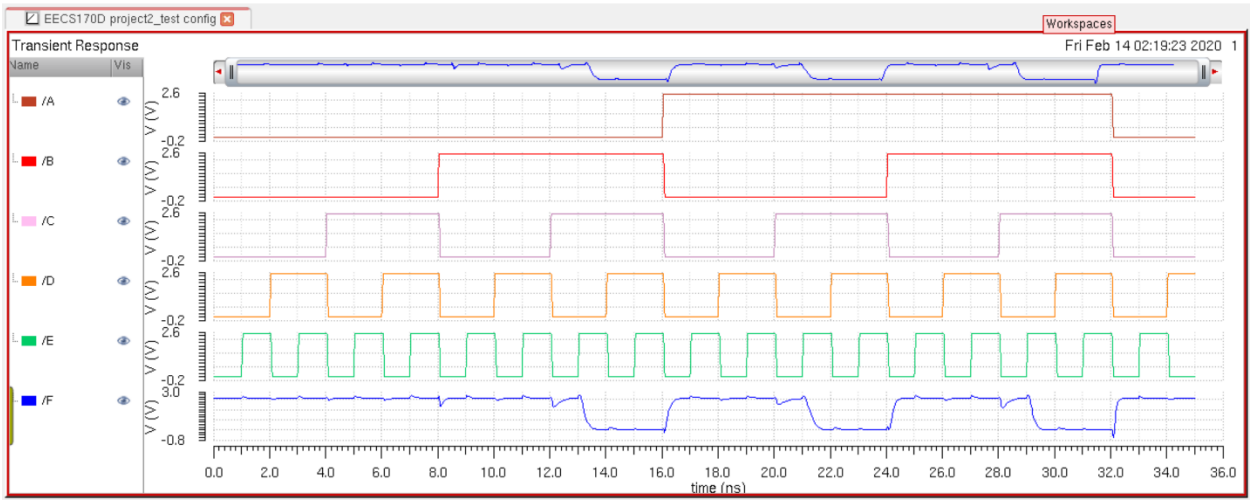

Figure 8: Simulated Waveform