EECS 170D

Project #1: Inverter and Oscillator

Enoch Chau 45179973

2/6/2020

Introduction

Inverters are a core component of digital logic design. A ring oscillator can be used to find propagation delay of inverters.

Inverter Design

To obtain an inverter where Vm = Vdd/2, we can use the approximation that:

$$V_m = \frac{r\,V_{dd}}{1+r} \text{ (eq.2)} \qquad r = \frac{k_p * V_{DSATp}}{k_n * V_{DSATn}} \text{ (eq.1)}$$

By equating the PMOS and NMOS current equations, we can derive the following expression:

$$\frac{W_p/L_p}{W_n/L_n} = \frac{k_n' V_{DSATn}(V_m - V_{tn} - \frac{V_{DSATn}}{2})}{k_p' V_{DSATp}(V_{dd} - V_m + V_{tp} - \frac{V_{DSATp}}{2})} \text{ (eq.3)}$$

This links Vm directly to the gate size of the NMOS and PMOS. The following parameters in Figure 1 are generalized for 0.25µ CMOS technology. The gate length is a static variable that cannot change for either NMOS or PMOS. The NMOS gate width would be smaller than the PMOS gate width. Using the variables from Figure 1 input into eq.3, we find that Wp must be 3.5 times greater than Wn in order to achieve Vm = Vdd/2.

	V_{T0}(V)	γ($V^{0.5}$)	V_{DSAT}(V)	k'(A/V^2)	λ(V^{-1})
NMOS	0.43	0.4	0.63	115 x 10^{-6}	0.06
PMOS	-0.4	-0.4	-1	-30 x 10^{-6}	-0.1

Figure 1: Parameters for 0.25µ CMOS technology

Another design parameter is for equal noise margins: $NM_H = NM_L$. The equations for noise margin are:

$$NM_H = Vdd - Vm - \frac{Vm}{g} \text{ (eq.4)} \qquad NM_L = Vm + \frac{(Vdd - Vm)}{g} - GND \text{ (eq.5)}$$

If Vm = Vdd/2 and GND = 0, eq.4 and eq.5 can be simplified:

$$NM_H = \frac{Vdd}{2} - \frac{Vdd}{2g} \text{ (eq.6)} \qquad NM_L = \frac{Vdd}{2} - \frac{Vdd}{2g} \text{ (eq.7)}$$

Showing that $NM_H = NM_L$.

Inverter Simulation

Using Cadence Virtuoso, first a schematic was created as shown in Figure 2. From this schematic, a layout was created as shown in Figure 3.

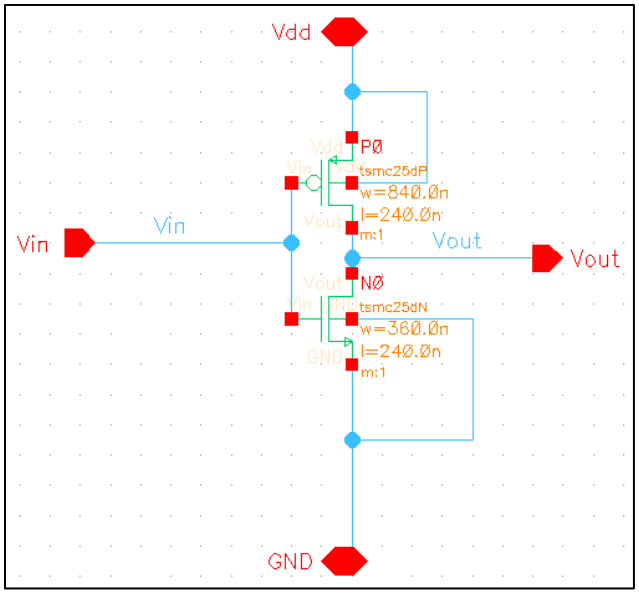

Figure 2: CMOS Inverter Schematic

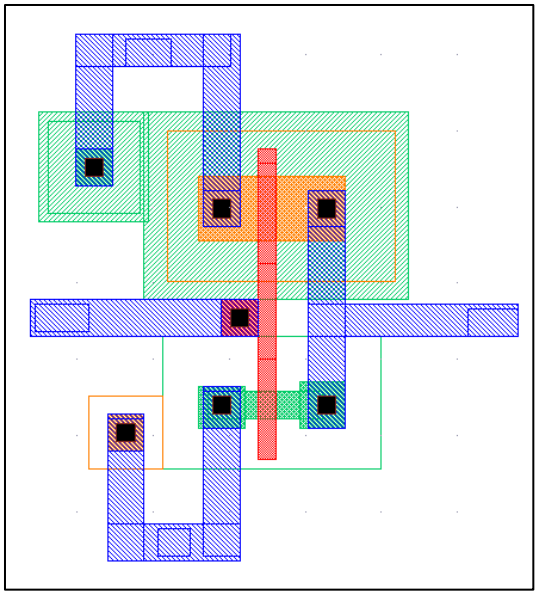

Figure 3: CMOS Inverter Layout

The layout was simulated using the following schematic in Figure 4. Two inverters were simulated, one using the regular configuration and one using the layout analog extracted configuration that included parasitic capacitance. Figure 5 shows the output waveform of a static pulse input with rise time and fall time of 100ps on the layout configured inverter. Figure 6 shows a dynamic DC sweep from 0 to Vdd=2.5V.

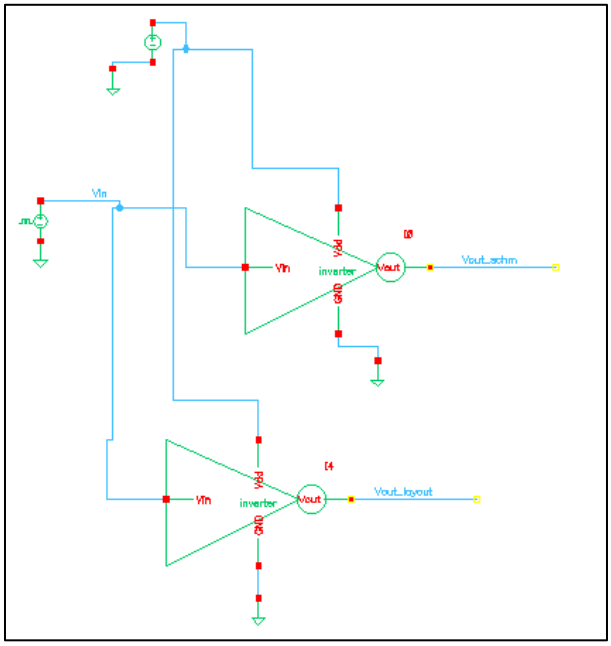

Figure 4: Inverter Test

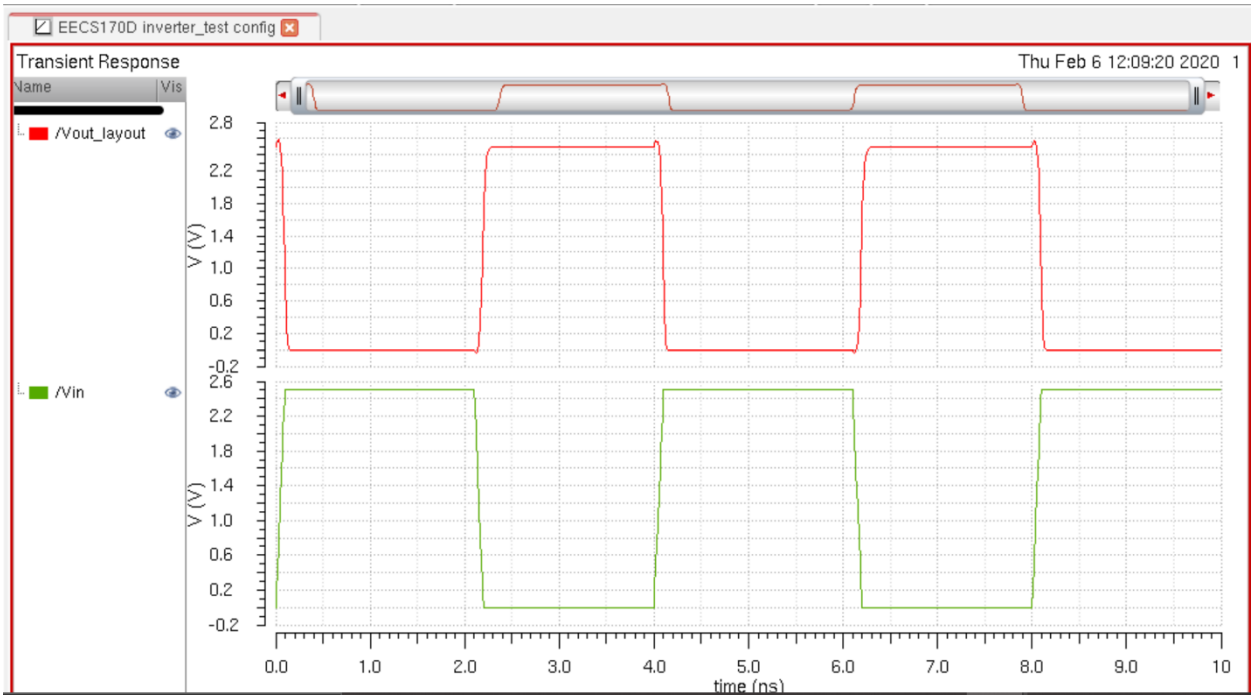

Figure 5: CMOS Inverter Static Waveform

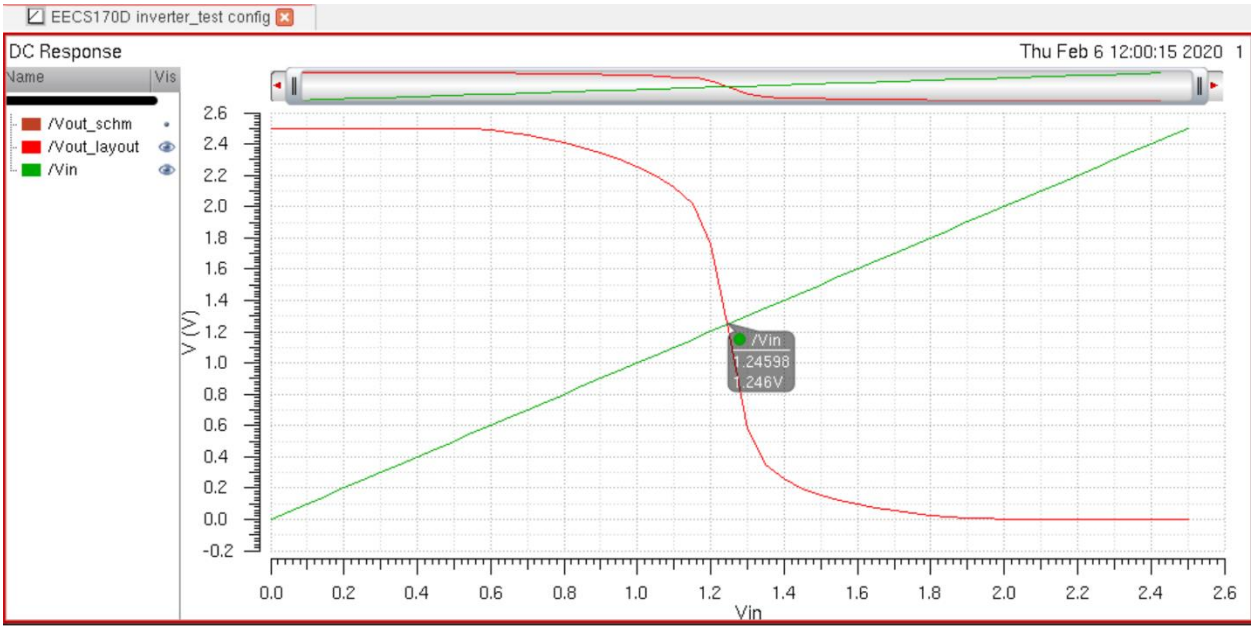

Figure 6: CMOS Inverter Dynamic Waveform

Figure 5 shows that Vm is about 1.25V. Vdd = 2.5V so Vm is approximately Vdd/2 which matches the calculated inverter design.

Using the calculator in Cadence ADE L on the graph shown in Figure 5, the propagation delay for low to high and high to low can be found to be t_{pLH} = 43.6 ps and t_{pHL} = 42.3 ps with overall propagation delay t_p = 42.95ps.

Besides propagation delay, the noise margins can also be calculated. Figure 7 shows the dynamic waveform along with its derivative plotted on the same graph. Examining the points where the derivative is -1, we can find the V_{IL} and V_{IH}.

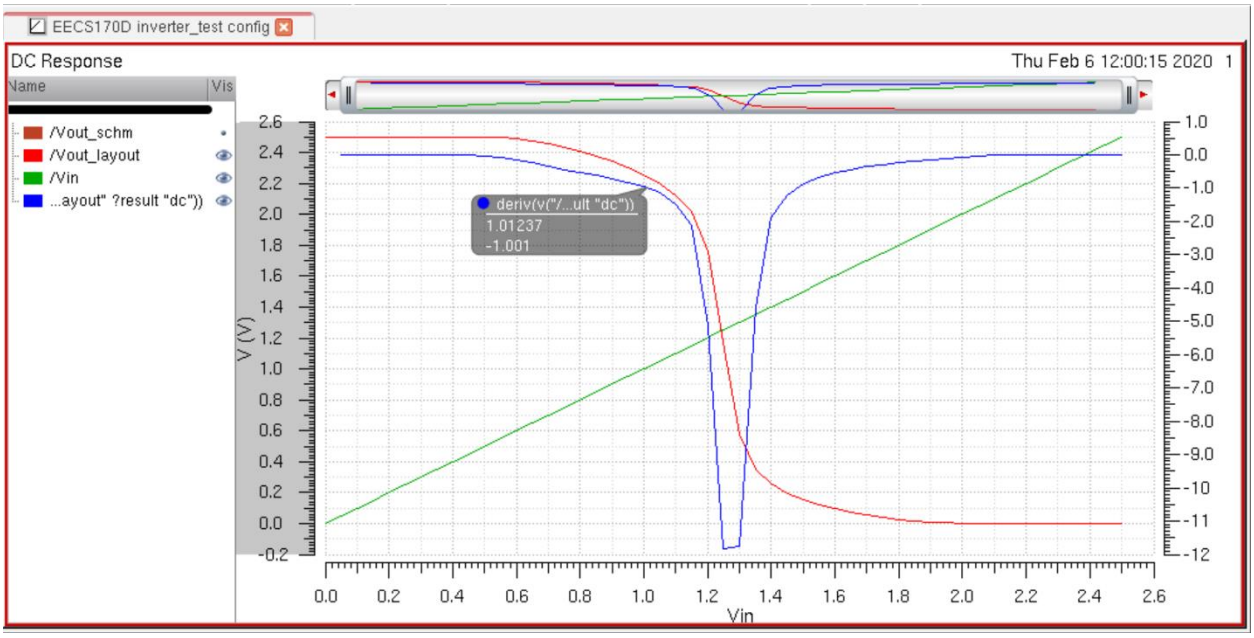

Figure 7: CMOS Inverter Dynamic Waveform with Derivative

The result of the noise margins are: $NM_H = 0.26V$ and $NM_L = 0.17V$. While not exactly equivalent, both values are small enough that they are within the error range to say that $NM_H \approx NM_L$.

Ring Oscillator Design

A ring oscillator can be made of any odd number of inverters that is greater than. Typical ring oscillators may use three inverters. In this project, we will be using 5 inverters to create a ring oscillator. When connected in series, the inverters will create oscillation. We can calculate the frequency of oscillation using eq.8:

$$f_{osc} = \frac{1}{n*2*t_p} \quad \text{(eq.8)}$$

Where fosc is the frequency of oscillation, n is the number of inverters, tp is the propagation delay of the inverter. Using the propagation delay calculated from the inverter's static waveform in Figure 5, we find that fosc = 2.33GHz.

Ring Oscillator Simulation

In Cadence Virtuoso, a ring oscillator was created using 5 inverters as shown in Figure 8. Simulation of this circuit provided the waveform shown in Figure 9. Each stage's output is labeled respectively starting with Vout0 to Vout4.

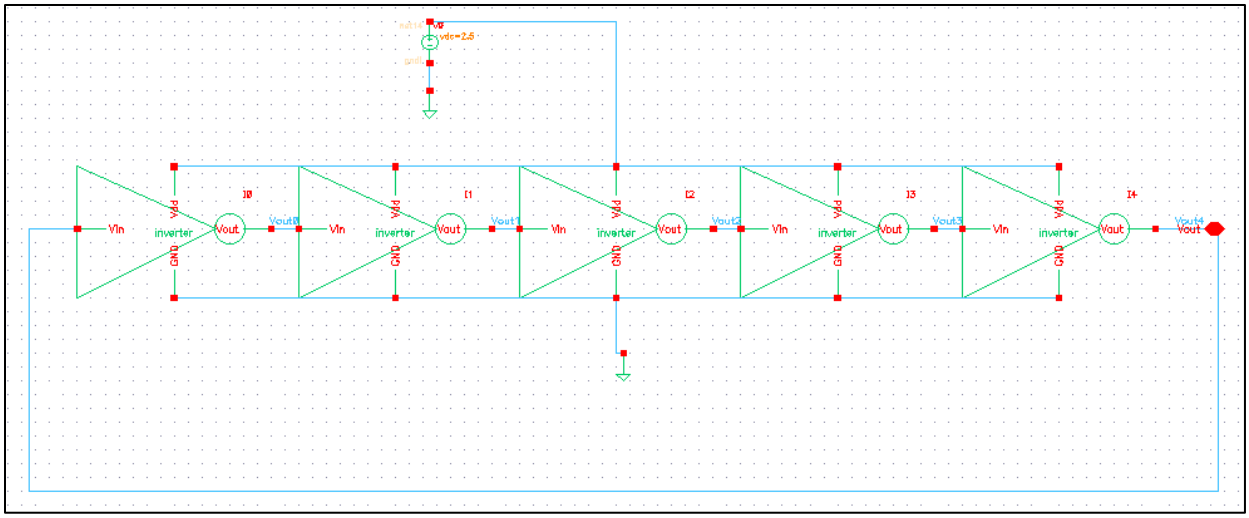

Figure 8: Five Stage Ring Oscillator

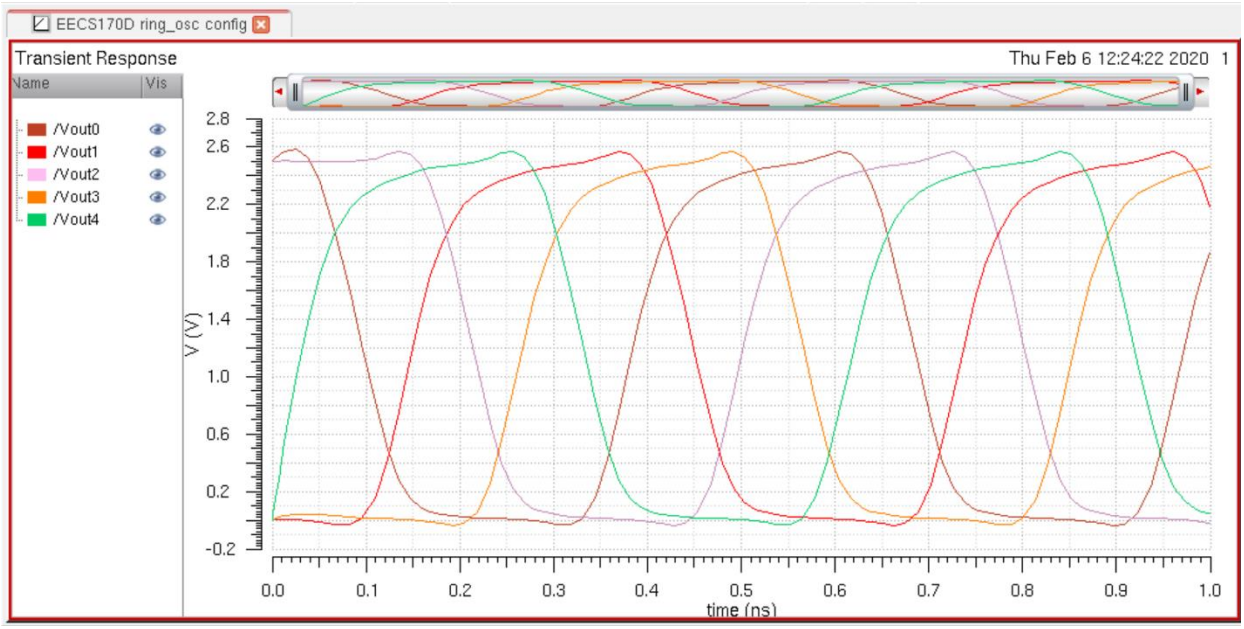

Figure 9: Oscillation Simulation Combined Graph

Examining the graphs show a period of 58.8ns. Converting to frequency, fosc is shown to be 1.7GHz.

The calculated frequency of 2.3GHz is not similar to the simulated frequency of 1.7GHz. This may be due to parasitic capacitance from previous stages providing external capacitance in addition to the inverter's internal capacitance.