EECS 170D

Project #3: BCD Adder

Enoch Chau 45179973

2/22/2020

Introduction

A 4-bit BCD adder outputs the sum of two 4-bit numbers. Instead of having a regular carry, the BCD adder will output it's sum as two binary numbers that form one decimal number. For example, if the sum is 16, the output will be 1 0100 which translates to 1 4 in decimal.

A BCD adder requires three types of components: two 4-bit adders, one 3-input OR gate, and two AND gates. A 3-input OR gate can be constructed from a three input NOR gate and an inverter. An AND gate can be realized from a NAND gate and an inverter. A 4-bit adder is made of four full adders. A full adder is made of three NAND gates and two XOR gates. The inverter was already created in Project 1. In this project, a NAND gate, XOR gate, full adder, 4-bit adder, AND gate, 3-input OR gate, and BCD adder are created using CMOS design.

NAND Gate Design

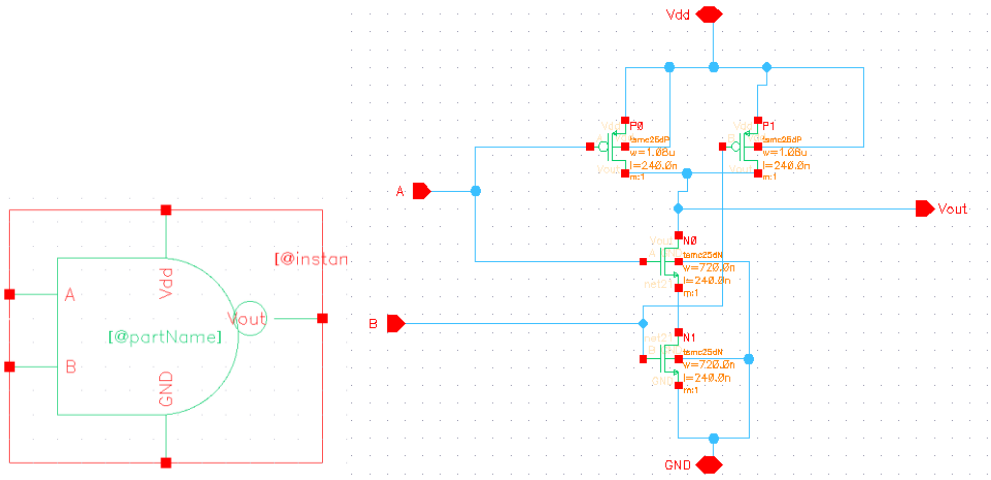

Figure 1: NAND Symbol and Schematic

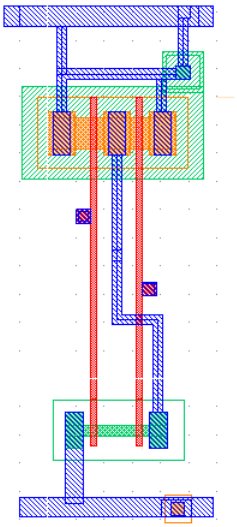

Figure 3: NAND Layout

XOR Gate Design

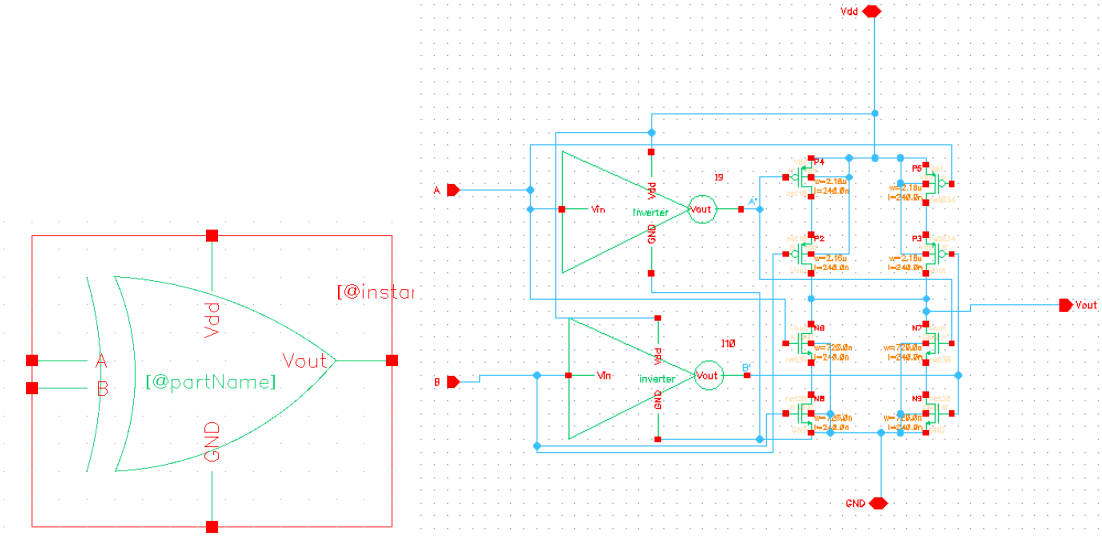

Figure 3: XOR Symbol and Schematic

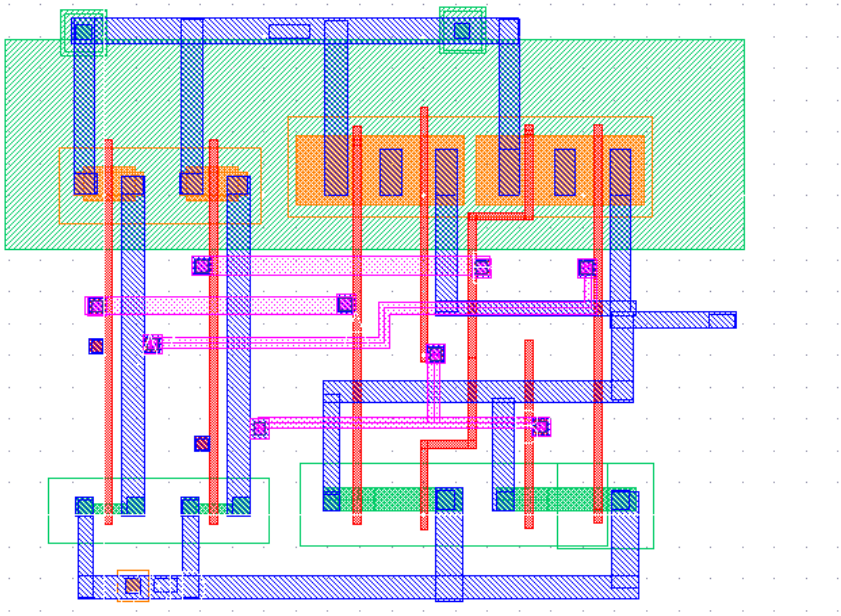

Figure 4: XOR Layout

Full Adder Design

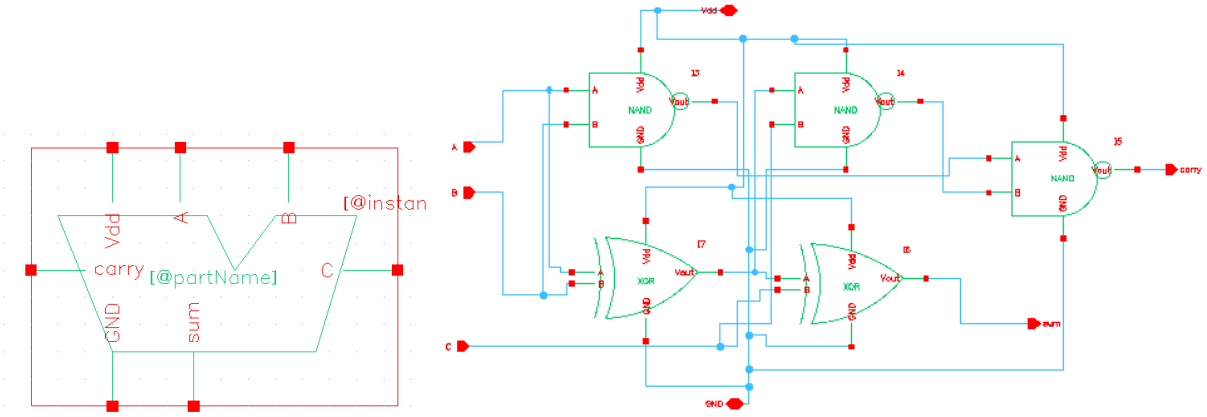

Figure 5: Full Adder Symbol and Schematic

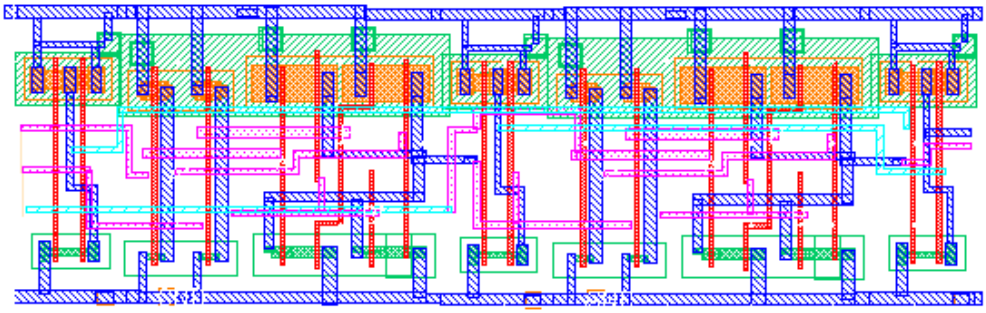

Figure 6: Full Adder Layout

4-Bit Adder

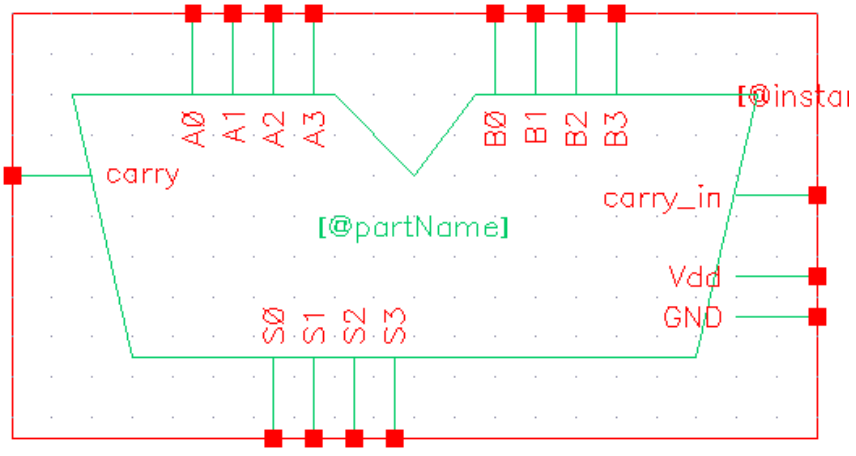

Figure 7: 4-Bit Adder Symbol

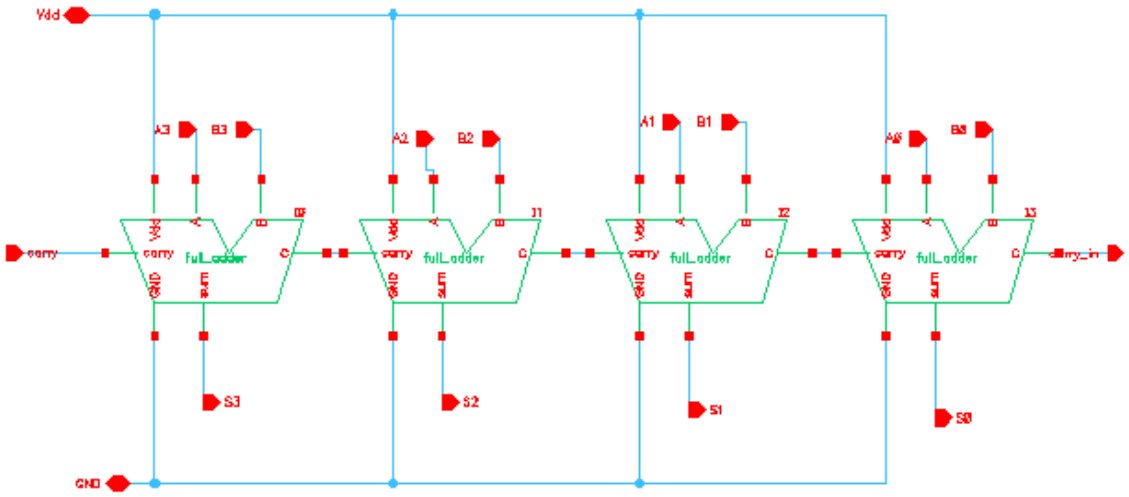

Figure 8: 4-Bit Adder Schematic

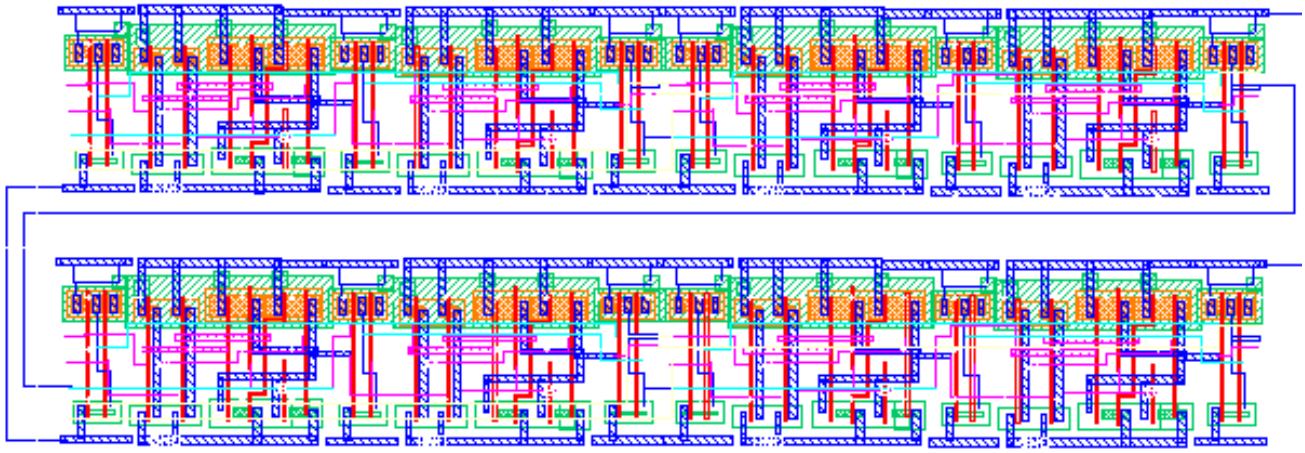

Figure 9: 4-Bit Adder Layout

AND Gate Design

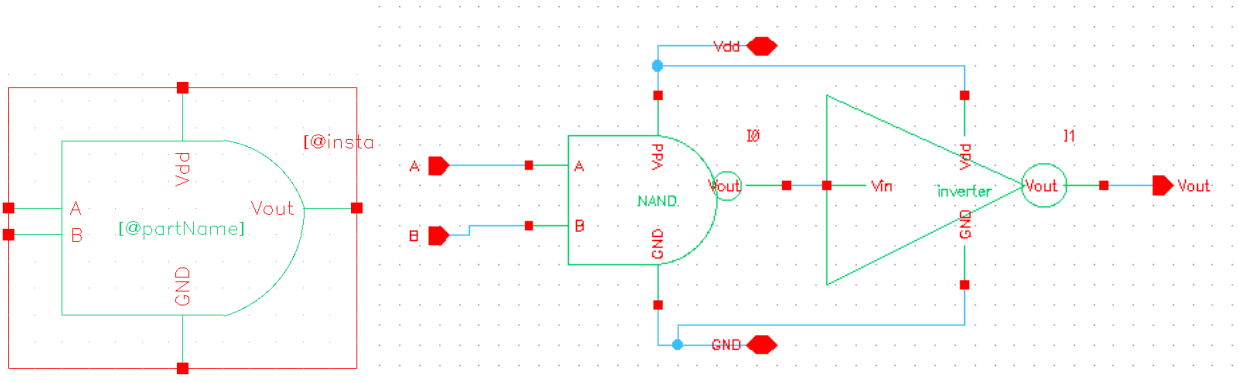

Figure 10: AND Symbol and Schematic

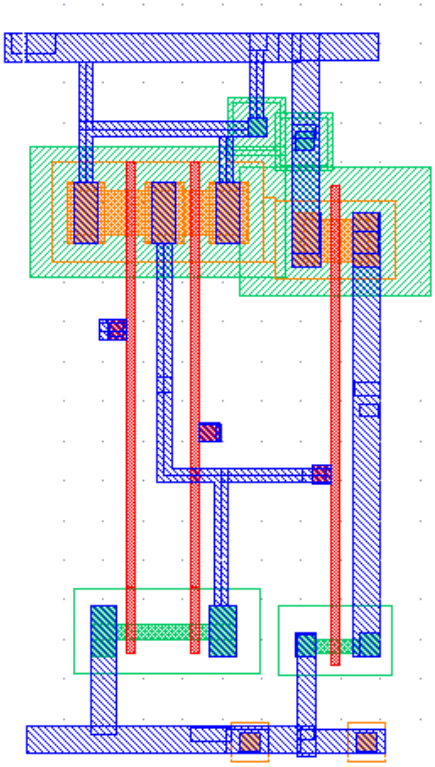

Figure 11: AND Layout

3 Input OR Gate Design

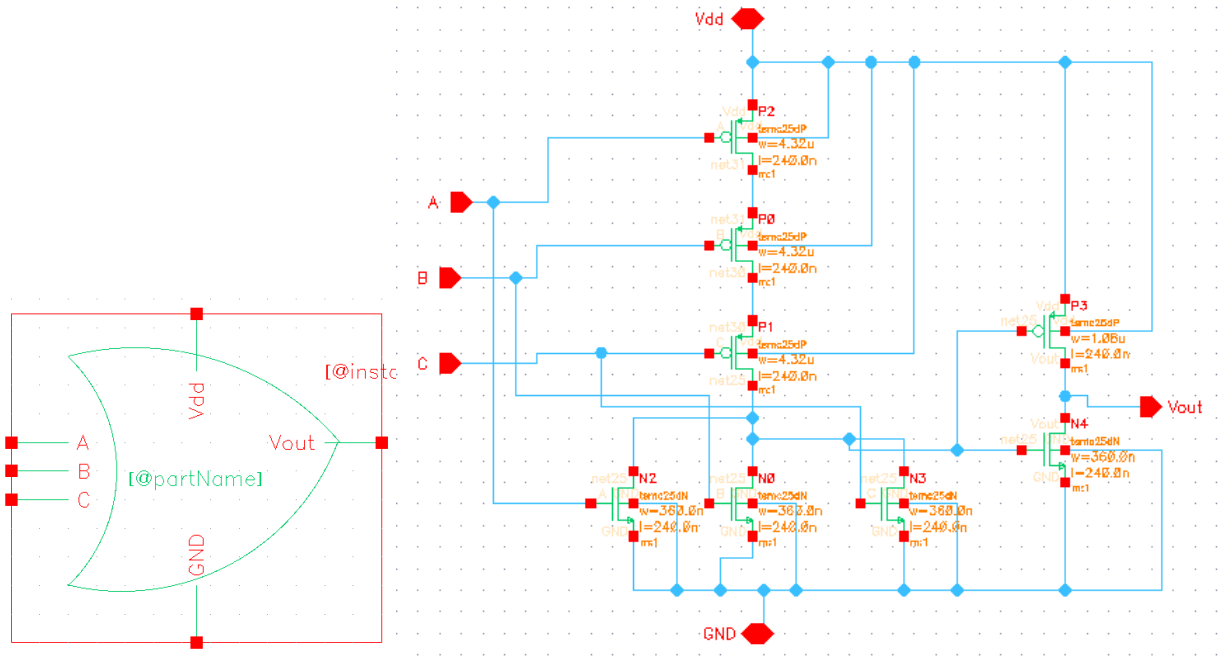

Figure 12: 3 Input OR Symbol and Schematic

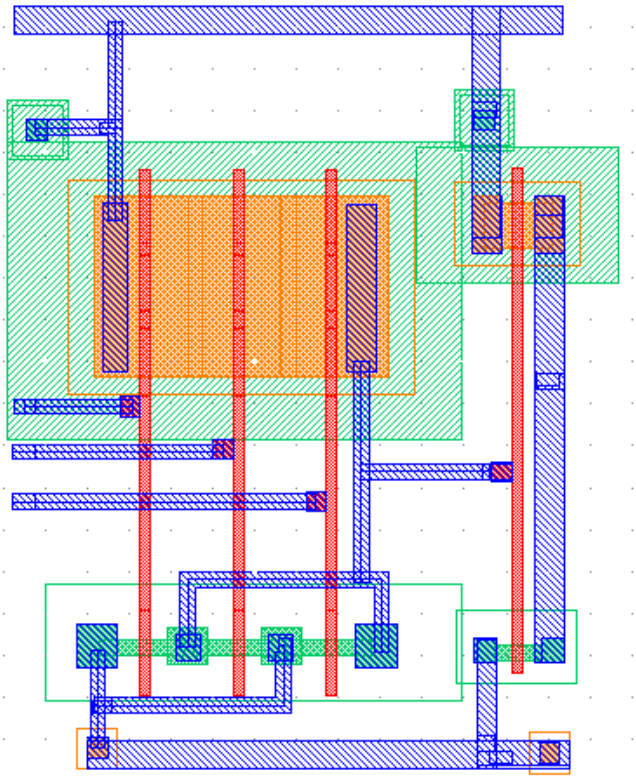

Figure 13: Three Input OR Layout

BCD Adder Design

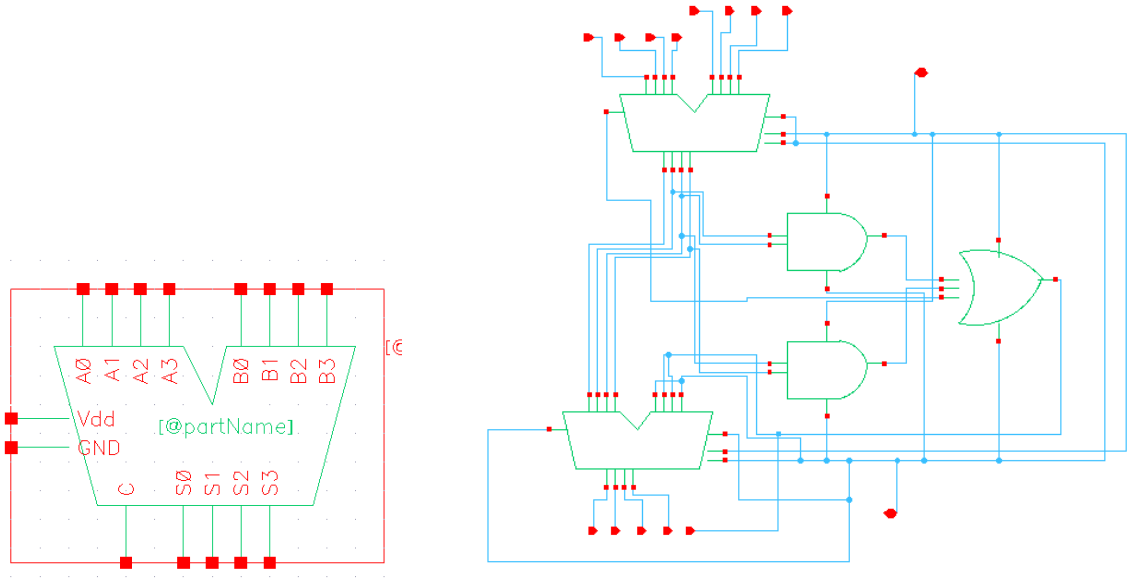

Figure 14: BCD Adder Symbol and Schematic

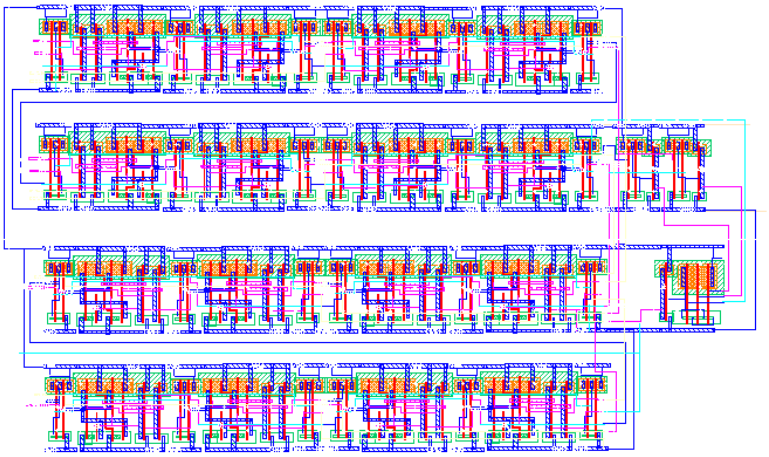

Figure 15: BCD Adder Layout

BCD Adder Verification

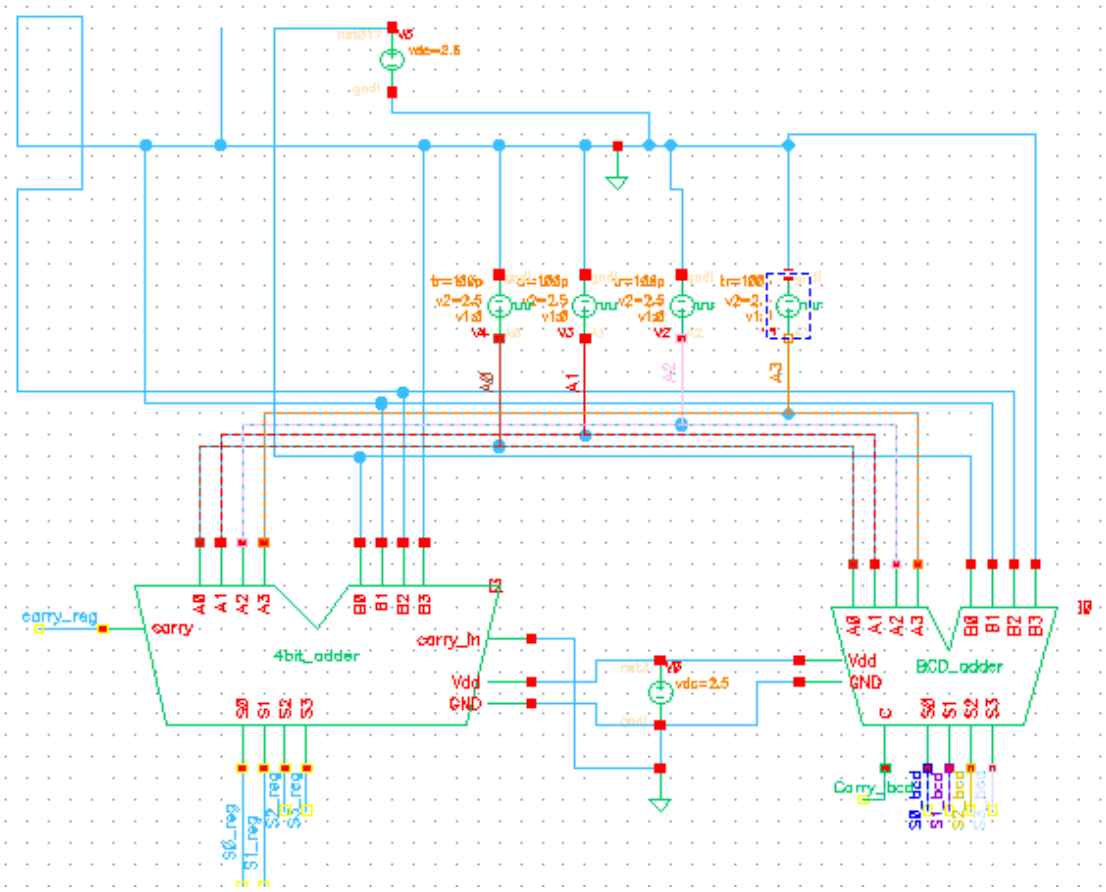

Figure 16: BCD Adder Verification Schematic

The circuit in Figure 16 is used to verify the circuit. Input A has alternating voltage pulse sources that give numbers from 0 to 15. For clarity of verification, each pulse was set at the microsecond level. Input B is manually connected to Vdd to get different outputs. Figure 17 is a

BCD adder truth table to aid in verification. Figures 18-21 have input B at different Boolean values.

C	S3	S2	S1	S0	Decimal
0	0	0	0	0	0
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
0	0	1	0	0	4
0	0	1	0	1	5
0	0	1	1	0	6
0	0	1	1	1	7
0	1	0	0	0	8
0	1	0	0	1	9
1	0	0	0	0	10
1	0	0	0	1	11
1	0	0	1	0	12
1	0	0	1	1	13
1	0	1	0	0	14
1	0	1	0	1	15
1	0	1	1	0	16
1	0	1	1	1	17
1	1	0	0	0	18
1	1	0	0	1	19

Figure 17: BCD Output Table

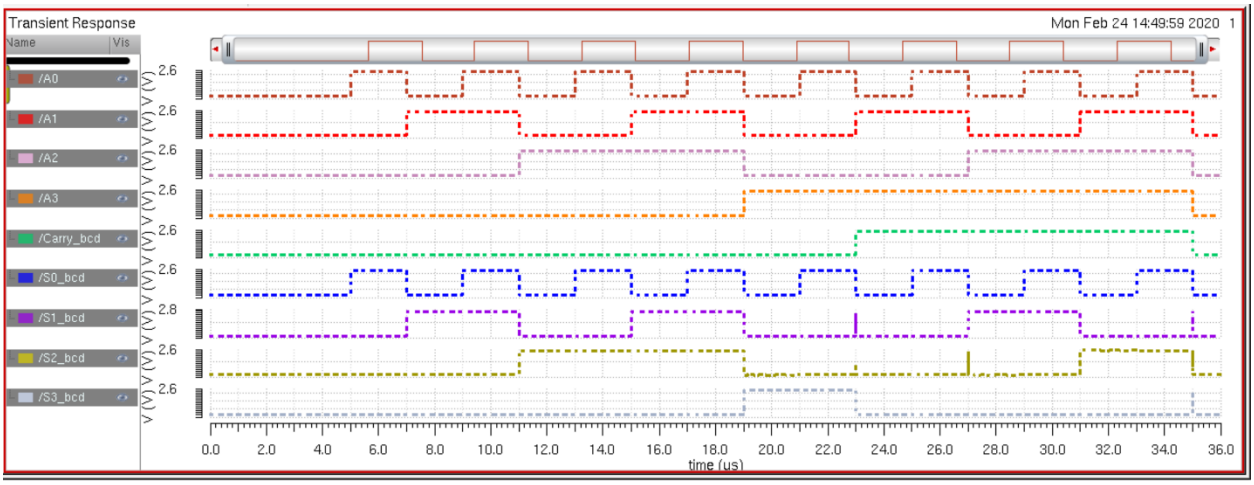

Figure 18: BCD A plus 0

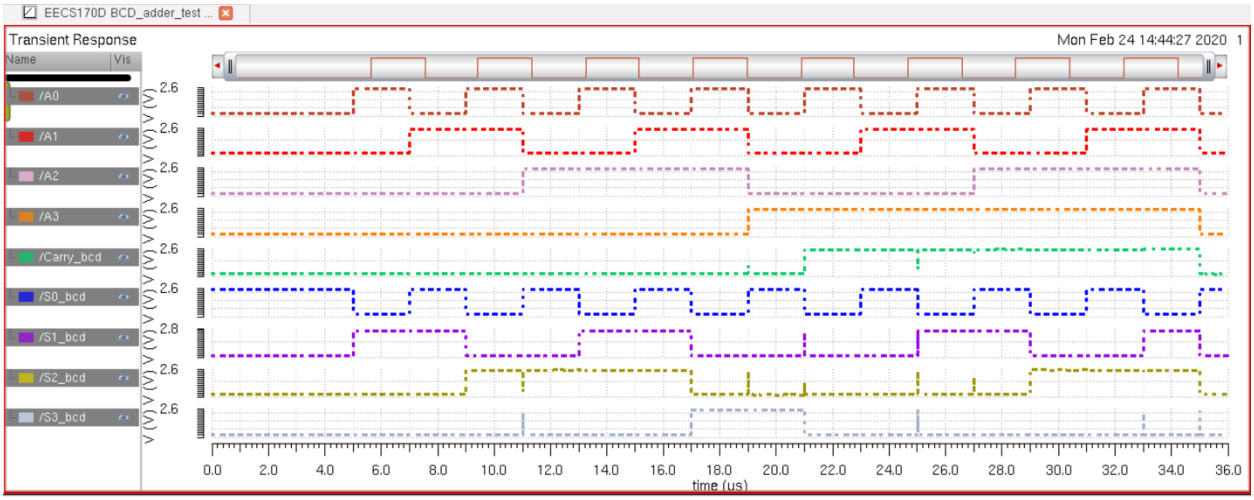

Figure 19: BCD A plus 1

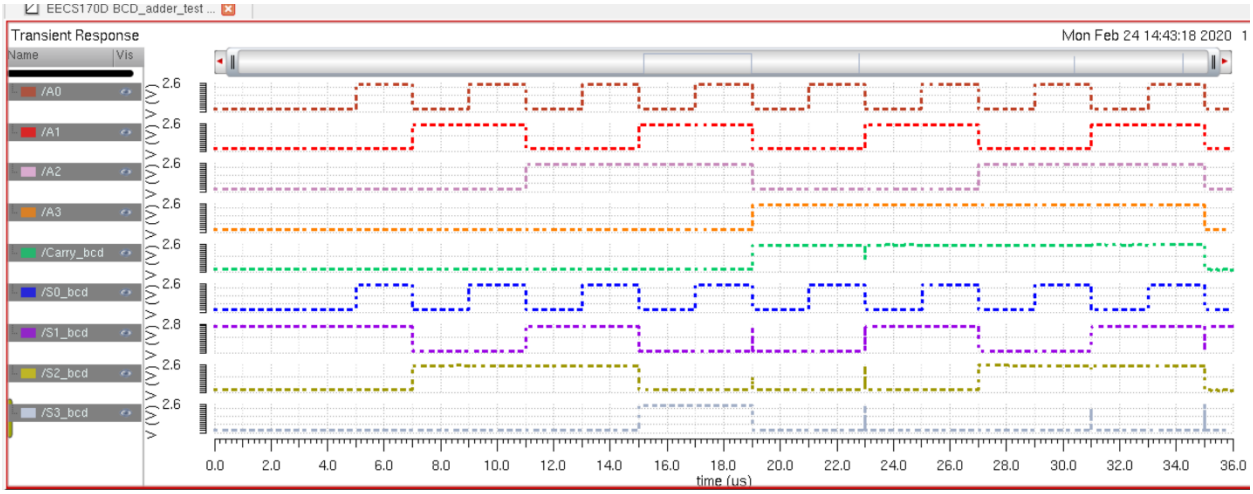

Figure 20: BCD A plus 2

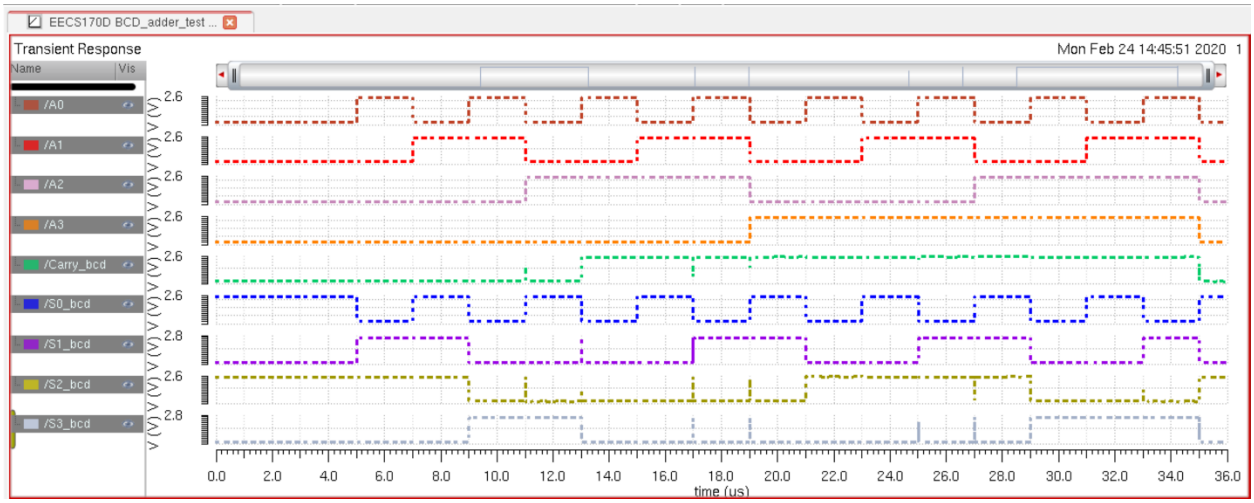

Figure 21: BCD A plus 3

Comparing the BCD truth table in Figure 16 to the outputs in Figures 17, 18, and 19, the BCD adder can be verified to give correct outputs. Input A has voltage pulse signals which switch giving binary representations of 0 through 16. Figure 17 has input B equal to 0. Figure 18 has input B equal to 1. Figure 19 has input B equal to 2. Figure 20 has input B equal to 3. A BCD adder can only give an output up to 19. Every output is verified.

Figure 21 is included to show the effects of parasitic capacitors. For this simulation, all voltage pulse sources were set at the nano second level which shows the effects of parasitic on rise and fall time. Figure 21 can be compared to 19 as they theoretically should have the same outputs but the effects of parasitic give much different curves as rise and fall times are shown more clearly in Figure 21.

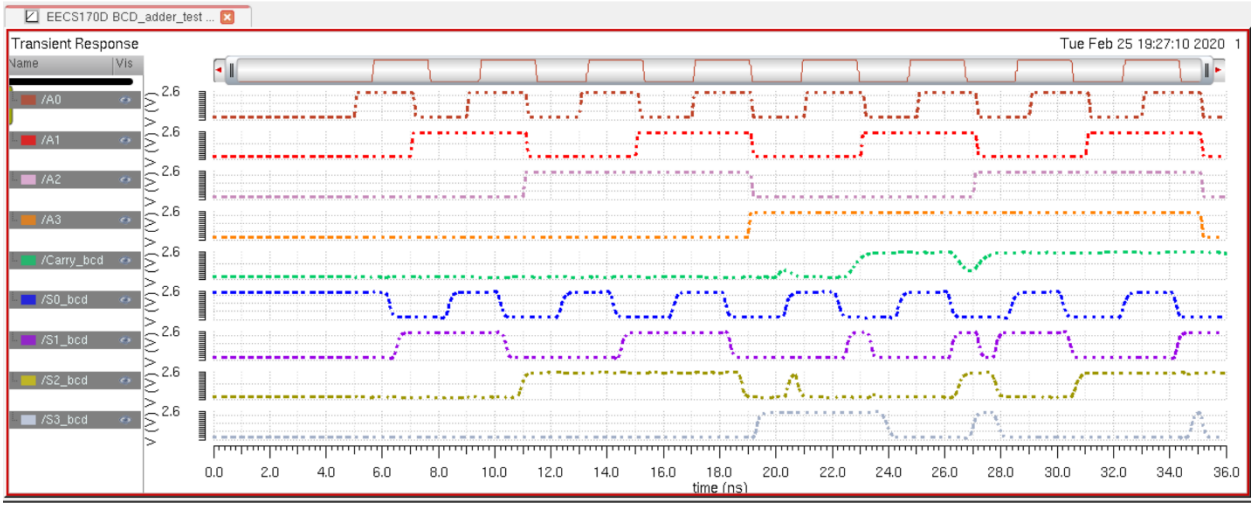

Figure 21: BCD A plus 1 at Nano Second level