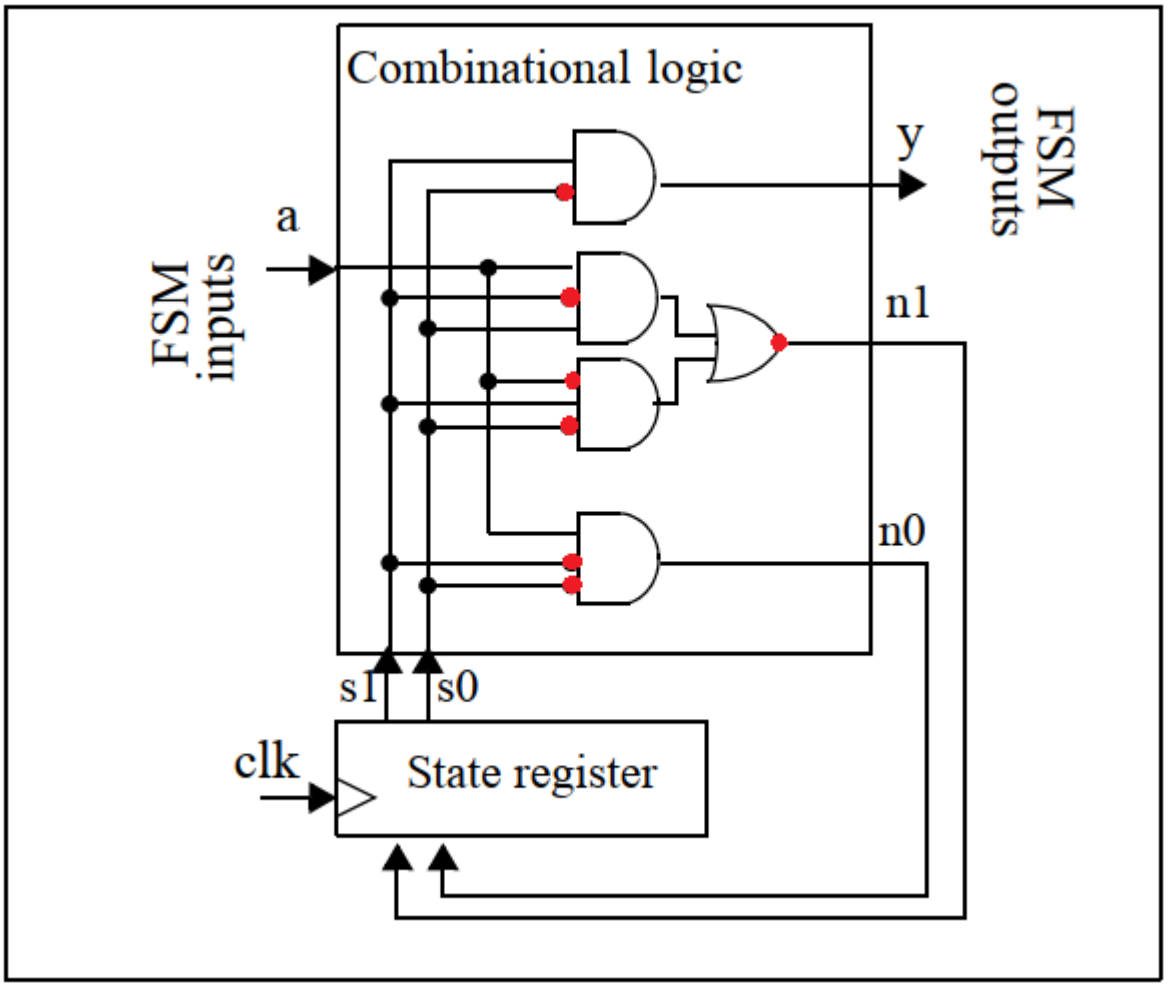
CSE232_HW_3

1- A synchronous sequential circuit is to be designed having a single input X and a single output Y to detect single change of level (from 0 to 1 or from 1 to 0) in a 3 bit word a procude an output Y=1, otherwise Y=0. When a new 3-bit word is to come, the circuit must be at its initial (reset) state and there should be a time delay of one clock cycle between the words. Draw the state diagram, draw the reduced state diagram, state transmission and output table. (60 p)

2- Make the truth table and draw the FSM diagram. (40 p)



Deadline: 08.05.2022 23:59