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(KNRTU-KAI)
Institute of Computer Technologies and Information Security
Department of Computer Systems

Report № 4

«Proteus Virtual System Modeling (VSM) »

«Architecture of embedded systems»

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Grade _____

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(signature, data)

[1] Please refers to the document "Laboratory Guidelines – Proteus Virtual System Modeling (VSM)"

Content

1. Tasks

a. List the binary counts for a counter and show how to gate the outputs of the 4-bit binary counter to implement this counter.

Table 1. List of outputs for a 4-bit binary counter (Q3 Most significant bit and Q0 least significant bit).

Q3	Q2	Q1	Q0	Count	Clock cycle
0	0	0	0	0	1st
0	0	0	1	1	2nd
0	0	1	0	2	3rd
0	0	1	1	3	4th
0	1	0	0	4	5th
0	1	0	1	5	6th
0	1	1	0	6	7th
0	1	1	1	7	8th
1	0	0	0	8	9th
1	0	0	1	9	10th
1	0	1	0	A	11th
1	0	1	1	B	12th
1	1	0	0	C	13th
1	1	0	1	D	14th
1	1	1	0	E	15th
1	1	1	1	F	16th

Table 1 shows all the outputs that can be generated by a 4-bit binary counter with any additional circuitry beyond the counter itself. However, what if you are interested in count from ground (b0000) to any other value from the table? For answering this question, it is relevant to understand how a binary counter is built using Flip-Flops. Figure 1 shows the schematic diagram for a 4-bit binary counter in the 74LS393 integrated circuit. In there the input signal is a clock signal and the outputs yield the different binary combinations shown in Table 1.

In order to set a specific counting range in the binary counter it is mandatory to aggregate additional circuitry that watch a desired output condition and restart the flip-flops once the condition is found. For instance, if you are interested in counting from 0 to 4 (0b0100), the

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output you should watch is the next output, i.e., the output 5 (0b0101). In Table 1, the blue highlighted rows correspond to the desired upper bound of your counter, whereas the blue rows indicate the output condition you should watch to obtain the desired output. A simple AND logic gate is required to watch the condition and restart the counter's output. Figure 2 shows how the AND logic gate restarts the counter when the condition 0b0101 is found, or the bits Q0 and Q2 output ones, in this case the upper bound is 4 (0b0100).

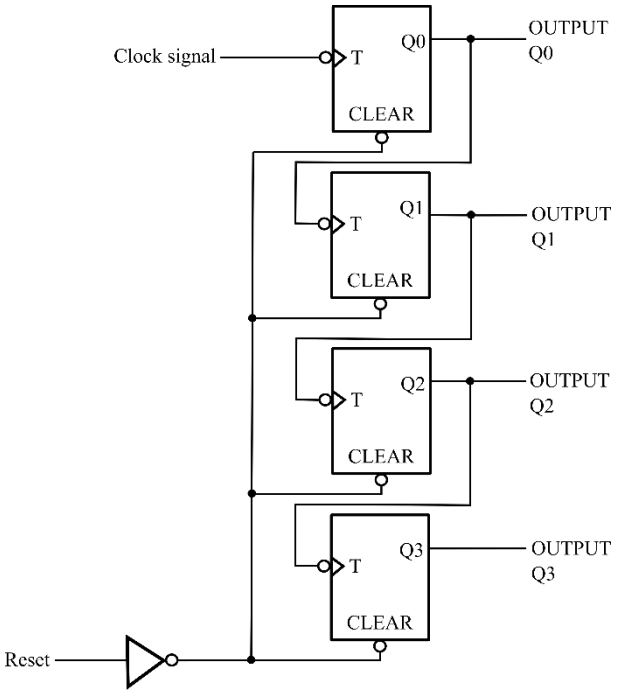

Figure 1. 74LS393 4-bit binary counter schematic diagram.

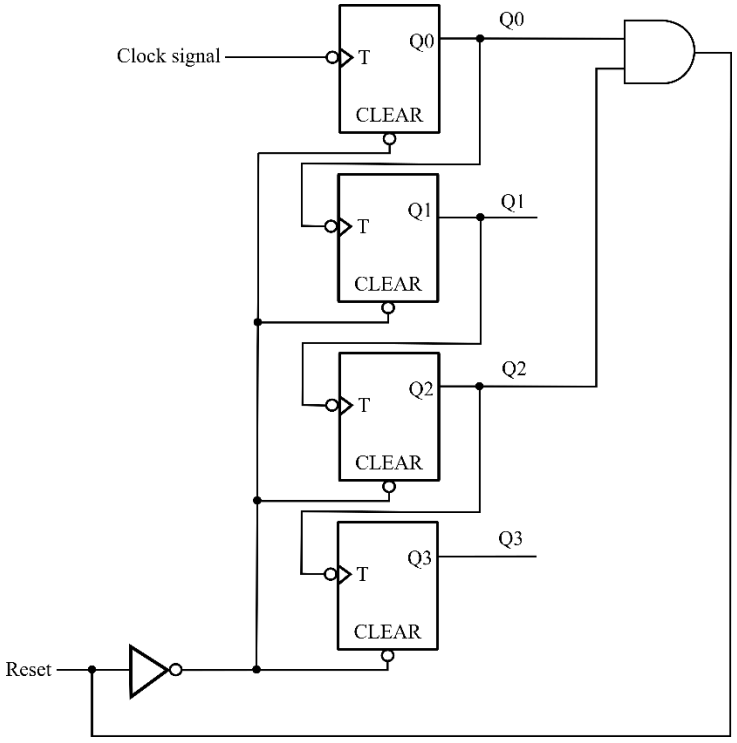

Figure 2. Additional output circuitry required for binary counting from zero to four.

Proteus Virtual System Modeling allows to simulate the circuit behavior. Please refers at the end of this section to read the outputs generated by the 4-bit binary counter with upper bound (counting

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from 0 to 4).

b. Referring to Figure 4.7[1] (guidelines for laboratory N° 4 “Proteus Virtual System Modeling (VSM”), place the following components into the Editing Windows: one 4-bit binary counter (74LS393), four 100 resistors, four light-emitting diodes, and one “AND” logic gate (74LS08).

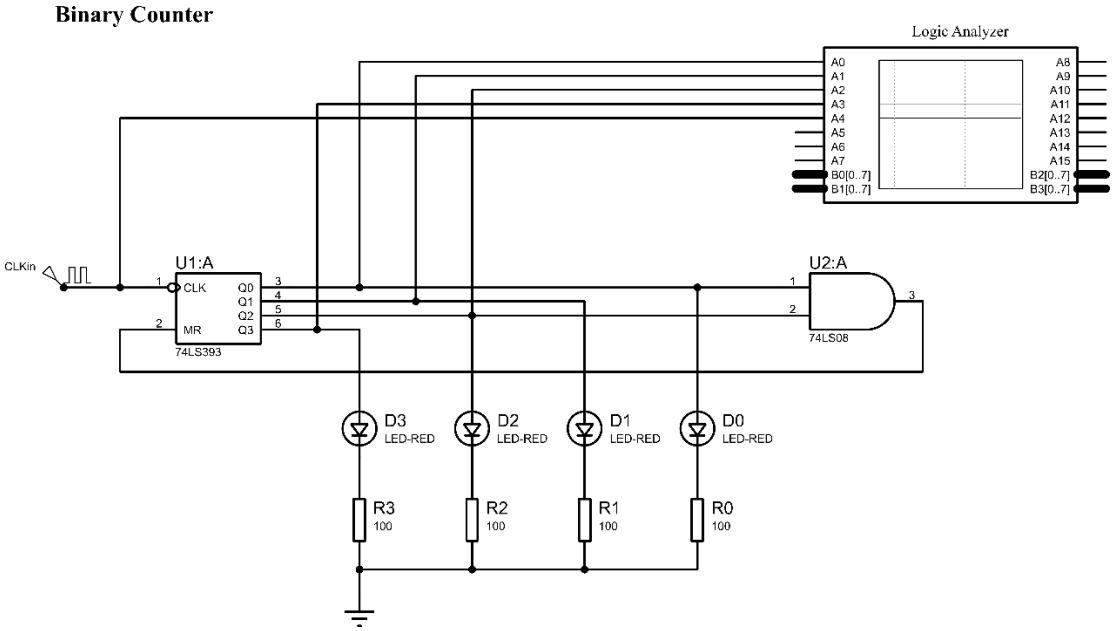


Figure 3. Schematic diagram of a 4-bit binary counter with upper bound circuitry (range from zero to four), it has been made using Proteus VSM.

c. Check the properties of the components you have place in Exercise b and modify their names according to Figure 4.7[1].

- Done in exercise b.

d. Referring to Figure 4.7[1] , wire up the components you have placed in Exercise b.

- Done in exercise b.

e. Referring to Figure 4.14[1], modify your schematic for the counter replacing direct connections with terminals and labeling them appropriately.

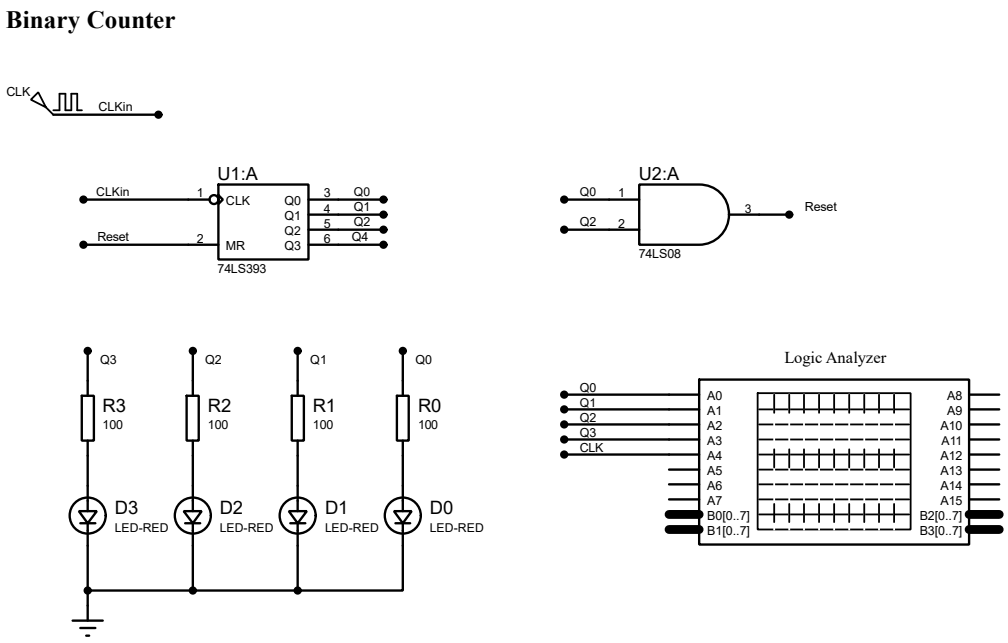
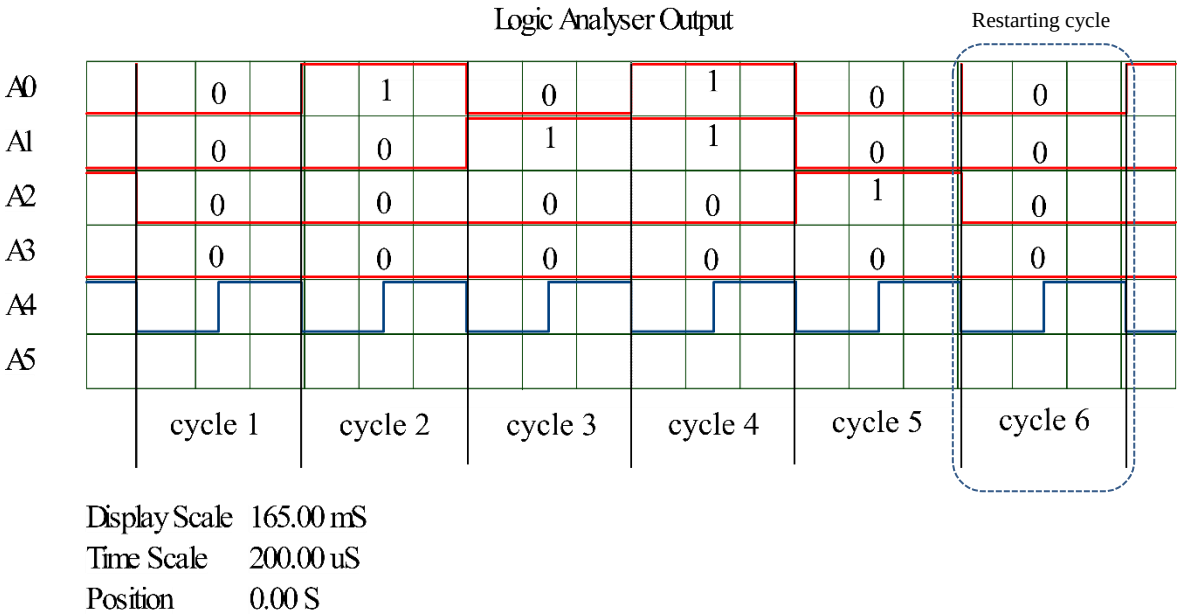


Figure 4. Schematic diagram (labeled wires) of a 4-bit binary counter, note how this diagram offers a clearer lecturing.

[1] Please refers to the document “Laboratory Guidelines – Proteus Virtual System Modeling (VSM)”

Simulation

For both circuits in Figure 3 and Figure 4, a simulation was made using the Proteus Virtual System Modeling. Additionally, a Logic Analyzer was added in order to have a clear perspective about the counting process over time. Note that this integrated circuit (74LS393) inverts the input clock signal for that reason flip-flops detect a rising edge.



2. Control Questions

a. How to create a new project?

Open Proteus 8 CAD Connected. In the File tab, click on New Project. Follow the Wizard instructions.

b. Why do we need the Editing modes?

Editing modes comprises all those tools required to create a schematic diagram, including components, sources and measurement tools that you probably require if you are interested in simulating your circuit.

c. Why do we need the Library?

Library is required to looking for those different components that the schematic is going to draw, e.g., resistors, capacitors, integrated circuits, etc. Additionally, you can see in the library the layout associated in case you are interested in creating a PCB based on your schematic diagram.

d. Why do we need the Properties Window?

Properties windows is mainly used for modifying the values and names of the diagram components. Additional properties such as orientation, alignment, hidden pins are

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encountered here.

e. How many editing modes do you know?

   I have experimented with most of them. Those that I do not know include the 2D Graphics and the Tape Recorder mode. Remaining components have been used for this laboratory practice.

3. Summary

Summarizing, this laboratory work has been mainly for getting experience using Proteus Virtual System Modeling with real examples and simulations. Specifically, a 4-bit binary counter has been simulated and a logic analyzer has been used to gather all the information generated over time. Simulations and expected results were encountered successfully.

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