# **Eccelerators Library IP specification**



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### 1. BusDividerIfc

## 1.1. Bus Divider Interface (BusDividerIfc)

Interface containing a basic Bus Divider block.

#### Table 1.1. Blocks of Bus Divider Interface

Blocks of Bus Divid	er Interface	
Block Address	ID	Block Name
0x000	BusDi- viderBlk	Bus Divider Block

#### Table 1.2. Resets of Bus Divider Interface

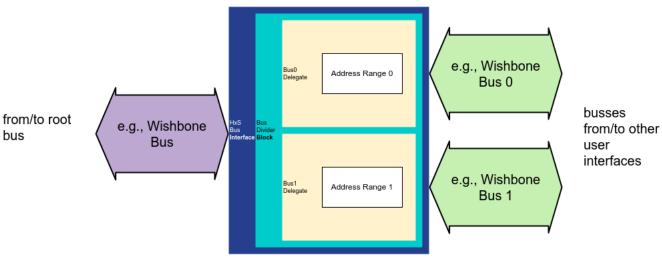
Resets of Registers of	of Bus Divider Interface
ID	Reset Name

### 1.1.1. Bus Divider Block (BusDividerBlk)

This block defines a basic bus divider e.g. to divide a bus into two busses by using HxS delegates.

#### Bus Divider details:

Figure 1.1. Bus Catcher details





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### BusDivider If c

#### Table 1.3. Registers or Delegates of Bus Divider Block

Registers or Delega	Registers or Delegates of Bus Divider Block		
0x000		Bus Divider Block	
0x1ff			
Address	ID	Name	
0x000	BusDele- gate0	Delegated Bus	
0x100	BusDele- gate1	Delegated Bus	

### 1.1.1.1 Delegated Bus (BusDelegate0)

#### Table 1.4. Area of Delegated Bus

Area of Delegated B	dus .
0x000	Delegated Bus (BusDelegate())
0x0ff	

### 1.1.1.2. Delegated Bus (BusDelegate1)

#### Table 1.5. Area of Delegated Bus

Area of Delegated Bus		
0x100	Delegated Bus (BusDelegate1)	
0x1ff		