## **Eccelerators Library IP specification**



### **Table of Contents**

1.	EventCatcherIfc	
	1.1. Interrupt Generator Interface (InterruptGeneratorIfc)	
	1.1.1. Interrupt Generator Block (InterruptGeneratorBlk)	



### **List of Figures**

1.1. Interrupt Generator details	i
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### **List of Tables**

1.1. Blocks of Interrupt Generator Interface	1
1.2. Resets of Interrupt Generator Interface	1
1.3. Registers or Delegates of Interrupt Generator Block	2
1.4. Bits of Control Register	
1.5. Values of ChannelOperation	
1.6. Resets of ChannelOperation	
1.7. Values of ChannelOperation	
1.8. Resets of ChannelOperation	
1.9. Values of ChannelOperation	
1.10. Resets of ChannelOperation	
1.11. Values of ChannelOperation	
1.12. Resets of ChannelOperation	
1.13. Bits of Status Register	
1.14. Values of ChannelStatus	3
1.15. Values of ChannelStatus	4
1.15. Values of ChannelStatus	4
1.16. Values of ChannelStatus	
1.17. Values of ChannelStatus	
1.18. Bits of Charged Count Register	
1.19. Resets of Count	
1.20. Bits of Charged Count Register	
1.21. Resets of Count	
1.22. Bits of Charged Count Register	
1.23. Resets of Count	
1.24. Bits of Charged Count Register	
1.25. Resets of Count	
1.26. Bits of Actual Count Register	
1.27. Bits of Actual Count Register	
1.28. Bits of Actual Count Register	
1.29. Bits of Actual Count Register	
1.30. Bits of Failure Count Register	
1.31. Bits of Failure Count Register	
1.32. Bits of Failure Count Register	
1.33. Bits of Failure Count Register	
1.34. Bits of Interval Register	
1.35. Resets of Interval	
1.36. Bits of Interval Register	
1.37. Resets of Interval	7
1.38. Bits of Interval Register	7
1.39. Resets of Interval	7
1.40. Bits of Interval Register	7
1.41. Resets of Interval	7
1.42. Bits of Reference Count Register	
1.43. Resets of Count	
1.44. Bits of Reference Count Register	
1.45. Resets of Count	
1.46. Bits of Reference Count Register	
1.47. Resets of Count	
1.48. Bits of Reference Count Register	
1.49. Resets of Count	



### 1. EventCatcherIfc

# 1.1. Interrupt Generator Interface (InterruptGeneratorIfc)

Interface containing a basic Interrupt Generator block as predictable source and execurion check for interrupt simulation.

#### Table 1.1. Blocks of Interrupt Generator Interface

Blocks of Interrupt Generator Interface								
Block Address	ID	Block Name						
0x00	InterruptGeneratorBlk	Interrupt Generator Block						

#### Table 1.2. Resets of Interrupt Generator Interface

Resets of Registers of	of Registers of Interrupt Generator Interface						
ID	Reset Name						

### 1.1.1. Interrupt Generator Block (InterruptGeneratorBlk)

This block defines a basic Interrupt Generator block as predictable source and execution check for interrupt simulation. It provides 4 channels to generate 4 interrupt sources.

#### Constraints:

- 1. Generate interrupts at a configurable rate for level triggered interrupt destinations.
- 2. Check if interrupts are executed in time.
- 3. Provide a failure output.

Interrupt Generator details:



Figure 1.1. Interrupt Generator details Generator e.g., Wishbone Bus Clk . Areset signals HxS Bus clock from clock and reset generator from/to user Reset e.g., ASync Bus Reset from clock and reset generator block eccelerators

Table 1.3. Registers or Delegates of Interrupt Generator Block

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Registers or Delegates of Interrupt Generator Block									
	Interrupt Generator Block								
ID	Name								
ControlReg	Control Register								
StatusReg	Status Register								
ChargedCountReg	Charged Count Register								
ChargedCountReg	Charged Count Register								
ChargedCountReg	Charged Count Register								
ChargedCountReg	Charged Count Register								
ActualCountReg	Actual Count Register								
ActualCountReg	<u>Actual Count Register</u>								
I ( )	D ControlReg StatusReg ChargedCountReg ChargedCountReg ChargedCountReg ChargedCountReg ActualCountReg								



0x18	ActualCountReg	Actual Count Register
0x1c	ActualCountReg	Actual Count Register
0x20	FailureCountReg	Failure Count Register
0x24	FailureCountReg	Failure Count Register
0x28	FailureCountReg	Failure Count Register
0x2c	FailureCountReg	Failure Count Register
0x30	IntervalReg	Interval Register
0x34	IntervalReg	Interval Register
0x38	IntervalReg	Interval Register
0x3c	IntervalReg	Interval Register
0x40	ReferenceCoun- tReg	Reference Count Register
0x44	ReferenceCoun- tReg	Reference Count Register
0x48	ReferenceCoun- tReg	Reference Count Register
0x4c	ReferenceCoun- tReg	Reference Count Register

### 1.1.1.1. Control Register (ControlReg)

#### Table 1.4. Bits of Control Register

Table	able 1.4. Bits of Control Register												
Bits o	f Control Register												
0x00													
Bits	ID	Type	Description	escription									
3	ChannelOperation	RW	Table 1.5. Values of	le 1.5. Values of ChannelOperation									
			Value	ID	Type	Descr	iption						
			0x1	Enabled	R	An In	terrupt is pending.						
			0x0	Disabled	R	An In	terrupt is not pending.						
			Table 1.6. Resets of	ChannelOpe	ration								
			0x0	BusReset		RW	Default Bus Reset						
2	ChannelOperation	RW	Table 1.7. Values of	ChannelOpe	eration								
			Value	ID	Туре	Descr	iption						
			0x1	Enabled	R	An In	terrupt is pending.						
			0×0	Disabled	R	An In	terrupt is not pending.						
Table 1.8. Resets of ChannelOperation													
			0×0	BusReset		RW	Default Bus Reset						
1	ChannelOperation	RW	Table 1.9. Values of	ble 1.9. Values of ChannelOperation									
			Value	ID	Type	Descr	iption						
			0x1	Enabled	R	An In	terrupt is pending.						
			0×0	Disabled	R	An In	terrupt is not pending.						
			Table 1.10. Resets of	f ChannelOp	eration								
			0x0 BusReset RW Default Bus Reset										
0	ChannelOperation	RW	Table 1.11. Values o	Table 1.11. Values of ChannelOperation									
			Value	ID	Туре	Descr	iption						
			0x1	Enabled	R	An In	terrupt is pending.						
			0x0	Disabled	R	An In	terrupt is not pending.						
			Table 1.12. Resets of	f ChannelOp	eration								
			0×0	BusReset		RW	Default Bus Reset						
1	1	1											

### 1.1.1.2. Status Register (StatusReg)

Table 1.13. Bits of Status Register

Bits of Status Register



0x00			Status Register (StatusReg).								
Bits	ID	Туре	Description	cription							
7	ChannelStatus	R	Table 1.14. Values of	able 1.14. Values of ChannelStatus							
			Value	ID	Type	Description					
6			0ь00	Idle	R	An Interrupt is pending.					
			0b01	Operating	R	An Interrupt is not pending.					
			0b1*	Ended	R	An Interrupt is not pending.					
5	ChannelStatus	R	Table 1.15. Values of	f ChannelSta	ntus						
			Value	ID	Туре	Description					
4			0600	Idle	R	An Interrupt is pending.					
		0b01 Operating		R	An Interrupt is not pending.						
			0b1*	Ended	R	An Interrupt is not pending.					
3	ChannelStatus	R	Table 1.16. Values of	Table 1.16. Values of ChannelStatus							
			Value	ID	Type	Description					
2			0ь00	Idle	R	An Interrupt is pending.					
			0b01	Operating	R	An Interrupt is not pending.					
			0b1*	Ended	R	An Interrupt is not pending.					
1	ChannelStatus	R	Table 1.17. Values of ChannelStatus								
			Value ID Type Description								
			<u> </u>		_	· ·					
0			0b00 Idle R An Interrupt is pending.								
			0b01	Operating	R	An Interrupt is not pending.					
			0b1*	Ended	R	An Interrupt is not pending.					

### 1.1.1.3. Charged Count Register (ChargedCountReg)

#### Table 1.18. Bits of Charged Count Register

Bits of	Bits of Charged Count Register										
0x00	Charged Count Register (ChargedCountReg)										
Bits	ID	Туре	Description	scription							
31	Count	RW	Number of interrupts	umber of interrupts to be generated and expected to be handled by SW.							
			Table 1.19. Resets of	ble 1.19. Resets of Count							
00			0x0000.0000	00.0000 BusReset RW Default Bus Reset							

### 1.1.1.4. Charged Count Register (ChargedCountReg)

#### Table 1.20. Bits of Charged Count Register

Bits o	its of Charged Count Register											
0x04 Charged Count Register (ChargedCountReg)												
Bits	ID	Туре	Description	scription								
31	Count	RW	Number of interrupts	umber of interrupts to be generated and expected to be handled by SW.								
			Table 1.21. Resets of	ble 1.21. Resets of Count								
00			0x0000.0000	x0000.0000 BusReset RW Default Bus Reset								

### 1.1.1.5. Charged Count Register (ChargedCountReg)

#### Table 1.22. Bits of Charged Count Register

Bits o	Sits of Charged Count Register									
0x08			Charged Count Register (ChargedCountReg)							
Bits	s ID Type De		Description							
31	Count RW		Number of interrupts to be generated and expected to be handled by SW.							
00										



	Table 1.23. Resets of Count				
	0x0000.0000	BusReset	RW	Default Bus Reset	

#### 1.1.1.6. Charged Count Register (ChargedCountReg)

#### Table 1.24. Bits of Charged Count Register

Bits of	Bits of Charged Count Register									
0x0c	0x0c Charged Count Register (ChargedCountReg)									
Bits	ID	Туре	Description	escription						
31	Count	RW	Number of interrupts	Number of interrupts to be generated and expected to be handled by SW.						
			Table 1.25. Resets of	able 1.25. Resets of Count						
00			0x0000.0000	BusReset	RW	Default Bus Reset				

### 1.1.1.7. Actual Count Register (ActualCountReg)

#### Table 1.26. Bits of Actual Count Register

Bits o	Sits of Actual Count Register							
0x10	0x10		Actual Count Register (ActualCountReg)					
Bits	ID	Type	Description					
31	Count	R	tual count of interrupts already generated.					
00								

### 1.1.1.8. Actual Count Register (ActualCountReg)

#### Table 1.27. Bits of Actual Count Register

Bits of	Bits of Actual Count Register							
0x14			Actual Count Register (ActualCountReg)					
Bits	its ID Type		Description					
31	Count	R	Actual count of interrupts already generated.					
00								

#### 1.1.1.9. Actual Count Register (ActualCountReg)

#### Table 1.28. Bits of Actual Count Register

Bits o	Bits of Actual Count Register							
0x18			Actual Count Register (ActualCountReg)					
Bits	ID Type		Description					
31	Count	R	Actual count of interrupts already generated.					
00								

### 1.1.1.10. Actual Count Register (ActualCountReg)

#### Table 1.29. Bits of Actual Count Register

Bits of Actual Count Register						
0x1c			Actual Count Register (ActualCountReg)			
Bits	ts ID Type		Description			
31	l Count R		Actual count of interrupts already generated.			



### 1.1.1.11. Failure Count Register (FailureCountReg)

#### Table 1.30. Bits of Failure Count Register

Bits of	kits of Failure Count Register							
0x20	0x20		Failure Count Register (FailureCountReg)					
Bits	ID	Type	Description					
31	Count	R	Failure count of missed interrupts.					
00								

### 1.1.1.12. Failure Count Register (FailureCountReg)

#### Table 1.31. Bits of Failure Count Register

Bits of	Bits of Failure Count Register							
0x24			Failure Count Register (FailureCountReg)					
Bits	s ID Type		Description					
31	Count R		Failure count of missed interrupts.					
00								

### 1.1.1.13. Failure Count Register (FailureCountReg)

#### Table 1.32. Bits of Failure Count Register

Bits of	Bits of Failure Count Register								
0x28			Failure Count Register (FailureCountReg)						
Bits	ID	Type	Description						
31	Count	R	Failure count of missed interrupts.						
00									

### 1.1.1.14. Failure Count Register (FailureCountReg)

#### Table 1.33. Bits of Failure Count Register

Bits of	Bits of Failure Count Register							
0x2c			Failure Count Register (FailureCountReg)					
Bits	ID	Type	Description					
31	Count	R	Failure count of missed interrupts.					
00								

### 1.1.1.15. Interval Register (IntervalReg)

#### Table 1.34. Bits of Interval Register

Bits o	Sits of Interval Register							
0x30			Interval Register (IntervalReg)					
Bits	ID	Type	Description					
31	Interval	RW	Interval of generated interrupt in nanaoseconds.					
00								



	0x0000.0000	BusReset	RW	Default Bus Reset	

### 1.1.1.16. Interval Register (IntervalReg)

#### Table 1.36. Bits of Interval Register

Bits o	s of Interval Register									
0x34	4 Interval Register (IntervalReg)									
Bits	ID	Type	Description	escription						
31	Interval	RW	Interval of generated	Interval of generated interrupt in nanaoseconds.						
			Table 1.37. Resets of	Fable 1.37. Resets of Interval						
00			0x0000.0000 BusReset RW Default Bus Reset							

### 1.1.1.17. Interval Register (IntervalReg)

#### Table 1.38. Bits of Interval Register

Bits o	ts of Interval Register									
0x38	x38 Interval Register (IntervalReg)									
Bits	ID	Type	Description	escription						
31	Interval	RW	Interval of generated	interval of generated interrupt in nanaoseconds.						
			Table 1.39. Resets of	Table 1.39. Resets of Interval						
00			0x0000.0000	BusReset	RW	Default Bus Reset				

#### 1.1.1.18. Interval Register (IntervalReg)

#### Table 1.40. Bits of Interval Register

Bits of	Sits of Interval Register									
0x3c	3c Interval Register (IntervalReg)									
Bits	ID	Type	Description	escription						
31	Interval	RW	Interval of generated	Interval of generated interrupt in nanaoseconds.						
			Table 1.41. Resets of	Table 1.41. Resets of Interval						
00	00 0x0000.0000 BusReset RW Default Bus Reset									

### 1.1.1.19. Reference Count Register (ReferenceCountReg)

#### Table 1.42. Bits of Reference Count Register

Bits of	s of Reference Count Register									
0x40	x40 Reference Count Register (ReferenceCountReg)									
Bits	ID	Type	Description	Pescription						
31	Count	RW	Reference count written by SW to acknowledge a processed interrupt.							
			Table 1.43. Resets of	Fable 1.43. Resets of Count						
00			0x0000.0000	BusReset	RW	Default Bus Reset				

### 1.1.1.20. Reference Count Register (ReferenceCountReg)

#### Table 1.44. Bits of Reference Count Register

Bits o	its of Reference Count Register									
0x44 Reference Count Register (ReferenceCountReg)										
Bits	ID	Type	escription							
31	Count	RW	eference count written by SW to acknowledge a processed interrupt.							
00										



		Table 1.45. Resets of Count					
		0x0000.0000	BusReset	RW	Default Bus Reset		

### 1.1.1.21. Reference Count Register (ReferenceCountReg)

#### Table 1.46. Bits of Reference Count Register

Bits o	its of Reference Count Register									
0x48	x48 Reference Count Register (ReferenceCountReg)									
Bits	ID	Type	Description	escription						
31	Count	RW	Reference count writt	Reference count written by SW to acknowledge a processed interrupt.						
			Table 1.47. Resets of	Γable 1.47. Resets of Count						
00 0x0000.0000 BusReset RW Default Bus Reset					Default Bus Reset					

### 1.1.1.22. Reference Count Register (ReferenceCountReg)

#### Table 1.48. Bits of Reference Count Register

its of Reference Count Register									
0x4c Reference Count Register (ReferenceCountReg)									
ID	Туре	Description	escription						
Count	RW	Reference count writt	Reference count written by SW to acknowledge a processed interrupt.						
		Table 1.49. Resets of	able 1.49. Resets of Count						
		0x0000.0000	BusReset	RW	Default Bus Reset				
	ID	ID Type Count RW	Reference Count Reg	Reference Count Register (ReferenceCount    ID	Reference Count Register (ReferenceCountReg)				