

Eccelerators Library IP specification

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1. EventCatcherIfc

1.1. Interrupt Generator Interface (InterruptGeneratorIfc)

Interface containing a basic Interrupt Generator block as predictable source and execution check for interrupt simulation.

Table 1.1. Blocks of Interrupt Generator Interface

Blocks of Interrupt Generator Interface		
Block Address	ID	Block Name
0x00	InterruptGeneratorBlk	Interrupt Generator Block

Table 1.2. Resets of Interrupt Generator Interface

Resets of Registers of Interrupt Generator Interface	
ID	Reset Name

1.1.1. Interrupt Generator Block (InterruptGeneratorBlk)

This block defines a basic Interrupt Generator block as predictable source and execution check for interrupt simulation. It provides 4 channels to generate 4 interrupt sources.

Constraints:

1. Generate interrupts at a configurable rate for level triggered interrupt destinations.
2. Check if interrupts are executed in time.
3. Provide a failure output.

Interrupt Generator details:

Figure 1.1. Interrupt Generator details

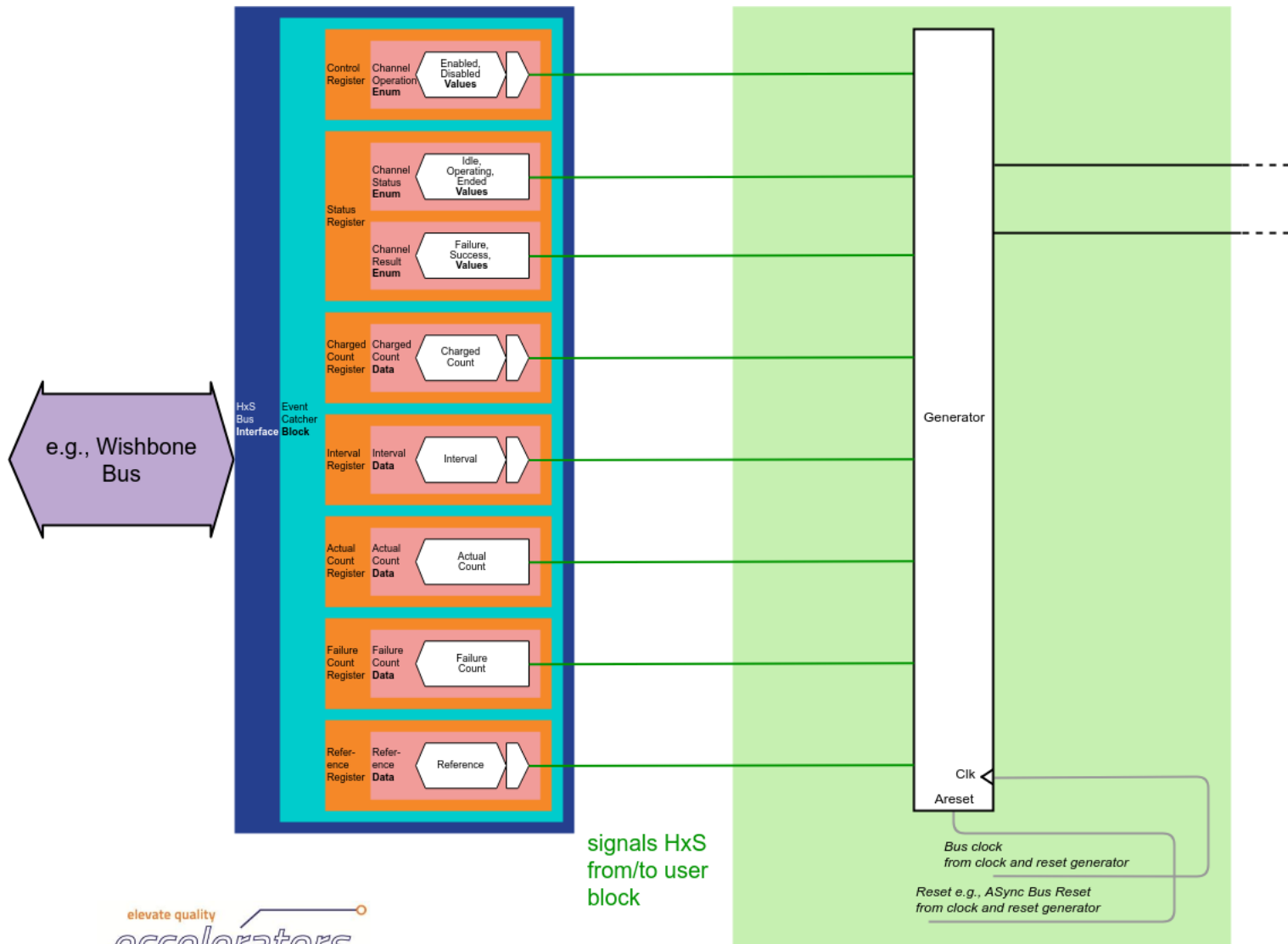


Table 1.3. Registers or Delegates of Interrupt Generator Block

Registers or Delegates of Interrupt Generator Block		
0x00		Interrupt Generator Block
...		
0x53		
Address	ID	Name
0x00	ControlReg	Control Register
0x00	StatusReg	Status Register
0x00	ChargedCountReg	Charged Count Register
0x04	ChargedCountReg	Charged Count Register
0x08	ChargedCountReg	Charged Count Register
0x0c	ChargedCountReg	Charged Count Register
0x10	ActualCountReg	Actual Count Register
0x14	ActualCountReg	Actual Count Register

0x18	ActualCountReg	Actual Count Register
0x1c	ActualCountReg	Actual Count Register
0x20	FailureCountReg	Failure Count Register
0x24	FailureCountReg	Failure Count Register
0x28	FailureCountReg	Failure Count Register
0x2c	FailureCountReg	Failure Count Register
0x30	IntervalReg	Interval Register
0x34	IntervalReg	Interval Register
0x38	IntervalReg	Interval Register
0x3c	IntervalReg	Interval Register
0x40	ReferenceCountReg	Reference Count Register
0x44	ReferenceCountReg	Reference Count Register
0x48	ReferenceCountReg	Reference Count Register
0x4c	ReferenceCountReg	Reference Count Register

1.1.1.1. Control Register (ControlReg)

Table 1.4. Bits of Control Register

Bits of Control Register						
0x00			Control Register (ControlReg)			
Bits	ID	Type	Description			
3	ChannelOperation	RW	Table 1.5. Values of ChannelOperation			
			Value	ID	Type	Description
			0x0	Disabled	R	An Interrupt is not pending.
			0x1	Enabled	R	An Interrupt is pending.
			Table 1.6. Resets of ChannelOperation			
0x0	BusReset	RW	Default Bus Reset			
2	ChannelOperation	RW	Table 1.7. Values of ChannelOperation			
			Value	ID	Type	Description
			0x0	Disabled	R	An Interrupt is not pending.
			0x1	Enabled	R	An Interrupt is pending.
			Table 1.8. Resets of ChannelOperation			
0x0	BusReset	RW	Default Bus Reset			
1	ChannelOperation	RW	Table 1.9. Values of ChannelOperation			
			Value	ID	Type	Description
			0x0	Disabled	R	An Interrupt is not pending.
			0x1	Enabled	R	An Interrupt is pending.
			Table 1.10. Resets of ChannelOperation			
0x0	BusReset	RW	Default Bus Reset			
0	ChannelOperation	RW	Table 1.11. Values of ChannelOperation			
			Value	ID	Type	Description
			0x0	Disabled	R	An Interrupt is not pending.
			0x1	Enabled	R	An Interrupt is pending.
			Table 1.12. Resets of ChannelOperation			
0x0	BusReset	RW	Default Bus Reset			

1.1.1.2. Status Register (StatusReg)

Table 1.13. Bits of Status Register

Bits of Status Register			
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0x00			Status Register (StatusReg)
Bits	ID	Type	Description
7	ChannelStatus	R	Table 1.14. Values of ChannelStatus
..			Value ID Type Description
6			0b00 Idle R An Interrupt is pending.
			0b01 Operating R An Interrupt is not pending.
			0b1 * Ended R An Interrupt is not pending.
5	ChannelStatus	R	Table 1.15. Values of ChannelStatus
..			Value ID Type Description
4			0b00 Idle R An Interrupt is pending.
			0b01 Operating R An Interrupt is not pending.
			0b1 * Ended R An Interrupt is not pending.
3	ChannelStatus	R	Table 1.16. Values of ChannelStatus
..			Value ID Type Description
2			0b00 Idle R An Interrupt is pending.
			0b01 Operating R An Interrupt is not pending.
			0b1 * Ended R An Interrupt is not pending.
1	ChannelStatus	R	Table 1.17. Values of ChannelStatus
..			Value ID Type Description
0			0b00 Idle R An Interrupt is pending.
			0b01 Operating R An Interrupt is not pending.
			0b1 * Ended R An Interrupt is not pending.

1.1.1.3. Charged Count Register (ChargedCountReg)

Table 1.18. Bits of Charged Count Register

Bits of Charged Count Register			Charged Count Register (ChargedCountReg)
0x00			
Bits	ID	Type	Description
31	Count	RW	Number of interrupts to be generated and expected to be handled by SW.
..			Table 1.19. Resets of Count
00			0x0000 . 0000 BusReset RW Default Bus Reset

1.1.1.4. Charged Count Register (ChargedCountReg)

Table 1.20. Bits of Charged Count Register

Bits of Charged Count Register			Charged Count Register (ChargedCountReg)
0x04			
Bits	ID	Type	Description
31	Count	RW	Number of interrupts to be generated and expected to be handled by SW.
..			Table 1.21. Resets of Count
00			0x0000 . 0000 BusReset RW Default Bus Reset

1.1.1.5. Charged Count Register (ChargedCountReg)

Table 1.22. Bits of Charged Count Register

Bits of Charged Count Register			Charged Count Register (ChargedCountReg)
0x08			
Bits	ID	Type	Description
31	Count	RW	Number of interrupts to be generated and expected to be handled by SW.
..			
00			

Table 1.23. Resets of Count

0x0000, 0000	BusReset	RW	Default Bus Reset
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1.1.1.6. Charged Count Register (ChargedCountReg)

Table 1.24. Bits of Charged Count Register

Bits of Charged Count Register			
0x0c		Charged Count Register (ChargedCountReg)	
Bits	ID	Type	Description
31	Count	RW	Number of interrupts to be generated and expected to be handled by SW.
..			
00			

Table 1.25. Resets of Count

0x0000, 0000	BusReset	RW	Default Bus Reset
--------------	----------	----	-------------------

1.1.1.7. Actual Count Register (ActualCountReg)

Table 1.26. Bits of Actual Count Register

Bits of Actual Count Register			
0x10		Actual Count Register (ActualCountReg)	
Bits	ID	Type	Description
31	Count	R	Actual count of interrupts already generated.
..			
00			

1.1.1.8. Actual Count Register (ActualCountReg)

Table 1.27. Bits of Actual Count Register

Bits of Actual Count Register			
0x14		Actual Count Register (ActualCountReg)	
Bits	ID	Type	Description
31	Count	R	Actual count of interrupts already generated.
..			
00			

1.1.1.9. Actual Count Register (ActualCountReg)

Table 1.28. Bits of Actual Count Register

Bits of Actual Count Register			
0x18		Actual Count Register (ActualCountReg)	
Bits	ID	Type	Description
31	Count	R	Actual count of interrupts already generated.
..			
00			

1.1.1.10. Actual Count Register (ActualCountReg)

Table 1.29. Bits of Actual Count Register

Bits of Actual Count Register			
0x1c		Actual Count Register (ActualCountReg)	
Bits	ID	Type	Description
31	Count	R	Actual count of interrupts already generated.
..			

00			
----	--	--	--

1.1.1.11. Failure Count Register (FailureCountReg)

Table 1.30. Bits of Failure Count Register

Bits of Failure Count Register			
0x20		Failure Count Register (FailureCountReg)	
Bits	ID	Type	Description
31	Count	R	Failure count of missed interrupts.
..			
00			

1.1.1.12. Failure Count Register (FailureCountReg)

Table 1.31. Bits of Failure Count Register

Bits of Failure Count Register			
0x24		Failure Count Register (FailureCountReg)	
Bits	ID	Type	Description
31	Count	R	Failure count of missed interrupts.
..			
00			

1.1.1.13. Failure Count Register (FailureCountReg)

Table 1.32. Bits of Failure Count Register

Bits of Failure Count Register			
0x28		Failure Count Register (FailureCountReg)	
Bits	ID	Type	Description
31	Count	R	Failure count of missed interrupts.
..			
00			

1.1.1.14. Failure Count Register (FailureCountReg)

Table 1.33. Bits of Failure Count Register

Bits of Failure Count Register			
0x2c		Failure Count Register (FailureCountReg)	
Bits	ID	Type	Description
31	Count	R	Failure count of missed interrupts.
..			
00			

1.1.1.15. Interval Register (IntervalReg)

Table 1.34. Bits of Interval Register

Bits of Interval Register			
0x30		Interval Register (IntervalReg)	
Bits	ID	Type	Description
31	Interval	RW	Interval of generated interrupt in nanoseconds.
..			
00			

Table 1.35. Resets of Interval

0x0000.0000	BusReset	RW	Default Bus Reset
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1.1.1.16. Interval Register (IntervalReg)

Table 1.36. Bits of Interval Register

Bits of Interval Register							
0x34			Interval Register (IntervalReg)				
Bits	ID	Type	Description				
31	Interval	RW	Interval of generated interrupt in nanaoseconds.				
..			Table 1.37. Resets of Interval				
00			<table><tr><td>0x0000.0000</td><td>BusReset</td><td>RW</td><td>Default Bus Reset</td></tr></table>			0x0000.0000	BusReset
0x0000.0000	BusReset	RW	Default Bus Reset				

1.1.1.17. Interval Register (IntervalReg)

Table 1.38. Bits of Interval Register

Bits of Interval Register						
0x38			Interval Register (IntervalReg)			
Bits	ID	Type	Description			
31	Interval	RW	Interval of generated interrupt in nanaoseconds.			
..			Table 1.39. Resets of Interval			
00			<table><tr><td>0x0000.0000</td><td>BusReset</td><td>RW</td><td>Default Bus Reset</td></tr></table>		0x0000.0000	BusReset
0x0000.0000	BusReset	RW	Default Bus Reset			

1.1.1.18. Interval Register (IntervalReg)

Table 1.40. Bits of Interval Register

Bits of Interval Register						
0x3c			Interval Register (IntervalReg)			
Bits	ID	Type	Description			
31	Interval	RW	Interval of generated interrupt in nanoseconds.			
..			Table 1.41. Resets of Interval			
00			<table><tr><td>0x0000.0000</td><td>BusReset</td><td>RW</td><td>Default Bus Reset</td></tr></table>		0x0000.0000	BusReset
0x0000.0000	BusReset	RW	Default Bus Reset			

1.1.1.19. Reference Count Register (ReferenceCountReg)

Table 1.42. Bits of Reference Count Register

Bits of Reference Count Register						
0x40			Reference Count Register (ReferenceCountReg)			
Bits	ID	Type	Description			
31	Count	RW	Reference count written by SW to acknowledge a processed interrupt.			
..			Table 1.43. Resets of Count			
00			<table><tr><td>0x0000.0000</td><td>BusReset</td><td>RW</td><td>Default Bus Reset</td></tr></table>		0x0000.0000	BusReset
0x0000.0000	BusReset	RW	Default Bus Reset			

1.1.1.20. Reference Count Register (ReferenceCountReg)

Table 1.44. Bits of Reference Count Register

Bits of Reference Count Register			
0x44		Reference Count Register (ReferenceCountReg)	
Bits	ID	Type	Description
31	Count	RW	Reference count written by SW to acknowledge a processed interrupt.
..			
00			

Table 1.45. Resets of Count

0x0000 . 0000	BusReset	RW	Default Bus Reset
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1.1.1.21. Reference Count Register (ReferenceCountReg)

Table 1.46. Bits of Reference Count Register

Bits of Reference Count Register					
0x48		Reference Count Register (ReferenceCountReg)			
Bits	ID	Type	Description		
31	Count	RW	Reference count written by SW to acknowledge a processed interrupt.		
..			Table 1.47. Resets of Count		
00			<table> <tr> <td>0x0000 . 0000</td><td>BusReset</td><td>RW</td><td>Default Bus Reset</td></tr> </table>	0x0000 . 0000	BusReset
0x0000 . 0000	BusReset	RW	Default Bus Reset		

1.1.1.22. Reference Count Register (ReferenceCountReg)

Table 1.48. Bits of Reference Count Register

Bits of Reference Count Register					
0x4c		Reference Count Register (ReferenceCountReg)			
Bits	ID	Type	Description		
31	Count	RW	Reference count written by SW to acknowledge a processed interrupt.		
..			Table 1.49. Resets of Count		
00			<table> <tr> <td>0x0000 . 0000</td><td>BusReset</td><td>RW</td><td>Default Bus Reset</td></tr> </table>	0x0000 . 0000	BusReset
0x0000 . 0000	BusReset	RW	Default Bus Reset		