Eccelerators Library IP specification



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1. EventCatcherIfc

1.1. Interrupt Generator Interface (InterruptGeneratorIfc)

Interface containing a basic Interrupt Generator block as predictable source and execurion check for interrupt simulation.

Table 1.1. Blocks of Interrupt Generator Interface

Blocks of Interrupt Generator Interface								
Block Address	ID	Block Name						
0x00	InterruptGeneratorBlk	Interrupt Generator Block						

Table 1.2. Resets of Interrupt Generator Interface

Resets of Registers of	of Registers of Interrupt Generator Interface								
ID	Reset Name								

1.1.1. Interrupt Generator Block (InterruptGeneratorBlk)

This block defines a basic Interrupt Generator block as predictable source and execution check for interrupt simulation. It provides 4 channels to generate 4 interrupt sources.

Constraints:

- 1. Generate interrupts at a configurable rate for level triggered interrupt destinations.
- 2. Check if interrupts are executed in time.
- 3. Provide a failure output.

Interrupt Generator details:



Figure 1.1. Interrupt Generator details Generator e.g., Wishbone Bus Clk . Areset signals HxS Bus clock from clock and reset generator from/to user Reset e.g., ASync Bus Reset from clock and reset generator block eccelerators

Table 1.3. Registers or Delegates of Interrupt Generator Block

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Registers or Delegates of Interrupt Generator Block										
	nterrupt Generator Block									
	Name									
rolReg	Control Register									
sReg	Status Register									
gedCountReg	Charged Count Register									
gedCountReg	Charged Count Register									
gedCountReg	Charged Count Register									
gedCountReg	Charged Count Register									
alCountReg	Actual Count Register									
alCountReg	Actual Count Register									
sR geo	Reg leg dCountReg dCountReg dCountReg dCountReg dCountReg									



0x19	ActualCountReg	Actual Count Register
0x1d	ActualCountReg	Actual Count Register
0x21	FailureCountReg	Failure Count Register
0x25	FailureCountReg	Failure Count Register
0x29	FailureCountReg	Failure Count Register
0x2d	FailureCountReg	Failure Count Register
0x31	IntervalReg	Interval Register
0x35	IntervalReg	Interval Register
0x39	IntervalReg	Interval Register
0x3d	IntervalReg	Interval Register
0x41	ReferenceCoun- tReg	Reference Count Register
0x45	ReferenceCoun- tReg	Reference Count Register
0x49	ReferenceCoun- tReg	Reference Count Register
0x4d	ReferenceCoun- tReg	Reference Count Register

1.1.1.1. Control Register (ControlReg)

Table 1.4. Bits of Control Register

Table 1	ble 1.4. Bits of Control Register										
Bits o	Bits of Control Register										
0x00											
Bits	ID	Туре	Description	scription							
3	ChannelOperation	RW	Table 1.5. Values of ChannelOperation								
			Value	ID	Type	Descrip	ption				
			0x0	Disabled	R	An Inte	errupt is not pending.				
			0x1	Enabled	R	An Inte	errupt is pending.				
			Table 1.6. Resets of	ChannelOpe	ration						
			0x0	BusReset		RW	Default Bus Reset				
2	ChannelOperation	RW	Table 1.7. Values of	ChannelOp	eration						
			Value	ID	Туре	Descrip	ption				
			0×0	Disabled	R	An Inte	errupt is not pending.				
			0x1	Enabled	R	An Inte	errupt is pending.				
			Table 1.8. Resets of	ChannelOpe	eration						
			0x0	BusReset		RW	Default Bus Reset				
1	ChannelOperation	RW	Table 1.9. Values of ChannelOperation								
			Value ID Type Description				ption				
			0×0	Disabled R An Interrupt is not pending.		An Inte	errupt is not pending.				
			0x1	Enabled	bled R An Interrupt is pending.		errupt is pending.				
Table 1.10. Resets of ChannelOperation											
			0x0	Default Bus Reset							
0	ChannelOperation	RW	Table 1.11. Values of ChannelOperation								
			Value	ID	Туре	Descrip	ption				
			0x0	Disabled	R	An Inte	errupt is not pending.				
			0x1	Enabled	R	An Inte	errupt is pending.				
			Table 1.12. Resets of	f ChannelOp	eration						
			0x0	BusReset		RW	Default Bus Reset				
1	1	1	1.								

1.1.1.2. Status Register (StatusReg)

Table 1.13. Bits of Status Register

Bits of Status Register



0x00			Status Register (StatusReg)							
Bits	ID	Type	Description	escription						
7	ChannelStatus	R	Table 1.14. Values of	Table 1.14. Values of ChannelStatus						
			Value	ID	Туре	Description				
6			0b00	Idle	R	An Interrupt is pending.				
			0b01	Operating	R	An Interrupt is not pending.				
			0b1*	Ended	R	An Interrupt is not pending.				
5	ChannelStatus	R	Table 1.15. Values of	f ChannelSta	ntus					
			Value	ID	Туре	Description				
4			0b00	Idle	R	An Interrupt is pending.				
			0b01	Operating	R	An Interrupt is not pending.				
			0b1*	Ended	R	An Interrupt is not pending.				
	G1 10 1	n	m 11 446 F1 1	le 1.16. Values of ChannelStatus						
3	ChannelStatus	R		ChannelSta	itus					
			Value	ID	Type	Description				
2			0b00	Idle	R	An Interrupt is pending.				
			0b01	Operating	R	An Interrupt is not pending.				
			0b1*	Ended	R	An Interrupt is not pending.				
1	ChannelStatus R Table 1.17. Values of ChannelStatus									
			Value	ID	Туре	Description				
0			0b00	Idle	R	An Interrupt is pending.				
			0b01	Operating	R	An Interrupt is not pending.				
			0b1*	Ended	R	An Interrupt is not pending.				

1.1.1.3. Charged Count Register (ChargedCountReg)

Table 1.18. Bits of Charged Count Register

Bits of	Bits of Charged Count Register											
0x01	Charged Count Register (ChargedCountReg)											
Bits	ID	Туре	Description	scription								
31	Count	RW	Number of interrupts	umber of interrupts to be generated and expected to be handled by SW.								
			Table 1.19. Resets of	ble 1.19. Resets of Count								
00			0x0000.0000	00.0000 BusReset RW Default Bus Reset								

1.1.1.4. Charged Count Register (ChargedCountReg)

Table 1.20. Bits of Charged Count Register

	130 Jan V. Changet Colla Regard											
Bits of	Bits of Charged Count Register											
0x05	x05 Charged Count Register (ChargedCountReg)											
Bits	ID	Туре	Description	ription								
31	Count	RW	Number of interrupts	nber of interrupts to be generated and expected to be handled by SW.								
			Table 1.21. Resets of	ole 1.21. Resets of Count								
00			0x0000.0000	.0000 BusReset RW Default Bus Reset								

1.1.1.5. Charged Count Register (ChargedCountReg)

Table 1.22. Bits of Charged Count Register

Bits o	Sits of Charged Count Register									
0x09			Charged Count Register (ChargedCountReg)							
Bits	ID	Type	Description							
31	Count	RW	Number of interrupts to be generated and expected to be handled by SW.							
00										



	Table 1.23. Resets of Count				
	0x0000.0000	BusReset	RW	Default Bus Reset	

1.1.1.6. Charged Count Register (ChargedCountReg)

Table 1.24. Bits of Charged Count Register

Bits o	Bits of Charged Count Register								
0x0d Charged Count Register (ChargedCountReg)									
Bits	ID	Туре	Description	scription					
31	Count	RW	Number of interrupts	Sumber of interrupts to be generated and expected to be handled by SW.					
			Table 1.25. Resets of	able 1.25. Resets of Count					
00			0x0000.0000	BusReset	RW	Default Bus Reset			

1.1.1.7. Actual Count Register (ActualCountReg)

Table 1.26. Bits of Actual Count Register

Bits o	Sits of Actual Count Register								
0x11	0x11		Actual Count Register (ActualCountReg)						
Bits	ID	Type	Description						
31	Count	R	ctual count of interrupts already generated.						
00									

1.1.1.8. Actual Count Register (ActualCountReg)

Table 1.27. Bits of Actual Count Register

Bits of	Actual Count Registe	r						
0x15			Actual Count Register (ActualCountReg)					
Bits	ID	Type	Description					
31	Count	R	ual count of interrupts already generated.					
00								

1.1.1.9. Actual Count Register (ActualCountReg)

Table 1.28. Bits of Actual Count Register

Bits of	Bits of Actual Count Register							
0x19			ctual Count Register (ActualCountReg)					
Bits	ts ID Type		Description					
31	Count	R	Actual count of interrupts already generated.					
00								

1.1.1.10. Actual Count Register (ActualCountReg)

Table 1.29. Bits of Actual Count Register

Bits o	Bits of Actual Count Register						
0x1d			Actual Count Register (ActualCountReg)				
Bits	ID	Туре	Description				
31	Count	R	Actual count of interrupts already generated.				



1.1.1.11. Failure Count Register (FailureCountReg)

Table 1.30. Bits of Failure Count Register

Bits of	its of Failure Count Register								
0x21			Failure Count Register (FailureCountReg)						
Bits	ID	Type	Description						
31	Count	R	Failure count of missed interrupts.						
00									

1.1.1.12. Failure Count Register (FailureCountReg)

Table 1.31. Bits of Failure Count Register

Bits o	Bits of Failure Count Register								
0x25	0x25		Failure Count Register (FailureCountReg)						
Bits	s ID Type		Description						
31	Count R		Failure count of missed interrupts.						
00									

1.1.1.13. Failure Count Register (FailureCountReg)

Table 1.32. Bits of Failure Count Register

Bits of	Failure Count Registe	er							
0x29			Failure Count Register (FailureCountReg)						
Bits	ID	Type	Description						
31	Count	R	Failure count of missed interrupts.						
00									

1.1.1.14. Failure Count Register (FailureCountReg)

Table 1.33. Bits of Failure Count Register

Bits of	Failure Count Registe	er						
0x2d			Failure Count Register (FailureCountReg)					
Bits	ID Type		Description					
31	Count	R	Failure count of missed interrupts.					
00								

1.1.1.15. Interval Register (IntervalReg)

Table 1.34. Bits of Interval Register

Bits o	Sits of Interval Register								
0x31			Interval Register (IntervalReg)						
Bits	ID	Type	Description						
31	Interval	RW	erval of generated interrupt in nanaoseconds.						
00									



'	Table 1.35. Resets of Interval				
	0x0000.0000	BusReset	RW	Default Bus Reset	

1.1.1.16. Interval Register (IntervalReg)

Table 1.36. Bits of Interval Register

Bits o	Bits of Interval Register									
0x35 Interval Register (IntervalReg)										
Bits	ID	Type	Description	escription						
31	Interval	RW	Interval of generated	Interval of generated interrupt in nanaoseconds.						
			Table 1.37. Resets of Interval							
00			0x0000.0000	BusReset	RW	Default Bus Reset				

1.1.1.17. Interval Register (IntervalReg)

Table 1.38. Bits of Interval Register

Bits of	Bits of Interval Register									
0x39	39 Interval Register (IntervalReg)									
Bits	ID	Type	Description	escription						
31	Interval	RW	Interval of generated	Interval of generated interrupt in nanaoseconds.						
			Table 1.39. Resets of	Table 1.39. Resets of Interval						
00			0x0000.0000	BusReset	RW	Default Bus Reset				

1.1.1.18. Interval Register (IntervalReg)

Table 1.40. Bits of Interval Register

Bits of	Bits of Interval Register									
0x3d	0x3d Interval Register (IntervalReg)									
Bits	ID	Type	Description	escription						
31	Interval	RW	Interval of generated	Interval of generated interrupt in nanaoseconds.						
			Table 1.41. Resets of	Table 1.41. Resets of Interval						
00			0x0000.0000	BusReset	RW	Default Bus Reset				

1.1.1.19. Reference Count Register (ReferenceCountReg)

Table 1.42. Bits of Reference Count Register

Bits of	Bits of Reference Count Register									
0x41	41 Reference Count Register (ReferenceCountReg)									
Bits	ID	Туре	Description	escription						
31	Count	RW	Reference count written by SW to acknowledge a processed interrupt.							
			Table 1.43. Resets of	Fable 1.43. Resets of Count						
00			0x0000.0000	BusReset	RW	Default Bus Reset				

1.1.1.20. Reference Count Register (ReferenceCountReg)

Table 1.44. Bits of Reference Count Register

Bits o	ts of Reference Count Register									
0x45 Reference Count Register (ReferenceCountReg)										
Bits	ID	Type	escription							
31	Count	RW	eference count written by SW to acknowledge a processed interrupt.							
00										



'	Table 1.45. Resets of Count					
	0x0000.0000	BusReset	RW	Default Bus Reset		

1.1.1.21. Reference Count Register (ReferenceCountReg)

Table 1.46. Bits of Reference Count Register

Bits o	its of Reference Count Register										
0x49	0x49 Reference Count Register (ReferenceCountReg)										
Bits	ID	Type	Description	escription							
31	Count	RW	Reference count writt	Reference count written by SW to acknowledge a processed interrupt.							
			Table 1.47. Resets of	Table 1.47. Resets of Count							
00			0x0000.0000	BusReset	RW	Default Bus Reset					

1.1.1.22. Reference Count Register (ReferenceCountReg)

Table 1.48. Bits of Reference Count Register

Bits o	Bits of Reference Count Register									
0x4d Reference Count Register (ReferenceCountReg)										
Bits	ID	Type	Description	escription						
31	Count	RW	Reference count writt	Reference count written by SW to acknowledge a processed interrupt.						
			Table 1.49. Resets of	Fable 1.49. Resets of Count						
00			0x0000.0000	BusReset	RW	Default Bus Reset				