Eccelerators Library IP specification



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1. InterruptGeneratorIfc

1.1. Interrupt Generator Interface (InterruptGeneratorIfc)

Interface containing a basic Interrupt Generator block as predictable source and execurion check for interrupt simulation.

Table 1.1. Blocks of Interrupt Generator Interface

Blocks of Interrupt Generator Interface								
Block Address ID Block Name								
0x00	InterruptGeneratorBlk	Interrupt Generator Block						

Table 1.2. Resets of Interrupt Generator Interface

Resets of Registers of Interrupt Generator Interface								
ID	Reset Name							

1.1.1. Interrupt Generator Block (InterruptGeneratorBlk)

This block defines a basic Interrupt Generator block as predictable source and execution check for interrupt simulation. It provides 4 channels to generate 4 interrupt sources.

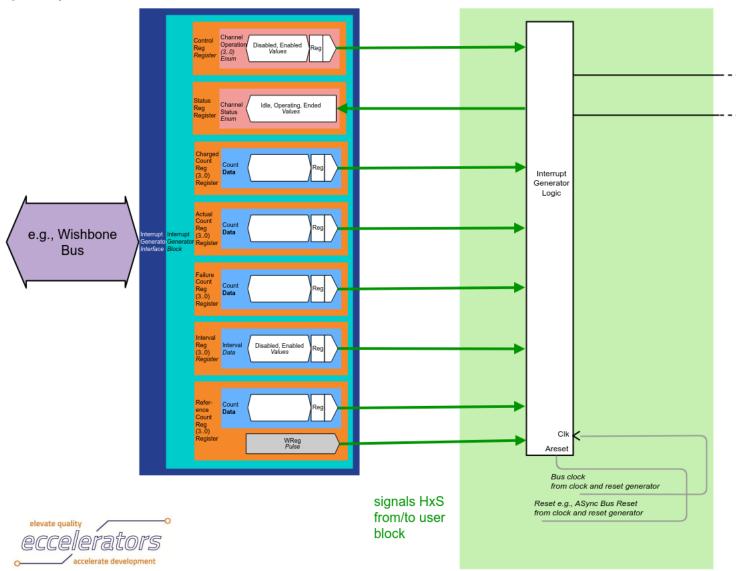
Constraints:

- 1. Generate interrupts at a configurable rate for level triggered interrupt destinations.
- 2. Check if interrupts are executed in time.
- 3. Provide a failure output.

Interrupt Generator details:



Figure 1.1. Interrupt Generator details



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Table 1.3. Registers or Delegates of Interrupt Generator Block

Registers or Delegates of Interrupt Generator Block										
0x00		Interrupt Generator Block								
0x57										
Address	ID	Name								
0x00	ControlReg	Control Register								
0x04	StatusReg	Status Register								
0x08	ChargedCountReg0	Charged Count Register								
0x0c	ChargedCountReg1	Charged Count Register								
0x10	ChargedCountReg2	Charged Count Register								
0x14	ChargedCountReg3	Charged Count Register								
0x18	ActualCountReg0	<u>Actual Count Register</u>								
0x1c	ActualCountReg1	<u>Actual Count Register</u>								
0x20	ActualCountReg2	Actual Count Register								
0x24	ActualCountReg3	Actual Count Register								
0x28	FailureCountReg0	Failure Count Register								



0x2c	FailureCountReg1	Failure Count Register
0x30	FailureCountReg2	Failure Count Register
0x34	FailureCountReg3	Failure Count Register
0x38	IntervalReg0	Interval Register
0x3c	IntervalReg1	Interval Register
0x40	IntervalReg2	Interval Register
0x44	IntervalReg3	Interval Register
0x48	ReferenceCoun- tReg0	Reference Count Register
0x4c	ReferenceCoun- tReg1	Reference Count Register
0x50	ReferenceCoun- tReg2	Reference Count Register
0x54	ReferenceCoun- tReg3	Reference Count Register

1.1.1.1. Control Register (ControlReg)

Table 1.4. Bits of Control Register

Bits o	Bits of Control Register									
0x00	0x00 Control Register (ControlReg)									
Bits	ID	Type	Description	Description						
03	ChannelOperation3	RW	Table 1.5. Values of ChannelOperation3							
			Value	ID	Type	Description				
			0x0	Disabled	R	An Interrupt is not pending.				
			0x1	Enabled	R	An Interrupt is pending.				
			Table 1.6. Resets of	ChannelOpe	ration3					
			0x0	BusReset		RW Default Bus Reset				
02	ChannelOperation2	RW	Table 1.7. Values of	ChannelOpe	ration2					
			Value	ID	Type	Description				
			0x0	Disabled	R	An Interrupt is not pending.				
			0x1	Enabled	R	An Interrupt is pending.				
			Table 1.8. Resets of	ChannelOpe	hannelOperation2					
			0x0	BusReset		RW Default Bus Reset				
01	ChannelOperation1	RW	Table 1.9. Values of	ble 1.9. Values of ChannelOperation1						
			Value	ID	Type	Description				
			0x0	Disabled	R	An Interrupt is not pending.				
			0x1	Enabled	R	An Interrupt is pending.				
			Table 1.10. Resets of	ChannelOp	eration1					
			0x0	BusReset		RW Default Bus Reset				
00	ChannelOperation0	RW	Table 1.11. Values of	f ChannelOp	eration0					
			Value	ID	Туре	Description				
			0x0	Disabled	R	An Interrupt is not pending.				
			0x1	Enabled	R	An Interrupt is pending.				
			Table 1.12. Resets of	able 1.12. Resets of ChannelOperation0						
			0x0	BusReset		RW Default Bus Reset				
				-	_	· · · · · · · · · · · · · · · · · · ·				

1.1.1.2. Status Register (StatusReg)

Table 1.13. Bits of Status Register

Bits of Status Register							
0x04			Status Register (StatusReg)				
Bits	Bits ID Type		Description				



07	ChannelStatus3	R	Table 1.14. Values of	Table 1.14. Values of ChannelStatus3						
			Value	ID	Type	Description				
06			0ь00	Idle	R	An Interrupt is pending.				
			0b01	Operating	R	An Interrupt is not pending.				
			0b1*	Ended	R	An Interrupt is not pending.				
				`						
05	ChannelStatus2	R	Table 1.15. Values of	f ChannelSta	itus2					
			Value	ID	Type	Description				
04			0ь00	Idle	R	An Interrupt is pending.				
			0b01	Operating	R	An Interrupt is not pending.				
			0b1*	Ended	R	An Interrupt is not pending.				
03	ChannelStatus l	R	Table 1.16. Values of	Table 1.16. Values of ChannelStatus1						
			Value	ID	Type	Description				
02			0ь00	Idle	R	An Interrupt is pending.				
			0b01	Operating	R	An Interrupt is not pending.				
			0b1*	Ended	R	An Interrupt is not pending.				
				`						
01	ChannelStatus0	R	Table 1.17. Values of	Table 1.17. Values of ChannelStatus0						
			Value	ID	Type	Description				
00			0ь00	Idle	R	An Interrupt is pending.				
			0b01	Operating	R	An Interrupt is not pending.				
			0b1*	Ended	R	An Interrupt is not pending.				

1.1.1.3. Charged Count Register (ChargedCountReg0)

Table 1.18. Bits of Charged Count Register

Bits o	bits of Charged Count Register									
0x08	0x08 Charged Count Register (ChargedCountReg0)									
Bits	ID	Type	Description	scription						
31	Count	RW	Number of interrupts	Number of interrupts to be generated and expected to be handled by SW.						
			Table 1.19. Resets of Count							
00			0x0000.0000	c0000.0000 BusReset RW Default Bus Reset						

1.1.1.4. Charged Count Register (ChargedCountReg1)

Table 1.20. Bits of Charged Count Register

Table	tanie 1.20. bils ii Chai ged Count Register										
Bits o	Bits of Charged Count Register										
0x0c	Co Charged Count Register (ChargedCountReg1)										
Bits	ID	Type	Description	scription							
31	Count	RW	Number of interrupts	fumber of interrupts to be generated and expected to be handled by SW.							
			Table 1.21. Resets of	Fable 1.21. Resets of Count							
00			0x0000.0000 BusReset RW Default Bus Reset								

1.1.1.5. Charged Count Register (ChargedCountReg2)

Table 1.22. Bits of Charged Count Register

Bits	Bits of Charged Count Register							
0x10 Charged Count Register (ChargedCountReg2)					<u>2)</u>			
Bits	ID	Type	Description	escription				
31	Count	RW	Number of interrupts	to be generated and ex	pected to	be handled by SW.		
			Table 1.23. Resets of	Table 1.23. Resets of Count				
00			0x0000.0000	Default Bus Reset				



1.1.1.6. Charged Count Register (ChargedCountReg3)

Table 1.24. Bits of Charged Count Register

Bits o	of Charged Count Register								
0x14 Charged Count Register (ChargedCountReg3)									
Bits	ID	Type	Description	scription					
31	Count	RW	Number of interrupts	imber of interrupts to be generated and expected to be handled by SW.					
			Table 1.25. Resets of	able 1.25. Resets of Count					
00			0x0000.0000 BusReset RW Default Bus Reset						

1.1.1.7. Actual Count Register (ActualCountReg0)

Table 1.26. Bits of Actual Count Register

Bits o	ts of Actual Count Register							
0x18	0x18		Actual Count Register (ActualCountReg0)					
Bits	ID Type		Description					
31	Count	R	Actual count of interrupts already generated.					
00								

1.1.1.8. Actual Count Register (ActualCountReg1)

Table 1.27. Bits of Actual Count Register

Bits o	its of Actual Count Register							
0x1c	0x1c		Actual Count Register (ActualCountReg1)					
Bits	ID	Type	Description					
31	Count	R	Actual count of interrupts already generated.					
00								

1.1.1.9. Actual Count Register (ActualCountReg2)

Table 1.28. Bits of Actual Count Register

Bits o	its of Actual Count Register							
0x20	0x20		Actual Count Register (ActualCountReg2)					
Bits	ID	Type	Description					
31	Count	R	Actual count of interrupts already generated.					
00								

1.1.1.10. Actual Count Register (ActualCountReg3)

Table 1.29. Bits of Actual Count Register

Bits of	is of Actual Count Register							
0x24	0x24		Actual Count Register (ActualCountReg3)					
Bits	ID Type		Description					
31	Count	R	Actual count of interrupts already generated.					
00								

1.1.1.11. Failure Count Register (FailureCountReg0)

Table 1.30. Bits of Failure Count Register

Bits of Failure Count Register



0x28			Failure Count Register (FailureCountReg0)
Bits	ID	Type	Description
31	Count	R	Failure count of missed interrupts.
00			

1.1.1.12. Failure Count Register (FailureCountReg1)

Table 1.31. Bits of Failure Count Register

Bits o	ts of Failure Count Register							
0x2c	0x2c		Failure Count Register (FailureCountReg 1)					
Bits	s ID Type		Description					
31	Count	R	Failure count of missed interrupts.					
00								

1.1.1.13. Failure Count Register (FailureCountReg2)

Table 1.32. Bits of Failure Count Register

Bits o	its of Failure Count Register							
0x30	0x30		Failure Count Register (FailureCountReg2)					
Bits	ID	Type	Description					
31	Count	R	Failure count of missed interrupts.					
00								

1.1.1.14. Failure Count Register (FailureCountReg3)

Table 1.33. Bits of Failure Count Register

Bits of	its of Failure Count Register							
0x34			Failure Count Register (FailureCountReg3)					
Bits	ID	Type	Description					
31	Count	R	Failure count of missed interrupts.					
00								

1.1.1.15. Interval Register (IntervalReg0)

Table 1.34. Bits of Interval Register

Bits of	Sits of Interval Register								
0x38 Interval Register (IntervalReg0)									
Bits	ID	Туре	Description	Description					
31	Interval	RW	Interval of generated	nterval of generated interrupt in nanaoseconds.					
			Table 1.35. Resets of	able 1.35. Resets of Interval					
00			0x0000.0000 BusReset RW Default Bus Reset						

1.1.1.16. Interval Register (IntervalReg1)

Table 1.36. Bits of Interval Register

Bits o	Bits of Interval Register						
0x3c	0x3c		Interval Register (IntervalReg1)				
Bits	ID	Type	Description				



31	Interval	RW	Interval of generated	interrupt in nanaosecoi	nds.		
			Table 1.37. Resets of	Interval			
00			0x0000.0000	BusReset	RW	Default Bus Reset	

1.1.1.17. Interval Register (IntervalReg2)

Table 1.38. Bits of Interval Register

Bits o	of Interval Register								
0x40	0x40 Interval Register (Interval Reg2)								
Bits	ID	Type	Description	cription					
31	Interval	RW	Interval of generated	terval of generated interrupt in nanaoseconds.					
			Table 1.39. Resets of	ble 1.39. Resets of Interval					
00			0x0000.0000	BusReset	RW	Default Bus Reset			

1.1.1.18. Interval Register (IntervalReg3)

Table 1.40. Bits of Interval Register

Bits of	of Interval Register								
0x44	4 Interval Register (Interval Reg3)								
Bits	ID	Type	Description	iption					
31	Interval	RW	Interval of generated	terval of generated interrupt in nanaoseconds.					
			Table 1.41. Resets of	ble 1.41. Resets of Interval					
00			0x0000.0000	BusReset	RW	Default Bus Reset			

1.1.1.19. Reference Count Register (ReferenceCountReg0)

Table 1.42. Bits of Reference Count Register

Bits o	its of Reference Count Register								
0x48	0x48 Reference Count Register (ReferenceCountReg0)								
Bits	ID	Type	Description	cription					
31	Count	RW	Reference count writt	teference count written by SW to acknowledge a processed interrupt.					
			Table 1.43. Resets of	able 1.43. Resets of Count					
00			0x0000.0000	BusReset	RW	Default Bus Reset			

1.1.1.20. Reference Count Register (ReferenceCountReg1)

Table 1.44. Bits of Reference Count Register

Bits of	its of Reference Count Register								
0x4c Reference Count Register (ReferenceCountReg1)									
Bits	ID	Type	Description	scription					
31	Count	RW	Reference count writt	reference count written by SW to acknowledge a processed interrupt.					
			Table 1.45. Resets of	able 1.45. Resets of Count					
00			0x0000.0000	BusReset	RW	Default Bus Reset			

1.1.1.21. Reference Count Register (ReferenceCountReg2)

Table 1.46. Bits of Reference Count Register

Bits of	Sits of Reference Count Register								
0x50			Reference Count Register (ReferenceCountReg2)						
Bits	ID	Type	Description						
31	Count	RW	Reference count written by SW to acknowledge a processed interrupt.						



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	'	Table 1.47. Resets of Count				
00		0x0000.0000	BusReset	RW	Default Bus Reset	
			*			

1.1.1.22. Reference Count Register (ReferenceCountReg3)

Table 1.48. Bits of Reference Count Register

Bits o	ts of Reference Count Register								
0x54	Reference Count Register (ReferenceCountReg3)								
Bits	ID	Туре	Description	scription					
31	Count	RW	Reference count writt	eference count written by SW to acknowledge a processed interrupt.					
			Table 1.49. Resets of	able 1.49. Resets of Count					
00 0x0000.0000 BusReset RW Default Bus Reset					Default Bus Reset				