Eccelerators Library IP specification



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1. EventCatcherIfc

1.1. Interrupt Generator Interface (InterruptGeneratorIfc)

Interface containing a basic Interrupt Generator block as predictable source and execurion check for interrupt simulation.

Table 1.1. Blocks of Interrupt Generator Interface

Blocks of Interrupt Generator Interface									
Block Address	ID	Block Name							
0x00	InterruptGeneratorBlk	Interrupt Generator Block							

Table 1.2. Resets of Interrupt Generator Interface

Resets of Registers of	of Interrupt Generator Interface
ID	Reset Name

1.1.1. Interrupt Generator Block (InterruptGeneratorBlk)

This block defines a basic Interrupt Generator block as predictable source and execution check for interrupt simulation. It provides 4 channels to generate 4 interrupt sources.

Constraints:

- 1. Generate interrupts at a configurable rate for level triggered interrupt destinations.
- 2. Check if interrupts are executed in time.
- 3. Provide a failure output.

Interrupt Generator details:



Figure 1.1. Interrupt Generator details Generator e.g., Wishbone Bus Clk . Areset signals HxS Bus clock from clock and reset generator from/to user Reset e.g., ASync Bus Reset from clock and reset generator block eccelerators

Table 1.3. Registers or Delegates of Interrupt Generator Block

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Registers or Delega	Registers or Delegates of Interrupt Generator Block									
0x00		pt Generator Block								
0x57										
Address	ID	Name								
0x00	ControlReg	Control Register								
0x04	StatusReg	Status Register								
0x08	ChargedCountReg	Charged Count Register								
0x0c	ChargedCountReg	Charged Count Register								
0x10	ChargedCountReg	Charged Count Register								
0x14	ChargedCountReg	Charged Count Register								
0x18	ActualCountReg	Actual Count Register								
0x1c	ActualCountReg	<u>Actual Count Register</u>								
0x18	ActualCountReg	Actual Count Register								



0x20	ActualCountReg	Actual Count Register
0x24	ActualCountReg	Actual Count Register
0x28	FailureCountReg	Failure Count Register
0x2c	FailureCountReg	Failure Count Register
0x30	FailureCountReg	Failure Count Register
0x34	FailureCountReg	Failure Count Register
0x38	IntervalReg	Interval Register
0x3c	IntervalReg	Interval Register
0x40	IntervalReg	Interval Register
0x44	IntervalReg	Interval Register
0x48	ReferenceCoun- tReg	Reference Count Register
0x4c	ReferenceCoun- tReg	Reference Count Register
0x50	ReferenceCoun- tReg	Reference Count Register
0x54	ReferenceCoun- tReg	Reference Count Register

1.1.1.1. Control Register (ControlReg)

Table 1.4. Bits of Control Register

Table 1	Table 1.4. Bits of Control Register											
Bits o	Bits of Control Register											
0x00			Control Register (ControlReg)									
Bits	ID	Type	Description	Description								
03	ChannelOperation3	RW	Table 1.5. Values of	ChannelOpe	nannelOperation3							
			Value	ID	Type	Descr	iption					
			0x0	Disabled	R	An In	terrupt is not pending.					
			0x1	Enabled	R	An In	terrupt is pending.					
			Table 1.6. Resets of	ChannelOpe	ration3							
			0x0	BusReset		RW	Default Bus Reset					
02	ChannelOperation2	RW	Table 1.7. Values of	ChannelOpe	eration2							
			Value	ID	Туре	Descr	iption					
			0×0	Disabled	R	An In	terrupt is not pending.					
			0x1	Enabled	R	An In	terrupt is pending.					
			Table 1.8. Resets of	ets of ChannelOperation2								
			0x0	BusReset		RW	Default Bus Reset					
01	ChannelOperation1	RW	Table 1.9. Values of	9. Values of ChannelOperation1								
			Value	ID	Туре	Descr	iption					
			0×0	Disabled	R	An In	terrupt is not pending.					
			0x1	Enabled	R	An In	terrupt is pending.					
			Table 1.10. Resets of	f ChannelOp	eration1							
			0x0	0x0 BusReset RW Default Bus Reset								
00	ChannelOperation0	RW	Table 1.11. Values o	f ChannelO _I	peration0							
			Value	ID	Туре	Descr	iption					
			0x0	Disabled	R	An In	terrupt is not pending.					
			0x1	Enabled	R	An Interrupt is pending.						
			Table 1.12. Resets of	ChannelOp	eration0	•						
			0×0	BusReset		RW	Default Bus Reset					
L	1	1		-								

1.1.1.2. Status Register (StatusReg)

Table 1.13. Bits of Status Register

Bits of Status Register



0x04			Status Register (StatusReg)																			
Bits	ID	Type	Description																			
07	ChannelStatus3	R	Table 1.14. Values of	able 1.14. Values of ChannelStatus3																		
			Value	ID	Туре	Description																
06			0b00	Idle	R	An Interrupt is pending.																
			0b01	Operating	R	An Interrupt is not pending.																
			0b1*	Ended	R	An Interrupt is not pending.																
05	ChannelStatus2	R	Table 1.15. Values of	f ChannalSte	ntue?																	
05	Chamieistatusz	K																				
			Value	ID	Туре	Description																
04			0b00	Idle	R	An Interrupt is pending.																
			0b01	Operating	R	An Interrupt is not pending.																
			0b1*	Ended	R	An Interrupt is not pending.																
03	ChannelStatus1 R Table 1.16. Values of ChannelStatus1			f ChannelSta	itus1																	
			Value	ID	Type	Description																
02			0000	Idle	R	An Interrupt is pending.																
																			0b01	Operating	R	An Interrupt is not pending.
			0b1*	Ended	R	An Interrupt is not pending.																
01	ChannelStatus0	R	Table 1.17. Values of	f ChannelSta	ntus0																	
			Value	ID	Type	Description																
00			0000	Idle	R	An Interrupt is pending.																
			0b01	Operating	R	An Interrupt is not pending.																
			0b1*	Ended	R	An Interrupt is not pending.																

1.1.1.3. Charged Count Register (ChargedCountReg)

Table 1.18. Bits of Charged Count Register

Bits of	Bits of Charged Count Register										
0x08	08 Charged Count Register (ChargedCountReg)										
Bits	ID	Type	Description	cription							
31	Count	RW	Number of interrupts	umber of interrupts to be generated and expected to be handled by SW.							
			Table 1.19. Resets of	ble 1.19. Resets of Count							
00			0x0000.0000	0.0000 BusReset RW Default Bus Reset							

1.1.1.4. Charged Count Register (ChargedCountReg)

Table 1.20. Bits of Charged Count Register

	130 Day of Change Count Report										
Bits o	Bits of Charged Count Register										
0x0c	0x0c Charged Count Register (ChargedCountReg)										
Bits	ID	Type	Description	ription							
31	Count	RW	Number of interrupts	nber of interrupts to be generated and expected to be handled by SW.							
			Table 1.21. Resets of	ble 1.21. Resets of Count							
00			0x0000.0000	00 BusReset RW Default Bus Reset							

1.1.1.5. Charged Count Register (ChargedCountReg)

Table 1.22. Bits of Charged Count Register

Bits o	Bits of Charged Count Register										
0x10			Charged Count Register (ChargedCountReg)								
Bits	ID	Type	Description								
31	Count	RW	Number of interrupts to be generated and expected to be handled by SW.								
00	00										



	Table 1.23. Resets of	f Count			
	0x0000.0000	BusReset	RW	Default Bus Reset	

1.1.1.6. Charged Count Register (ChargedCountReg)

Table 1.24. Bits of Charged Count Register

scription						
umber of interrupts to be generated and expected to be handled by SW.						

1.1.1.7. Actual Count Register (ActualCountReg)

Table 1.26. Bits of Actual Count Register

Bits o	Sits of Actual Count Register							
0x18			Actual Count Register (ActualCountReg)					
Bits	Bits ID Type		Description					
31	31 Count R		Actual count of interrupts already generated.					
00	00							

1.1.1.8. Actual Count Register (ActualCountReg)

Table 1.27. Bits of Actual Count Register

Bits of	Bits of Actual Count Register							
0x1c Actual Count Register (ActualCountReg)								
Bits	Bits ID Type		Description					
31 Count R Actual count of interrupts already generated.		R	Actual count of interrupts already generated.					
00								

1.1.1.9. Actual Count Register (ActualCountReg)

Table 1.28. Bits of Actual Count Register

Bits o	Bits of Actual Count Register						
0x20			Actual Count Register (ActualCountReg)				
Bits	Bits ID Type		Description				
31	31 Count R		Actual count of interrupts already generated.				
00							

1.1.1.10. Actual Count Register (ActualCountReg)

Table 1.29. Bits of Actual Count Register

Bits o	Bits of Actual Count Register						
0x24			Actual Count Register (ActualCountReg)				
Bits	ID	Туре	Description				
31	Count	R	Actual count of interrupts already generated.				



1.1.1.11. Failure Count Register (FailureCountReg)

Table 1.30. Bits of Failure Count Register

Bits of	bis of Failure Count Register							
0x28	0x28		Failure Count Register (FailureCountReg)					
Bits	Bits ID Type		Description					
31	l Count R		Failure count of missed interrupts.					
00								

1.1.1.12. Failure Count Register (FailureCountReg)

Table 1.31. Bits of Failure Count Register

Bits o	Bits of Failure Count Register						
0x2c	0x2c		Failure Count Register (FailureCountReg)				
Bits	its ID Type		Description				
31	l Count R		Failure count of missed interrupts.				
00	00						

1.1.1.13. Failure Count Register (FailureCountReg)

Table 1.32. Bits of Failure Count Register

Bits of	Bits of Failure Count Register						
0x30 Failure Count Register (FailureCountReg)							
Bits	Bits ID Type Description		Description				
31	31 Count R Failure count of missed interrupts.						
00							

1.1.1.14. Failure Count Register (FailureCountReg)

Table 1.33. Bits of Failure Count Register

Bits of	Bits of Failure Count Register						
0x34			Failure Count Register (FailureCountReg)				
Bits	Bits ID Type		Description				
31	l Count R		Failure count of missed interrupts.				
00							

1.1.1.15. Interval Register (IntervalReg)

Table 1.34. Bits of Interval Register

Bits o	Sits of Interval Register						
0x38			Interval Register (IntervalReg)				
Bits	Bits ID Type		Description				
31 Interval RW Interval of generated inter		RW	Interval of generated interrupt in nanaoseconds.				
00							



		Interval		
	0x0000.0000	BusReset	RW	Default Bus Reset
				·

1.1.1.16. Interval Register (IntervalReg)

Table 1.36. Bits of Interval Register

Bits of	Bits of Interval Register									
0x3c Interval Register (IntervalReg)										
Bits	ID	Type	Description	escription						
31	Interval	RW	Interval of generated	interval of generated interrupt in nanaoseconds.						
			Table 1.37. Resets of Interval							
00			0x0000.0000	BusReset	RW	Default Bus Reset				

1.1.1.17. Interval Register (IntervalReg)

Table 1.38. Bits of Interval Register

Bits of	Bits of Interval Register									
0x40	Interval Register (IntervalReg)									
Bits	ID	Type	Description	escription						
31	Interval	RW	Interval of generated	Interval of generated interrupt in nanaoseconds.						
			Table 1.39. Resets of	Table 1.39. Resets of Interval						
00			0x0000.0000	BusReset	RW	Default Bus Reset				

1.1.1.18. Interval Register (IntervalReg)

Table 1.40. Bits of Interval Register

Bits of	Bits of Interval Register									
0x44	Interval Register (IntervalReg)									
Bits	ID	Type	Description	escription						
31	Interval	RW	Interval of generated	nterval of generated interrupt in nanaoseconds.						
			Table 1.41. Resets of	able 1.41. Resets of Interval						
00			0x0000.0000	BusReset	RW	Default Bus Reset				

1.1.1.19. Reference Count Register (ReferenceCountReg)

Table 1.42. Bits of Reference Count Register

Bits of	Bits of Reference Count Register									
0x48	Reference Count Register (ReferenceCountReg)									
Bits	ID	Type	Description	Asscription						
31	Count	RW	Reference count writt	Reference count written by SW to acknowledge a processed interrupt.						
			Table 1.43. Resets of	Table 1.43. Resets of Count						
00			0x0000.0000	BusReset	RW	Default Bus Reset				

1.1.1.20. Reference Count Register (ReferenceCountReg)

Table 1.44. Bits of Reference Count Register

Bits o	its of Reference Count Register									
0x4c Reference Count Register (ReferenceCountReg)										
Bits	ID	Type	escription							
31	Count	RW	eference count written by SW to acknowledge a processed interrupt.							
00										



'	Table 1.45. Resets of Count					
	0x0000.0000	BusReset	RW	Default Bus Reset		

1.1.1.21. Reference Count Register (ReferenceCountReg)

Table 1.46. Bits of Reference Count Register

Bits o	Bits of Reference Count Register									
0x50	0x50 Reference Count Register (ReferenceCountReg)									
Bits	ID	Type	Description	escription						
31	Count	RW	Reference count writte	Reference count written by SW to acknowledge a processed interrupt.						
			Table 1.47. Resets of	Γable 1.47. Resets of Count						
00			0x0000.0000	BusReset	RW	Default Bus Reset				

1.1.1.22. Reference Count Register (ReferenceCountReg)

Table 1.48. Bits of Reference Count Register

Bits o	Bits of Reference Count Register									
0x54 Reference Count Register (ReferenceCountReg)										
Bits	ID	Type	Description	escription						
31	Count	RW	Reference count writt	Reference count written by SW to acknowledge a processed interrupt.						
			Table 1.49. Resets of	Table 1.49. Resets of Count						
00			0x0000.0000	BusReset	RW	Default Bus Reset				