Eccelerators Library IP specification



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1. EventCatcherIfc

1.1. Interrupt Generator Interface (InterruptGeneratorIfc)

Interface containing a basic Interrupt Generator block as predictable source and execurion check for interrupt simulation.

Table 1.1. Blocks of Interrupt Generator Interface

Blocks of Interrupt Generator Interface									
Block Address	ID	Block Name							
0x0000	InterruptGeneratorBlk	Interrupt Generator Block							

Table 1.2. Resets of Interrupt Generator Interface

Resets of Registers	ets of Registers of Interrupt Generator Interface									
ID	Reset Name									

1.1.1. Interrupt Generator Block (InterruptGeneratorBlk)

This block defines a basic Interrupt Generator block as predictable source and execution check for interrupt simulation. It provides 4 channels to generate 4 interrupt sources.

Constraints:

- 1. Generate interrupts at a configurable rate for level triggered interrupt destinations.
- 2. Check if interrupts are executed in time.
- 3. Provide a failure output.

Interrupt Generator details:



Figure 1.1. Interrupt Generator details Generator e.g., Wishbone Bus Clk . Areset signals HxS Bus clock from clock and reset generator from/to user Reset e.g., ASync Bus Reset from clock and reset generator block eccelerators

Table 1.3. Registers or Delegates of Interrupt Generator Block

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Registers or Delegat	Registers or Delegates of Interrupt Generator Block									
0x0000		errupt Generator Block								
0x0053										
Address	ID	Name								
0x0000	ControlReg	Control Register								
0x0000	StatusReg	<u>Status Register</u>								
0x0000	ChargedCountReg	Charged Count Register								
0x0004	ChargedCountReg	Charged Count Register								
0x0008	ChargedCountReg	Charged Count Register								
0x000c	ChargedCountReg	Charged Count Register								
0x0010	ActualCountReg	Actual Count Register								
0x0014	ActualCountReg	Actual Count Register								



0x0018	ActualCountReg	Actual Count Register
0x001c	ActualCountReg	Actual Count Register
0x0020	FailureCountReg	Failure Count Register
0x0024	FailureCountReg	Failure Count Register
0x0028	FailureCountReg	Failure Count Register
0x002c	FailureCountReg	Failure Count Register
0x0030	IntervalReg	Interval Register
0x0034	IntervalReg	Interval Register
0x0038	IntervalReg	Interval Register
0x003c	IntervalReg	Interval Register
0x0040	ReferenceCoun- tReg	Reference Count Register
0x0044	ReferenceCoun- tReg	Reference Count Register
0x0048	ReferenceCoun- tReg	Reference Count Register
0x004c	ReferenceCoun- tReg	Reference Count Register

1.1.1.1. Control Register (ControlReg)

Table 1.4. Bits of Control Register

Table 1	.4. Bits of Control R	gister									
Bits o	Bits of Control Register										
0x00	0x0000 Control Register (ControlReg)										
Bits	ID	Type	Description	scription							
3	ChannelOperation	RW	Table 1.5. Values of	e 1.5. Values of ChannelOperation							
			Value	ID	Туре	Descrip	ption				
			0x1	Enabled	R	An Inte	errupt is pending.				
			0x0	Disabled	R	An Inte	errupt is not pending.				
			Table 1.6. Resets of	ChannelOpe	ration						
			0×0	BusReset	1	RW	Default Bus Reset				
2	ChannelOperation	RW	Table 1.7. Values of	ChannelOp	eration						
			Value	ID	Type	Descrip	ption				
			0x1	Enabled	R	An Inte	errupt is pending.				
			0x0	Disabled	R	An Inte	errupt is not pending.				
		Table 1.8. Resets of ChannelOperation									
			0x0	BusReset		RW	Default Bus Reset				
1	ChannelOperation	RW	Table 1.9. Values of	Fable 1.9. Values of ChannelOperation							
		Value ID Type Description				ption					
		0x1 Enabled R An Interrupt is pending.		errupt is pending.							
			0x0	Disabled	Disabled R An Interrupt is not pending.		errupt is not pending.				
			Table 1.10. Resets of	ChannelOp	eration						
			0x0	BusReset		RW	Default Bus Reset				
0	ChannelOperation	RW	Table 1.11. Values of	f ChannelO _J	peration						
Value ID				ID	Type	Descrip	ption				
			0x1	Enabled	R	An Inte	errupt is pending.				
			0x0	Disabled	R	An Inte	errupt is not pending.				
			Table 1.12. Resets of	ChannelOp	eration						
			0x0	BusReset	1	RW	Default Bus Reset				
1	1	1	-								

1.1.1.2. Status Register (StatusReg)

Table 1.13. Bits of Status Register

Bits of Status Register



0x0000 Status Register (StatusReg).										
Bits	ID	Type	Description	scription						
7	ChannelStatus	R	Table 1.14. Values of	able 1.14. Values of ChannelStatus						
			Value	ID	Type	Description				
6			0600	Idle	R	An Interrupt is pending.				
			0b01	Operating	R	An Interrupt is not pending.				
			0b1*	Ended	R	An Interrupt is not pending.				
5	ChannelStatus	R	Table 1.15. Values of	f ChannelSta	itus					
			Value	ID	Type	Description				
4			0600	Idle	R	An Interrupt is pending.				
			0b01	Operating	R	An Interrupt is not pending.				
			0b1*	Ended	R	An Interrupt is not pending.				
3	ChannelStatus	R	Table 1.16. Values of ChannelStatus							
		-		Value ID Type Description						
2			0600	Idle	R	An Interrupt is pending.				
_			0b01	Operating	R	An Interrupt is not pending.				
			0b1*	Ended	R	An Interrupt is not pending.				
				,	ļ					
1	ChannelStatus	R	Table 1.17. Values of	Table 1.17. Values of ChannelStatus						
			Value	ID	Type	Description				
0			0600	Idle	R	An Interrupt is pending.				
			0b01	Operating	R	An Interrupt is not pending.				
			0b1*	Ended	R	An Interrupt is not pending.				
		1								

1.1.1.3. Charged Count Register (ChargedCountReg)

Table 1.18. Bits of Charged Count Register

Bits of	Bits of Charged Count Register											
0x0000 Charged Count Register (Charged CountReg)												
Bits	ID	Туре	Description	ription								
31	Count	RW	Number of interrupts	umber of interrupts to be generated and expected to be handled by SW.								
			Table 1.19. Resets of	able 1.19. Resets of Count								
00			0x0000.0000	00.0000 BusReset RW Default Bus Reset								

1.1.1.4. Charged Count Register (ChargedCountReg)

Table 1.20. Bits of Charged Count Register

Table .	inte Lao. Dies of Changed Count Negater										
Bits o	its of Charged Count Register										
0x00	0x0004 Charged Count Register (ChargedCountReg)										
Bits	ID	Type	Description	ription							
31	Count	RW	Number of interrupts	mber of interrupts to be generated and expected to be handled by SW.							
			Table 1.21. Resets of	able 1.21. Resets of Count							
00			0x0000.0000	0.0000 BusReset RW Default Bus Reset							

1.1.1.5. Charged Count Register (ChargedCountReg)

Table 1.22. Bits of Charged Count Register

Bits o	Sits of Charged Count Register									
0x00	08		Charged Count Register (ChargedCountReg)							
Bits	ID	Type	Description							
31	Count	RW	Number of interrupts to be generated and expected to be handled by SW.							
00										



	Table 1.23. Resets of Count			
	0x0000.0000	BusReset	RW	Default Bus Reset

1.1.1.6. Charged Count Register (ChargedCountReg)

Table 1.24. Bits of Charged Count Register

Bits of	Bits of Charged Count Register									
0x000c Charged Count Register (ChargedCountReg)										
Bits	ID	Type	Description	escription						
31	Count	RW	Number of interrupts	Number of interrupts to be generated and expected to be handled by SW.						
			Table 1.25. Resets of Count							
00			0x0000.0000	BusReset	RW	Default Bus Reset				
00			0x0000.0000	BusReset	RW	Default Bus Reset				

1.1.1.7. Actual Count Register (ActualCountReg)

Table 1.26. Bits of Actual Count Register

Bits of	Bits of Actual Count Register							
0x0010			Actual Count Register (ActualCountReg)					
Bits	ID	Type	Description					
31	Count	R	tual count of interrupts already generated.					
00								

1.1.1.8. Actual Count Register (ActualCountReg)

Table 1.27. Bits of Actual Count Register

Bits of	Bits of Actual Count Register							
0x0014			Actual Count Register (ActualCountReg)					
Bits	Bits ID Type		Description					
31	Count	R	Actual count of interrupts already generated.					
00								

1.1.1.9. Actual Count Register (ActualCountReg)

Table 1.28. Bits of Actual Count Register

Bits o	Bits of Actual Count Register						
0x0018			Actual Count Register (ActualCountReg)				
Bits	Bits ID Type		Description				
31	Count	R	ctual count of interrupts already generated.				
00							

1.1.1.10. Actual Count Register (ActualCountReg)

Table 1.29. Bits of Actual Count Register

Bits of Actual Count Register						
0x001c			Actual Count Register (ActualCountReg)			
Bits	its ID Type		Description			
31	Count R		Actual count of interrupts already generated.			



1.1.1.11. Failure Count Register (FailureCountReg)

Table 1.30. Bits of Failure Count Register

Bits o	Bits of Failure Count Register								
0x00	0x0020		Failure Count Register (FailureCountReg)						
Bits	ID	Type	Description						
31	Count	R	Failure count of missed interrupts.						
00									

1.1.1.12. Failure Count Register (FailureCountReg)

Table 1.31. Bits of Failure Count Register

Bits o	Bits of Failure Count Register							
0x0024			Failure Count Register (FailureCountReg)					
Bits	ID	Type	Description					
31	Count	R	Failure count of missed interrupts.					
00								

1.1.1.13. Failure Count Register (FailureCountReg)

Table 1.32. Bits of Failure Count Register

Bits of Failure Count Register								
0x0028			Failure Count Register (FailureCountReg)					
Bits	Bits ID Type		Description					
31	Count	R	Failure count of missed interrupts.					
00								

1.1.1.14. Failure Count Register (FailureCountReg)

Table 1.33. Bits of Failure Count Register

Bits of	Bits of Failure Count Register							
0x002c			Failure Count Register (FailureCountReg)					
Bits	ID Type		Description					
31	Count	R	allure count of missed interrupts.					
00								

1.1.1.15. Interval Register (IntervalReg)

Table 1.34. Bits of Interval Register

Bits o	Bits of Interval Register							
0x0030			Interval Register (IntervalReg)					
Bits	ID	Type	Description					
31	Interval	RW	rryal of generated interrupt in nanaoseconds.					
00								



	Table 1.35. Resets of Interval				
	0x0000.0000	BusReset	RW	Default Bus Reset	
				· · · · · · · · · · · · · · · · · · ·	_

1.1.1.16. Interval Register (IntervalReg)

Table 1.36. Bits of Interval Register

Bits o	its of Interval Register									
0x0034 Interval Register (IntervalReg)										
Bits	ID	Type	Description	escription						
31	Interval	RW	Interval of generated	Interval of generated interrupt in nanaoseconds.						
			Table 1.37. Resets of Interval							
00			0x0000.0000	BusReset	RW	Default Bus Reset				

1.1.1.17. Interval Register (IntervalReg)

Table 1.38. Bits of Interval Register

Bits o	its of Interval Register										
0x0038 Interval Register (IntervalReg)											
Bits	ID	Type	Description	escription							
31	Interval	RW	Interval of generated	Interval of generated interrupt in nanaoseconds.							
			Table 1.39. Resets of Interval								
00			0x0000.0000	BusReset	RW	Default Bus Reset					

1.1.1.18. Interval Register (IntervalReg)

Table 1.40. Bits of Interval Register

Bits of	Sits of Interval Register									
0x00	0x003c Interval Register (IntervalReg)									
Bits	ID	Туре	Description	Asscription						
31	Interval	RW	Interval of generated interrupt in nanaoseconds.							
			Table 1.41. Resets of	Fable 1.41. Resets of Interval						
00 0x0000.0000 BusReset RW Default Bus Reset										

1.1.1.19. Reference Count Register (ReferenceCountReg)

Table 1.42. Bits of Reference Count Register

Bits of	its of Reference Count Register									
0x0040 Reference Count Register (ReferenceCountReg)										
Bits	ID	Type	Description	Description						
31	Count	RW	Reference count written by SW to acknowledge a processed interrupt.							
			Table 1.43. Resets of Count							
00			0x0000.0000	BusReset	RW	Default Bus Reset				

1.1.1.20. Reference Count Register (ReferenceCountReg)

Table 1.44. Bits of Reference Count Register

Bits o	s of Reference Count Register									
0x0044 Reference Count Register (ReferenceCountReg)										
Bits	ID	Type	escription							
31	Count	RW	eference count written by SW to acknowledge a processed interrupt.							
00										



	Table 1.45. Resets of Count					
	0x0000.0000	BusReset	RW	Default Bus Reset		

1.1.1.21. Reference Count Register (ReferenceCountReg)

Table 1.46. Bits of Reference Count Register

Bits o	its of Reference Count Register									
0x0048 Reference Count Register (ReferenceCountReg)										
Bits	ID	Type	Description	Description						
31	Count	RW	Reference count written by SW to acknowledge a processed interrupt.							
			Table 1.47. Resets of Count							
00			0x0000.0000 BusReset RW Default Bus Reset							

1.1.1.22. Reference Count Register (ReferenceCountReg)

Table 1.48. Bits of Reference Count Register

Bits of Reference Count Register									
0x004c Reference Count Register (ReferenceCountReg)									
ID	Туре	Description	escription						
Count	RW	Reference count writt	Reference count written by SW to acknowledge a processed interrupt.						
		Table 1.49. Resets of	able 1.49. Resets of Count						
		0x0000.0000	BusReset	RW	Default Bus Reset				
)	004c	ID Type Count RW		Document Description	Description Reference Count Register (ReferenceCountReg) Description Count RW Reference count written by SW to acknowledge a procure to the count Table 1.49. Resets of Count Reference count written by SW to acknowledge a procure to the count Table 1.49. Resets of Count Reference				