#### Interrupt Generator Interface (InterruptGeneratorIfc)

Interface containing a basic Interrupt Generator block as predictable source and execurion check for interrupt simulation.

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| --- | --- | --- |
| Blocks of Interrupt Generator Interface | | |
| Block Address | ID | Block Name |
| 0x00 | InterruptGeneratorBlk | [Interrupt Generator Block](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk) |

|  |  |
| --- | --- |
| Resets of Registers of Interrupt Generator Interface | |
| ID | Reset Name |

##### Interrupt Generator Block (InterruptGeneratorBlk)

This block defines a basic Interrupt Generator block as predictable source and execution check for   
interrupt simulation. It provides 4 channels to generate 4 interrupt sources.  
   
Constraints:  
   
1. Generate interrupts at a configurable rate for level triggered interrupt destinations.  
2. Check if interrupts are executed in time.  
3. Provide a failure output.   
   
Interrupt Generator details:  
   
.. figure:: resources/InterruptGeneratorUserLogic.png  
 :scale: 50  
   
 Interrupt Generator details

|  |  |  |
| --- | --- | --- |
| Registers or Delegates of Interrupt Generator Block | | |
| 0x00 .. 0x57 | | [Interrupt Generator Block](#ifc:InterruptGeneratorIfc/blk-lst:InterruptGeneratorBlk) |
| Address | ID | Name |
| 0x00 | ControlReg | [Control Register](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld:ControlReg) |
| 0x04 | StatusReg | [Status Register](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld:StatusReg) |
| 0x08 | ChargedCountReg0 | [Charged Count Register](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld:ChargedCountReg0) |
| 0x0c | ChargedCountReg1 | [Charged Count Register](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld:ChargedCountReg1) |
| 0x10 | ChargedCountReg2 | [Charged Count Register](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld:ChargedCountReg2) |
| 0x14 | ChargedCountReg3 | [Charged Count Register](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld:ChargedCountReg3) |
| 0x18 | ActualCountReg0 | [Actual Count Register](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld:ActualCountReg0) |
| 0x1c | ActualCountReg1 | [Actual Count Register](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld:ActualCountReg1) |
| 0x20 | ActualCountReg2 | [Actual Count Register](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld:ActualCountReg2) |
| 0x24 | ActualCountReg3 | [Actual Count Register](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld:ActualCountReg3) |
| 0x28 | FailureCountReg0 | [Failure Count Register](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld:FailureCountReg0) |
| 0x2c | FailureCountReg1 | [Failure Count Register](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld:FailureCountReg1) |
| 0x30 | FailureCountReg2 | [Failure Count Register](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld:FailureCountReg2) |
| 0x34 | FailureCountReg3 | [Failure Count Register](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld:FailureCountReg3) |
| 0x38 | IntervalReg0 | [Interval Register](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld:IntervalReg0) |
| 0x3c | IntervalReg1 | [Interval Register](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld:IntervalReg1) |
| 0x40 | IntervalReg2 | [Interval Register](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld:IntervalReg2) |
| 0x44 | IntervalReg3 | [Interval Register](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld:IntervalReg3) |
| 0x48 | ReferenceCountReg0 | [Reference Count Register](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld:ReferenceCountReg0) |
| 0x4c | ReferenceCountReg1 | [Reference Count Register](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld:ReferenceCountReg1) |
| 0x50 | ReferenceCountReg2 | [Reference Count Register](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld:ReferenceCountReg2) |
| 0x54 | ReferenceCountReg3 | [Reference Count Register](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld:ReferenceCountReg3) |

###### Control Register (ControlReg)

|  |  |  |  |
| --- | --- | --- | --- |
| Bits of Control Register | | | |
| 0x00 | | | [Control Register (ControlReg)](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld-lst:ControlReg) |
| Bits | ID | Type | Description |
| 03 | ChannelOperation3 | RW | |  |  |  |  | | --- | --- | --- | --- | | Value | ID | Type | Description | | 0x0 | Disabled | R | An Interrupt is not pending. | | 0x1 | Enabled | R | An Interrupt is pending. |  |  |  |  |  | | --- | --- | --- | --- | | 0x0 | BusReset | RW | Default Bus Reset | |
| 02 | ChannelOperation2 | RW | |  |  |  |  | | --- | --- | --- | --- | | Value | ID | Type | Description | | 0x0 | Disabled | R | An Interrupt is not pending. | | 0x1 | Enabled | R | An Interrupt is pending. |  |  |  |  |  | | --- | --- | --- | --- | | 0x0 | BusReset | RW | Default Bus Reset | |
| 01 | ChannelOperation1 | RW | |  |  |  |  | | --- | --- | --- | --- | | Value | ID | Type | Description | | 0x0 | Disabled | R | An Interrupt is not pending. | | 0x1 | Enabled | R | An Interrupt is pending. |  |  |  |  |  | | --- | --- | --- | --- | | 0x0 | BusReset | RW | Default Bus Reset | |
| 00 | ChannelOperation0 | RW | |  |  |  |  | | --- | --- | --- | --- | | Value | ID | Type | Description | | 0x0 | Disabled | R | An Interrupt is not pending. | | 0x1 | Enabled | R | An Interrupt is pending. |  |  |  |  |  | | --- | --- | --- | --- | | 0x0 | BusReset | RW | Default Bus Reset | |

###### Status Register (StatusReg)

|  |  |  |  |
| --- | --- | --- | --- |
| Bits of Status Register | | | |
| 0x04 | | | [Status Register (StatusReg)](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld-lst:StatusReg) |
| Bits | ID | Type | Description |
| 07 .. 06 | ChannelStatus3 | R | |  |  |  |  | | --- | --- | --- | --- | | Value | ID | Type | Description | | 0b00 | Idle | R | An Interrupt is pending. | | 0b01 | Operating | R | An Interrupt is not pending. | | 0b1\* | Ended | R | An Interrupt is not pending. | |
| 05 .. 04 | ChannelStatus2 | R | |  |  |  |  | | --- | --- | --- | --- | | Value | ID | Type | Description | | 0b00 | Idle | R | An Interrupt is pending. | | 0b01 | Operating | R | An Interrupt is not pending. | | 0b1\* | Ended | R | An Interrupt is not pending. | |
| 03 .. 02 | ChannelStatus1 | R | |  |  |  |  | | --- | --- | --- | --- | | Value | ID | Type | Description | | 0b00 | Idle | R | An Interrupt is pending. | | 0b01 | Operating | R | An Interrupt is not pending. | | 0b1\* | Ended | R | An Interrupt is not pending. | |
| 01 .. 00 | ChannelStatus0 | R | |  |  |  |  | | --- | --- | --- | --- | | Value | ID | Type | Description | | 0b00 | Idle | R | An Interrupt is pending. | | 0b01 | Operating | R | An Interrupt is not pending. | | 0b1\* | Ended | R | An Interrupt is not pending. | |

###### Charged Count Register (ChargedCountReg0)

|  |  |  |  |
| --- | --- | --- | --- |
| Bits of Charged Count Register | | | |
| 0x08 | | | [Charged Count Register (ChargedCountReg0)](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld-lst:ChargedCountReg0) |
| Bits | ID | Type | Description |
| 31 .. 00 | Count | RW | Number of interrupts to be generated and expected to be handled by SW.   |  |  |  |  | | --- | --- | --- | --- | | 0x0000.0000 | BusReset | RW | Default Bus Reset | |

###### Charged Count Register (ChargedCountReg1)

|  |  |  |  |
| --- | --- | --- | --- |
| Bits of Charged Count Register | | | |
| 0x0c | | | [Charged Count Register (ChargedCountReg1)](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld-lst:ChargedCountReg1) |
| Bits | ID | Type | Description |
| 31 .. 00 | Count | RW | Number of interrupts to be generated and expected to be handled by SW.   |  |  |  |  | | --- | --- | --- | --- | | 0x0000.0000 | BusReset | RW | Default Bus Reset | |

###### Charged Count Register (ChargedCountReg2)

|  |  |  |  |
| --- | --- | --- | --- |
| Bits of Charged Count Register | | | |
| 0x10 | | | [Charged Count Register (ChargedCountReg2)](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld-lst:ChargedCountReg2) |
| Bits | ID | Type | Description |
| 31 .. 00 | Count | RW | Number of interrupts to be generated and expected to be handled by SW.   |  |  |  |  | | --- | --- | --- | --- | | 0x0000.0000 | BusReset | RW | Default Bus Reset | |

###### Charged Count Register (ChargedCountReg3)

|  |  |  |  |
| --- | --- | --- | --- |
| Bits of Charged Count Register | | | |
| 0x14 | | | [Charged Count Register (ChargedCountReg3)](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld-lst:ChargedCountReg3) |
| Bits | ID | Type | Description |
| 31 .. 00 | Count | RW | Number of interrupts to be generated and expected to be handled by SW.   |  |  |  |  | | --- | --- | --- | --- | | 0x0000.0000 | BusReset | RW | Default Bus Reset | |

###### Actual Count Register (ActualCountReg0)

|  |  |  |  |
| --- | --- | --- | --- |
| Bits of Actual Count Register | | | |
| 0x18 | | | [Actual Count Register (ActualCountReg0)](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld-lst:ActualCountReg0) |
| Bits | ID | Type | Description |
| 31 .. 00 | Count | R | Actual count of interrupts already generated. |

###### Actual Count Register (ActualCountReg1)

|  |  |  |  |
| --- | --- | --- | --- |
| Bits of Actual Count Register | | | |
| 0x1c | | | [Actual Count Register (ActualCountReg1)](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld-lst:ActualCountReg1) |
| Bits | ID | Type | Description |
| 31 .. 00 | Count | R | Actual count of interrupts already generated. |

###### Actual Count Register (ActualCountReg2)

|  |  |  |  |
| --- | --- | --- | --- |
| Bits of Actual Count Register | | | |
| 0x20 | | | [Actual Count Register (ActualCountReg2)](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld-lst:ActualCountReg2) |
| Bits | ID | Type | Description |
| 31 .. 00 | Count | R | Actual count of interrupts already generated. |

###### Actual Count Register (ActualCountReg3)

|  |  |  |  |
| --- | --- | --- | --- |
| Bits of Actual Count Register | | | |
| 0x24 | | | [Actual Count Register (ActualCountReg3)](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld-lst:ActualCountReg3) |
| Bits | ID | Type | Description |
| 31 .. 00 | Count | R | Actual count of interrupts already generated. |

###### Failure Count Register (FailureCountReg0)

|  |  |  |  |
| --- | --- | --- | --- |
| Bits of Failure Count Register | | | |
| 0x28 | | | [Failure Count Register (FailureCountReg0)](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld-lst:FailureCountReg0) |
| Bits | ID | Type | Description |
| 31 .. 00 | Count | R | Failure count of missed interrupts. |

###### Failure Count Register (FailureCountReg1)

|  |  |  |  |
| --- | --- | --- | --- |
| Bits of Failure Count Register | | | |
| 0x2c | | | [Failure Count Register (FailureCountReg1)](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld-lst:FailureCountReg1) |
| Bits | ID | Type | Description |
| 31 .. 00 | Count | R | Failure count of missed interrupts. |

###### Failure Count Register (FailureCountReg2)

|  |  |  |  |
| --- | --- | --- | --- |
| Bits of Failure Count Register | | | |
| 0x30 | | | [Failure Count Register (FailureCountReg2)](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld-lst:FailureCountReg2) |
| Bits | ID | Type | Description |
| 31 .. 00 | Count | R | Failure count of missed interrupts. |

###### Failure Count Register (FailureCountReg3)

|  |  |  |  |
| --- | --- | --- | --- |
| Bits of Failure Count Register | | | |
| 0x34 | | | [Failure Count Register (FailureCountReg3)](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld-lst:FailureCountReg3) |
| Bits | ID | Type | Description |
| 31 .. 00 | Count | R | Failure count of missed interrupts. |

###### Interval Register (IntervalReg0)

|  |  |  |  |
| --- | --- | --- | --- |
| Bits of Interval Register | | | |
| 0x38 | | | [Interval Register (IntervalReg0)](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld-lst:IntervalReg0) |
| Bits | ID | Type | Description |
| 31 .. 00 | Interval | RW | Interval of generated interrupt in nanaoseconds.   |  |  |  |  | | --- | --- | --- | --- | | 0x0000.0000 | BusReset | RW | Default Bus Reset | |

###### Interval Register (IntervalReg1)

|  |  |  |  |
| --- | --- | --- | --- |
| Bits of Interval Register | | | |
| 0x3c | | | [Interval Register (IntervalReg1)](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld-lst:IntervalReg1) |
| Bits | ID | Type | Description |
| 31 .. 00 | Interval | RW | Interval of generated interrupt in nanaoseconds.   |  |  |  |  | | --- | --- | --- | --- | | 0x0000.0000 | BusReset | RW | Default Bus Reset | |

###### Interval Register (IntervalReg2)

|  |  |  |  |
| --- | --- | --- | --- |
| Bits of Interval Register | | | |
| 0x40 | | | [Interval Register (IntervalReg2)](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld-lst:IntervalReg2) |
| Bits | ID | Type | Description |
| 31 .. 00 | Interval | RW | Interval of generated interrupt in nanaoseconds.   |  |  |  |  | | --- | --- | --- | --- | | 0x0000.0000 | BusReset | RW | Default Bus Reset | |

###### Interval Register (IntervalReg3)

|  |  |  |  |
| --- | --- | --- | --- |
| Bits of Interval Register | | | |
| 0x44 | | | [Interval Register (IntervalReg3)](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld-lst:IntervalReg3) |
| Bits | ID | Type | Description |
| 31 .. 00 | Interval | RW | Interval of generated interrupt in nanaoseconds.   |  |  |  |  | | --- | --- | --- | --- | | 0x0000.0000 | BusReset | RW | Default Bus Reset | |

###### Reference Count Register (ReferenceCountReg0)

|  |  |  |  |
| --- | --- | --- | --- |
| Bits of Reference Count Register | | | |
| 0x48 | | | [Reference Count Register (ReferenceCountReg0)](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld-lst:ReferenceCountReg0) |
| Bits | ID | Type | Description |
| 31 .. 00 | Count | RW | Reference count written by SW to acknowledge a processed interrupt.   |  |  |  |  | | --- | --- | --- | --- | | 0x0000.0000 | BusReset | RW | Default Bus Reset | |

###### Reference Count Register (ReferenceCountReg1)

|  |  |  |  |
| --- | --- | --- | --- |
| Bits of Reference Count Register | | | |
| 0x4c | | | [Reference Count Register (ReferenceCountReg1)](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld-lst:ReferenceCountReg1) |
| Bits | ID | Type | Description |
| 31 .. 00 | Count | RW | Reference count written by SW to acknowledge a processed interrupt.   |  |  |  |  | | --- | --- | --- | --- | | 0x0000.0000 | BusReset | RW | Default Bus Reset | |

###### Reference Count Register (ReferenceCountReg2)

|  |  |  |  |
| --- | --- | --- | --- |
| Bits of Reference Count Register | | | |
| 0x50 | | | [Reference Count Register (ReferenceCountReg2)](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld-lst:ReferenceCountReg2) |
| Bits | ID | Type | Description |
| 31 .. 00 | Count | RW | Reference count written by SW to acknowledge a processed interrupt.   |  |  |  |  | | --- | --- | --- | --- | | 0x0000.0000 | BusReset | RW | Default Bus Reset | |

###### Reference Count Register (ReferenceCountReg3)

|  |  |  |  |
| --- | --- | --- | --- |
| Bits of Reference Count Register | | | |
| 0x54 | | | [Reference Count Register (ReferenceCountReg3)](#ifc:InterruptGeneratorIfc/blk:InterruptGeneratorBlk/fld-lst:ReferenceCountReg3) |
| Bits | ID | Type | Description |
| 31 .. 00 | Count | RW | Reference count written by SW to acknowledge a processed interrupt.   |  |  |  |  | | --- | --- | --- | --- | | 0x0000.0000 | BusReset | RW | Default Bus Reset | |