Digital Relaying with an Instantaneous Overcurrent Element: A SLG Fault Simulink Case Study

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***Abstract*—This paper presents a digital relaying scheme for detecting single line-to-ground (SLG) faults using a digital signal processing approach within MATLAB Simulink environment. Although the power system is modeled with 12 generators, they are interconnected on a common bus, effectively representing a single-machine equivalent for analysis. The objective is to evaluate steady-state, permanent, and transient fault conditions while ensuring reliable overcurrent element performance. The proposed method employs a robust filtering subsystem that combines a second-order Butterworth filter, zero-order hold sampling, a 16-tap FIR filter, and a discrete Fourier transform block to accurately extract the fundamental 60Hz component from the current signals. The extracted signal is then compared against a threshold within a tripping logic scheme, which triggers the fault detection. Simulation results demonstrate successful detection of single line-to-ground faults at various line conditions, confirming the method's accuracy and reliability.**

I. Introduction

The reliable operation of modern power systems depends on fast and accurate fault detection and isolation. Protective relays are key elements in this framework, with overcurrent relays being among the most commonly used due to their simplicity and effectiveness. As power systems grow in complexity due to high-capacity generation, long transmission lines, and diverse operating conditions, traditional protection methods face increasing limitations in adaptability, speed, and precision.

Digital signal processing (DSP) has opened new possibilities in the field of protective relaying, enabling the development of intelligent, reconfigurable, and high-performance digital relays. These systems can implement advanced filtering and decision-making algorithms to improve fault detection, especially under challenging conditions such as high-impedance faults or noisy environments. The ability to sample, process, and extract the fundamental frequency component of a current signal in near real-time makes digital relays particularly attractive for modern applications.

This paper presents a Simulink case study of a digital instantaneous overcurrent relay designed to detect single line-to-ground (SLG) faults. The test system consists of twelve 350 MVA generators connected to a common bus, modeled as a single equivalent machine, feeding a 13.8/735 kV step-up transformer. Two long (200 km) high-voltage transmission lines connect the transformer to a remote bus, which is tied to an infinite bus rated at 20,000 MVA. Due to the significant capacitance of the lines, 200 MVAR of reactive compensation is applied at each line terminal.

Traditional overcurrent protection schemes have typically relied on electromechanical relays using instantaneous or inverse-time characteristics. While these methods are effective under many conditions, they are less suited to high-speed, high fidelity fault detection in today's dynamic grid environments. More recent approaches incorporate digital filtering such as active Butterworth filters and finite impulse response (FIR) filters combined with phasor estimation techniques like the Discrete Fourier Transform (DFT). These techniques have been shown to significantly improve fault detection accuracy and reduce false trips, especially under non-ideal conditions.

In this work, a multi-stage filtering and tripping architecture is developed using Simulink. The relay system includes a second-order Butterworth bandpass filter, zero-order hold sampling, a 16-tap FIR filter, and a DFT phasor extraction stage. The resulting RMS current values are compared against a predefined pickup threshold in a logic block that generates trip signals when overcurrent conditions are detected.

This paper is organized as follows.

- **Section II**: Describes the power system in Simulink, including all it's relevant parameters.
- **Section III**: Presents the design of the digital relay architecture.
- **Section IV**: Outlines the protection scenarios studied and discusses the simulation results
  - Steady-state conditions,
  - Permanent faults,
  - Transient fault conditions with reclosing.
- **Section V**: Conclusions about the work developed are given.

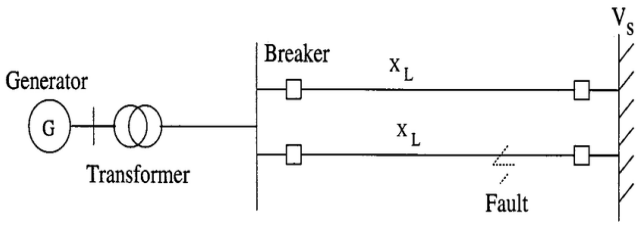

Fig. 1. General and Simplified One Line Diagram of the Case Study System.

II. Case Study System

The simulated system represents a high capacity generation site connected to a remote grid through long-distance transmission lines. The generation plant consists of twelve identical synchronous generators, each rated at 350 MVA and connected to a common 13.8 kV bus. For analysis purposes, this arrangement is treated as a single equivalent machine with an aggregated rating of 4200 MVA.

The 13.8 kV bus feeds a step-up transformer rated at 4200 MVA, 13.8/735 kV. On the high-voltage side, two 200 km overhead transmission lines connect the system to a remote bus, which interfaces with an infinite bus representing the external grid. The equivalent generator operates under steady-state conditions with a mechanical power input of 0.77 pu and field excitation set at 1.03 pu. The infinite bus is modeled with a short-circuit strength of 20,000 MVA to emulate a strong grid connection.

Fig. 1 shows the single-line diagram of the system, including the generator block, step up transformer, transmission lines, shunt compensators, and the infinite bus. From table I to table III the parameters of the model are shown.

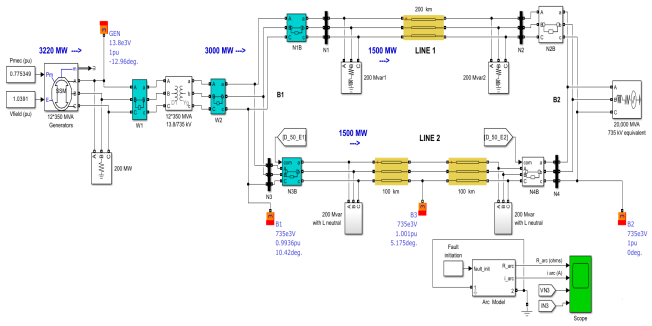

Fig. 2. Detailed Simulink System.

TABLE I
Transmission Line Parameters

Parameter	Line 1	Line 2
Resistance (ohm/km)	0.01165	0.01165
Inductance (H/km)	0.8679×10^{-3}	0.8679×10^{-3}
Capacitance (F/km)	13.41×10^{-9}	13.41×10^{-9}
Length (km)	200	200

TABLE II
Transformer Parameters (D1-Yg)

Parameter	Winding 1	Winding 2
Phase Voltage (V)	13.8 kV	735 kV
Winding Resistance	0.002	0.002
Leakage Reactance	0.08	0.08
Magnetization:	Resistance = 500, Inductance = 500	

A. Simulation Settings

The model is implemented and executed in Simulink using a fixed-step solver (ode4, Runge–Kutta). The simulation is set to run for 1 second with a fixed time step of 1e-5 s, which ensures sufficient accuracy to capture fast transient dynamics. Discrete blocks such as the filtering system and fault initiation modules are also configured with a sampling time of 1e-5 s, providing high-resolution signal processing for fault detection.

To improve performance while preserving numerical accuracy, zero crossing detection is enabled, which is particularly important for tracking the precise instant of fault inception and breaker operation. These settings ensure that the system dynamics, filtering behavior, and trip signals are accurately captured.

TABLE III
Generator Parameters

Parameter	Value
Rated Power	12×350 MVA (4,200 MVA)
Terminal Voltage	13.8 kV
Frequency	60 Hz
Inertia	∞
Damping Factor	0
Number of Pole Pairs	2
Internal Impedance	$R = 0.22/15 \approx 0.0147$, $X = 0.22$
Mechanical Power (P_{mec})	0.7753 pu
Field Voltage (V_{field})	1.0391 pu
Initial Conditions	dw% = 0, th = $-3.67°$, $I_a = I_b = I_c = 0.7694$, $\phi_a = -17.78°$, $\phi_b = -137.78°$, $\phi_c = 102.22°$

III. Relay Signal Processing Architecture

The relay signal processing architecture is the core of the digital protection scheme, responsible for accurately filtering the raw current signals and generating a trip command upon detecting overcurrent conditions. This section outlines the two main subsystems: the filtering subsystem and the relay logic with threshold setting (tripping stage).

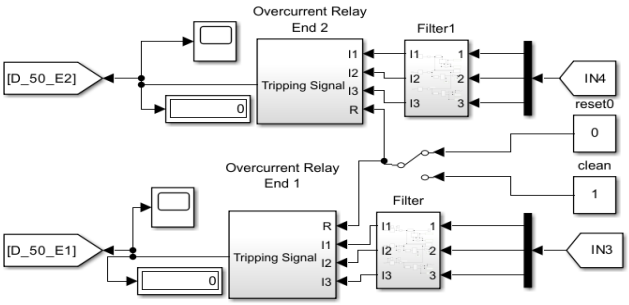

Fig. 3. Measurement, Filtering and Tripping Blocks.

A. Filtering Subsystem

The filtering subsystem is designed to isolate the fundamental 60 Hz component from the current transformer (CT) outputs while rejecting unwanted noise and harmonics. This process is performed in several stages, as described below.

1) Butterworth 2nd-Order Bandpass Filter: Initially, the analog signal from the CT is conditioned by a second-order Butterworth lowpass filter. This filter is set with a edge of $2\pi \cdot 360$ rad/s (360 Hz) to attenuate high-frequency noise and harmonics that are not of interest.

2) Zero-Order Hold Sampling: After analog conditioning, the filtered signal is discretized using a zero-order hold (ZOH) sampler. In our configuration, the ZOH produces approximately 8 samples per cycle. With an effective sampling frequency of about 500 Hz (sample time of 0.002 s), the digital representation preserves the information for accurate processing.

3) 16-Tap FIR Filter: Following the ZOH, the digitized signal is processed by a 16-tap Finite Impulse Response (FIR) filter designed to isolate the fundamental 60 Hz component by reducing the frequency content to a narrow band around 60 Hz (55 Hz to 65 Hz). The output $y[n]$ of the FIR filter is defined by the convolution of the input signal $x[n]$ with the filter's impulse response $h[k]$:

$$y[n] = \sum_{k=0}^{N-1} h[k]\, x[n-k], \tag{1}$$

where $N = 16$ is the number of taps.

To design the FIR filter, we start with the ideal impulse response of a bandpass filter that passes frequencies between ω_1 and ω_2. The ideal impulse response is given by:

$$h_{\text{ideal}}[n] = \begin{cases} \dfrac{\sin\left[\omega_2\,(n-\alpha)\right] - \sin\left[\omega_1\,(n-\alpha)\right]}{\pi\,(n-\alpha)}, & n \neq \alpha, \\ \dfrac{\omega_2 - \omega_1}{\pi}, & n = \alpha, \end{cases} \tag{2}$$

where the center index α is defined as:

$$\alpha = \frac{N-1}{2}. \tag{3}$$

For our design, a bandwidth from 55 Hz to 65 Hz with a sampling frequency of $f_s = 500$ Hz, the normalized angular frequencies (in rad/sample) are:

$$\omega_1 = 2\pi\frac{55}{500} \quad \text{and} \quad \omega_2 = 2\pi\frac{65}{500}. \tag{4}$$

Since the ideal impulse response in Equation (2) is infinite in length, it is truncated to $N = 16$ taps. To mitigate the spectral leakage introduced by truncation, a window function is applied. A common choice is the Hamming window, defined as:

$$w[n] = 0.54 - 0.46\cos\left(\frac{2\pi n}{N-1}\right), \quad n = 0, 1, \ldots, N-1. \tag{5}$$

The final FIR filter coefficients are computed by multiplying the ideal impulse response by the window function:

$$h[n] = h_{\text{ideal}}[n]\, w[n], \quad n = 0, 1, \ldots, N-1. \tag{6}$$

For instance, in MATLAB the coefficients can be obtained using:

```
fs=500;          % Sampling frequency in Hz
passband=[55 65]; % Desired passband in Hz
N = 16;                    % Number of taps
b = fir1(N-1, passband/(fs/2),
'bandpass', hamming(N));
```

TABLE IV
FIR FILTER COEFFICIENTS

Coefficient	Value	Coefficient	Value
$h[0]$	-0.0013	$h[1]$	-0.0048
$h[2]$	-0.0086	$h[3]$	0.0032
$h[4]$	0.0201	$h[5]$	0.0347
$h[6]$	0.0412	$h[7]$	0.0438
$h[8]$	0.0438	$h[9]$	0.0412
$h[10]$	0.0347	$h[11]$	0.0201
$h[12]$	0.0032	$h[13]$	-0.0086
$h[14]$	-0.0048	$h[15]$	-0.0013

A representative set of coefficients is:

The FIR filter is an essential component of our digital relaying scheme. It narrows the frequency band to capture only the 60 Hz fundamental.

4) DFT and Peak-to-RMS Conversion: After the FIR filter, the signal undergoes further processing through a Discrete Fourier Transform (DFT) block to extract the 60 Hz phasor. The DFT computes the frequency spectrum of the filtered signal, isolating the magnitude and phase of the fundamental frequency component. The extracted peak value is then converted to its RMS equivalent, providing an accurate measure of the fault current magnitude for comparison against a predetermined threshold in the relay logic.

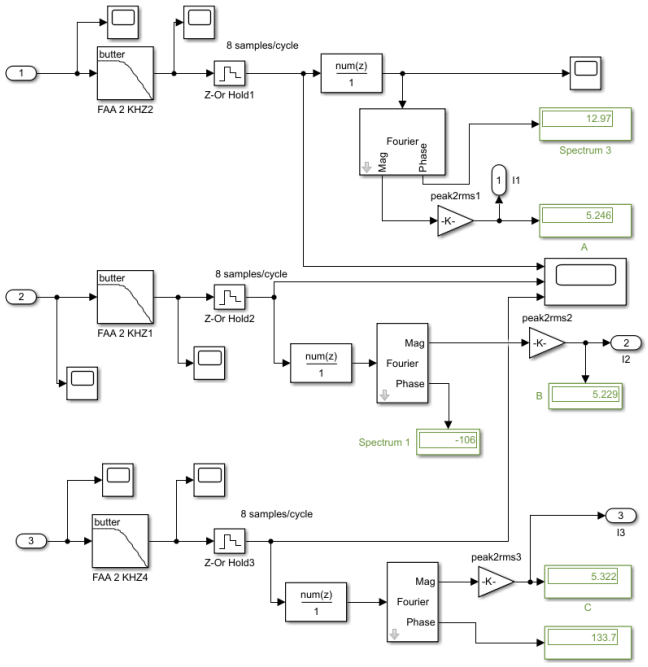

Fig. 4. Filtering Subsystem: Butterworth Filter, Zero Order Holder, 16 Tap FIR Filter and a DFT Block to Obtain the 60Hz RMS Phasor Measurement.

B. Tripping Stage

The tripping stage is responsible for comparing the processed current signals against a predetermined overcurrent threshold and generating a trip command when a fault condition is detected. This stage operates on the signal after it has

been filtered, sampled, and processed by the 16-tap FIR filter and DFT block to extract the 60 Hz fundamental component.

The overcurrent condition for each phase is determined by comparing I_{rms} to the pickup threshold I_{pickup}. Mathematically, the trip decision for each phase is expressed as:

$$T = \begin{cases} 1, & \text{if } I_{\text{rms}} > I_{\text{pickup}}, \\ 0, & \text{otherwise.} \end{cases} \tag{7}$$

Once the overcurrent condition is evaluated for each phase, the overall trip signal T is generated by combining the phase-specific trip outputs using an OR logic operation:

$$T = T_a \vee T_b \vee T_c. \tag{8}$$

This ensures that if any phase exceeds the pickup threshold, the relay will trip.

Additionally, an SR flip-flop is employed in the tripping stage to latch the trip condition. Once set ($T = 1$), the flip-flop maintains the trip state until a reset signal is provided. This tripping stage can be realized with digital comparators and logic gates in a microprocessor-based relay system.

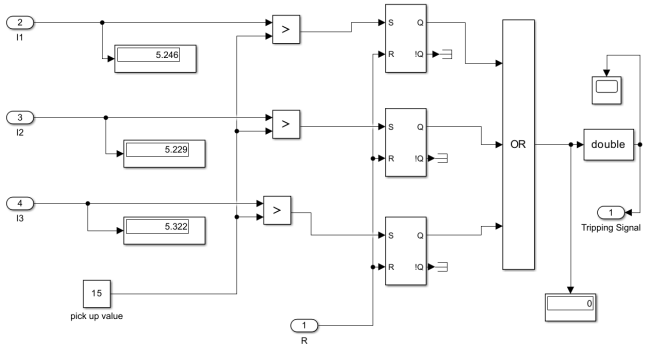

Fig. 5. Tripping Subsystem: Digital Comparator, Latching System and Logic Decision Blocks.

IV. Case Study: Simulation Results and Discussion

The case study is divided into three main parts: analysis of steady-state conditions, evaluation of permanent faults, and examination of transient fault conditions with automatic recloser operation.

A. Steady-State Analysis

The system is analyzed under normal operating conditions (without any fault). The primary objectives are to verify that the system maintains stable voltage and current profiles and that the relay does not trip in the absence of a fault. Under steady state, the raw current measurements show a peak value of 14.9 A, corresponding to an RMS value of 10.53 A. However, after sampling, filtering, and fundamental extraction, the computed RMS value is approximately 5.3 A. This reduction in amplitude is primarily due to the FIR filter design, which deliberately narrows the passband (55 Hz to 65 Hz) to isolate the 60 Hz fundamental component. Although this filtering process attenuates the signal, the relative relationship remains consistent, so a calibration factor can be applied to display the real RMS value if required.

Figures 6 and 7 show the steady state operation: node 3 and node 4 voltages and currents.

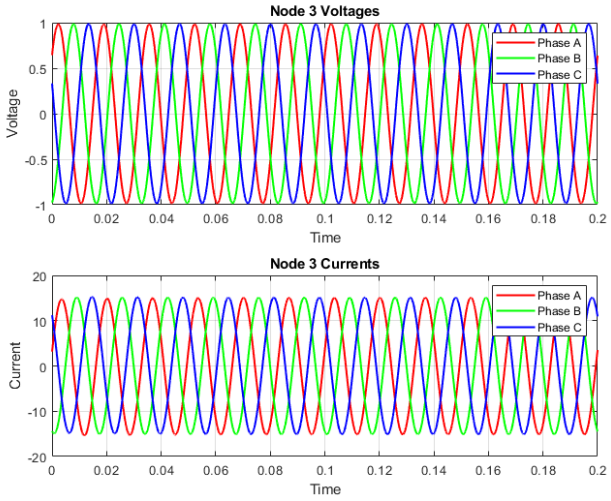

Fig. 6. Node 3 Steady State Voltages and Currents.

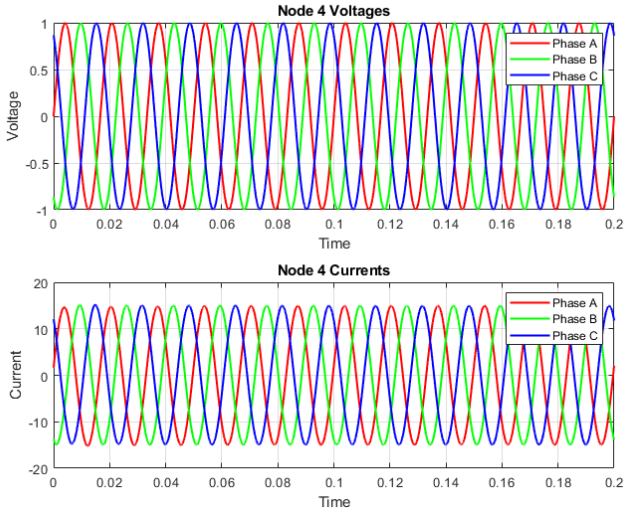

Fig. 7. Node 4 Steady State Voltages and Currents.

The sampler output for the phase A current (node 3 measurement) with 8 samples per cycle and the FIR filter output for phase A (Fig. 8) reveals a lower amplitude compared to the raw sampled signal. This phenomenon is expected, as windowed FIR filters (such as our 16-tap design) inherently introduce an attenuation factor due to the effects of truncation and windowing. Importantly, this reduction is consistent across operating conditions; hence, the decision logic in the relay is based on the relative change in current magnitude rather than its absolute value.

The steady state analysis confirms that the system operates at approximately 1 p.u. voltage with a processed RMS current of 5.3 A. Currents that exceed this steady state level indicate

the presence of a fault, which justifies the need for accurate steady state characterization to properly set the relay pickup value.

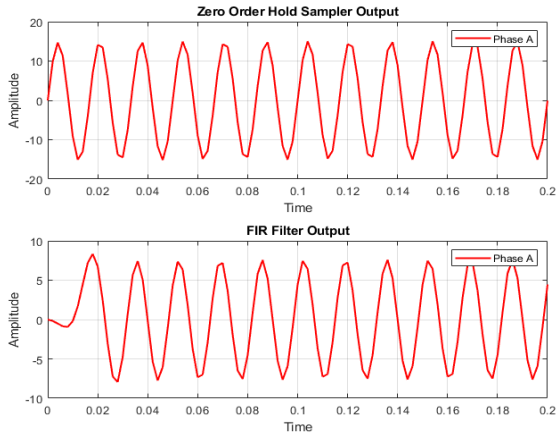

Fig. 8. Zero Order Holder Sampler and FIR Filter from the Node 3: Steady State Outputs.

B. Permanent Fault Analysis

This subsection evaluates the system response when a permanent single line-to-ground (SLG) fault is introduced. Two fault locations are considered: one at the bus end (2% of the line) and another at 80% of the line length. Faults are simulated with both 0 ohm and high fault impedance.

1) Fault at 2% of the Line and 0Ω Fault Impedance: The single line to ground fault (unbalanced fault) at 2% of the line produces significant asymmetry through the injection of positive, negative, and zero sequence components. As a result, both the faulted phase A and the non-faulted phase C experience voltage depressions (0.55 pu at the fault node), even though only phase A is directly affected. The fault generates an initial transient surge in phase A current (peaking near 290 A) that decays to a steady-state value (around 168 A), while phase B and phase C currents also exhibit notable changes (phase B increasing from 15 to 30 A), these phenomena is shown in Fig. 9.

The zero-order and FIR filter outputs (see Figure 11) capture these transient phenomena, with the filtered fundamental RMS component in phase A remaining elevated relative to its steady-state level.

At bus 4, the effects are attenuated by the line impedance. Here, although phase B again doubles from its pre-fault value (15 to 30 A), the fault-induced imbalance is less severe, so that phase A voltage recovers to about 0.63 pu and its current settles near 40 A, while phase C drops to a lower steady state (around 7 A). This spatial variation is explained by the transformation and propagation of the sequence components along the line, it results in a moderated unbalance at the remote end compared to the fault location (see Figures 9 and 10).

The observed differences between the fault node (bus 3) and the remote node (bus 4) are a consequence of the system's symmetrical component behavior, the distribution of fault currents through interconnected sequence networks, and the impedance effects along the transmission line.

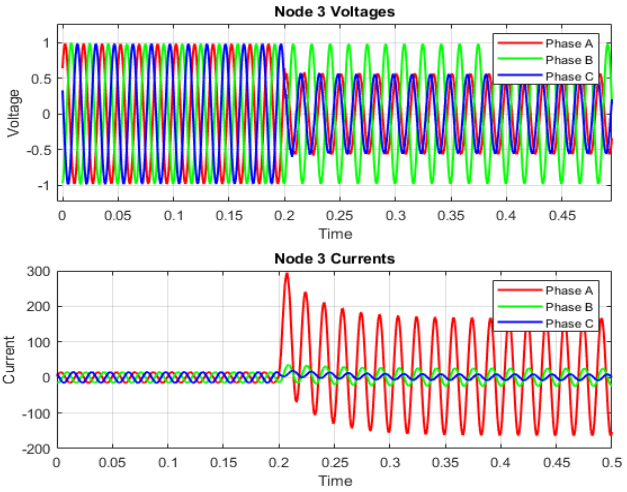

Fig. 9. Node 3 Permanent Fault (2% Line and 0Ω Fault Impedance) Voltages and Currents.

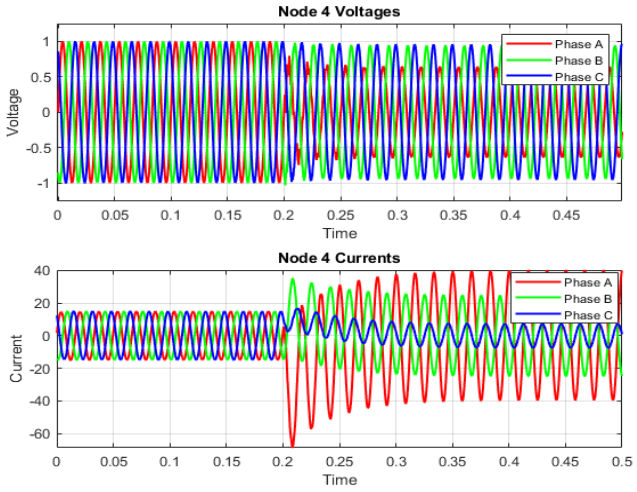

Fig. 10. Node 4 Permanent Fault (2% Line and 0Ω Fault Impedance) Voltages and Currents.

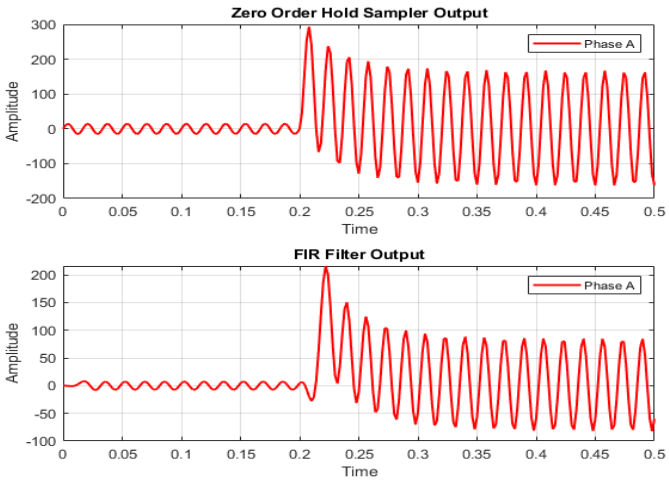

Fig. 11. Zero Order Holder Sampler and FIR Filter from the Node 3: Permanent Fault (2% Line and 0Ω Fault Impedance) Outputs.

2) Fault at 80% of the Line and 0Ω Fault Impedance: At Node 3, which is further from the fault location, the fault results in a moderate voltage depression on phases A and C (0.77 pu), while phase B maintains its nominal voltage of 1 pu. The transient behavior in phase A is evident as the current initially surges to 64 A before decaying to a steady-state value of 38 A. Although the currents in the other phases remain largely unchanged, their frequency and phase characteristics exhibit slight transient disturbances.

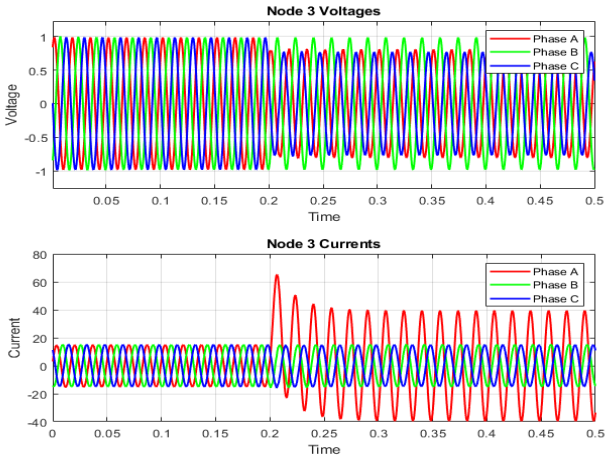

Fig. 12. Node 3 Voltages and Currents under a Fault at 80% of the Line with $Z_f = 0$.

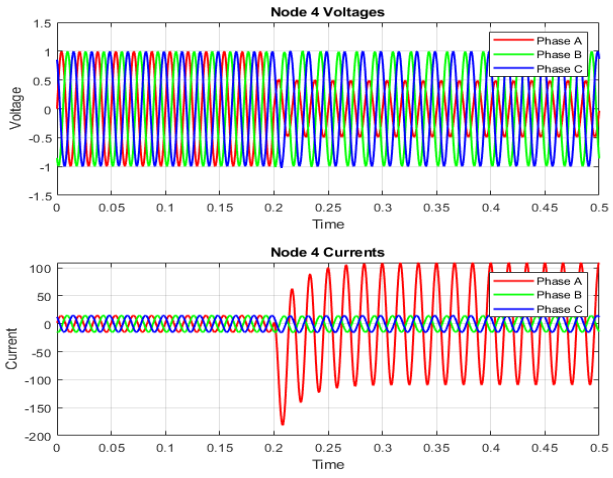

Fig. 13. Node 4 Voltages and Currents under a Fault at 80% of the Line with $Z_f = 0$.

In contrast, node 4, being closer to the fault (separated by only 20% of the line impedance), displays more pronounced fault effects. Here, the voltages on phases B and C hold at 1 pu, but phase A is severely depressed to around 0.49 pu. The phase A current exhibits a dramatic initial negative transient, with a spike of -180 A, before reaching a steady state of 108 A. This marked difference in voltage and current profiles between Node 3 and Node 4 highlights the attenuation and phase transformation effects introduced by the line impedance.

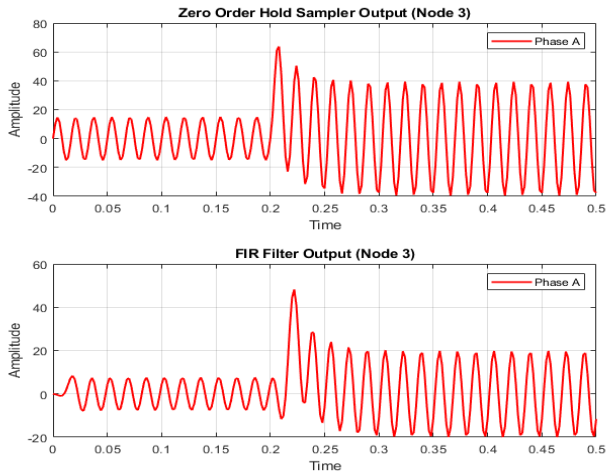

Fig. 14. Zero Order Hold Sampler and FIR Filter outputs for Phase A Current at Node 3 under Fault at 80% of the Line with $Z_f = 0$.

Fig. 14 shows the dynamic response of phase A current at node 3 as processed by the zero order hold sampler and FIR filter. The positive transient spike captured here reflects the initial surge in phase A current due to the fault, followed by its decay to the permanent fault level. This processed output effectively isolates the fundamental components while demonstrating the transient behavior associated with the fault.

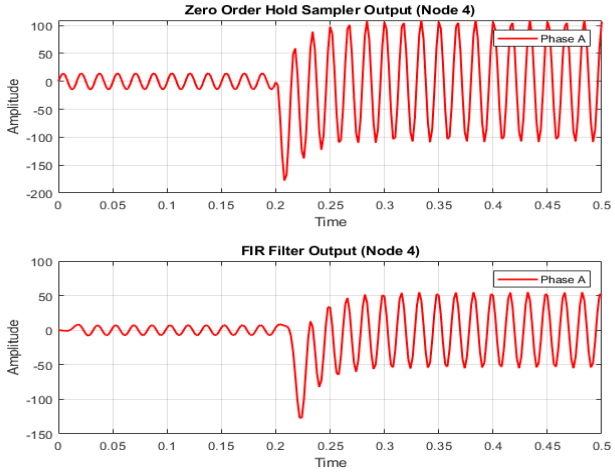

Fig. 15. Zero Order Hold Sampler and FIR Filter outputs for Phase A Current at Node 4 under Fault at 80% of the Line with $Z_f = 0$.

Fig. 15 presents the corresponding sampler and FIR filter output for phase A at Node 4. Here, the processed signal reveals a pronounced negative transient spike that is almost three times as severe as that at Node 3. This difference shows the stronger fault impact at Node 4 due to its closer proximity to the fault, despite the fault occurring with zero fault impedance.

3) Fault at 80% of the Line with 175Ω Fault Impedance:

At Node 3, the fault condition with a 175Ω impedance results in a slight depression of the phase A voltage (0.945 pu) compared to the other phases (0.98 pu). The fault current in phase A increases to 22 A, while the load currents in the remaining phases remain unchanged. This moderate change indicates that the fault is not as severe at this node, yet it still imposes a noticeable asymmetry on the system.

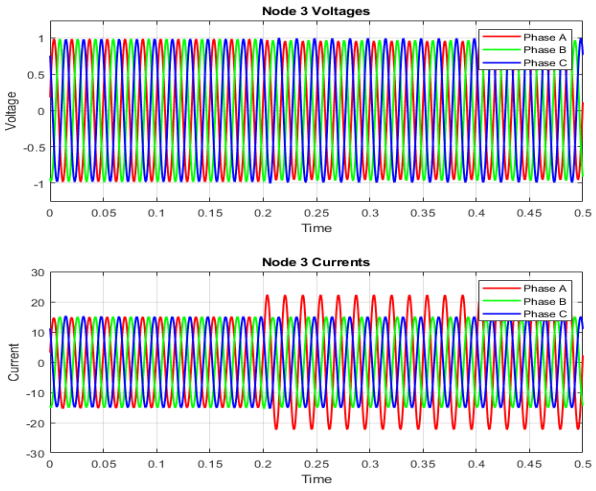

Fig. 16. Node 3 Voltages and Currents under Fault at 80% of the Line with 175 175Ω Fault Impedance.

Node 4 is located closer to the fault, the phase A voltage recovers to about 0.974 pu with the other phase voltages sustaining 1.0 pu. Interestingly, the phase A current decreases from its normal load value (14.9A) to 9 A. This reduction in current is critical because it implies that a conventional overcurrent protection element would not see a sufficient fault current at Node 4 to initiate a trip.

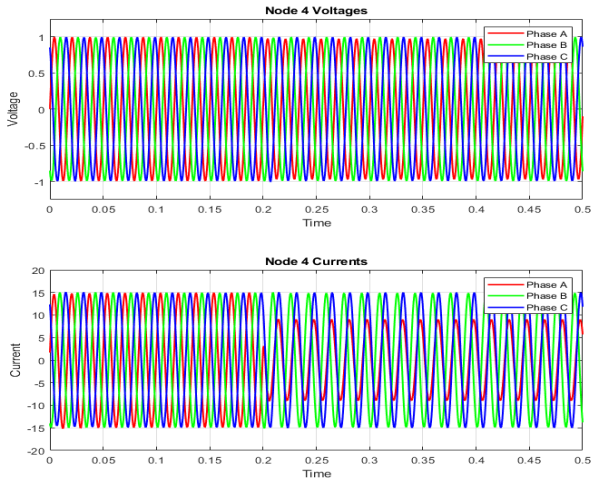

Fig. 17. Node 4 Voltages and Currents under Fault at 80% of the Line with 175Ω Fault Impedance.

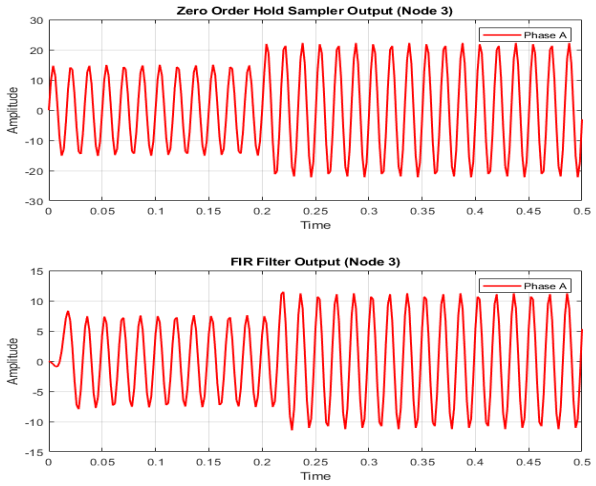

Fig. 18. Zero Order Hold Sampler and FIR Filter output for Node 3 Phase A current under Fault with 175Ω Impedance.

The outputs from the zero order hold sampler and FIR filter for Node 3 clearly capture a transient amplification of the phase A current about 1.4 times its normal value. Based on this behavior, we infer that for the relay to reliably detect and clear the fault at Node 3, the minimum fault pickup current should be set to approximately 1.4 times the steady-state load current. With a steady-state current of 14.9 A, this translates to a peak pickup of 20.86 A (14.75 A RMS).

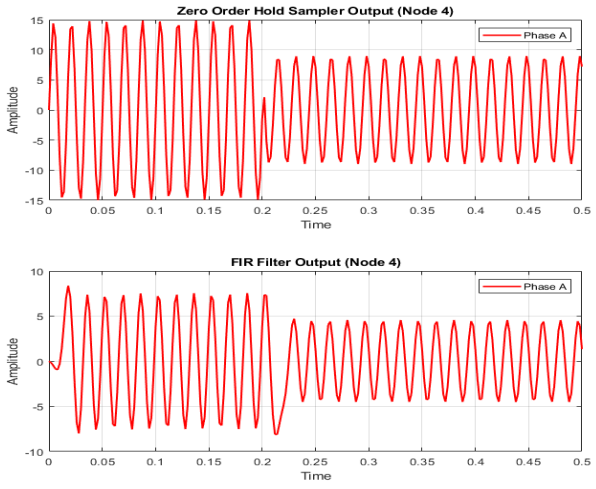

Fig. 19. Zero Order Hold Sampler and FIR Filter output for Node 4 Phase A current under Fault with 175Ω Impedance.

At node 4, the sampled and filtered data reveal a reduction in the phase A current to nearly 60% of its steady-state level. This diminished current means that conventional overcurrent protection cannot reliably detect the fault at Node 4, the measured current is lower than the normal load current. In such scenarios, alternative protection schemes must be considered.

High impedance faults (HIFs) which are characterized by fault currents significantly lower than conventional levels due to high fault impedance require special detection techniques. These techniques often incorporate methods such as harmonic analysis, transient waveform monitoring, and pattern recognition to identify the subtle signatures of HIFs, ensuring that even low-level fault currents are detected and appropriate remedial action (such as breaker tripping or alarm generation) is initiated.

For a fault at 80% of the line with a 175Ω fault impedance, node 3 shows a moderate increase in phase A current from 14.9A to 22A and a voltage dip to 0.945 pu, resulting in a current pickup requirement of approximately 1.4 times the steady state value for tripping (14.75A RMS or 7.375A RMS after the FIR filter). At node 4, the fault current in phase A drops below the load current, hence, the use of high impedance fault detection techniques must be used to ensure proper protection.

C. Transient Fault Analysis with Automatic Recloser

Transient faults are characterized by a fault occurrence followed by clearance and subsequent reclosing of the breaker. This subsection details the dynamic response of the system during these events. A single line-to-ground fault (phase A) is applied at 50% of the line between node 3 and node 4. The fault initiates at 0.2 s with 0Ω impedance, and an automatic recloser commands at 0.4 s and 0.8 s.

Before the fault at node 3 the voltage remains steady at 1 p.u. When the fault occurs at 0.2 s, the relay trips and clears the fault within 20 ms, causing a transient voltage dip to approximately 0.65 p.u. A reclose at 0.4 s produces a transient overshoot with a voltage peak near 1.09 p.u., and after the second reclose at 0.8 s the voltage quickly returns to 1 p.u. Meanwhile, the node 3 current shows positive peaks reaching nearly 100 A during the transient events.

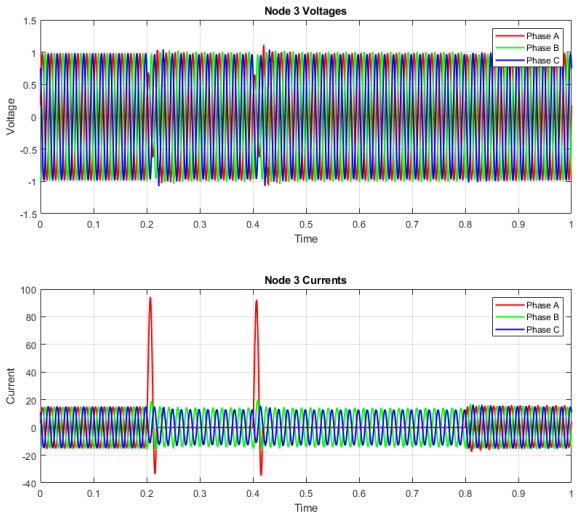

Fig. 20. Node 3 voltage and current waveforms during transient fault and reclose events.

At node 4, a similar transient behavior is observed, however, the interaction between phase A and phase C introduces additional ripple in the voltage. The node 4 voltage exhibits transient oscillations during fault clearance, and the phase A current at node 4 shows a negative peak near -100 A with pronounced ripple and a residual DC component after the fault is cleared at 0.8 s.

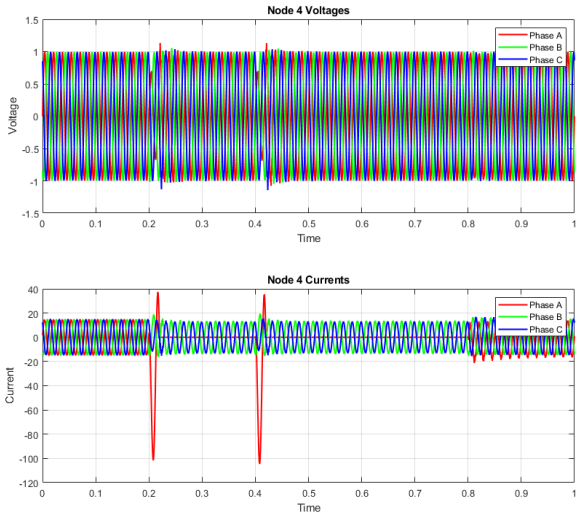

Fig. 21. Node 4 voltage and phase A current waveforms showing transient response and DC offset during recovery.

The zero-order hold sampler captures the signal with 8 samples per cycle, preserving the detailed waveform shape. After sampling, the 16-tap FIR filter narrows the frequency content to the 55–65 Hz band.

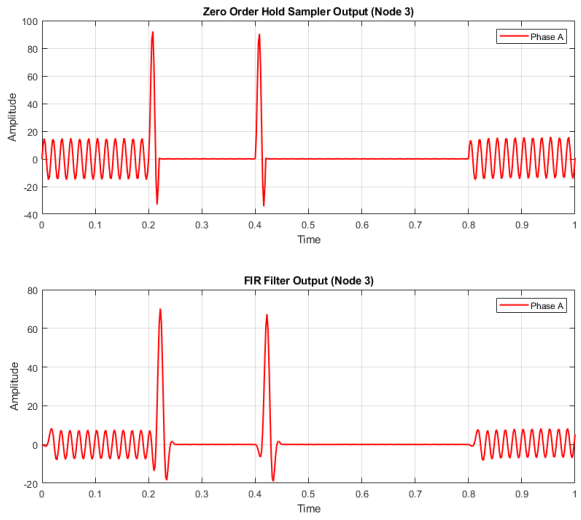

Fig. 22. Zero Order Hold Sampler and FIR Filter output for Node 3 Phase A current under a Transient Fault with 0Ω Impedance at the 50% of the Line.

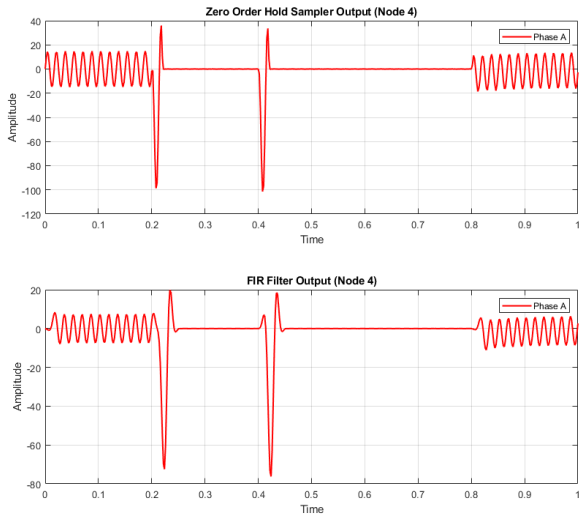

Fig. 23. Zero Order Hold Sampler and FIR Filter output for Node 4 Phase A current under a Transient Fault with 0Ω Impedance at the 50% of the Line.

In both Figures 22 and 23 , the fundamental 60 Hz component is clearly captured with the expected behavior. The relay logic successfully tracks the peaks of the FIR filter output, triggering the breaker trip signals when overcurrent conditions are detected.

These results validate the digital relaying scheme's capability to detect faults accurately and to coordinate automatic recloser operations.

V. Conclusions

This study demonstrates that a digital overcurrent relay, implemented in a MATLAB Simulink environment, is capable of accurately detecting single line-to-ground (SLG) faults under a variety of operating conditions. The proposed multi stage filtering architecture which incorporates a second-order Butterworth filter, zero-order hold sampling, a 16-tap FIR filter, and a DFT-based phasor extraction has been shown to reliably extract the 60 Hz fundamental component, even though the FIR filter introduces a consistent attenuation. This attenuation, while reducing the processed RMS current (from a raw 10.53 A to approximately 5.3 A under steady state), does not impede fault detection since the relay logic is based on the relative increase in current magnitude.

Simulation results confirm that under steady state conditions the system maintains stable voltage (1 p.u.) due to the location of our measurement devices and that any current level exceeding the calibrated steady state indicates the occurrence of a fault. Both permanent and transient fault scenarios were tested, the transient fault analysis, in particular, showed that the relay responds rapidly and that the automatic recloser effectively coordinates the clearing and reclosing actions. The distinct responses observed at different nodes are due to the impedance effects and the distribution of sequence components.

In general, the work confirms that digital relaying with an instantaneous overcurrent element can provide precise and reliable protection.

References

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