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Lab 7
3/21/17

Worksheet 1:

	h	g	f	p	d	
stage 1		1	2	2	1 1/3	3 1/3
stage 2		1	1 1/3	1 1/3	2	3 1/3
stage 3		6	2	12	1 1/3	13 1/3
Total						20

Worksheet 2:

	h	g	f	p	d	
stage 1		1	2		1 1/3	
stage 2		1	1 1/3		2	
stage 3		6	2		1 1/3	
Total		6	5.333333	32	4.666667	
			3.174802			14.19107

Modified Circuit:

	h	g	f	p	d	
stage 1		1	2	2	1 1/3	3 1/3
stage 2		1	1 1/3	1 1/3	2	3 1/3
stage 3		3	2	6	1 1/3	7 1/3
Total						14

C3 – pmos size: 2 lambda x 32 lambda **nmos size:** 2 lambda x 16 lambda
C2 – pmos size: 2 lambda x 24 lambda **nmos size:** 2 lambda x 24 lambda
C1 – pmos size: 2 lambda x 32 lambda **nmos size:** 2 lambda x 16 lambda

These sizes correspond to doubled widths of both the NAND and NOR circuits. Each stage now has input capacitance's of 12C. When driving the same 36C load, this reduces our H from 6 in the original design to 3 in our modified. This circuit was then driven with the same inverter drivers as Lab 6.

Original yzdet timing:
****** transient analysis tnom= 25.000 temp= 25.000 ******
tpdr1= 686.0806p targ= 6.0719n trig= 5.3858n
tpdf1= 723.7016p targ= 11.1046n trig= 10.3809n
tpd1= 704.8911p
tpdr7= 338.4113p targ= 15.7179n trig= 15.3795n
tpdf7= 813.4812p targ= 21.1891n trig= 20.3757n
tpd7= 575.9463p

trise= 504.5170p targ= 11.4054n trig= 10.9009n
tfall= 307.8549p targ= 6.2350n trig= 5.9272n

Improved yzdet timing:

****** transient analysis tnom= 25.000 temp= 25.000 ******
tpdr1= 467.1540p targ= 5.8778n trig= 5.4106n
tpdf1= 495.6098p targ= 10.9073n trig= 10.4117n
tpd1= 481.3819p
tpdr7= 225.7273p targ= 15.6332n trig= 15.4074n
tpdf7= 575.2619p targ= 20.9800n trig= 20.4047n
tpd7= 400.4946p
trise= 279.2990p targ= 11.0756n trig= 10.7963n
tfall= 166.5131p targ= 5.9647n trig= 5.7981n

The new circuit is much faster than the original, propagation delays were nearly cut in half all across the board.

Power analysis:

The average power was measured in the spice simulation during the worst case switching scenario, and during a quiescent period. This gives dynamic and static power for both the original and modified circuit:

Original circuit

Dynamic: avg_d_power= -10.1811m from= 15.0000n to= 16.0000n
Static: avg_q_power= -3.3815u from= 16.0000n to= 20.0000n

Improved circuit
Dynamic: avg_d_power= -13.7649m from= 15.0000n to= 16.0000n
Static: avg_q_power= -3.3802u from= 16.0000n to= 20.0000n

Both circuits have a very similar static power value, but the faster circuit draws more power during switching (~30% more power).

Estimated time to complete the lab: 4.5 hours.