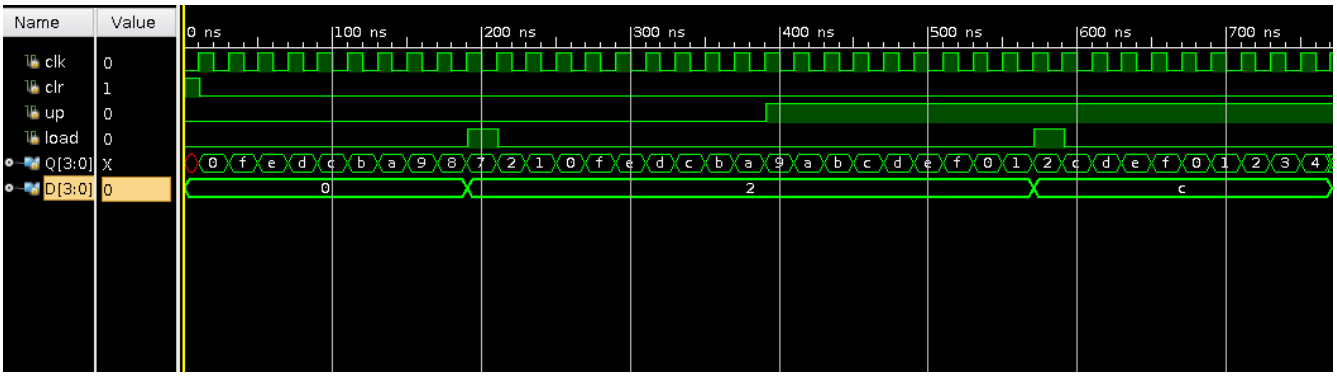
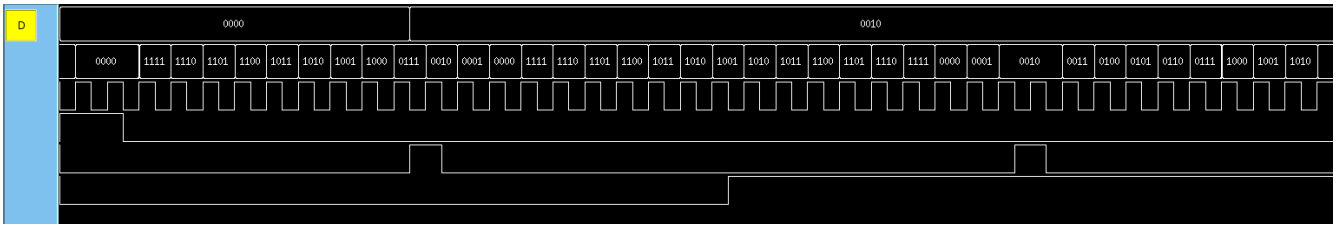
Adam Ness and Marty Townley
VLSI
Lab8

Counter simulation:

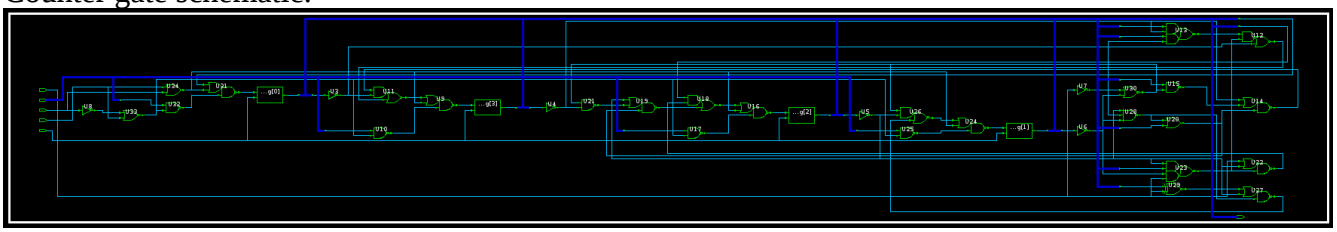


Counter IRSIM waveform:

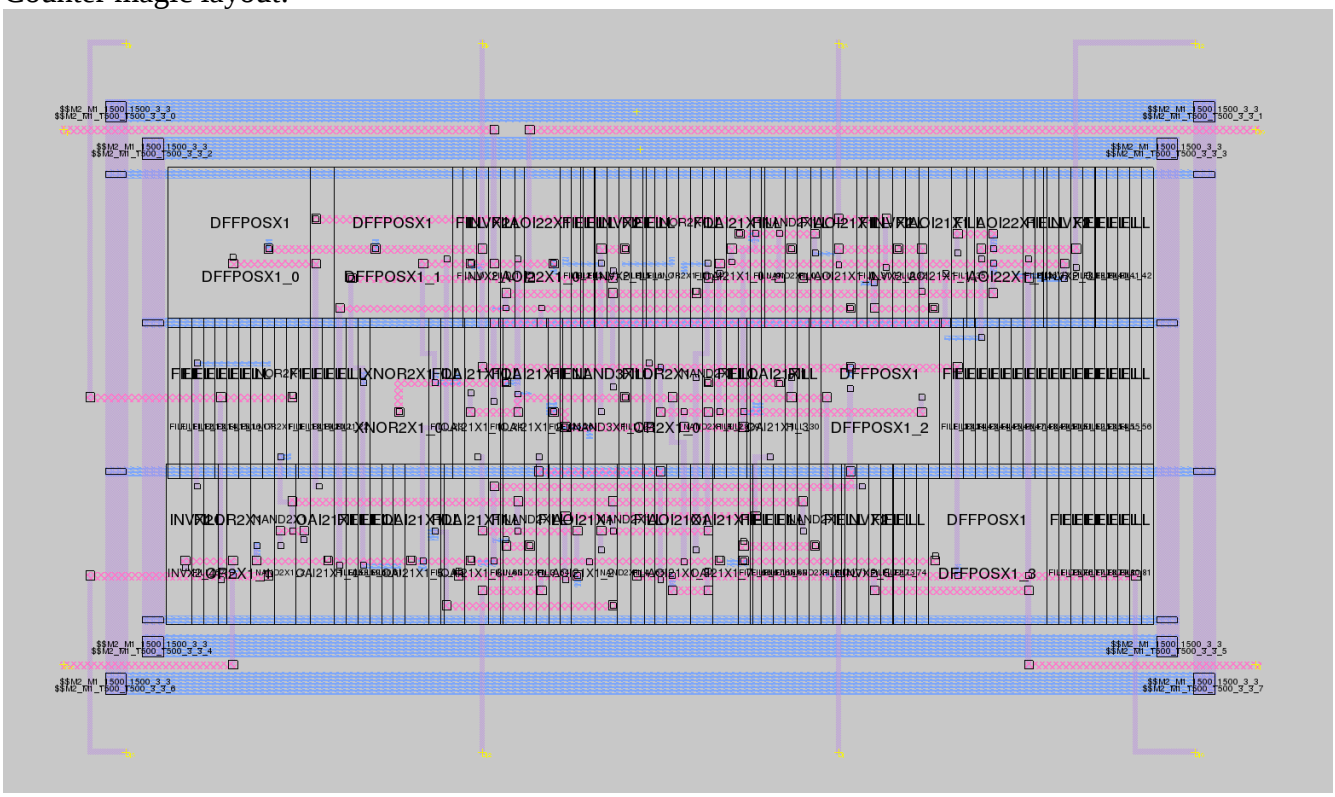


The order of the signals on the above waveform is:
D, Q, clk, clr, load, up

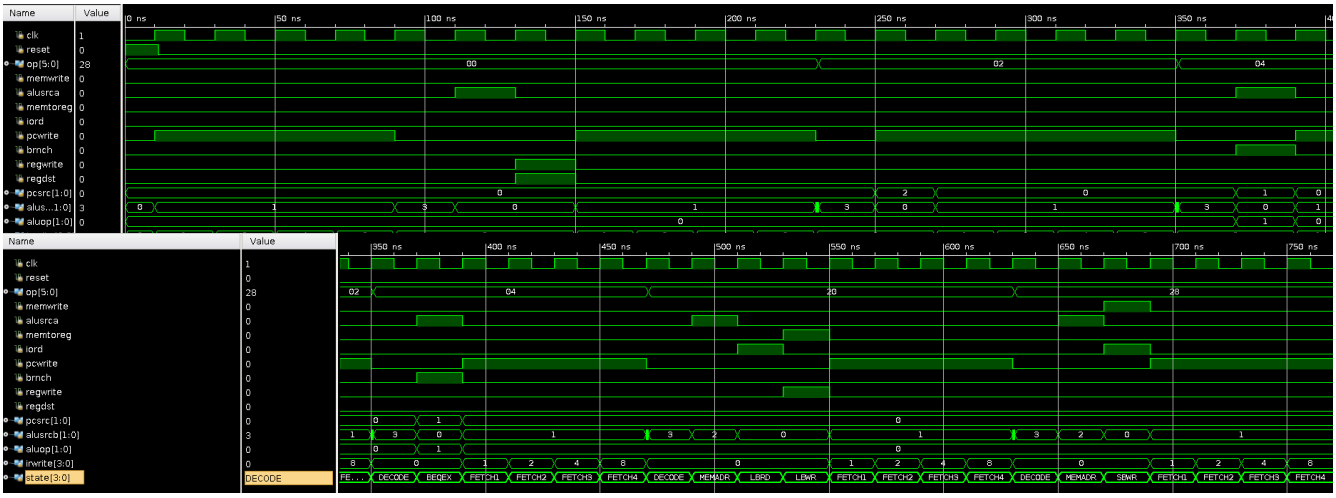
Counter gate schematic:



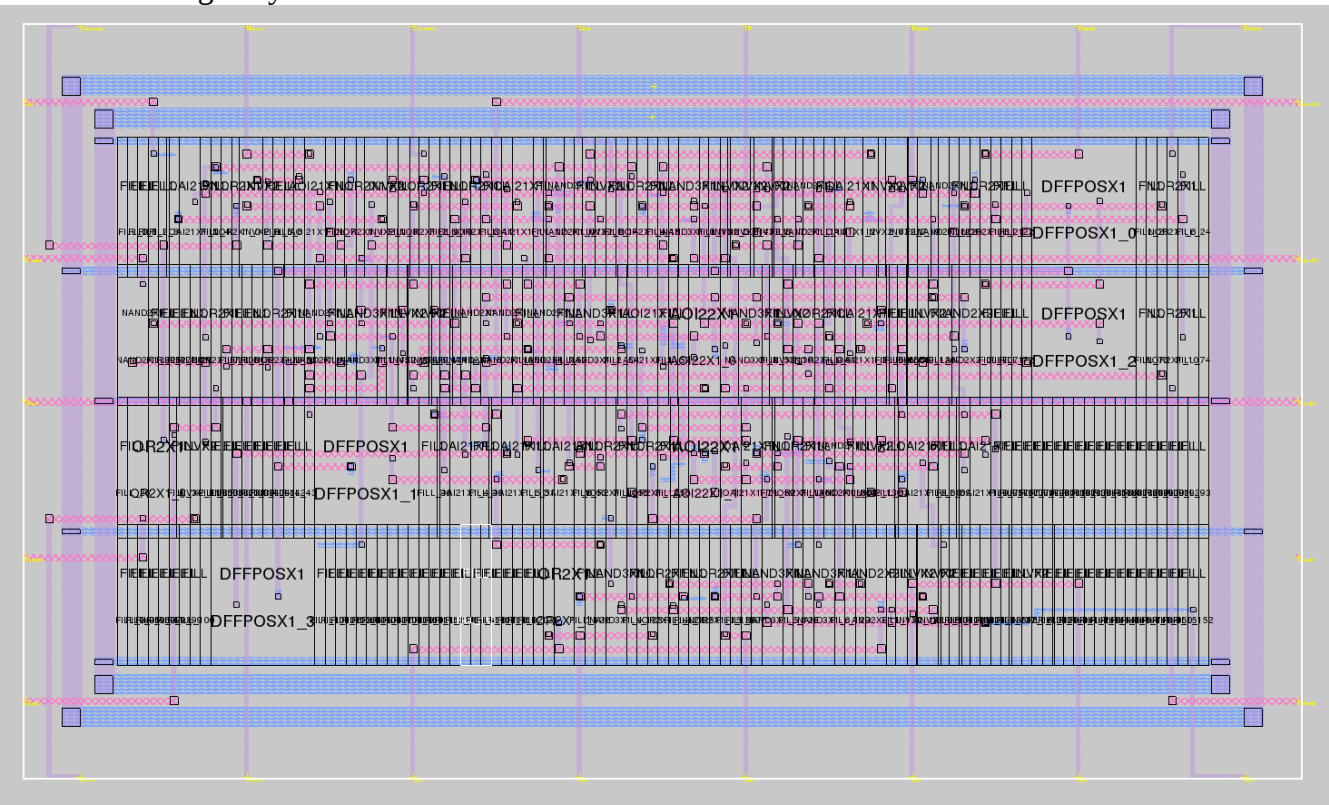
Counter magic layout:



MIPS FSM Simulation waveform:



MIPS FSM Magic layout:



MIPS FSM Magic layout sizing:

microns: 295.20 x 174.00 (0.00, 0.00), (295.20, 174.00) 51364.80
lambda: 984 x 580 (0, 0), (984, 580) 570720

Summary:
No major problems were encountered in this lab, the only issue we had was trying to figure out how to deal with a typedef enum as an input.

It took about 4 hours to do this lab