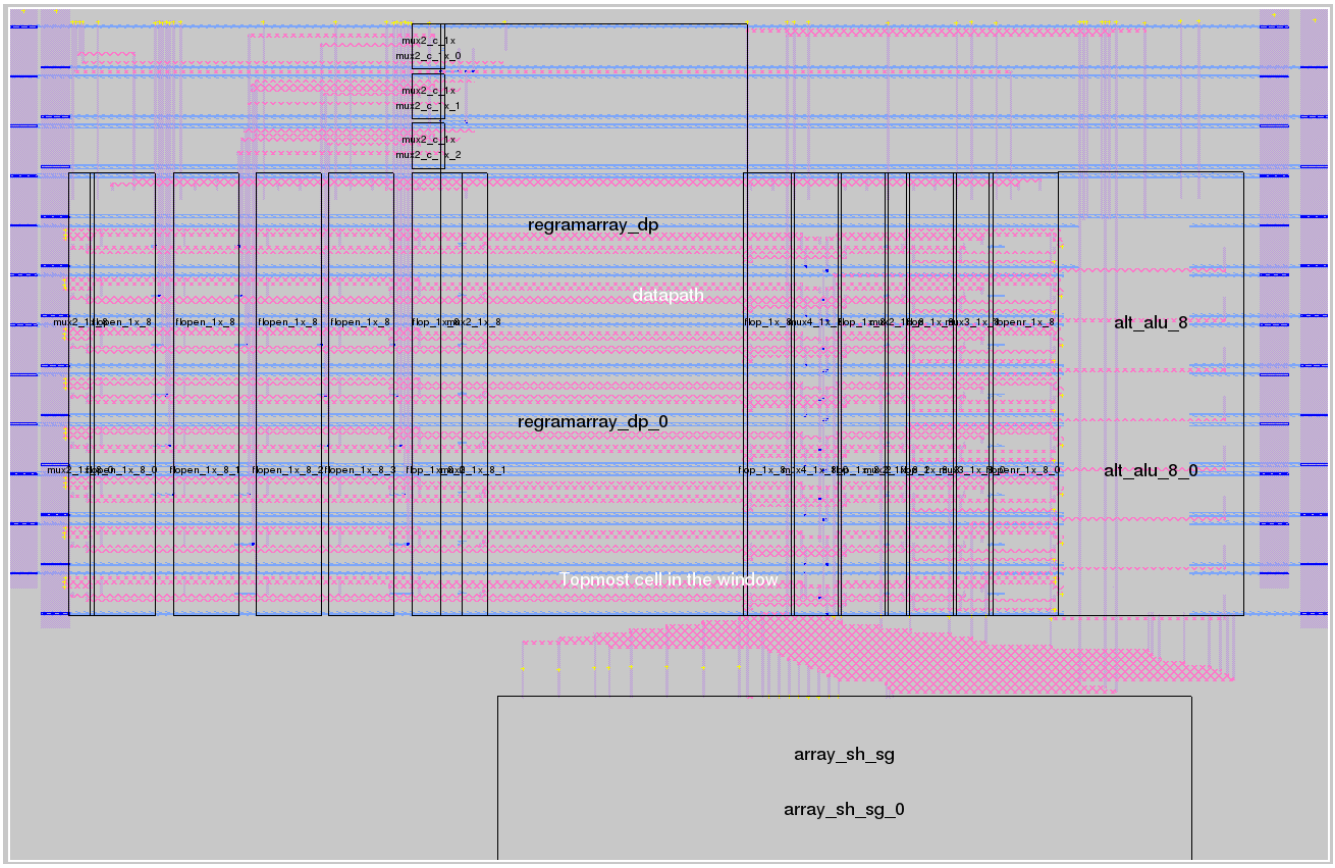
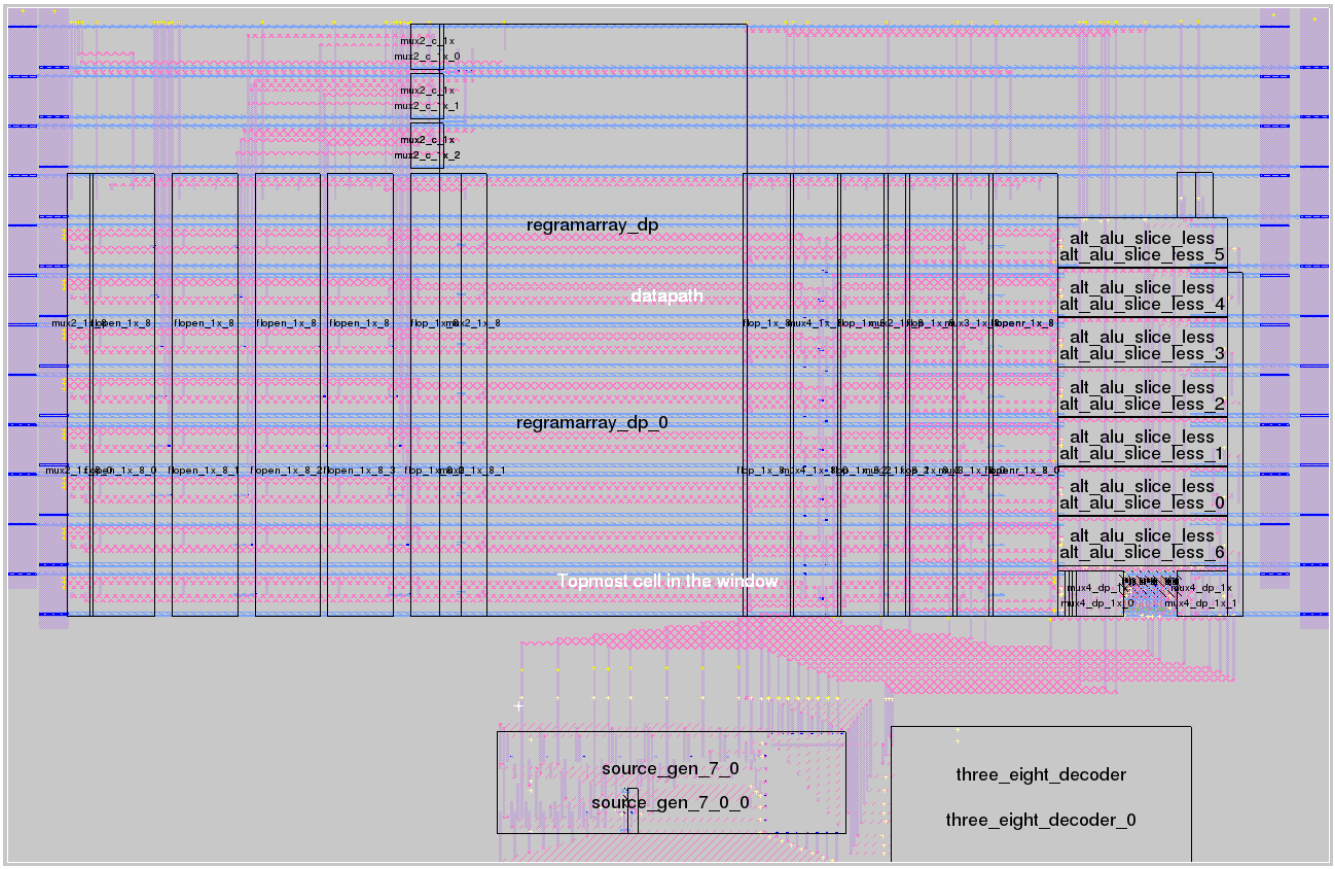
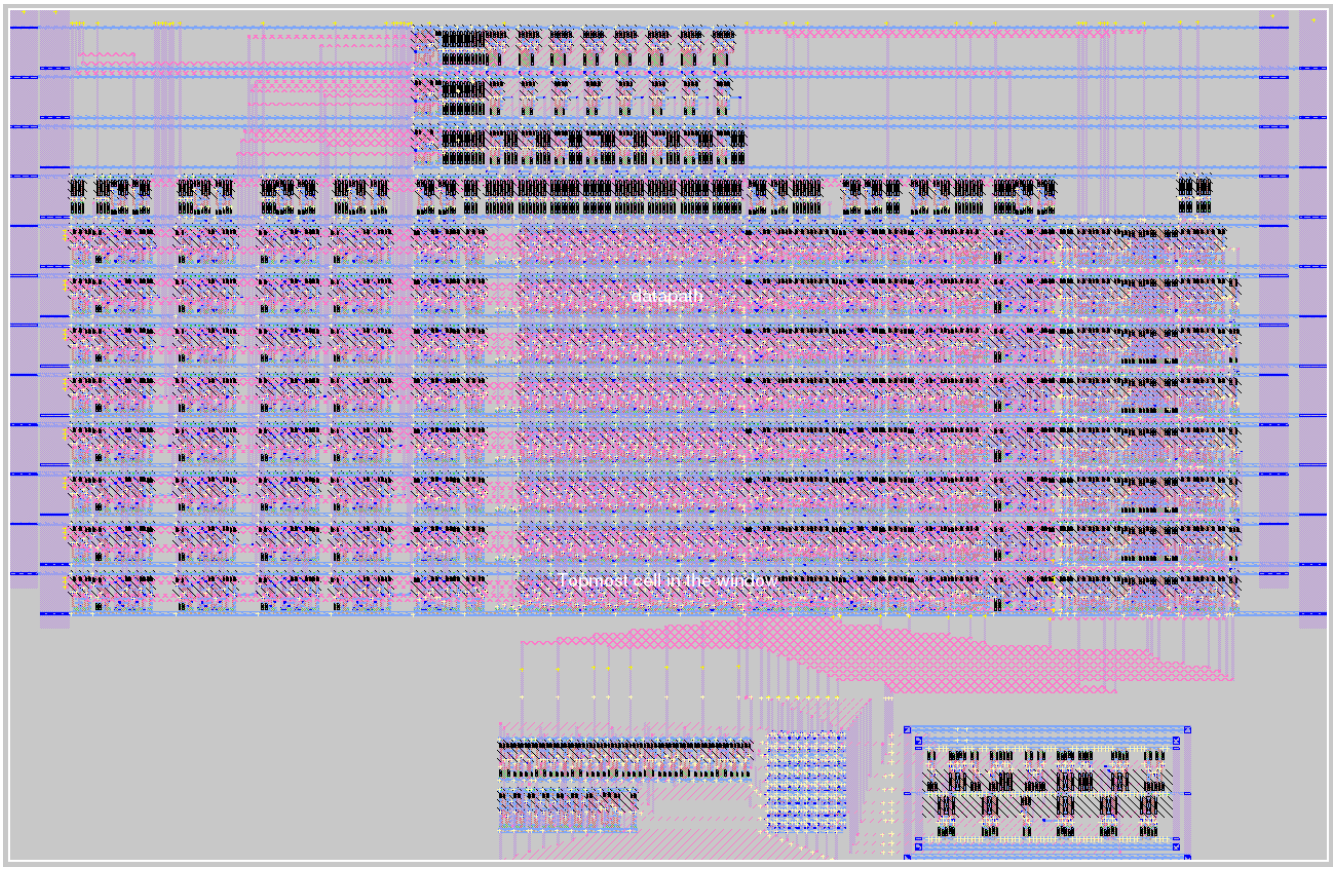
Adam Ness & Marty Townley
VLSI
4/25/17 – MIPS Project Milestone 3

Layout Plots:

Overall datapath including new alu and shifter:



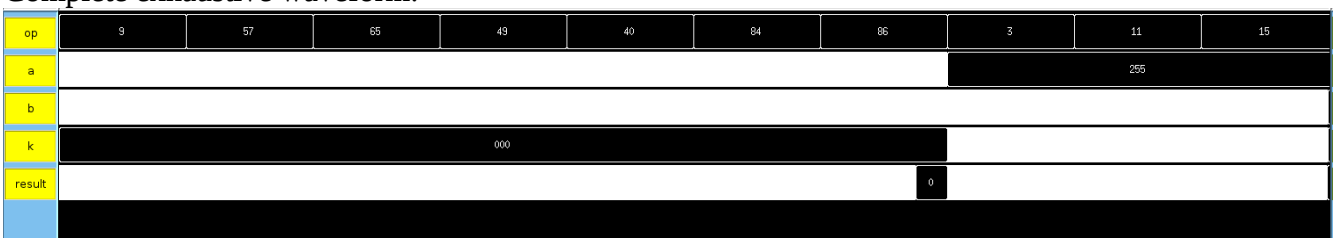

regramarray_dp
datapath
regramarray_dp_0
alt_alu_slice_less
alt_alu_slice_less_5
alt_alu_slice_less
alt_alu_slice_less_4
alt_alu_slice_less
alt_alu_slice_less_3
alt_alu_slice_less
alt_alu_slice_less_2
alt_alu_slice_less
alt_alu_slice_less_1
alt_alu_slice_less
alt_alu_slice_less_0
alt_alu_slice_less
alt_alu_slice_less_6
Topmost cell in the window
source_gen_7_0
source_gen_7_0_0
three_eight_decoder
three_eight_decoder_0


datapath
Topmost cell in the window

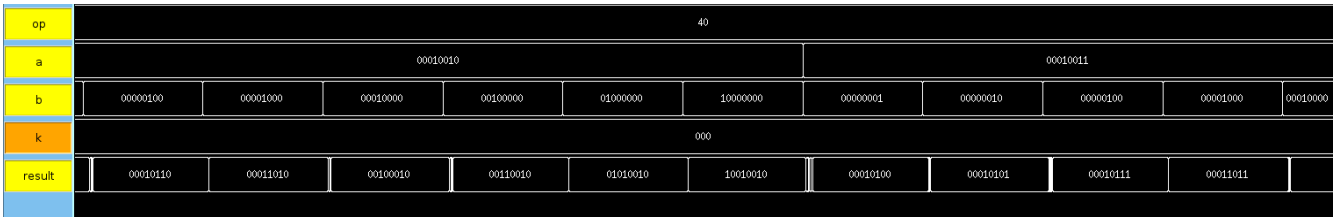
Simulation:

The datapath was tested in irsim, using exhaustive testing on the shifter (demonstrating all possible input values for b and k). The alu operation was also tested the same way as in lab 4. The design passes all tests. Below are a few selected test waveforms:

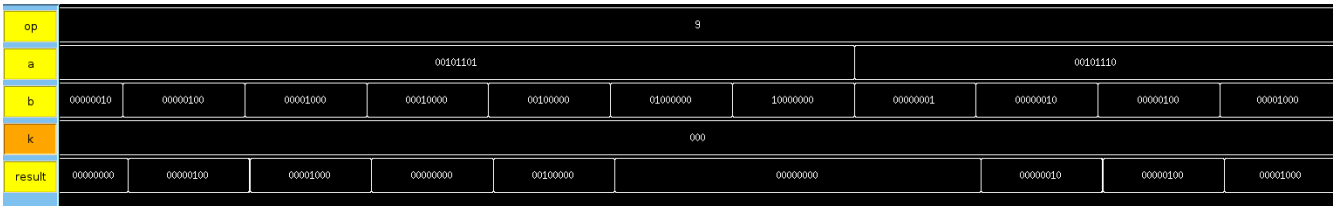
Complete exhaustive waveform:



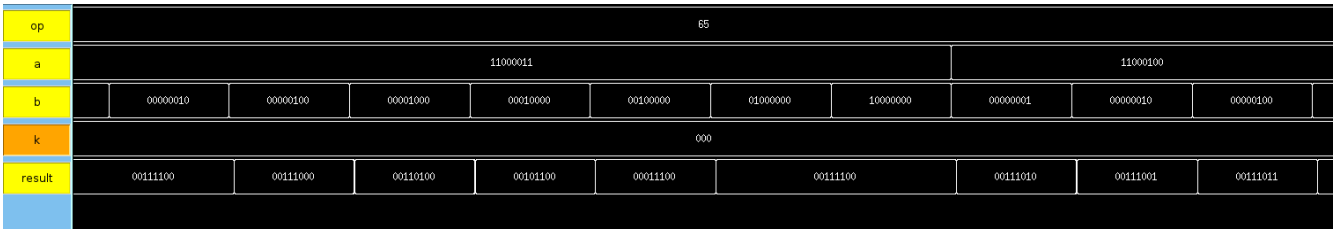
add:



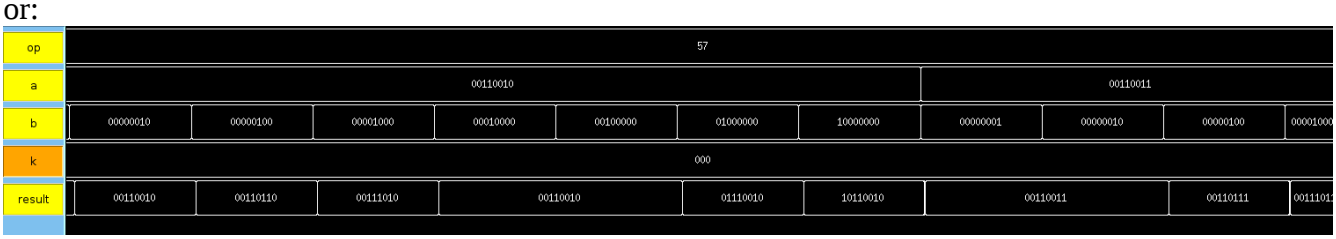
and



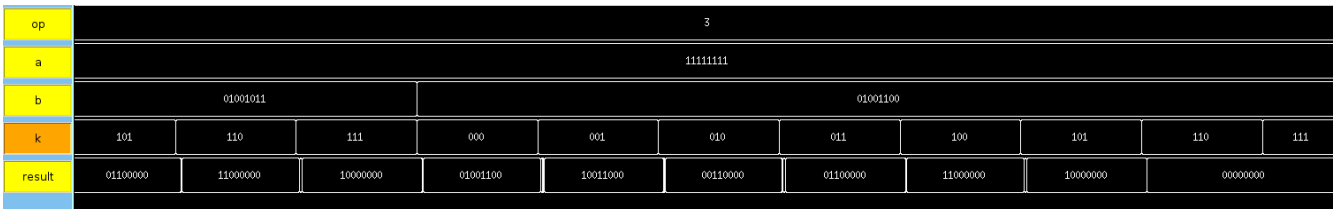
nor:



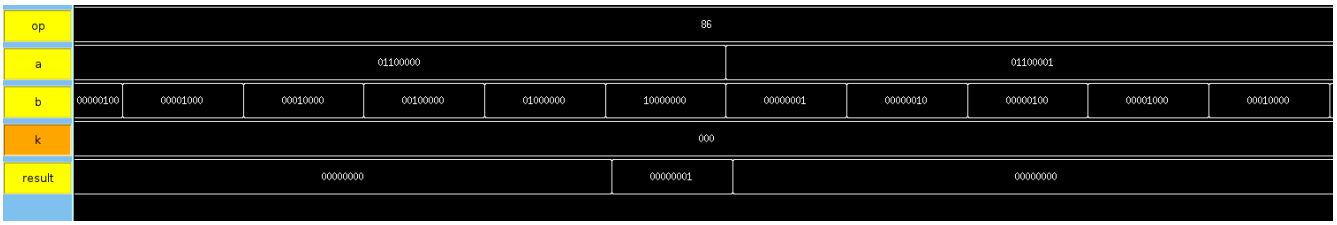
or:



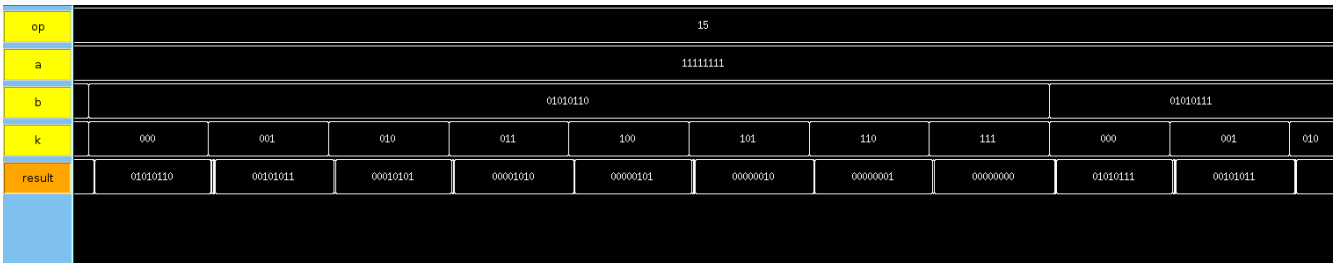
sll:



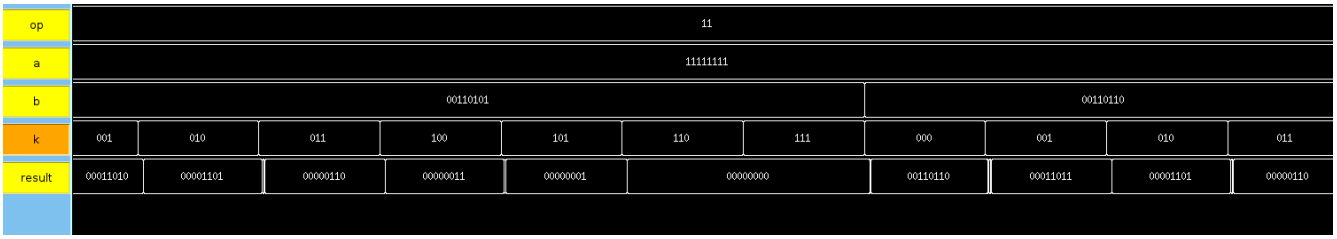
slt:



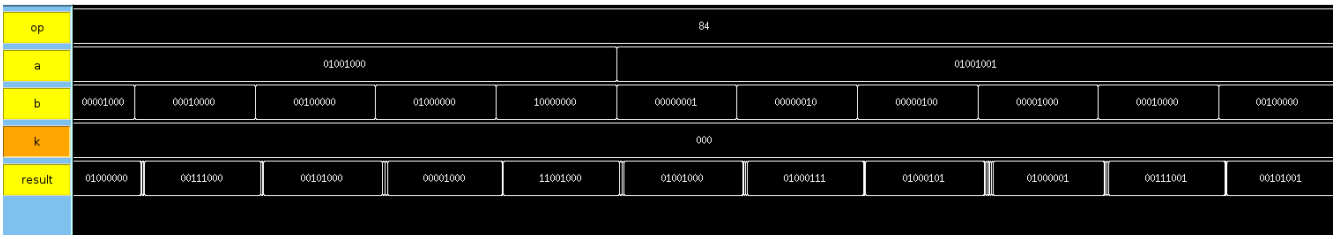
sra:



srl:



sub:



xor: