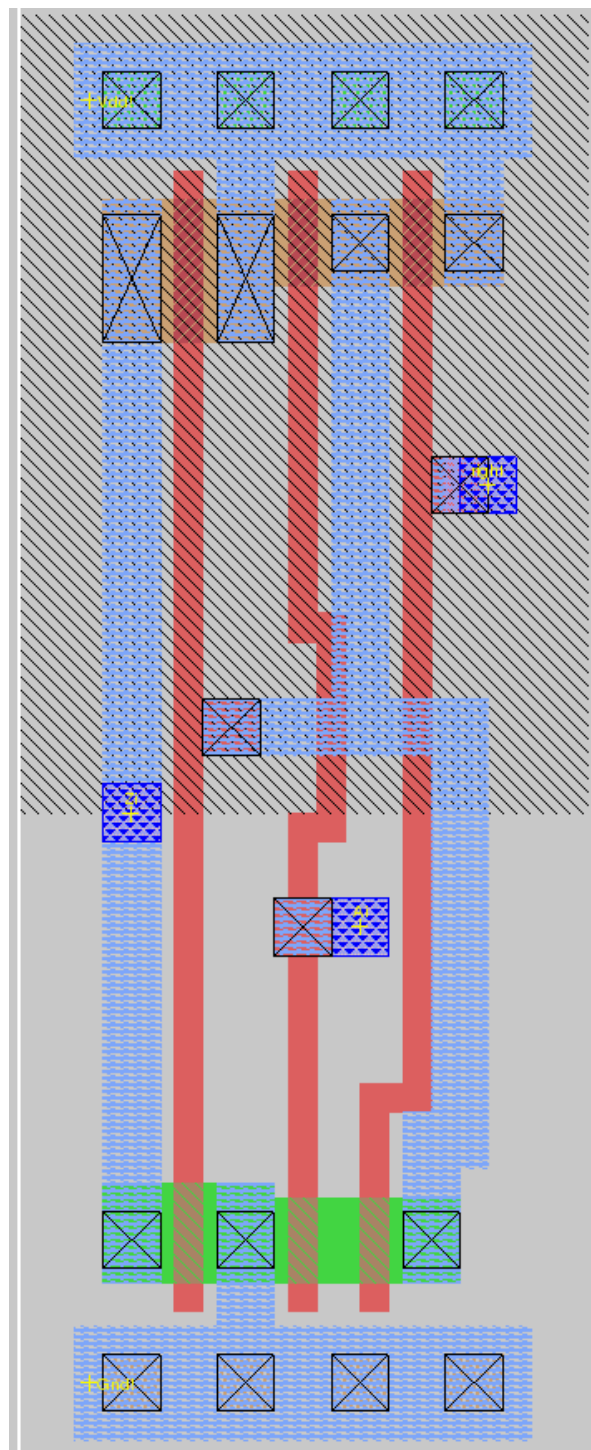Marty Townley and Adam Ness
ECE425
4/18/17
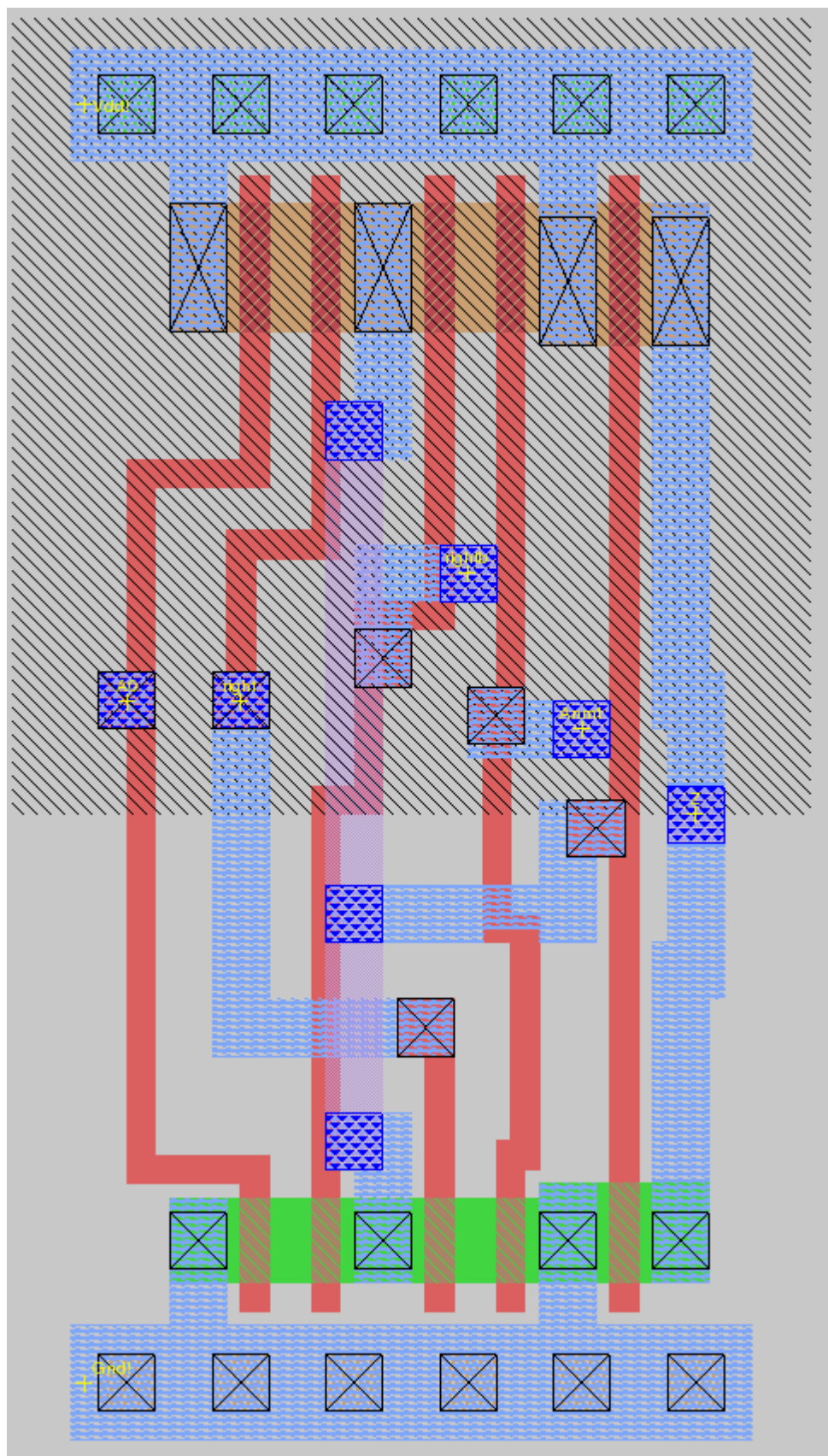
Week 2 Project Deliverable: Complete Funnel Shifter Design (Pass-Transistor Array)

Source Generator Logic:
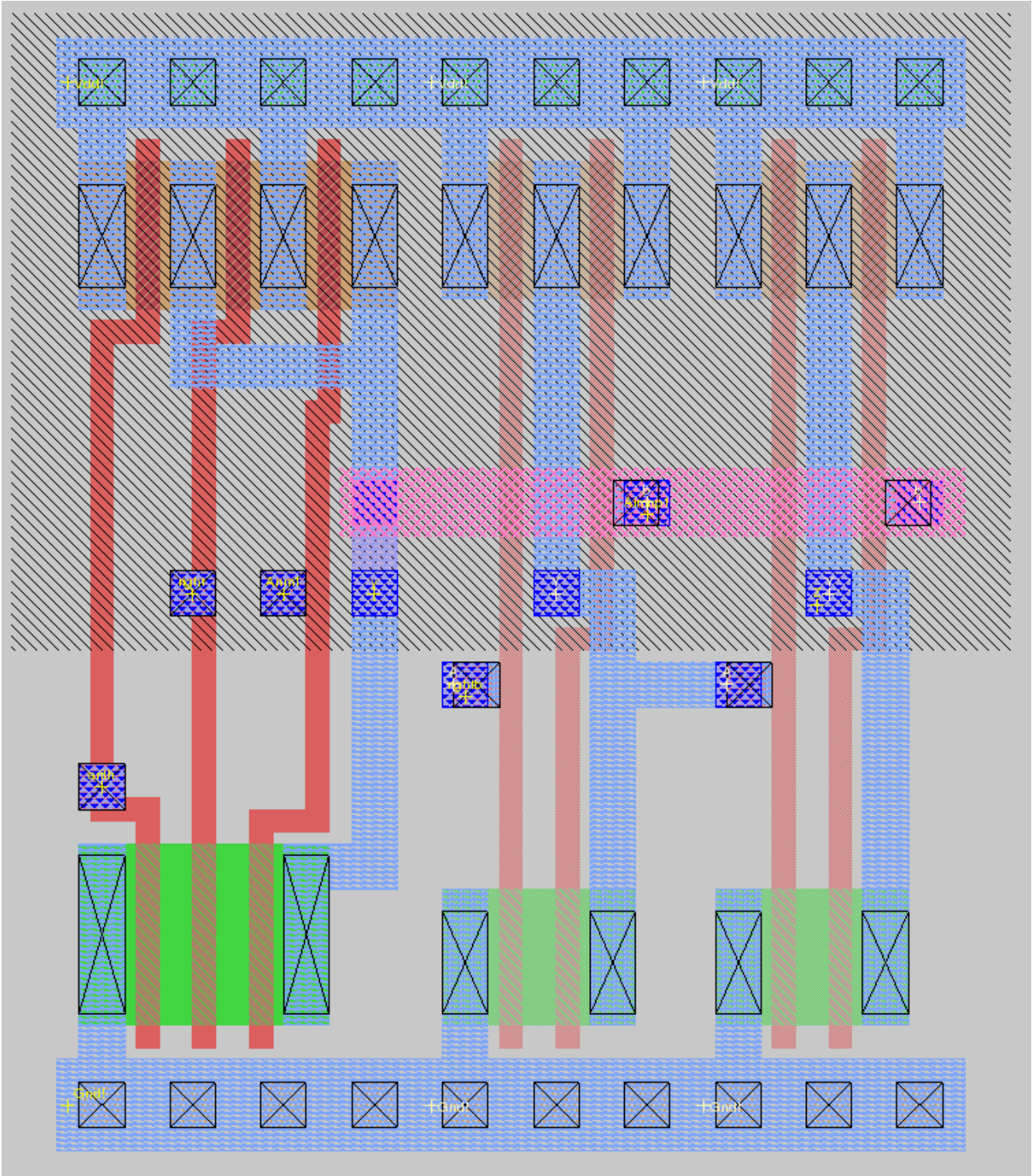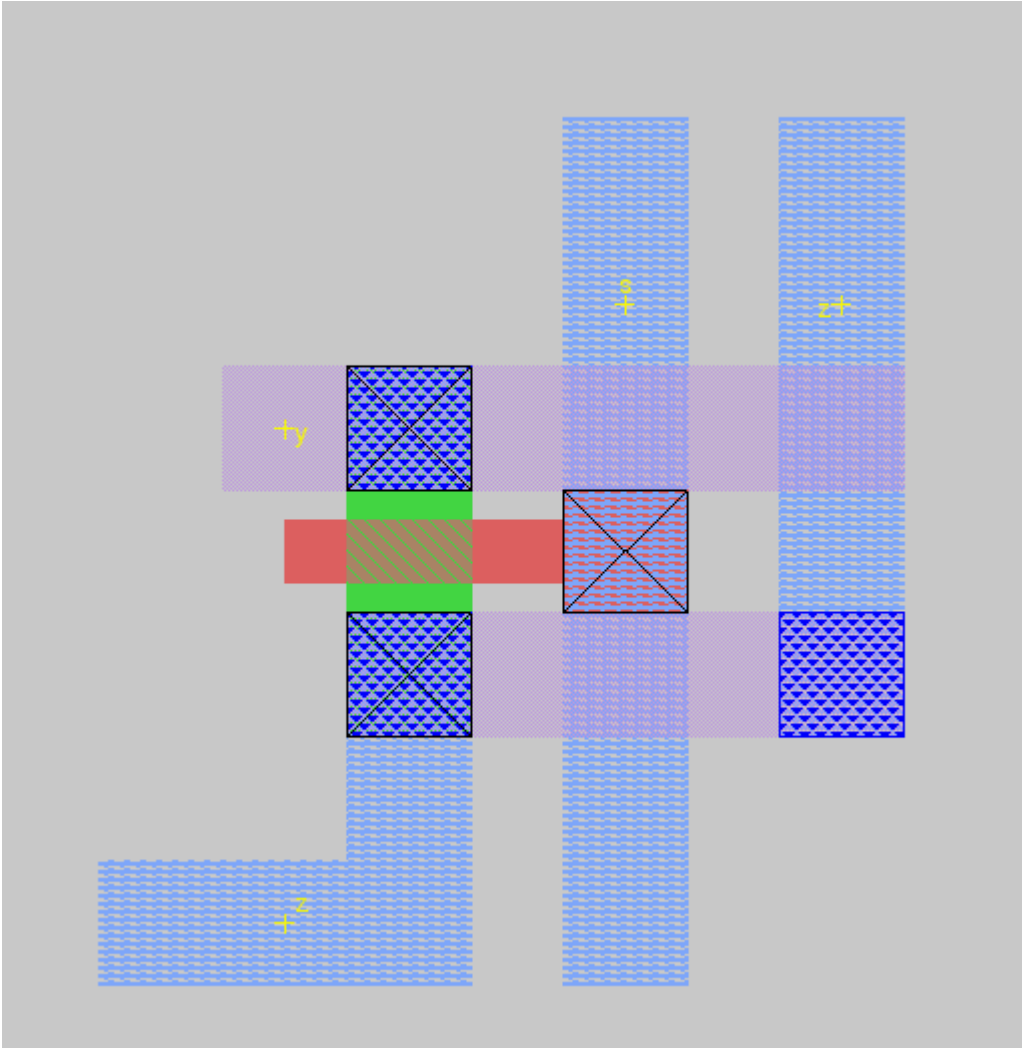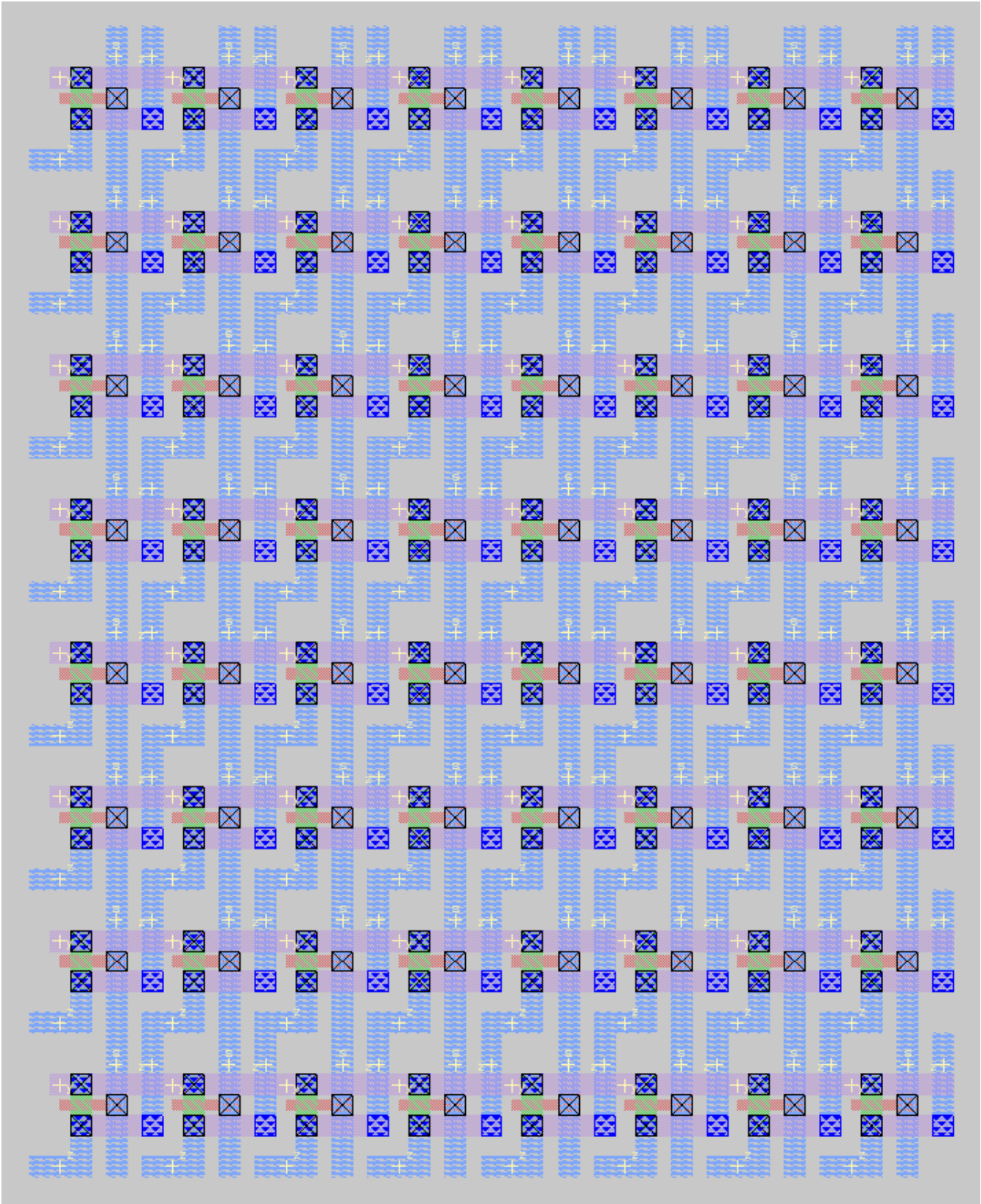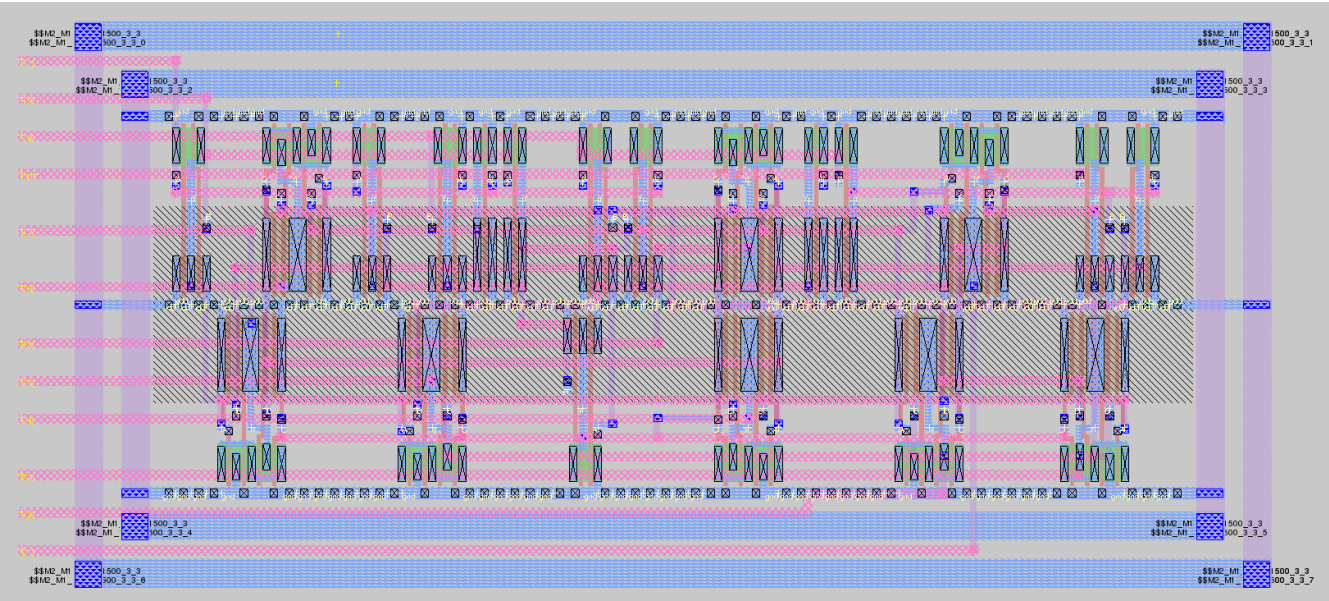
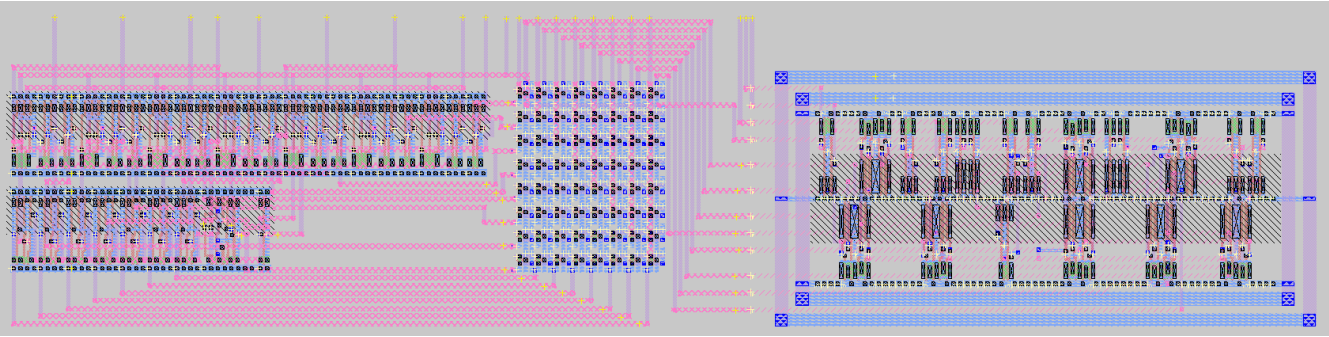N-2:0:

N-1:

2N-2:N
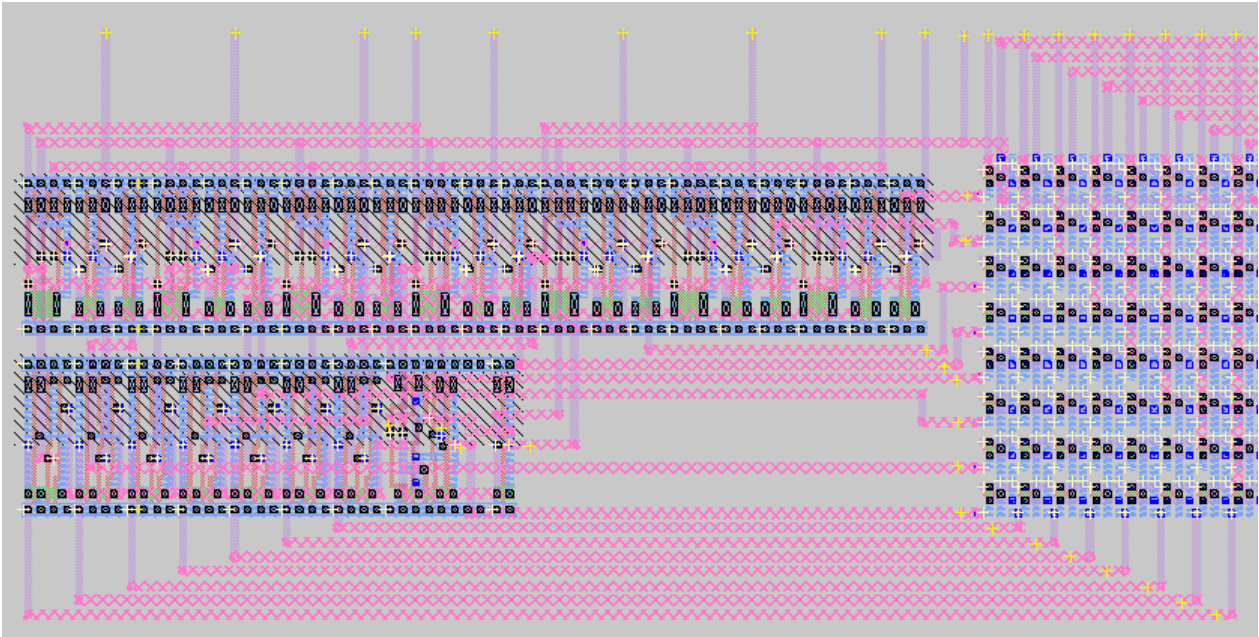
Array Shifter:

Tile:

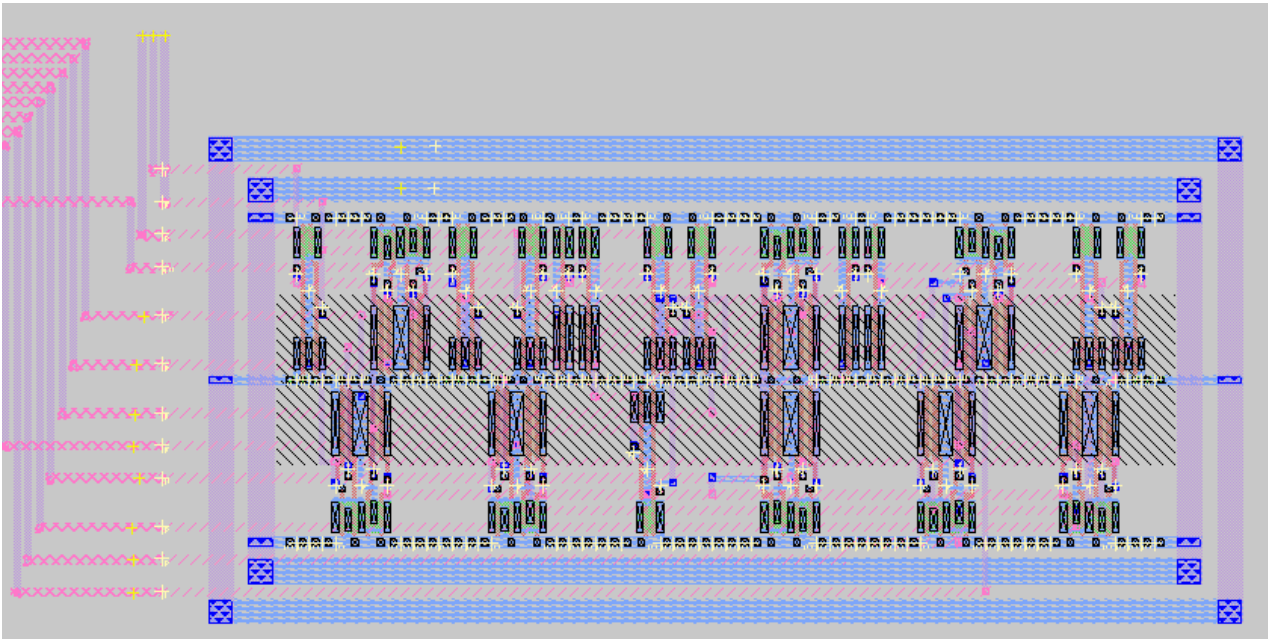Array:

Three-Eight Decoder:

Shifter (Complete):

Shifter (Left side detail):

Shifter (Right side detail):

IRSIM Simulation Plots

Left shift with arith low:

right					0
arith					0
A	10100111	10101000	10101001	10101010	10101010
K			2		2
Y	10011100	10100000	10100100	10101000	10101000

Left shift with arith high:

right						0
arith						1
A	01000100	01000101	01000110	01000111	01001000	01000111
K			2			2
Y	00010000	00010100	00011000	00011100	00100000	00011100

Right logical shift:

right					1
arith					0
A	10010000	10010001	10010010	10010011	10010100	10010010
K			2			2
Y		00100100			00100101	00100100

Right arithmetic shift:

right						1
arith						1
A	10110011	10110100	10110101	10110110	10110111	10110111
K			2			2
Y	11101100	11101101				11101101