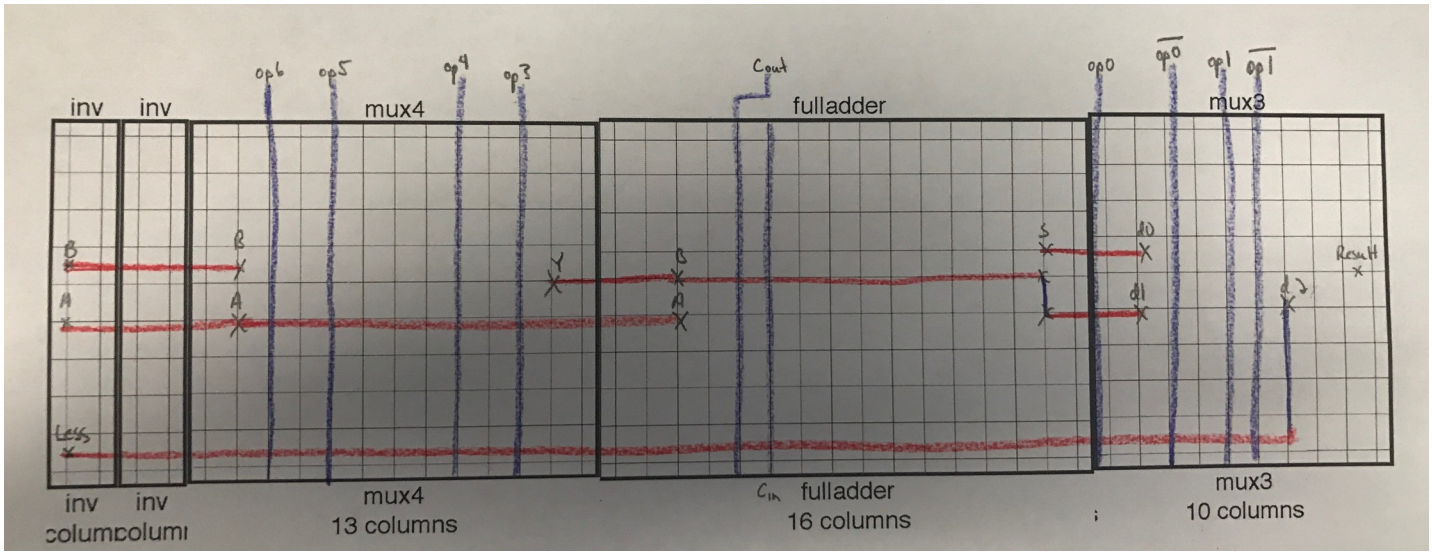
Adam Ness and Marty Townley
ECE425
2/27/17

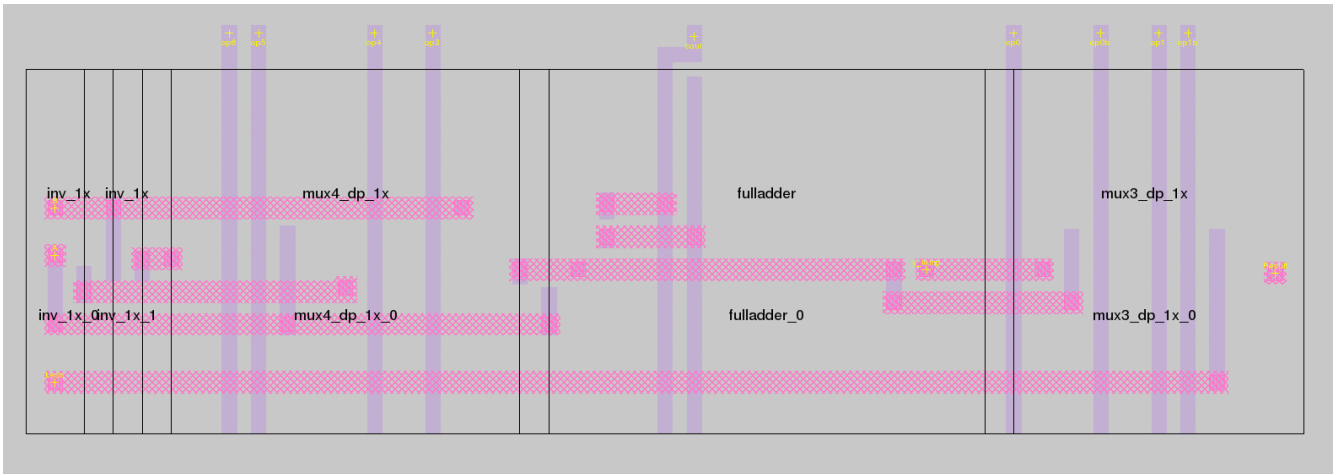
Lab 4

Annotated Slice plan:

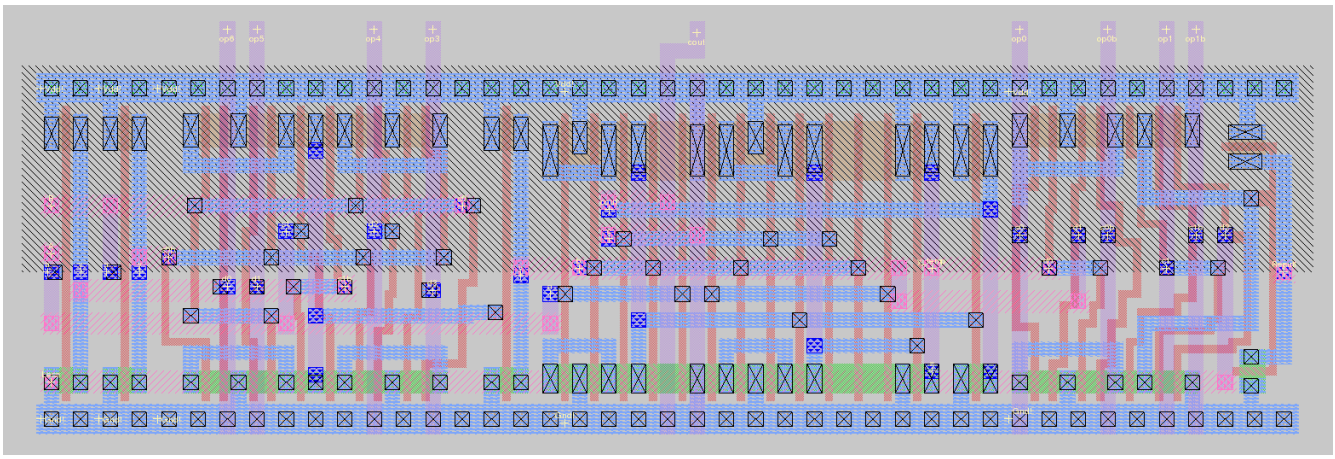


ALU Plots:

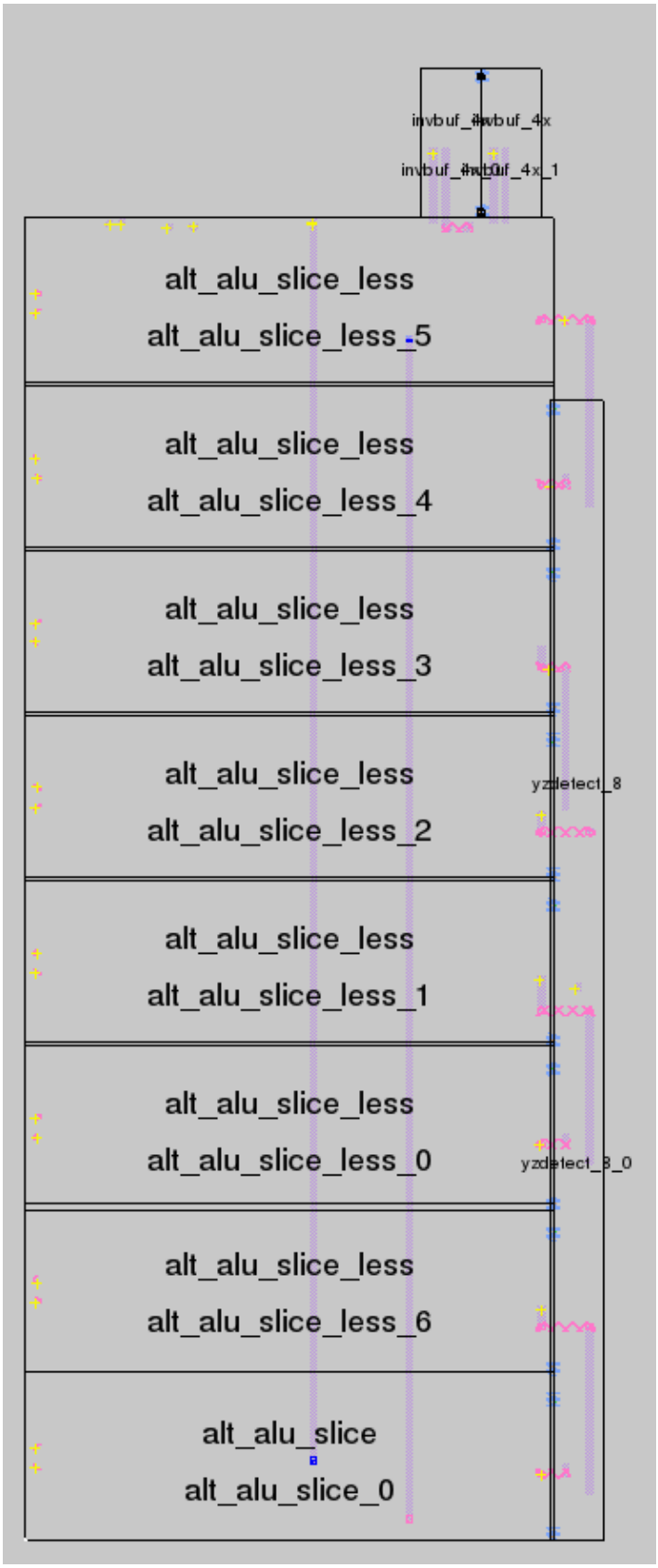
Unexpanded ALU Slice:



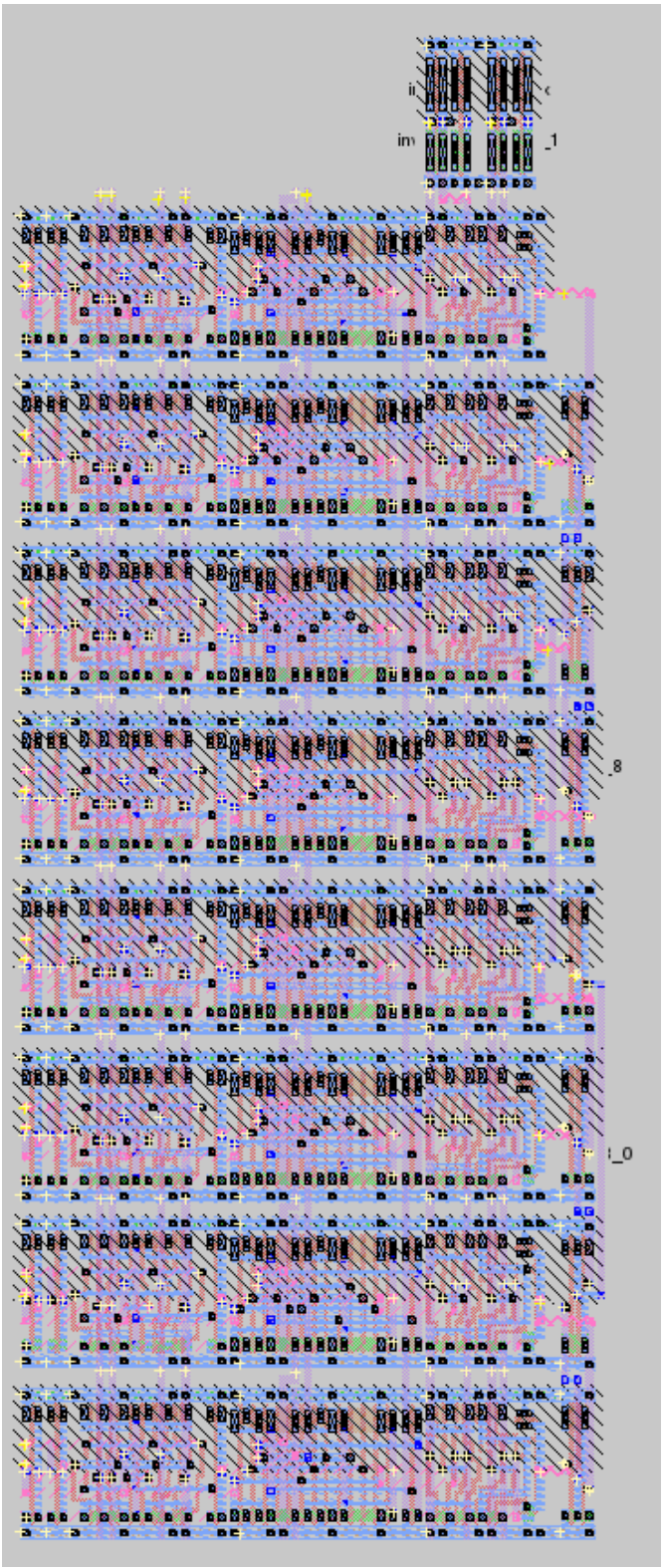
Expanded ALU Slice:



Unexpanded ALU:



Expanded ALU:



Comparison vs. Original ALU:

```
alt_alu size:
          width x height (llx, lly)    , (urx, ury)    area (units^2)
microns:  184.50x293.40  (-5.10, -1.20), (179.40, 292.20)  54132.30
lambda:      615x978     (  -17, -4)   , (   598,  974)    601470

alu size:
          width x height (llx, lly)  , (urx, ury)      area (units^2)
microns:  112.80x294.00  (1.20, 0.00), (114.00, 294.00)    33163.20
lambda:      376x980     (   4, 0)   , (   380,  980)      368480
```

From the information above, it can be seen that the alternative ALU we created in this lab is substantially smaller than the default ALU that was originally given. Our ALU design is approximately 39% smaller (area) than the original (33163.20um^2 vs. 541132.30 um^2).

Simulation Description:

The simulation command file works by setting the op, then cycling through all possible inputs for a, then a few inputs for b (1, 2, 4, 8, 16, etc.). This is done automatically using the cmd file as a tcl script. After op a and b have been set, the cmd file steps (with a stepsize of 250), then checks the answer. The answer is checked by looking at op, a and b, and figuring out what the appropriate result should be. This expected result is calculated, then compared to the result using the assert command.

It was not realistic to cycle through every possible input for b, due to the fact that this would have taken upwards of 10 hours. Thus, cycling through all a and 8 possibilities of b is regarded as extensive testing. In the end, after running the tests and making fixes, no errors were found.

Time Estimate:

This lab took approximately 10 hours to complete.