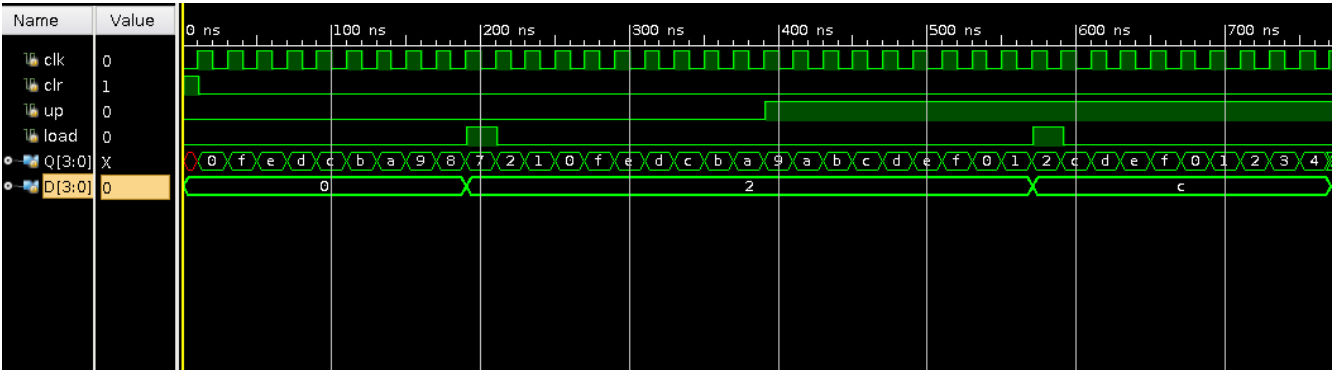
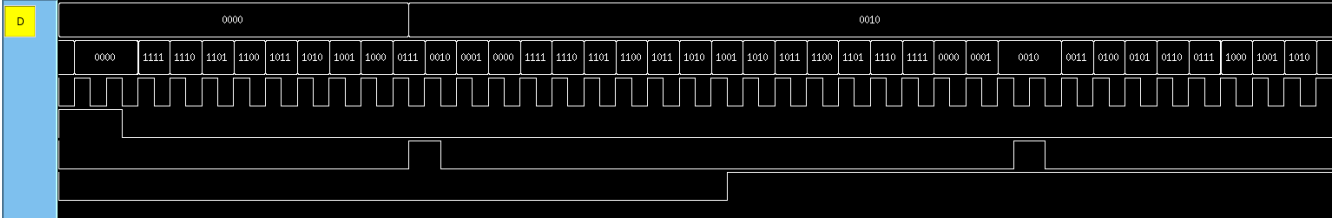


Counter simulation:

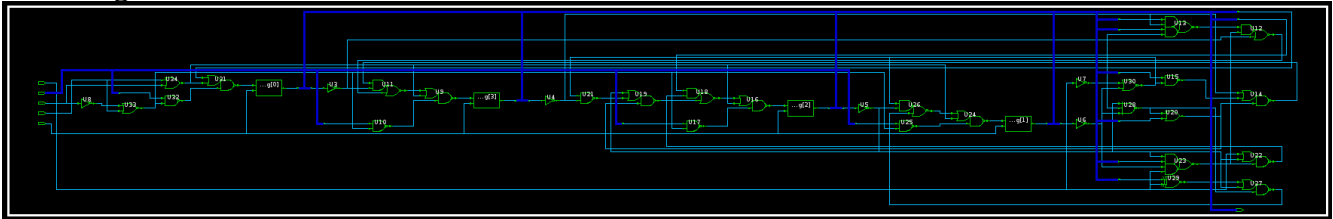


Counter IRSIM waveform:



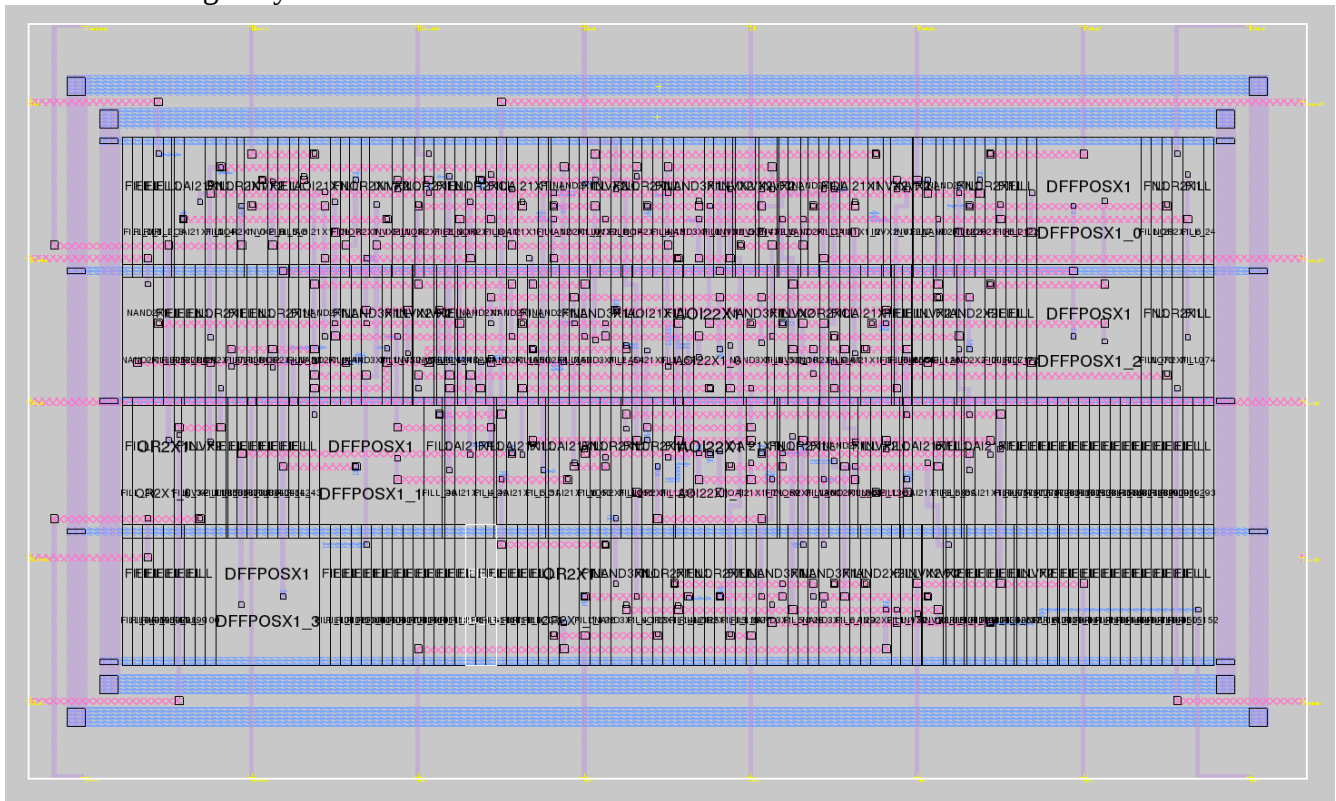
The order of the signals on the above waveform is:
D, Q, clk, clr, load, up

Counter gate schematic:



Timing diagram showing signals for the first 350 ns of the processor simulation. The signals include clock, reset, op[3:0], memwrite, alusrc, memtoreg, lard, pcwrite, branch, regwrite, regdst, pcsrc[1:0], alus...1[0], and alup[1:0]. The clock is a periodic square wave. Reset is active low. The ALU and register file are shown with their inputs and outputs. The ALU output is 0 for the first 100 ns, then 28 for the next 100 ns, then 0 for the next 100 ns, and finally 0 for the last 50 ns. The register file output is 0 for the first 100 ns, then 28 for the next 100 ns, then 0 for the next 100 ns, and finally 0 for the last 50 ns.

MIPS FSM Magic layout:



MIPS FSM Magic layout sizing:

microns: 295.20 x 174.00 (0.00, 0.00), (295.20, 174.00) 51364.80

lambda: 984 x 580 (0, 0), (984, 580) 570720

Summary:

No major problems were encountered in this lab, the only issue we had was trying to figure out how to deal with a typedef enum as an input.

It took about 4 hours to do this lab