```
u59497@s005-n007:~/acc-op/hw/synth$ ${OPAE_PLATFORM_ROOT}/bin/run.sh
Restoring blue bitstream lib files
==================================
Info: ******************************************************************
Info: Running Quartus Prime Shell
    Info: Version 19.2.0 Build 57 06/24/2019 Patches 0.01rc SJ Pro Edition
    Info: Copyright (C) 2019  Intel Corporation. All rights reserved.
    Info: Your use of Intel Corporation's design tools, logic functions
    Info: and other software and tools, and any partner logic
    Info: functions, and any output files from any of the foregoing
    Info: (including device programming or simulation files), and any
    Info: associated documentation or information are expressly subject
    Info: to the terms and conditions of the Intel Program License
    Info: Subscription Agreement, the Intel Quartus Prime License Agreement,
    Info: the Intel FPGA IP License Agreement, or other applicable license
    Info: agreement, including, without limitation, that your use is for
    Info: the sole purpose of programming logic devices manufactured by
    Info: Intel and sold by Intel or its authorized distributors.  Please
    Info: refer to the applicable agreement for further details, at
    Info: https://fpgasoftware.intel.com/eula.
    Info: Processing started: Fri May  7 17:09:13 2021
Info: Command: quartus_sh -t ./a10_partial_reconfig/flow.tcl -nobasecheck
-setup_script ./a10_partial_reconfig/setup.tcl -impl afu_default
Info: Quartus(args): -nobasecheck -setup_script ./a10_partial_reconfig/setup.tcl -impl
afu_default
Info: flow.tcl version: #1
Info: Using setup script /home/u59497/acc-op/hw/synth/build/a10_partial_reconfig/
setup.tcl
Arria 10 Partial Reconfiguration Flow
-------------------------------------------------------------------------------
   Project name                    : dcp
   Output directory                : output_files
   Base revision name              : dcp
   Reconfigurable partition names : green_region
   Implementation Revision : afu_default
      Reconfigurable Partition Name : green_region
Info: Compiling PR implementation afu_default.
Info: ******************************************************************
Info: Running Quartus Prime IP Generation Tool
    Info: Version 19.2.0 Build 57 06/24/2019 Patches 0.01rc SJ Pro Edition
    Info: Processing started: Fri May  7 17:09:16 2021
Info: Command: quartus_ipgenerate dcp -c afu_default --run_default_mode_op
Info: Found 1 IP file(s) in the project.
    Info: IP file /home/u59497/acc-op/hw/synth/build/platform/AFU_debug/SCJIO.qsys was
found in the project.
Info: Started running qsys-validate on Platform Designer system /home/u59497/acc-op/
hw/synth/build/platform/AFU_debug/SCJIO.qsys
Info: Performing Platform Designer system validation using the command line: /glob/
development-tools/versions/fpgasupportstack/a10/1.2.1/intelFPGA_pro/quartus/../qsys/
bin/qsys-validate /home/u59497/acc-op/hw/synth/build/platform/AFU_debug/SCJIO.qsys
Info: SCJIO: All Generic Component instances match their respective ip files.
Info: Finished running qsys-validate on Platform Designer system /home/u59497/acc-op/
hw/synth/build/platform/AFU_debug/SCJIO.qsys
Info: Elaborating Platform Designer system entity /home/u59497/acc-op/hw/synth/build/
platform/AFU_debug/SCJIO.qsys.
Info: Only synthesis files will be generated.
Info: Performing IP Generation using the command line: /glob/development-tools/
versions/fpgasupportstack/a10/1.2.1/intelFPGA_pro/quartus/sopc_builder/bin/qsys-
generate --top-level-generation=true {--family=Arria 10} --synthesis=verilog --
part=10AX115N2F40E2LG --block-symbol-file --pro --quartus-project=/home/u59497/acc-op/
hw/synth/build/dcp --rev=afu_default /home/u59497/acc-op/hw/synth/build/platform/
AFU_debug/SCJIO.qsys --parallel=off
```

```
Info: Saving generation log to /home/u59497/acc-op/hw/synth/build/platform/AFU_debug/
SCJIO/SCJIO_generation.rpt
Info: Generated by version: 19.2 build 57
Info: Starting: Create block symbol file (.bsf)
Info: qsys-generate /home/u59497/acc-op/hw/synth/build/platform/AFU_debug/SCJIO.qsys
--block-symbol-file --output-directory=/home/u59497/acc-op/hw/synth/build/platform/
AFU_debug/SCJIO --family="Arria 10" --part=10AX115N2F40E2LG
Info: Loading AFU_debug/SCJIO.qsys
Info: Reading input file
Info: Adding soft_core_jtag_io_0 [altera_soft_core_jtag_io 19.1]
Info: Parameterizing module soft_core_jtag_io_0
Info: Building connections
Info: Parameterizing connections
Info: Validating
Info: Done reading input file
Info: qsys-generate succeeded.
Info: Finished: Create block symbol file (.bsf)
Info: Starting: Create HDL design files for synthesis
Info: qsys-generate /home/u59497/acc-op/hw/synth/build/platform/AFU_debug/SCJIO.qsys
--synthesis=VERILOG --output-directory=/home/u59497/acc-op/hw/synth/build/platform/
AFU_debug/SCJIO --family="Arria 10" --part=10AX115N2F40E2LG
Info: Loading AFU_debug/SCJIO.qsys
Info: Reading input file
Info: Adding soft_core_jtag_io_0 [altera_soft_core_jtag_io 19.1]
Info: Parameterizing module soft_core_jtag_io_0
Info: Building connections
Info: Parameterizing connections
Info: Validating
Info: Done reading input file
Info: SCJIO: "Transforming system: SCJIO"
Info: SCJIO: "Naming system components in system: SCJIO"
Info: SCJIO: "Processing generation queue"
Info: SCJIO: "Generating: SCJIO"
Info: SCJIO: "Generating: altera_soft_core_jtag_io"
Info: SCJIO: Done "SCJIO" with 2 modules, 1 files
Info: qsys-generate succeeded.
Info: Finished: Create HDL design files for synthesis
Info: Finished elaborating Platform Designer system entity /home/u59497/acc-op/hw/
synth/build/platform/AFU_debug/SCJIO.qsys
Info: Finished generating IP file(s) in the project.
Info: Quartus Prime IP Generation Tool was successful. 0 errors, 0 warnings
    Info: Peak virtual memory: 1136 megabytes
    Info: Processing ended: Fri May  7 17:09:26 2021
    Info: Elapsed time: 00:00:10
Info: ******************************************************************
Info: Running Quartus Prime Synthesis
    Info: Version 19.2.0 Build 57 06/24/2019 Patches 0.01rc SJ Pro Edition
    Info: Processing started: Fri May  7 17:09:30 2021
Info: Command: quartus_syn --read_settings_files=on --write_settings_files=off dcp -c
afu_default
Info: qis_default_flow_script.tcl version: #1
Info: Initializing Synthesis...
Info: Project = "dcp"
Info: Revision = "afu_default"
Info: Analyzing source files
Info (16303): High Performance Effort optimization mode selected -- timing performance
will be prioritized at the potential cost of increased compilation time
Info (19806): Entity rebinding has been applied to partition "fpga_top|inst_green_bs".
The entity has been remapped from "green_bs" to "green_bs".
Info (16734): Loading "final" snapshot for partition "root_partition".
Info (16734): Loading "final" snapshot for partition "root_partition_2cedade0".
Warning (13228): Verilog HDL or VHDL warning at ccip_if_pkg.sv(36): parameter declared
inside package 'ccip_if_pkg' shall be treated as localparam File: /usr/share/opae/
platform/platform_if/rtl/device_if/ccip_if_pkg.sv Line: 36
```

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Warning (13228): Verilog HDL or VHDL warning at ccip_if_pkg.sv(38): parameter declared
inside package 'ccip_if_pkg' shall be treated as localparam File: /usr/share/opae/
platform/platform_if/rtl/device_if/ccip_if_pkg.sv Line: 38
Warning (13228): Verilog HDL or VHDL warning at ccip_if_pkg.sv(39): parameter declared
inside package 'ccip_if_pkg' shall be treated as localparam File: /usr/share/opae/
platform/platform_if/rtl/device_if/ccip_if_pkg.sv Line: 39
Warning (13228): Verilog HDL or VHDL warning at ccip_if_pkg.sv(41): parameter declared
inside package 'ccip_if_pkg' shall be treated as localparam File: /usr/share/opae/
platform/platform_if/rtl/device_if/ccip_if_pkg.sv Line: 41
Warning (13228): Verilog HDL or VHDL warning at ccip_if_pkg.sv(42): parameter declared
inside package 'ccip_if_pkg' shall be treated as localparam File: /usr/share/opae/
platform/platform_if/rtl/device_if/ccip_if_pkg.sv Line: 42
Warning (13228): Verilog HDL or VHDL warning at ccip_if_pkg.sv(43): parameter declared
inside package 'ccip_if_pkg' shall be treated as localparam File: /usr/share/opae/
platform/platform_if/rtl/device_if/ccip_if_pkg.sv Line: 43
Warning (13228): Verilog HDL or VHDL warning at ccip_if_pkg.sv(45): parameter declared
inside package 'ccip_if_pkg' shall be treated as localparam File: /usr/share/opae/
platform/platform_if/rtl/device_if/ccip_if_pkg.sv Line: 45
Warning (13228): Verilog HDL or VHDL warning at ccip_if_pkg.sv(48): parameter declared
inside package 'ccip_if_pkg' shall be treated as localparam File: /usr/share/opae/
platform/platform_if/rtl/device_if/ccip_if_pkg.sv Line: 48
Warning (13228): Verilog HDL or VHDL warning at ccip_if_pkg.sv(51): parameter declared
inside package 'ccip_if_pkg' shall be treated as localparam File: /usr/share/opae/
platform/platform_if/rtl/device_if/ccip_if_pkg.sv Line: 51
Warning (13228): Verilog HDL or VHDL warning at ccip_if_pkg.sv(53): parameter declared
inside package 'ccip_if_pkg' shall be treated as localparam File: /usr/share/opae/
platform/platform_if/rtl/device_if/ccip_if_pkg.sv Line: 53
Warning (13228): Verilog HDL or VHDL warning at ccip_if_pkg.sv(136): parameter
declared inside package 'ccip_if_pkg' shall be treated as localparam File: /usr/share/
opae/platform/platform_if/rtl/device_if/ccip_if_pkg.sv Line: 136
Warning (13228): Verilog HDL or VHDL warning at ccip_if_pkg.sv(149): parameter
declared inside package 'ccip_if_pkg' shall be treated as localparam File: /usr/share/
opae/platform/platform_if/rtl/device_if/ccip_if_pkg.sv Line: 149
Warning (13228): Verilog HDL or VHDL warning at ccip_if_pkg.sv(178): parameter
declared inside package 'ccip_if_pkg' shall be treated as localparam File: /usr/share/
opae/platform/platform_if/rtl/device_if/ccip_if_pkg.sv Line: 178
Warning (13228): Verilog HDL or VHDL warning at ccip_if_pkg.sv(190): parameter
declared inside package 'ccip_if_pkg' shall be treated as localparam File: /usr/share/
opae/platform/platform_if/rtl/device_if/ccip_if_pkg.sv Line: 190
Warning (13228): Verilog HDL or VHDL warning at ccip_if_pkg.sv(218): parameter
declared inside package 'ccip_if_pkg' shall be treated as localparam File: /usr/share/
opae/platform/platform_if/rtl/device_if/ccip_if_pkg.sv Line: 218
Warning (13228): Verilog HDL or VHDL warning at ccip_if_pkg.sv(223): parameter
declared inside package 'ccip_if_pkg' shall be treated as localparam File: /usr/share/
opae/platform/platform_if/rtl/device_if/ccip_if_pkg.sv Line: 223
Info (16884): Verilog HDL info at ccip_cfg_pkg.sv(31): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
device_cfg/ccip_cfg_pkg.sv Line: 31
Info (13230): Verilog HDL or VHDL information at ccip_cfg_pkg.sv(31): back to file '/
usr/share/opae/platform/platform_if/rtl/device_cfg/ccip_cfg_pkg.sv' File: /usr/share/
opae/platform/platform_if/rtl/device_cfg/ccip_cfg_pkg.sv Line: 31
Warning (13228): Verilog HDL or VHDL warning at ccip_cfg_pkg.sv(47): parameter
declared inside package 'ccip_cfg_pkg' shall be treated as localparam File: /usr/
share/opae/platform/platform_if/rtl/device_cfg/ccip_cfg_pkg.sv Line: 47
Warning (13228): Verilog HDL or VHDL warning at ccip_cfg_pkg.sv(75): parameter
declared inside package 'ccip_cfg_pkg' shall be treated as localparam File: /usr/
share/opae/platform/platform_if/rtl/device_cfg/ccip_cfg_pkg.sv Line: 75
Warning (13228): Verilog HDL or VHDL warning at ccip_cfg_pkg.sv(76): parameter
declared inside package 'ccip_cfg_pkg' shall be treated as localparam File: /usr/
share/opae/platform/platform_if/rtl/device_cfg/ccip_cfg_pkg.sv Line: 76
Warning (13228): Verilog HDL or VHDL warning at ccip_cfg_pkg.sv(77): parameter
declared inside package 'ccip_cfg_pkg' shall be treated as localparam File: /usr/
share/opae/platform/platform_if/rtl/device_cfg/ccip_cfg_pkg.sv Line: 77
```

```
Warning (13228): Verilog HDL or VHDL warning at ccip_cfg_pkg.sv(80): parameter
declared inside package 'ccip_cfg_pkg' shall be treated as localparam File: /usr/
share/opae/platform/platform_if/rtl/device_cfg/ccip_cfg_pkg.sv Line: 80
Warning (13228): Verilog HDL or VHDL warning at ccip_cfg_pkg.sv(87): parameter
declared inside package 'ccip_cfg_pkg' shall be treated as localparam File: /usr/
share/opae/platform/platform_if/rtl/device_cfg/ccip_cfg_pkg.sv Line: 87
Warning (13228): Verilog HDL or VHDL warning at ccip_cfg_pkg.sv(90): parameter
declared inside package 'ccip_cfg_pkg' shall be treated as localparam File: /usr/
share/opae/platform/platform_if/rtl/device_cfg/ccip_cfg_pkg.sv Line: 90
Warning (13228): Verilog HDL or VHDL warning at ccip_cfg_pkg.sv(91): parameter
declared inside package 'ccip_cfg_pkg' shall be treated as localparam File: /usr/
share/opae/platform/platform_if/rtl/device_cfg/ccip_cfg_pkg.sv Line: 91
Warning (13228): Verilog HDL or VHDL warning at ccip_cfg_pkg.sv(94): parameter
declared inside package 'ccip_cfg_pkg' shall be treated as localparam File: /usr/
share/opae/platform/platform_if/rtl/device_cfg/ccip_cfg_pkg.sv Line: 94
Warning (13228): Verilog HDL or VHDL warning at ccip_cfg_pkg.sv(100): parameter
declared inside package 'ccip_cfg_pkg' shall be treated as localparam File: /usr/
share/opae/platform/platform_if/rtl/device_cfg/ccip_cfg_pkg.sv Line: 100
Warning (13228): Verilog HDL or VHDL warning at ccip_cfg_pkg.sv(101): parameter
declared inside package 'ccip_cfg_pkg' shall be treated as localparam File: /usr/
share/opae/platform/platform_if/rtl/device_cfg/ccip_cfg_pkg.sv Line: 101
Warning (13228): Verilog HDL or VHDL warning at ccip_cfg_pkg.sv(104): parameter
declared inside package 'ccip_cfg_pkg' shall be treated as localparam File: /usr/
share/opae/platform/platform_if/rtl/device_cfg/ccip_cfg_pkg.sv Line: 104
Info (16884): Verilog HDL info at hssi_cfg_pkg.sv(31): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
device_cfg/hssi_cfg_pkg.sv Line: 31
Info (13230): Verilog HDL or VHDL information at hssi_cfg_pkg.sv(31): back to file '/
usr/share/opae/platform/platform_if/rtl/device_cfg/hssi_cfg_pkg.sv' File: /usr/share/
opae/platform/platform_if/rtl/device_cfg/hssi_cfg_pkg.sv Line: 31
Info (16884): Verilog HDL info at local_mem_cfg_pkg.sv(31): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
device_cfg/local_mem_cfg_pkg.sv Line: 31
Info (13230): Verilog HDL or VHDL information at local_mem_cfg_pkg.sv(31): back to
file '/usr/share/opae/platform/platform_if/rtl/device_cfg/local_mem_cfg_pkg.sv'
File: /usr/share/opae/platform/platform_if/rtl/device_cfg/local_mem_cfg_pkg.sv Line:
31
Info (16884): Verilog HDL info at ccip_if_clock.sv(31): analyzing included file /usr/
share/opae/platform/platform_if/rtl/platform_if.vh File: /usr/share/opae/platform/
platform_if/rtl/device_if/ccip_if_clock.sv Line: 31
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at ccip_if_clock.sv(31): back to file '/
usr/share/opae/platform/platform_if/rtl/device_if/ccip_if_clock.sv' File: /usr/share/
opae/platform/platform_if/rtl/device_if/ccip_if_clock.sv Line: 31
Info (16884): Verilog HDL info at platform_shim_ccip_std_afu.sv(39): analyzing
included file /usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /usr/
```

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share/opae/platform/platform_if/rtl/platform_shims/platform_shim_ccip_std_afu.sv Line:
39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at platform_shim_ccip_std_afu.sv(39):
back to file '/usr/share/opae/platform/platform_if/rtl/platform_shims/
platform_shim_ccip_std_afu.sv' File: /usr/share/opae/platform/platform_if/rtl/
platform_shims/platform_shim_ccip_std_afu.sv Line: 39
Info (16884): Verilog HDL info at platform_shim_ccip.sv(36): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /usr/share/opae/platform/
platform_if/rtl/platform_shims/platform_shim_ccip.sv Line: 36
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at platform_shim_ccip.sv(36): back to
file '/usr/share/opae/platform/platform_if/rtl/platform_shims/platform_shim_ccip.sv'
File: /usr/share/opae/platform/platform_if/rtl/platform_shims/platform_shim_ccip.sv
Line: 36
Info (16884): Verilog HDL info at platform_shim_avalon_mem_if.sv(36): analyzing
included file /usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /usr/
share/opae/platform/platform_if/rtl/platform_shims/platform_shim_avalon_mem_if.sv
Line: 36
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
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Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at platform_shim_avalon_mem_if.sv(36):
back to file '/usr/share/opae/platform/platform_if/rtl/platform_shims/
platform_shim_avalon_mem_if.sv' File: /usr/share/opae/platform/platform_if/rtl/
platform_shims/platform_shim_avalon_mem_if.sv Line: 36
Info (16884): Verilog HDL info at avalon_mem_if_async_shim.sv(35): analyzing included
file /usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_shims/utils/avalon_mem_if_async_shim.sv Line: 35
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at avalon_mem_if_async_shim.sv(35): back
to file '/usr/share/opae/platform/platform_if/rtl/platform_shims/utils/
avalon_mem_if_async_shim.sv' File: /usr/share/opae/platform/platform_if/rtl/
platform_shims/utils/avalon_mem_if_async_shim.sv Line: 35
Info (16884): Verilog HDL info at avalon_mem_if_reg.sv(37): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /usr/share/opae/platform/
platform_if/rtl/platform_shims/utils/avalon_mem_if_reg.sv Line: 37
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at avalon_mem_if_reg.sv(37): back to
file '/usr/share/opae/platform/platform_if/rtl/platform_shims/utils/
avalon_mem_if_reg.sv' File: /usr/share/opae/platform/platform_if/rtl/platform_shims/
utils/avalon_mem_if_reg.sv Line: 37
```

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Info (16884): Verilog HDL info at avalon_mem_if_reg_simple.sv(39): analyzing included
file /usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_shims/utils/avalon_mem_if_reg_simple.sv Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at avalon_mem_if_reg_simple.sv(39): back
to file '/usr/share/opae/platform/platform_if/rtl/platform_shims/utils/
avalon_mem_if_reg_simple.sv' File: /usr/share/opae/platform/platform_if/rtl/
platform_shims/utils/avalon_mem_if_reg_simple.sv Line: 39
Info (16884): Verilog HDL info at platform_utils_ccip_async_shim.sv(41): analyzing
included file /usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /usr/
share/opae/platform/platform_if/rtl/platform_shims/utils/
platform_utils_ccip_async_shim.sv Line: 41
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at
platform_utils_ccip_async_shim.sv(41): back to file '/usr/share/opae/platform/
platform_if/rtl/platform_shims/utils/platform_utils_ccip_async_shim.sv' File: /usr/
share/opae/platform/platform_if/rtl/platform_shims/utils/
platform_utils_ccip_async_shim.sv Line: 41
Warning (16752): Verilog HDL warning at platform_utils_ccip_async_shim.sv(253):
potential always loop found File: /usr/share/opae/platform/platform_if/rtl/
platform_shims/utils/platform_utils_ccip_async_shim.sv Line: 253
Warning (16752): Verilog HDL warning at platform_utils_ccip_async_shim.sv(390):
potential always loop found File: /usr/share/opae/platform/platform_if/rtl/
platform_shims/utils/platform_utils_ccip_async_shim.sv Line: 390
Warning (16818): Verilog HDL warning at platform_utils_ccip_reg.sv(86): block
identifier is required on this block File: /usr/share/opae/platform/platform_if/rtl/
platform_shims/utils/platform_utils_ccip_reg.sv Line: 86
Warning (16818): Verilog HDL warning at platform_utils_ccip_reg.sv(117): block
identifier is required on this block File: /usr/share/opae/platform/platform_if/rtl/
platform_shims/utils/platform_utils_ccip_reg.sv Line: 117
```

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Warning (16818): Verilog HDL warning at platform_utils_ccip_reg.sv(147): block
identifier is required on this block File: /usr/share/opae/platform/platform_if/rtl/
platform_shims/utils/platform_utils_ccip_reg.sv Line: 147
Warning (16818): Verilog HDL warning at platform_utils_ccip_reg.sv(181): block
identifier is required on this block File: /usr/share/opae/platform/platform_if/rtl/
platform_shims/utils/platform_utils_ccip_reg.sv Line: 181
Warning (13228): Verilog HDL or VHDL warning at ccis_if_pkg.sv(9): parameter declared
inside package 'ccis_if_pkg' shall be treated as localparam File: /home/u59497/intel-
fpga-bbb/BBB_cci_mpf/hw/rtl/cci-if/ccis_if_pkg.sv Line: 9
Warning (13228): Verilog HDL or VHDL warning at ccis_if_pkg.sv(10): parameter declared
inside package 'ccis_if_pkg' shall be treated as localparam File: /home/u59497/intel-
fpga-bbb/BBB_cci_mpf/hw/rtl/cci-if/ccis_if_pkg.sv Line: 10
Warning (13228): Verilog HDL or VHDL warning at ccis_if_pkg.sv(11): parameter declared
inside package 'ccis_if_pkg' shall be treated as localparam File: /home/u59497/intel-
fpga-bbb/BBB_cci_mpf/hw/rtl/cci-if/ccis_if_pkg.sv Line: 11
Warning (13228): Verilog HDL or VHDL warning at ccis_if_pkg.sv(14): parameter declared
inside package 'ccis_if_pkg' shall be treated as localparam File: /home/u59497/intel-
fpga-bbb/BBB_cci_mpf/hw/rtl/cci-if/ccis_if_pkg.sv Line: 14
Warning (13228): Verilog HDL or VHDL warning at ccis_if_pkg.sv(54): parameter declared
inside package 'ccis_if_pkg' shall be treated as localparam File: /home/u59497/intel-
fpga-bbb/BBB_cci_mpf/hw/rtl/cci-if/ccis_if_pkg.sv Line: 54
Warning (13228): Verilog HDL or VHDL warning at ccis_if_pkg.sv(61): parameter declared
inside package 'ccis_if_pkg' shall be treated as localparam File: /home/u59497/intel-
fpga-bbb/BBB_cci_mpf/hw/rtl/cci-if/ccis_if_pkg.sv Line: 61
Info (16884): Verilog HDL info at cci_mpf_if_pkg.sv(21): analyzing included file /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if_pkg.sv Line: 21
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if_pkg.sv(21): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if_pkg.sv' File: /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if_pkg.sv Line: 21
Warning (13228): Verilog HDL or VHDL warning at cci_mpf_if_pkg.sv(49): parameter
declared inside package 'cci_mpf_if_pkg' shall be treated as localparam File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if_pkg.sv Line: 49
Warning (13228): Verilog HDL or VHDL warning at cci_mpf_if_pkg.sv(50): parameter
declared inside package 'cci_mpf_if_pkg' shall be treated as localparam File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if_pkg.sv Line: 50
Warning (13228): Verilog HDL or VHDL warning at cci_mpf_if_pkg.sv(52): parameter
declared inside package 'cci_mpf_if_pkg' shall be treated as localparam File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if_pkg.sv Line: 52
```

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Warning (13228): Verilog HDL or VHDL warning at cci_mpf_if_pkg.sv(53): parameter
declared inside package 'cci_mpf_if_pkg' shall be treated as localparam File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if_pkg.sv Line: 53
Warning (13228): Verilog HDL or VHDL warning at cci_mpf_if_pkg.sv(55): parameter
declared inside package 'cci_mpf_if_pkg' shall be treated as localparam File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if_pkg.sv Line: 55
Warning (13228): Verilog HDL or VHDL warning at cci_mpf_if_pkg.sv(60): parameter
declared inside package 'cci_mpf_if_pkg' shall be treated as localparam File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if_pkg.sv Line: 60
Warning (13228): Verilog HDL or VHDL warning at cci_mpf_if_pkg.sv(67): parameter
declared inside package 'cci_mpf_if_pkg' shall be treated as localparam File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if_pkg.sv Line: 67
Warning (13228): Verilog HDL or VHDL warning at cci_mpf_if_pkg.sv(81): parameter
declared inside package 'cci_mpf_if_pkg' shall be treated as localparam File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if_pkg.sv Line: 81
Warning (13228): Verilog HDL or VHDL warning at cci_mpf_if_pkg.sv(93): parameter
declared inside package 'cci_mpf_if_pkg' shall be treated as localparam File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if_pkg.sv Line: 93
Warning (13228): Verilog HDL or VHDL warning at cci_mpf_if_pkg.sv(95): parameter
declared inside package 'cci_mpf_if_pkg' shall be treated as localparam File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if_pkg.sv Line: 95
Warning (13228): Verilog HDL or VHDL warning at cci_mpf_if_pkg.sv(98): parameter
declared inside package 'cci_mpf_if_pkg' shall be treated as localparam File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if_pkg.sv Line: 98
Warning (13228): Verilog HDL or VHDL warning at cci_mpf_if_pkg.sv(100): parameter
declared inside package 'cci_mpf_if_pkg' shall be treated as localparam File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if_pkg.sv Line: 100
Warning (13228): Verilog HDL or VHDL warning at cci_mpf_if_pkg.sv(184): parameter
declared inside package 'cci_mpf_if_pkg' shall be treated as localparam File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if_pkg.sv Line: 184
Warning (13228): Verilog HDL or VHDL warning at cci_mpf_if_pkg.sv(185): parameter
declared inside package 'cci_mpf_if_pkg' shall be treated as localparam File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if_pkg.sv Line: 185
Warning (13228): Verilog HDL or VHDL warning at cci_mpf_if_pkg.sv(196): parameter
declared inside package 'cci_mpf_if_pkg' shall be treated as localparam File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if_pkg.sv Line: 196
Warning (13228): Verilog HDL or VHDL warning at cci_mpf_if_pkg.sv(229): parameter
declared inside package 'cci_mpf_if_pkg' shall be treated as localparam File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if_pkg.sv Line: 229
Warning (13228): Verilog HDL or VHDL warning at cci_mpf_if_pkg.sv(250): parameter
declared inside package 'cci_mpf_if_pkg' shall be treated as localparam File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if_pkg.sv Line: 250
Warning (13228): Verilog HDL or VHDL warning at cci_mpf_if_pkg.sv(258): parameter
declared inside package 'cci_mpf_if_pkg' shall be treated as localparam File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if_pkg.sv Line: 258
Warning (13228): Verilog HDL or VHDL warning at ccip_feature_list_pkg.sv(9): parameter
declared inside package 'ccip_feature_list_pkg' shall be treated as localparam File: /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-if/ccip_feature_list_pkg.sv Line: 9
Warning (13228): Verilog HDL or VHDL warning at ccip_feature_list_pkg.sv(10):
parameter declared inside package 'ccip_feature_list_pkg' shall be treated as
localparam File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-if/
ccip_feature_list_pkg.sv Line: 10
Info (16884): Verilog HDL info at cci_mpf_csrs_pkg.sv(42): analyzing included file /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/sw/include/opae/mpf/cci_mpf_csrs.h File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs_pkg.sv Line: 42
Info (13230): Verilog HDL or VHDL information at cci_mpf_csrs_pkg.sv(42): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs_pkg.sv' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs_pkg.sv Line: 42
Warning (13228): Verilog HDL or VHDL warning at cci_mpf_csrs_pkg.sv(56): parameter
declared inside package 'cci_mpf_csrs_pkg' shall be treated as localparam File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs_pkg.sv Line: 56
Info (16884): Verilog HDL info at cci_mpf.sv(37): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh File: /home/u59497/
intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf.sv Line: 37
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Info (16884): Verilog HDL info at cci_mpf_if.vh(8): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if.vh(8): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Info (13230): Verilog HDL or VHDL information at cci_mpf.sv(37): back to file '/home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf.sv' File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci_mpf.sv Line: 37
Info (16884): Verilog HDL info at cci_mpf.sv(38): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh File: /home/u59497/intel-
fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf.sv Line: 38
Info (16884): Verilog HDL info at cci_mpf_csrs.vh(34): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-if/cci_csr_if.vh File: /home/u59497/
intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh Line: 34
Info (13230): Verilog HDL or VHDL information at cci_mpf_csrs.vh(34): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh' File: /home/u59497/
intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh Line: 34
Info (13230): Verilog HDL or VHDL information at cci_mpf.sv(38): back to file '/home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf.sv' File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci_mpf.sv Line: 38
Info (16884): Verilog HDL info at cci_mpf.sv(39): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_edge/
cci_mpf_shim_edge.vh File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf.sv
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf.sv(39): back to file '/home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf.sv' File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci_mpf.sv Line: 39
Info (16884): Verilog HDL info at cci_mpf.sv(40): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/
cci_mpf_shim_pwrite.vh File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf.sv
Line: 40
Info (16884): Verilog HDL info at cci_mpf_shim_pwrite.vh(34): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh File: /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/
cci_mpf_shim_pwrite.vh Line: 34
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_pwrite.vh(34): back to
file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
```

cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.vh' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.vh Line: 34
Info (13230): Verilog HDL or VHDL information at cci_mpf.sv(40): back to file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf.sv Line: 40
Info (16884): Verilog HDL info at cci_mpf_null.sv(41): analyzing included file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_null.sv Line: 41
Info (16884): Verilog HDL info at cci_mpf_if.vh(8): analyzing included file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if.vh(8): back to file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Warning (16817): Verilog HDL warning at cci_mpf_if.vh(135): overwriting previous definition of cci_mpf_if interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 135
Info (18437): Verilog HDL info at cci_mpf_if.vh(135): previous definition of module cci_mpf_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 135
Info (13230): Verilog HDL or VHDL information at cci_mpf_null.sv(41): back to file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_null.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_null.sv Line: 41
Info (16884): Verilog HDL info at cci_mpf_null.sv(42): analyzing included file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_null.sv Line: 42
Info (16884): Verilog HDL info at cci_mpf_csrs.vh(34): analyzing included file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-if/cci_csr_if.vh File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh Line: 34
Info (13230): Verilog HDL or VHDL information at cci_mpf_csrs.vh(34): back to file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh Line: 34
Warning (16817): Verilog HDL warning at cci_mpf_csrs.vh(204): overwriting previous definition of cci_mpf_csrs interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh Line: 204
Info (18437): Verilog HDL info at cci_mpf_csrs.vh(204): previous definition of module cci_mpf_csrs is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh Line: 204

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Info (13230): Verilog HDL or VHDL information at cci_mpf_null.sv(42): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_null.sv' File: /home/u59497/
intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_null.sv Line: 42
Info (16884): Verilog HDL info at cci_mpf_null.sv(43): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_edge/
cci_mpf_shim_edge.vh File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/
cci_mpf_null.sv Line: 43
Warning (16817): Verilog HDL warning at cci_mpf_shim_edge.vh(88): overwriting previous
definition of cci_mpf_shim_edge_if interface File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_edge/cci_mpf_shim_edge.vh Line: 88
Info (18437): Verilog HDL info at cci_mpf_shim_edge.vh(88): previous definition of
module cci_mpf_shim_edge_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-shims/cci_mpf_shim_edge/cci_mpf_shim_edge.vh Line: 88
Info (13230): Verilog HDL or VHDL information at cci_mpf_null.sv(43): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_null.sv' File: /home/u59497/
intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_null.sv Line: 43
Info (16884): Verilog HDL info at cci_mpf_null.sv(44): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/
cci_mpf_shim_pwrite.vh File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/
cci_mpf_null.sv Line: 44
Info (16884): Verilog HDL info at cci_mpf_shim_pwrite.vh(34): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh File: /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/
cci_mpf_shim_pwrite.vh Line: 34
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_pwrite.vh(34): back to
file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.vh' File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.vh Line: 34
Warning (16817): Verilog HDL warning at cci_mpf_shim_pwrite.vh(95): overwriting
previous definition of cci_mpf_shim_pwrite_if interface File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.vh Line:
95
Info (18437): Verilog HDL info at cci_mpf_shim_pwrite.vh(95): previous definition of
module cci_mpf_shim_pwrite_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/
hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.vh Line: 95
Warning (16817): Verilog HDL warning at cci_mpf_shim_pwrite.vh(131): overwriting
previous definition of cci_mpf_shim_pwrite_lock_if interface File: /home/u59497/intel-
fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.vh
Line: 131
Info (18437): Verilog HDL info at cci_mpf_shim_pwrite.vh(131): previous definition of
module cci_mpf_shim_pwrite_lock_if is here File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.vh Line: 131
Info (13230): Verilog HDL or VHDL information at cci_mpf_null.sv(44): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_null.sv' File: /home/u59497/
intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_null.sv Line: 44
Info (16884): Verilog HDL info at cci_mpf_pipe_std.sv(48): analyzing included file /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_pipe_std.sv Line: 48
Info (16884): Verilog HDL info at cci_mpf_if.vh(8): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
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Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if.vh(8): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Warning (16817): Verilog HDL warning at cci_mpf_if.vh(135): overwriting previous
definition of cci_mpf_if interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-if/cci_mpf_if.vh Line: 135
Info (18437): Verilog HDL info at cci_mpf_if.vh(135): previous definition of module
cci_mpf_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/
cci_mpf_if.vh Line: 135
Info (13230): Verilog HDL or VHDL information at cci_mpf_pipe_std.sv(48): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_pipe_std.sv' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_pipe_std.sv Line: 48
Info (16884): Verilog HDL info at cci_mpf_pipe_std.sv(49): analyzing included file /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh File: /home/u59497/
intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_pipe_std.sv Line: 49
Info (16884): Verilog HDL info at cci_mpf_csrs.vh(34): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-if/cci_csr_if.vh File: /home/u59497/
intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh Line: 34
Info (13230): Verilog HDL or VHDL information at cci_mpf_csrs.vh(34): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh' File: /home/u59497/
intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh Line: 34
Warning (16817): Verilog HDL warning at cci_mpf_csrs.vh(204): overwriting previous
definition of cci_mpf_csrs interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci_mpf_csrs.vh Line: 204
Info (18437): Verilog HDL info at cci_mpf_csrs.vh(204): previous definition of module
cci_mpf_csrs is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/
cci_mpf_csrs.vh Line: 204
Info (13230): Verilog HDL or VHDL information at cci_mpf_pipe_std.sv(49): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_pipe_std.sv' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_pipe_std.sv Line: 49
Info (16884): Verilog HDL info at cci_mpf_pipe_std.sv(50): analyzing included file /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_edge/
cci_mpf_shim_edge.vh File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/
cci_mpf_pipe_std.sv Line: 50
Warning (16817): Verilog HDL warning at cci_mpf_shim_edge.vh(88): overwriting previous
definition of cci_mpf_shim_edge_if interface File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_edge/cci_mpf_shim_edge.vh Line: 88
Info (18437): Verilog HDL info at cci_mpf_shim_edge.vh(88): previous definition of
module cci_mpf_shim_edge_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-shims/cci_mpf_shim_edge/cci_mpf_shim_edge.vh Line: 88
Info (13230): Verilog HDL or VHDL information at cci_mpf_pipe_std.sv(50): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_pipe_std.sv' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_pipe_std.sv Line: 50
Info (16884): Verilog HDL info at cci_mpf_pipe_std.sv(51): analyzing included file /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/
cci_mpf_shim_pwrite.vh File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/
cci_mpf_pipe_std.sv Line: 51
Info (16884): Verilog HDL info at cci_mpf_shim_pwrite.vh(34): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh File: /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/
cci_mpf_shim_pwrite.vh Line: 34
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Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_pwrite.vh(34): back to
file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.vh' File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.vh Line: 34
Warning (16817): Verilog HDL warning at cci_mpf_shim_pwrite.vh(95): overwriting
previous definition of cci_mpf_shim_pwrite_if interface File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.vh Line:
95
Info (18437): Verilog HDL info at cci_mpf_shim_pwrite.vh(95): previous definition of
module cci_mpf_shim_pwrite_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/
hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.vh Line: 95
Warning (16817): Verilog HDL warning at cci_mpf_shim_pwrite.vh(131): overwriting
previous definition of cci_mpf_shim_pwrite_lock_if interface File: /home/u59497/intel-
fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.vh
Line: 131
Info (18437): Verilog HDL info at cci_mpf_shim_pwrite.vh(131): previous definition of
module cci_mpf_shim_pwrite_lock_if is here File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.vh Line: 131
Info (13230): Verilog HDL or VHDL information at cci_mpf_pipe_std.sv(51): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_pipe_std.sv' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_pipe_std.sv Line: 51
Info (16884): Verilog HDL info at cci_mpf_pipe_std.sv(52): analyzing included file /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_shim_vtp.vh File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/
cci_mpf_pipe_std.sv Line: 52
Info (16884): Verilog HDL info at cci_mpf_shim_vtp.vh(34): analyzing included file /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_shim_vtp.vh Line: 34
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_vtp.vh(34): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_shim_vtp.vh' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 34
Info (13230): Verilog HDL or VHDL information at cci_mpf_pipe_std.sv(52): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_pipe_std.sv' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_pipe_std.sv Line: 52
Info (16884): Verilog HDL info at ccip_wires_to_mpf.sv(5): analyzing included file /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/ccip_wires_to_mpf.sv Line: 5
Info (16884): Verilog HDL info at cci_mpf_if.vh(8): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
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Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if.vh(8): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Warning (16817): Verilog HDL warning at cci_mpf_if.vh(135): overwriting previous
definition of cci_mpf_if interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-if/cci_mpf_if.vh Line: 135
Info (18437): Verilog HDL info at cci_mpf_if.vh(135): previous definition of module
cci_mpf_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/
cci_mpf_if.vh Line: 135
Info (13230): Verilog HDL or VHDL information at ccip_wires_to_mpf.sv(5): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/ccip_wires_to_mpf.sv' File:
/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/ccip_wires_to_mpf.sv Line: 5
Warning (16818): Verilog HDL warning at ccip_wires_to_mpf.sv(94): block identifier is
required on this block File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
if/ccip_wires_to_mpf.sv Line: 94
Warning (16818): Verilog HDL warning at ccip_wires_to_mpf.sv(132): block identifier is
required on this block File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
if/ccip_wires_to_mpf.sv Line: 132
Info (16884): Verilog HDL info at ccis_wires_to_mpf.sv(11): analyzing included file /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/ccis_wires_to_mpf.sv Line: 11
Info (16884): Verilog HDL info at cci_mpf_if.vh(8): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if.vh(8): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Warning (16817): Verilog HDL warning at cci_mpf_if.vh(135): overwriting previous
definition of cci_mpf_if interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-if/cci_mpf_if.vh Line: 135
Info (18437): Verilog HDL info at cci_mpf_if.vh(135): previous definition of module
cci_mpf_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/
cci_mpf_if.vh Line: 135
Info (13230): Verilog HDL or VHDL information at ccis_wires_to_mpf.sv(11): back to
file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/ccis_wires_to_mpf.sv'
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File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/ccis_wires_to_mpf.sv
Line: 11
Info (16884): Verilog HDL info at cci_mpf_prim_fifo_bram.sv(37): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-prims/
cci_mpf_prim_fifo_bram.sv Line: 37
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_prim_fifo_bram.sv(37): back
to file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-prims/
cci_mpf_prim_fifo_bram.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-
mpf-prims/cci_mpf_prim_fifo_bram.sv Line: 37
Info (16884): Verilog HDL info at cci_mpf_prim_ram_dualport.sv(42): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-prims/
cci_mpf_prim_ram_dualport.sv Line: 42
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
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Info (13230): Verilog HDL or VHDL information at cci_mpf_prim_ram_dualport.sv(42):
back to file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-prims/
cci_mpf_prim_ram_dualport.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/
cci-mpf-prims/cci_mpf_prim_ram_dualport.sv Line: 42
Info (16884): Verilog HDL info at cci_mpf_prim_ram_simple.sv(36): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-prims/
cci_mpf_prim_ram_simple.sv Line: 36
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_prim_ram_simple.sv(36): back
to file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-prims/
cci_mpf_prim_ram_simple.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-
mpf-prims/cci_mpf_prim_ram_simple.sv Line: 36
Info (16884): Verilog HDL info at cci_mpf_prim_track_active_reqs.sv(35): analyzing
included file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-prims/
cci_mpf_prim_track_active_reqs.sv Line: 35
Info (16884): Verilog HDL info at cci_mpf_if.vh(8): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
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Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if.vh(8): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Warning (16817): Verilog HDL warning at cci_mpf_if.vh(135): overwriting previous
definition of cci_mpf_if interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-if/cci_mpf_if.vh Line: 135
Info (18437): Verilog HDL info at cci_mpf_if.vh(135): previous definition of module
cci_mpf_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/
cci_mpf_if.vh Line: 135
Info (13230): Verilog HDL or VHDL information at
cci_mpf_prim_track_active_reqs.sv(35): back to file '/home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-prims/cci_mpf_prim_track_active_reqs.sv' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-prims/
cci_mpf_prim_track_active_reqs.sv Line: 35
Info (16884): Verilog HDL info at cci_mpf_prim_track_multi_write.sv(31): analyzing
included file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-prims/
cci_mpf_prim_track_multi_write.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_if.vh(8): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if.vh(8): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Warning (16817): Verilog HDL warning at cci_mpf_if.vh(135): overwriting previous
definition of cci_mpf_if interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-if/cci_mpf_if.vh Line: 135
Info (18437): Verilog HDL info at cci_mpf_if.vh(135): previous definition of module
cci_mpf_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/
cci_mpf_if.vh Line: 135
Info (13230): Verilog HDL or VHDL information at
cci_mpf_prim_track_multi_write.sv(31): back to file '/home/u59497/intel-fpga-bbb/
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BBB_cci_mpf/hw/rtl/cci-mpf-prims/cci_mpf_prim_track_multi_write.sv' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-prims/
cci_mpf_prim_track_multi_write.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_shim_buffer_afu.sv(31): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh File: /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_buffer_afu.sv
Line: 31
Info (16884): Verilog HDL info at cci_mpf_if.vh(8): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if.vh(8): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Warning (16817): Verilog HDL warning at cci_mpf_if.vh(135): overwriting previous
definition of cci_mpf_if interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-if/cci_mpf_if.vh Line: 135
Info (18437): Verilog HDL info at cci_mpf_if.vh(135): previous definition of module
cci_mpf_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/
cci_mpf_if.vh Line: 135
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_buffer_afu.sv(31): back
to file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_buffer_afu.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-
mpf-shims/cci_mpf_shim_buffer_afu.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_shim_buffer_afu_epoch.sv(31): analyzing
included file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_buffer_afu_epoch.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_if.vh(8): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
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Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if.vh(8): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Warning (16817): Verilog HDL warning at cci_mpf_if.vh(135): overwriting previous
definition of cci_mpf_if interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-if/cci_mpf_if.vh Line: 135
Info (18437): Verilog HDL info at cci_mpf_if.vh(135): previous definition of module
cci_mpf_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/
cci_mpf_if.vh Line: 135
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_buffer_afu_epoch.sv(31):
back to file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_buffer_afu_epoch.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-shims/cci_mpf_shim_buffer_afu_epoch.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_shim_buffer_afu_epoch.sv(32): analyzing
included file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-prims/
cci_mpf_prim_hash.vh File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_buffer_afu_epoch.sv Line: 32
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_buffer_afu_epoch.sv(32):
back to file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_buffer_afu_epoch.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-shims/cci_mpf_shim_buffer_afu_epoch.sv Line: 32
Info (16884): Verilog HDL info at cci_mpf_shim_buffer_afu_lockstep.sv(31): analyzing
included file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_buffer_afu_lockstep.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_if.vh(8): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
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Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if.vh(8): back to file '/
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u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Warning (16817): Verilog HDL warning at cci_mpf_if.vh(135): overwriting previous
definition of cci_mpf_if interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-if/cci_mpf_if.vh Line: 135
Info (18437): Verilog HDL info at cci_mpf_if.vh(135): previous definition of module
cci_mpf_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/
cci_mpf_if.vh Line: 135
Info (13230): Verilog HDL or VHDL information at
cci_mpf_shim_buffer_afu_lockstep.sv(31): back to file '/home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_buffer_afu_lockstep.sv' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_buffer_afu_lockstep.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_shim_buffer_fiu.sv(31): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh File: /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_buffer_fiu.sv
Line: 31
Info (16884): Verilog HDL info at cci_mpf_if.vh(8): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if.vh(8): back to file '/
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u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Warning (16817): Verilog HDL warning at cci_mpf_if.vh(135): overwriting previous
definition of cci_mpf_if interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-if/cci_mpf_if.vh Line: 135
Info (18437): Verilog HDL info at cci_mpf_if.vh(135): previous definition of module
cci_mpf_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/
cci_mpf_if.vh Line: 135
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_buffer_fiu.sv(31): back
to file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
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cci_mpf_shim_buffer_fiu.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-
mpf-shims/cci_mpf_shim_buffer_fiu.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_shim_csr.sv(31): analyzing included file /
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u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_csr.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_if.vh(8): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if.vh(8): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Warning (16817): Verilog HDL warning at cci_mpf_if.vh(135): overwriting previous
definition of cci_mpf_if interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-if/cci_mpf_if.vh Line: 135
Info (18437): Verilog HDL info at cci_mpf_if.vh(135): previous definition of module
cci_mpf_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/
cci_mpf_if.vh Line: 135
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_csr.sv(31): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_csr.sv'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_csr.sv
Line: 31
Info (16884): Verilog HDL info at cci_mpf_shim_csr.sv(32): analyzing included file /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh File: /home/u59497/
intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_csr.sv Line: 32
Info (16884): Verilog HDL info at cci_mpf_csrs.vh(34): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-if/cci_csr_if.vh File: /home/u59497/
intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh Line: 34
Info (13230): Verilog HDL or VHDL information at cci_mpf_csrs.vh(34): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh' File: /home/u59497/
intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh Line: 34
Warning (16817): Verilog HDL warning at cci_mpf_csrs.vh(204): overwriting previous
definition of cci_mpf_csrs interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci_mpf_csrs.vh Line: 204
Info (18437): Verilog HDL info at cci_mpf_csrs.vh(204): previous definition of module
cci_mpf_csrs is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/
cci_mpf_csrs.vh Line: 204
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_csr.sv(32): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_csr.sv'
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File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_csr.sv
Line: 32
Warning (13228): Verilog HDL or VHDL warning at cci_mpf_shim_csr.sv(42): parameter
declared inside compilation unit
'$unit__home_u59497_intel_fpga_bbb_BBB_cci_mpf_hw_rtl_cci_mpf_shims_cci_mpf_shim_csr_s
v' shall be treated as localparam File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-shims/cci_mpf_shim_csr.sv Line: 42
Warning (13228): Verilog HDL or VHDL warning at cci_mpf_shim_csr.sv(45): parameter
declared inside compilation unit
'$unit__home_u59497_intel_fpga_bbb_BBB_cci_mpf_hw_rtl_cci_mpf_shims_cci_mpf_shim_csr_s
v' shall be treated as localparam File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-shims/cci_mpf_shim_csr.sv Line: 45
Warning (13228): Verilog HDL or VHDL warning at cci_mpf_shim_csr.sv(53): parameter
declared inside compilation unit
'$unit__home_u59497_intel_fpga_bbb_BBB_cci_mpf_hw_rtl_cci_mpf_shims_cci_mpf_shim_csr_s
v' shall be treated as localparam File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-shims/cci_mpf_shim_csr.sv Line: 53
Warning (13228): Verilog HDL or VHDL warning at cci_mpf_shim_csr.sv(55): parameter
declared inside compilation unit
'$unit__home_u59497_intel_fpga_bbb_BBB_cci_mpf_hw_rtl_cci_mpf_shims_cci_mpf_shim_csr_s
v' shall be treated as localparam File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-shims/cci_mpf_shim_csr.sv Line: 55
Warning (13228): Verilog HDL or VHDL warning at cci_mpf_shim_csr.sv(57): parameter
declared inside compilation unit
'$unit__home_u59497_intel_fpga_bbb_BBB_cci_mpf_hw_rtl_cci_mpf_shims_cci_mpf_shim_csr_s
v' shall be treated as localparam File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-shims/cci_mpf_shim_csr.sv Line: 57
Warning (13228): Verilog HDL or VHDL warning at cci_mpf_shim_csr.sv(59): parameter
declared inside compilation unit
'$unit__home_u59497_intel_fpga_bbb_BBB_cci_mpf_hw_rtl_cci_mpf_shims_cci_mpf_shim_csr_s
v' shall be treated as localparam File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-shims/cci_mpf_shim_csr.sv Line: 59
Warning (13228): Verilog HDL or VHDL warning at cci_mpf_shim_csr.sv(61): parameter
declared inside compilation unit
'$unit__home_u59497_intel_fpga_bbb_BBB_cci_mpf_hw_rtl_cci_mpf_shims_cci_mpf_shim_csr_s
v' shall be treated as localparam File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-shims/cci_mpf_shim_csr.sv Line: 61
Warning (13228): Verilog HDL or VHDL warning at cci_mpf_shim_csr.sv(63): parameter
declared inside compilation unit
'$unit__home_u59497_intel_fpga_bbb_BBB_cci_mpf_hw_rtl_cci_mpf_shims_cci_mpf_shim_csr_s
v' shall be treated as localparam File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-shims/cci_mpf_shim_csr.sv Line: 63
Warning (13228): Verilog HDL or VHDL warning at cci_mpf_shim_csr.sv(67): parameter
declared inside compilation unit
'$unit__home_u59497_intel_fpga_bbb_BBB_cci_mpf_hw_rtl_cci_mpf_shims_cci_mpf_shim_csr_s
v' shall be treated as localparam File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-shims/cci_mpf_shim_csr.sv Line: 67
Warning (13228): Verilog HDL or VHDL warning at cci_mpf_shim_csr.sv(70): parameter
declared inside compilation unit
'$unit__home_u59497_intel_fpga_bbb_BBB_cci_mpf_hw_rtl_cci_mpf_shims_cci_mpf_shim_csr_s
v' shall be treated as localparam File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-shims/cci_mpf_shim_csr.sv Line: 70
Info (16884): Verilog HDL info at cci_mpf_shim_dedup_reads.sv(31): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh File: /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_dedup_reads.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_if.vh(8): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
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Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if.vh(8): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Warning (16817): Verilog HDL warning at cci_mpf_if.vh(135): overwriting previous
definition of cci_mpf_if interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-if/cci_mpf_if.vh Line: 135
Info (18437): Verilog HDL info at cci_mpf_if.vh(135): previous definition of module
cci_mpf_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/
cci_mpf_if.vh Line: 135
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_dedup_reads.sv(31): back
to file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_dedup_reads.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-
mpf-shims/cci_mpf_shim_dedup_reads.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_shim_detect_eop.sv(31): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh File: /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_detect_eop.sv
Line: 31
Info (16884): Verilog HDL info at cci_mpf_if.vh(8): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
```

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Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if.vh(8): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Warning (16817): Verilog HDL warning at cci_mpf_if.vh(135): overwriting previous
definition of cci_mpf_if interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-if/cci_mpf_if.vh Line: 135
Info (18437): Verilog HDL info at cci_mpf_if.vh(135): previous definition of module
cci_mpf_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/
cci_mpf_if.vh Line: 135
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_detect_eop.sv(31): back
to file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_detect_eop.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-
mpf-shims/cci_mpf_shim_detect_eop.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_shim_edge_afu.sv(31): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh File: /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_edge/
cci_mpf_shim_edge_afu.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_if.vh(8): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if.vh(8): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Warning (16817): Verilog HDL warning at cci_mpf_if.vh(135): overwriting previous
definition of cci_mpf_if interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-if/cci_mpf_if.vh Line: 135
Info (18437): Verilog HDL info at cci_mpf_if.vh(135): previous definition of module
cci_mpf_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/
cci_mpf_if.vh Line: 135
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_edge_afu.sv(31): back to
file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_edge/
cci_mpf_shim_edge_afu.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-
mpf-shims/cci_mpf_shim_edge/cci_mpf_shim_edge_afu.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_shim_edge_afu.sv(32): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_edge/
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cci_mpf_shim_edge.vh File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_edge/cci_mpf_shim_edge_afu.sv Line: 32
Warning (16817): Verilog HDL warning at cci_mpf_shim_edge.vh(88): overwriting previous
definition of cci_mpf_shim_edge_if interface File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_edge/cci_mpf_shim_edge.vh Line: 88
Info (18437): Verilog HDL info at cci_mpf_shim_edge.vh(88): previous definition of
module cci_mpf_shim_edge_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-shims/cci_mpf_shim_edge/cci_mpf_shim_edge.vh Line: 88
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_edge_afu.sv(32): back to
file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_edge/
cci_mpf_shim_edge_afu.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-
mpf-shims/cci_mpf_shim_edge/cci_mpf_shim_edge_afu.sv Line: 32
Info (16884): Verilog HDL info at cci_mpf_shim_edge_afu.sv(33): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/
cci_mpf_shim_pwrite.vh File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_edge/cci_mpf_shim_edge_afu.sv Line: 33
Info (16884): Verilog HDL info at cci_mpf_shim_pwrite.vh(34): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh File: /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/
cci_mpf_shim_pwrite.vh Line: 34
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_pwrite.vh(34): back to
file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.vh' File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.vh Line: 34
Warning (16817): Verilog HDL warning at cci_mpf_shim_pwrite.vh(95): overwriting
previous definition of cci_mpf_shim_pwrite_if interface File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.vh Line:
95
Info (18437): Verilog HDL info at cci_mpf_shim_pwrite.vh(95): previous definition of
module cci_mpf_shim_pwrite_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/
hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.vh Line: 95
Warning (16817): Verilog HDL warning at cci_mpf_shim_pwrite.vh(131): overwriting
previous definition of cci_mpf_shim_pwrite_lock_if interface File: /home/u59497/intel-
fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.vh
Line: 131
Info (18437): Verilog HDL info at cci_mpf_shim_pwrite.vh(131): previous definition of
module cci_mpf_shim_pwrite_lock_if is here File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.vh Line: 131
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_edge_afu.sv(33): back to
file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_edge/
cci_mpf_shim_edge_afu.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-
mpf-shims/cci_mpf_shim_edge/cci_mpf_shim_edge_afu.sv Line: 33
Info (16884): Verilog HDL info at cci_mpf_shim_edge_fiu.sv(31): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh File: /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_edge/
cci_mpf_shim_edge_fiu.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_if.vh(8): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
```

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Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if.vh(8): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Warning (16817): Verilog HDL warning at cci_mpf_if.vh(135): overwriting previous
definition of cci_mpf_if interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-if/cci_mpf_if.vh Line: 135
Info (18437): Verilog HDL info at cci_mpf_if.vh(135): previous definition of module
cci_mpf_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/
cci_mpf_if.vh Line: 135
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_edge_fiu.sv(31): back to
file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_edge/
cci_mpf_shim_edge_fiu.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-
mpf-shims/cci_mpf_shim_edge/cci_mpf_shim_edge_fiu.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_shim_edge_fiu.sv(32): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim.vh
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_edge/
cci_mpf_shim_edge_fiu.sv Line: 32
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_edge_fiu.sv(32): back to
file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_edge/
cci_mpf_shim_edge_fiu.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-
mpf-shims/cci_mpf_shim_edge/cci_mpf_shim_edge_fiu.sv Line: 32
Info (16884): Verilog HDL info at cci_mpf_shim_edge_fiu.sv(33): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_edge/
cci_mpf_shim_edge.vh File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_edge/cci_mpf_shim_edge_fiu.sv Line: 33
Warning (16817): Verilog HDL warning at cci_mpf_shim_edge.vh(88): overwriting previous
definition of cci_mpf_shim_edge_if interface File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_edge/cci_mpf_shim_edge.vh Line: 88
Info (18437): Verilog HDL info at cci_mpf_shim_edge.vh(88): previous definition of
module cci_mpf_shim_edge_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-shims/cci_mpf_shim_edge/cci_mpf_shim_edge.vh Line: 88
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_edge_fiu.sv(33): back to
file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_edge/
cci_mpf_shim_edge_fiu.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-
mpf-shims/cci_mpf_shim_edge/cci_mpf_shim_edge_fiu.sv Line: 33
Info (16884): Verilog HDL info at cci_mpf_shim_edge_fiu.sv(34): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/
cci_mpf_shim_pwrite.vh File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_edge/cci_mpf_shim_edge_fiu.sv Line: 34
Info (16884): Verilog HDL info at cci_mpf_shim_pwrite.vh(34): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh File: /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/
cci_mpf_shim_pwrite.vh Line: 34
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_pwrite.vh(34): back to
file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.vh' File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.vh Line: 34
Warning (16817): Verilog HDL warning at cci_mpf_shim_pwrite.vh(95): overwriting
previous definition of cci_mpf_shim_pwrite_if interface File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.vh Line:
95
Info (18437): Verilog HDL info at cci_mpf_shim_pwrite.vh(95): previous definition of
module cci_mpf_shim_pwrite_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/
hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.vh Line: 95
```

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Warning (16817): Verilog HDL warning at cci_mpf_shim_pwrite.vh(131): overwriting
previous definition of cci_mpf_shim_pwrite_lock_if interface File: /home/u59497/intel-
fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.vh
Line: 131
Info (18437): Verilog HDL info at cci_mpf_shim_pwrite.vh(131): previous definition of
module cci_mpf_shim_pwrite_lock_if is here File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.vh Line: 131
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_edge_fiu.sv(34): back to
file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_edge/
cci_mpf_shim_edge_fiu.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-
mpf-shims/cci_mpf_shim_edge/cci_mpf_shim_edge_fiu.sv Line: 34
Info (16884): Verilog HDL info at cci_mpf_shim_latency_qos.sv(31): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh File: /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_latency_qos.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_if.vh(8): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if.vh(8): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Warning (16817): Verilog HDL warning at cci_mpf_if.vh(135): overwriting previous
definition of cci_mpf_if interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-if/cci_mpf_if.vh Line: 135
Info (18437): Verilog HDL info at cci_mpf_if.vh(135): previous definition of module
cci_mpf_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/
cci_mpf_if.vh Line: 135
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_latency_qos.sv(31): back
to file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_latency_qos.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-
mpf-shims/cci_mpf_shim_latency_qos.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_shim_latency_qos.sv(32): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-if/cci_csr_if.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_latency_qos.sv
Line: 32
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_latency_qos.sv(32): back
to file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_latency_qos.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-
mpf-shims/cci_mpf_shim_latency_qos.sv Line: 32
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Info (16884): Verilog HDL info at cci_mpf_shim_mux.sv(31): analyzing included file /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_mux.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_if.vh(8): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if.vh(8): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Warning (16817): Verilog HDL warning at cci_mpf_if.vh(135): overwriting previous
definition of cci_mpf_if interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-if/cci_mpf_if.vh Line: 135
Info (18437): Verilog HDL info at cci_mpf_if.vh(135): previous definition of module
cci_mpf_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/
cci_mpf_if.vh Line: 135
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_mux.sv(31): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_mux.sv'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_mux.sv
Line: 31
Info (16884): Verilog HDL info at cci_mpf_shim_null.sv(31): analyzing included file /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_null.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_if.vh(8): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
```

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Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if.vh(8): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Warning (16817): Verilog HDL warning at cci_mpf_if.vh(135): overwriting previous
definition of cci_mpf_if interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-if/cci_mpf_if.vh Line: 135
Info (18437): Verilog HDL info at cci_mpf_if.vh(135): previous definition of module
cci_mpf_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/
cci_mpf_if.vh Line: 135
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_null.sv(31): back to
file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_null.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_null.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_shim_pwrite.sv(31): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh File: /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/
cci_mpf_shim_pwrite.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_if.vh(8): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if.vh(8): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Warning (16817): Verilog HDL warning at cci_mpf_if.vh(135): overwriting previous
definition of cci_mpf_if interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-if/cci_mpf_if.vh Line: 135
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Info (18437): Verilog HDL info at cci_mpf_if.vh(135): previous definition of module
cci_mpf_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/
cci_mpf_if.vh Line: 135
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_pwrite.sv(31): back to
file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.sv' File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_shim_pwrite.sv(32): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim.vh
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.sv Line: 32
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_pwrite.sv(32): back to
file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.sv' File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.sv Line: 32
Info (16884): Verilog HDL info at cci_mpf_shim_pwrite.sv(33): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/
cci_mpf_shim_pwrite.vh File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.sv Line: 33
Info (16884): Verilog HDL info at cci_mpf_shim_pwrite.vh(34): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh File: /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/
cci_mpf_shim_pwrite.vh Line: 34
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_pwrite.vh(34): back to
file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.vh' File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.vh Line: 34
Warning (16817): Verilog HDL warning at cci_mpf_shim_pwrite.vh(95): overwriting
previous definition of cci_mpf_shim_pwrite_if interface File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.vh Line:
95
Info (18437): Verilog HDL info at cci_mpf_shim_pwrite.vh(95): previous definition of
module cci_mpf_shim_pwrite_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/
hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.vh Line: 95
Warning (16817): Verilog HDL warning at cci_mpf_shim_pwrite.vh(131): overwriting
previous definition of cci_mpf_shim_pwrite_lock_if interface File: /home/u59497/intel-
fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.vh
Line: 131
Info (18437): Verilog HDL info at cci_mpf_shim_pwrite.vh(131): previous definition of
module cci_mpf_shim_pwrite_lock_if is here File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.vh Line: 131
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_pwrite.sv(33): back to
file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.sv' File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_pwrite/cci_mpf_shim_pwrite.sv Line: 33
Info (16884): Verilog HDL info at cci_mpf_shim_rsp_order.sv(31): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh File: /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_rsp_order.sv
Line: 31
Info (16884): Verilog HDL info at cci_mpf_if.vh(8): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
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Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if.vh(8): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Warning (16817): Verilog HDL warning at cci_mpf_if.vh(135): overwriting previous
definition of cci_mpf_if interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-if/cci_mpf_if.vh Line: 135
Info (18437): Verilog HDL info at cci_mpf_if.vh(135): previous definition of module
cci_mpf_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/
cci_mpf_if.vh Line: 135
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_rsp_order.sv(31): back
to file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_rsp_order.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-
mpf-shims/cci_mpf_shim_rsp_order.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_shim_rsp_order.sv(32): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_rsp_order.sv Line:
32
Info (16884): Verilog HDL info at cci_mpf_csrs.vh(34): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-if/cci_csr_if.vh File: /home/u59497/
intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh Line: 34
Info (13230): Verilog HDL or VHDL information at cci_mpf_csrs.vh(34): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh' File: /home/u59497/
intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh Line: 34
Warning (16817): Verilog HDL warning at cci_mpf_csrs.vh(204): overwriting previous
definition of cci_mpf_csrs interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci_mpf_csrs.vh Line: 204
Info (18437): Verilog HDL info at cci_mpf_csrs.vh(204): previous definition of module
cci_mpf_csrs is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/
cci_mpf_csrs.vh Line: 204
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_rsp_order.sv(32): back
to file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_rsp_order.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-
mpf-shims/cci_mpf_shim_rsp_order.sv Line: 32
Info (16884): Verilog HDL info at cci_mpf_shim_vc_map.sv(31): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh File: /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vc_map.sv
Line: 31
Info (16884): Verilog HDL info at cci_mpf_if.vh(8): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
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Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if.vh(8): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Warning (16817): Verilog HDL warning at cci_mpf_if.vh(135): overwriting previous
definition of cci_mpf_if interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-if/cci_mpf_if.vh Line: 135
Info (18437): Verilog HDL info at cci_mpf_if.vh(135): previous definition of module
cci_mpf_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/
cci_mpf_if.vh Line: 135
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_vc_map.sv(31): back to
file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_vc_map.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_vc_map.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_shim_vc_map.sv(32): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vc_map.sv Line: 32
Info (16884): Verilog HDL info at cci_mpf_csrs.vh(34): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-if/cci_csr_if.vh File: /home/u59497/
intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh Line: 34
Info (13230): Verilog HDL or VHDL information at cci_mpf_csrs.vh(34): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh' File: /home/u59497/
intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh Line: 34
Warning (16817): Verilog HDL warning at cci_mpf_csrs.vh(204): overwriting previous
definition of cci_mpf_csrs interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci_mpf_csrs.vh Line: 204
Info (18437): Verilog HDL info at cci_mpf_csrs.vh(204): previous definition of module
cci_mpf_csrs is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/
cci_mpf_csrs.vh Line: 204
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_vc_map.sv(32): back to
file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_vc_map.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_vc_map.sv Line: 32
Info (16884): Verilog HDL info at cci_mpf_shim_vc_map.sv(34): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-prims/cci_mpf_prim_hash.vh
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_vc_map.sv Line: 34
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_vc_map.sv(34): back to
file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_vc_map.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_vc_map.sv Line: 34
Info (16884): Verilog HDL info at cci_mpf_shim_vtp.sv(31): analyzing included file /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_shim_vtp.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_if.vh(8): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
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Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if.vh(8): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Warning (16817): Verilog HDL warning at cci_mpf_if.vh(135): overwriting previous
definition of cci_mpf_if interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-if/cci_mpf_if.vh Line: 135
Info (18437): Verilog HDL info at cci_mpf_if.vh(135): previous definition of module
cci_mpf_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/
cci_mpf_if.vh Line: 135
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_vtp.sv(31): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_shim_vtp.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_shim_vtp.sv(32): analyzing included file /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_shim_vtp.vh File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.sv Line: 32
Info (16884): Verilog HDL info at cci_mpf_shim_vtp.vh(34): analyzing included file /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_shim_vtp.vh Line: 34
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_vtp.vh(34): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_shim_vtp.vh' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 34
Warning (16817): Verilog HDL warning at cci_mpf_shim_vtp.vh(219): overwriting previous
definition of cci_mpf_shim_vtp_svc_if interface File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 219
Info (18437): Verilog HDL info at cci_mpf_shim_vtp.vh(219): previous definition of
module cci_mpf_shim_vtp_svc_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/
hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 219
Warning (16817): Verilog HDL warning at cci_mpf_shim_vtp.vh(305): overwriting previous
definition of cci_mpf_shim_vtp_tlb_if interface File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 305
Info (18437): Verilog HDL info at cci_mpf_shim_vtp.vh(305): previous definition of
module cci_mpf_shim_vtp_tlb_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/
hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 305
```

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Warning (16817): Verilog HDL warning at cci_mpf_shim_vtp.vh(374): overwriting previous
definition of cci_mpf_shim_vtp_pt_walk_if interface File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 374
Info (18437): Verilog HDL info at cci_mpf_shim_vtp.vh(374): previous definition of
module cci_mpf_shim_vtp_pt_walk_if is here File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 374
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_vtp.sv(32): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_shim_vtp.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.sv Line: 32
Info (16884): Verilog HDL info at cci_mpf_shim_vtp.sv(34): analyzing included file /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_config.vh File: /home/u59497/
intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.sv
Line: 34
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_vtp.sv(34): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_shim_vtp.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.sv Line: 34
Info (16884): Verilog HDL info at cci_mpf_svc_vtp.sv(31): analyzing included file /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_svc_vtp.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_if.vh(8): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if.vh(8): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Warning (16817): Verilog HDL warning at cci_mpf_if.vh(135): overwriting previous
definition of cci_mpf_if interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-if/cci_mpf_if.vh Line: 135
Info (18437): Verilog HDL info at cci_mpf_if.vh(135): previous definition of module
cci_mpf_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/
cci_mpf_if.vh Line: 135
Info (13230): Verilog HDL or VHDL information at cci_mpf_svc_vtp.sv(31): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_svc_vtp.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_vtp/cci_mpf_svc_vtp.sv Line: 31
```

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Info (16884): Verilog HDL info at cci_mpf_svc_vtp.sv(32): analyzing included file /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh File: /home/u59497/
intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_svc_vtp.sv
Line: 32
Info (16884): Verilog HDL info at cci_mpf_csrs.vh(34): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-if/cci_csr_if.vh File: /home/u59497/
intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh Line: 34
Info (13230): Verilog HDL or VHDL information at cci_mpf_csrs.vh(34): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh' File: /home/u59497/
intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh Line: 34
Warning (16817): Verilog HDL warning at cci_mpf_csrs.vh(204): overwriting previous
definition of cci_mpf_csrs interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci_mpf_csrs.vh Line: 204
Info (18437): Verilog HDL info at cci_mpf_csrs.vh(204): previous definition of module
cci_mpf_csrs is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/
cci_mpf_csrs.vh Line: 204
Info (13230): Verilog HDL or VHDL information at cci_mpf_svc_vtp.sv(32): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_svc_vtp.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_vtp/cci_mpf_svc_vtp.sv Line: 32
Info (16884): Verilog HDL info at cci_mpf_svc_vtp.sv(34): analyzing included file /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_shim_vtp.vh File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_vtp/cci_mpf_svc_vtp.sv Line: 34
Info (16884): Verilog HDL info at cci_mpf_shim_vtp.vh(34): analyzing included file /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_shim_vtp.vh Line: 34
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_vtp.vh(34): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_shim_vtp.vh' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 34
Warning (16817): Verilog HDL warning at cci_mpf_shim_vtp.vh(219): overwriting previous
definition of cci_mpf_shim_vtp_svc_if interface File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 219
Info (18437): Verilog HDL info at cci_mpf_shim_vtp.vh(219): previous definition of
module cci_mpf_shim_vtp_svc_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/
hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 219
Warning (16817): Verilog HDL warning at cci_mpf_shim_vtp.vh(305): overwriting previous
definition of cci_mpf_shim_vtp_tlb_if interface File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 305
Info (18437): Verilog HDL info at cci_mpf_shim_vtp.vh(305): previous definition of
module cci_mpf_shim_vtp_tlb_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/
hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 305
Warning (16817): Verilog HDL warning at cci_mpf_shim_vtp.vh(374): overwriting previous
definition of cci_mpf_shim_vtp_pt_walk_if interface File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 374
Info (18437): Verilog HDL info at cci_mpf_shim_vtp.vh(374): previous definition of
module cci_mpf_shim_vtp_pt_walk_if is here File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 374
Info (13230): Verilog HDL or VHDL information at cci_mpf_svc_vtp.sv(34): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
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shims/cci_mpf_shim_vtp/cci_mpf_svc_vtp.sv Line: 34
Info (16884): Verilog HDL info at cci_mpf_svc_vtp.sv(35): analyzing included file /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_config.vh File: /home/u59497/
intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_svc_vtp.sv
Line: 35
Info (13230): Verilog HDL or VHDL information at cci_mpf_svc_vtp.sv(35): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_svc_vtp.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_vtp/cci_mpf_svc_vtp.sv Line: 35
Info (16884): Verilog HDL info at cci_mpf_svc_vtp_pipe.sv(31): analyzing included file
/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh File: /home/
```

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u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_svc_vtp_pipe.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_if.vh(8): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if.vh(8): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Warning (16817): Verilog HDL warning at cci_mpf_if.vh(135): overwriting previous
definition of cci_mpf_if interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-if/cci_mpf_if.vh Line: 135
Info (18437): Verilog HDL info at cci_mpf_if.vh(135): previous definition of module
cci_mpf_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/
cci_mpf_if.vh Line: 135
Info (13230): Verilog HDL or VHDL information at cci_mpf_svc_vtp_pipe.sv(31): back to
file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_svc_vtp_pipe.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_vtp/cci_mpf_svc_vtp_pipe.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_svc_vtp_pipe.sv(32): analyzing included file
/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh File: /home/u59497/
intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_svc_vtp_pipe.sv Line: 32
Info (16884): Verilog HDL info at cci_mpf_csrs.vh(34): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-if/cci_csr_if.vh File: /home/u59497/
intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh Line: 34
Info (13230): Verilog HDL or VHDL information at cci_mpf_csrs.vh(34): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh' File: /home/u59497/
intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh Line: 34
Warning (16817): Verilog HDL warning at cci_mpf_csrs.vh(204): overwriting previous
definition of cci_mpf_csrs interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci_mpf_csrs.vh Line: 204
Info (18437): Verilog HDL info at cci_mpf_csrs.vh(204): previous definition of module
cci_mpf_csrs is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/
cci_mpf_csrs.vh Line: 204
Info (13230): Verilog HDL or VHDL information at cci_mpf_svc_vtp_pipe.sv(32): back to
file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_svc_vtp_pipe.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_vtp/cci_mpf_svc_vtp_pipe.sv Line: 32
```

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Info (16884): Verilog HDL info at cci_mpf_svc_vtp_pipe.sv(34): analyzing included file
/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_shim_vtp.vh File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_vtp/cci_mpf_svc_vtp_pipe.sv Line: 34
Info (16884): Verilog HDL info at cci_mpf_shim_vtp.vh(34): analyzing included file /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_shim_vtp.vh Line: 34
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_vtp.vh(34): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_shim_vtp.vh' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 34
Warning (16817): Verilog HDL warning at cci_mpf_shim_vtp.vh(219): overwriting previous
definition of cci_mpf_shim_vtp_svc_if interface File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 219
Info (18437): Verilog HDL info at cci_mpf_shim_vtp.vh(219): previous definition of
module cci_mpf_shim_vtp_svc_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/
hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 219
Warning (16817): Verilog HDL warning at cci_mpf_shim_vtp.vh(305): overwriting previous
definition of cci_mpf_shim_vtp_tlb_if interface File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 305
Info (18437): Verilog HDL info at cci_mpf_shim_vtp.vh(305): previous definition of
module cci_mpf_shim_vtp_tlb_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/
hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 305
Warning (16817): Verilog HDL warning at cci_mpf_shim_vtp.vh(374): overwriting previous
definition of cci_mpf_shim_vtp_pt_walk_if interface File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 374
Info (18437): Verilog HDL info at cci_mpf_shim_vtp.vh(374): previous definition of
module cci_mpf_shim_vtp_pt_walk_if is here File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 374
Info (13230): Verilog HDL or VHDL information at cci_mpf_svc_vtp_pipe.sv(34): back to
file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_svc_vtp_pipe.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_vtp/cci_mpf_svc_vtp_pipe.sv Line: 34
Info (16884): Verilog HDL info at cci_mpf_svc_vtp_pt_walk.sv(32): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh File: /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_svc_vtp_pt_walk.sv Line: 32
Info (16884): Verilog HDL info at cci_mpf_if.vh(8): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
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File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if.vh(8): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Warning (16817): Verilog HDL warning at cci_mpf_if.vh(135): overwriting previous
definition of cci_mpf_if interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-if/cci_mpf_if.vh Line: 135
Info (18437): Verilog HDL info at cci_mpf_if.vh(135): previous definition of module
cci_mpf_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/
cci_mpf_if.vh Line: 135
Info (13230): Verilog HDL or VHDL information at cci_mpf_svc_vtp_pt_walk.sv(32): back
to file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_vtp/cci_mpf_svc_vtp_pt_walk.sv' File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_svc_vtp_pt_walk.sv Line: 32
Info (16884): Verilog HDL info at cci_mpf_svc_vtp_pt_walk.sv(33): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_svc_vtp_pt_walk.sv Line: 33
Info (16884): Verilog HDL info at cci_mpf_csrs.vh(34): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-if/cci_csr_if.vh File: /home/u59497/
intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh Line: 34
Info (13230): Verilog HDL or VHDL information at cci_mpf_csrs.vh(34): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh' File: /home/u59497/
intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh Line: 34
Warning (16817): Verilog HDL warning at cci_mpf_csrs.vh(204): overwriting previous
definition of cci_mpf_csrs interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci_mpf_csrs.vh Line: 204
Info (18437): Verilog HDL info at cci_mpf_csrs.vh(204): previous definition of module
cci_mpf_csrs is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/
cci_mpf_csrs.vh Line: 204
Info (13230): Verilog HDL or VHDL information at cci_mpf_svc_vtp_pt_walk.sv(33): back
to file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_vtp/cci_mpf_svc_vtp_pt_walk.sv' File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_svc_vtp_pt_walk.sv Line: 33
Info (16884): Verilog HDL info at cci_mpf_svc_vtp_pt_walk.sv(35): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_shim_vtp.vh File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_vtp/cci_mpf_svc_vtp_pt_walk.sv Line: 35
Info (16884): Verilog HDL info at cci_mpf_shim_vtp.vh(34): analyzing included file /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_shim_vtp.vh Line: 34
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_vtp.vh(34): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_shim_vtp.vh' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 34
Warning (16817): Verilog HDL warning at cci_mpf_shim_vtp.vh(219): overwriting previous
definition of cci_mpf_shim_vtp_svc_if interface File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 219
Info (18437): Verilog HDL info at cci_mpf_shim_vtp.vh(219): previous definition of
module cci_mpf_shim_vtp_svc_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/
hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 219
Warning (16817): Verilog HDL warning at cci_mpf_shim_vtp.vh(305): overwriting previous
definition of cci_mpf_shim_vtp_tlb_if interface File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 305
Info (18437): Verilog HDL info at cci_mpf_shim_vtp.vh(305): previous definition of
module cci_mpf_shim_vtp_tlb_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/
hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 305
Warning (16817): Verilog HDL warning at cci_mpf_shim_vtp.vh(374): overwriting previous
definition of cci_mpf_shim_vtp_pt_walk_if interface File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 374
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Info (18437): Verilog HDL info at cci_mpf_shim_vtp.vh(374): previous definition of
module cci_mpf_shim_vtp_pt_walk_if is here File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 374
Info (13230): Verilog HDL or VHDL information at cci_mpf_svc_vtp_pt_walk.sv(35): back
to file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_vtp/cci_mpf_svc_vtp_pt_walk.sv' File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_svc_vtp_pt_walk.sv Line: 35
Info (16884): Verilog HDL info at cci_mpf_svc_vtp_pt_walk.sv(36): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-prims/cci_mpf_prim_hash.vh
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_svc_vtp_pt_walk.sv Line: 36
Info (13230): Verilog HDL or VHDL information at cci_mpf_svc_vtp_pt_walk.sv(36): back
to file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_vtp/cci_mpf_svc_vtp_pt_walk.sv' File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_svc_vtp_pt_walk.sv Line: 36
Info (16884): Verilog HDL info at cci_mpf_svc_vtp_tlb.sv(32): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh File: /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_svc_vtp_tlb.sv Line: 32
Info (16884): Verilog HDL info at cci_mpf_if.vh(8): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if.vh(8): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Warning (16817): Verilog HDL warning at cci_mpf_if.vh(135): overwriting previous
definition of cci_mpf_if interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-if/cci_mpf_if.vh Line: 135
Info (18437): Verilog HDL info at cci_mpf_if.vh(135): previous definition of module
cci_mpf_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/
cci_mpf_if.vh Line: 135
Info (13230): Verilog HDL or VHDL information at cci_mpf_svc_vtp_tlb.sv(32): back to
file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_svc_vtp_tlb.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_vtp/cci_mpf_svc_vtp_tlb.sv Line: 32
Info (16884): Verilog HDL info at cci_mpf_svc_vtp_tlb.sv(33): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_svc_vtp_tlb.sv Line: 33
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Info (16884): Verilog HDL info at cci_mpf_csrs.vh(34): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-if/cci_csr_if.vh File: /home/u59497/
intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh Line: 34
Info (13230): Verilog HDL or VHDL information at cci_mpf_csrs.vh(34): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh' File: /home/u59497/
intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_csrs.vh Line: 34
Warning (16817): Verilog HDL warning at cci_mpf_csrs.vh(204): overwriting previous
definition of cci_mpf_csrs interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci_mpf_csrs.vh Line: 204
Info (18437): Verilog HDL info at cci_mpf_csrs.vh(204): previous definition of module
cci_mpf_csrs is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/
cci_mpf_csrs.vh Line: 204
Info (13230): Verilog HDL or VHDL information at cci_mpf_svc_vtp_tlb.sv(33): back to
file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_svc_vtp_tlb.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_vtp/cci_mpf_svc_vtp_tlb.sv Line: 33
Info (16884): Verilog HDL info at cci_mpf_svc_vtp_tlb.sv(35): analyzing included
file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_shim_vtp.vh File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_vtp/cci_mpf_svc_vtp_tlb.sv Line: 35
Info (16884): Verilog HDL info at cci_mpf_shim_vtp.vh(34): analyzing included file /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_shim_vtp.vh Line: 34
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_vtp.vh(34): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_shim_vtp.vh' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 34
Warning (16817): Verilog HDL warning at cci_mpf_shim_vtp.vh(219): overwriting previous
definition of cci_mpf_shim_vtp_svc_if interface File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 219
Info (18437): Verilog HDL info at cci_mpf_shim_vtp.vh(219): previous definition of
module cci_mpf_shim_vtp_svc_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/
hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 219
Warning (16817): Verilog HDL warning at cci_mpf_shim_vtp.vh(305): overwriting previous
definition of cci_mpf_shim_vtp_tlb_if interface File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 305
Info (18437): Verilog HDL info at cci_mpf_shim_vtp.vh(305): previous definition of
module cci_mpf_shim_vtp_tlb_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/
hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 305
Warning (16817): Verilog HDL warning at cci_mpf_shim_vtp.vh(374): overwriting previous
definition of cci_mpf_shim_vtp_pt_walk_if interface File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 374
Info (18437): Verilog HDL info at cci_mpf_shim_vtp.vh(374): previous definition of
module cci_mpf_shim_vtp_pt_walk_if is here File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_shim_vtp.vh Line: 374
Info (13230): Verilog HDL or VHDL information at cci_mpf_svc_vtp_tlb.sv(35): back to
file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/
cci_mpf_svc_vtp_tlb.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_vtp/cci_mpf_svc_vtp_tlb.sv Line: 35
Info (16884): Verilog HDL info at cci_mpf_shim_wro.sv(31): analyzing included file /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_wro/
cci_mpf_shim_wro.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_if.vh(8): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
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Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if.vh(8): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Warning (16817): Verilog HDL warning at cci_mpf_if.vh(135): overwriting previous
definition of cci_mpf_if interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-if/cci_mpf_if.vh Line: 135
Info (18437): Verilog HDL info at cci_mpf_if.vh(135): previous definition of module
cci_mpf_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/
cci_mpf_if.vh Line: 135
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_wro.sv(31): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_wro/
cci_mpf_shim_wro.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_wro/cci_mpf_shim_wro.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_shim_wro.sv(33): analyzing included file /
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci_mpf_config.vh File: /home/u59497/
intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_wro/cci_mpf_shim_wro.sv
Line: 33
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_wro.sv(33): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_wro/
cci_mpf_shim_wro.sv' File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_wro/cci_mpf_shim_wro.sv Line: 33
Info (16884): Verilog HDL info at cci_mpf_shim_wro_filter_group.sv(31): analyzing
included file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_wro/
cci_mpf_shim_wro_filter_group.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_if.vh(8): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
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Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if.vh(8): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Warning (16817): Verilog HDL warning at cci_mpf_if.vh(135): overwriting previous
definition of cci_mpf_if interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-if/cci_mpf_if.vh Line: 135
Info (18437): Verilog HDL info at cci_mpf_if.vh(135): previous definition of module
cci_mpf_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/
cci_mpf_if.vh Line: 135
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_wro_filter_group.sv(31):
back to file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_wro/cci_mpf_shim_wro_filter_group.sv' File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_wro/cci_mpf_shim_wro_filter_group.sv
Line: 31
Info (16884): Verilog HDL info at cci_mpf_shim_wro_filter_group.sv(32): analyzing
included file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_wro/cci_mpf_shim_wro.vh File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-shims/cci_mpf_shim_wro/cci_mpf_shim_wro_filter_group.sv Line: 32
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_wro_filter_group.sv(32):
back to file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_wro/cci_mpf_shim_wro_filter_group.sv' File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_wro/cci_mpf_shim_wro_filter_group.sv
Line: 32
Info (16884): Verilog HDL info at cci_mpf_shim_wro_filter_group.sv(33): analyzing
included file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-prims/
cci_mpf_prim_hash.vh File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_wro/cci_mpf_shim_wro_filter_group.sv Line: 33
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_wro_filter_group.sv(33):
back to file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_wro/cci_mpf_shim_wro_filter_group.sv' File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_wro/cci_mpf_shim_wro_filter_group.sv
Line: 33
Info (16884): Verilog HDL info at cci_mpf_shim_wro_epoch_order.sv(31): analyzing
included file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_wro/
cci_mpf_shim_wro_epoch_order.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_if.vh(8): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
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Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if.vh(8): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Warning (16817): Verilog HDL warning at cci_mpf_if.vh(135): overwriting previous
definition of cci_mpf_if interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-if/cci_mpf_if.vh Line: 135
Info (18437): Verilog HDL info at cci_mpf_if.vh(135): previous definition of module
cci_mpf_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/
cci_mpf_if.vh Line: 135
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_wro_epoch_order.sv(31):
back to file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_wro/cci_mpf_shim_wro_epoch_order.sv' File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_wro/cci_mpf_shim_wro_epoch_order.sv
Line: 31
Info (16884): Verilog HDL info at cci_mpf_shim_wro_epoch_order.sv(32): analyzing
included file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_wro/cci_mpf_shim_wro.vh File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-shims/cci_mpf_shim_wro/cci_mpf_shim_wro_epoch_order.sv Line: 32
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_wro_epoch_order.sv(32):
back to file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_wro/cci_mpf_shim_wro_epoch_order.sv' File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_wro/cci_mpf_shim_wro_epoch_order.sv
Line: 32
Info (16884): Verilog HDL info at cci_mpf_shim_wro_epoch_order.sv(33): analyzing
included file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-prims/
cci_mpf_prim_hash.vh File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
shims/cci_mpf_shim_wro/cci_mpf_shim_wro_epoch_order.sv Line: 33
Info (13230): Verilog HDL or VHDL information at cci_mpf_shim_wro_epoch_order.sv(33):
back to file '/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/
cci_mpf_shim_wro/cci_mpf_shim_wro_epoch_order.sv' File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_wro/cci_mpf_shim_wro_epoch_order.sv
Line: 33
Info (16884): Verilog HDL info at cci_dma.sv(23): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh File: /home/u59497/
acc-op/hw/cci_dma.sv Line: 23
Info (16884): Verilog HDL info at cci_mpf_if.vh(8): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
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Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if.vh(8): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Warning (16817): Verilog HDL warning at cci_mpf_if.vh(135): overwriting previous
definition of cci_mpf_if interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-if/cci_mpf_if.vh Line: 135
Info (18437): Verilog HDL info at cci_mpf_if.vh(135): previous definition of module
cci_mpf_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/
cci_mpf_if.vh Line: 135
Info (13230): Verilog HDL or VHDL information at cci_dma.sv(23): back to file '/home/
u59497/acc-op/hw/cci_dma.sv' File: /home/u59497/acc-op/hw/cci_dma.sv Line: 23
Info (16884): Verilog HDL info at afu.sv(69): analyzing included file /home/u59497/
intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh File: /home/u59497/acc-op/
hw/afu.sv Line: 69
Info (16884): Verilog HDL info at cci_mpf_if.vh(8): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if.vh(8): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Warning (16817): Verilog HDL warning at cci_mpf_if.vh(135): overwriting previous
definition of cci_mpf_if interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-if/cci_mpf_if.vh Line: 135
Info (18437): Verilog HDL info at cci_mpf_if.vh(135): previous definition of module
cci_mpf_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/
cci_mpf_if.vh Line: 135
Info (13230): Verilog HDL or VHDL information at afu.sv(69): back to file '/home/
u59497/acc-op/hw/afu.sv' File: /home/u59497/acc-op/hw/afu.sv Line: 69
```

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Info (16884): Verilog HDL info at csr_mgr.sv(31): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh File: /home/u59497/
acc-op/hw/csr_mgr.sv Line: 31
Info (16884): Verilog HDL info at cci_mpf_if.vh(8): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if.vh(8): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Warning (16817): Verilog HDL warning at cci_mpf_if.vh(135): overwriting previous
definition of cci_mpf_if interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-if/cci_mpf_if.vh Line: 135
Info (18437): Verilog HDL info at cci_mpf_if.vh(135): previous definition of module
cci_mpf_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/
cci_mpf_if.vh Line: 135
Info (13230): Verilog HDL or VHDL information at csr_mgr.sv(31): back to file '/home/
u59497/acc-op/hw/csr_mgr.sv' File: /home/u59497/acc-op/hw/csr_mgr.sv Line: 31
Info (16884): Verilog HDL info at csr_mgr.sv(32): analyzing included file /home/
u59497/acc-op/hw/cci_mpf_app_conf_default.vh File: /home/u59497/acc-op/hw/csr_mgr.sv
Line: 32
Info (16884): Verilog HDL info at cci_mpf_app_conf_default.vh(32): analyzing included
file /home/u59497/acc-op/hw/cci_mpf_app_conf.vh File: /home/u59497/acc-op/hw/
cci_mpf_app_conf_default.vh Line: 32
Info (13230): Verilog HDL or VHDL information at cci_mpf_app_conf_default.vh(32): back
to file '/home/u59497/acc-op/hw/cci_mpf_app_conf_default.vh' File: /home/u59497/acc-
op/hw/cci_mpf_app_conf_default.vh Line: 32
Info (13230): Verilog HDL or VHDL information at csr_mgr.sv(32): back to file '/home/
u59497/acc-op/hw/csr_mgr.sv' File: /home/u59497/acc-op/hw/csr_mgr.sv Line: 32
Info (16884): Verilog HDL info at csr_mgr.sv(33): analyzing included file /home/
u59497/acc-op/hw/csr_mgr.vh File: /home/u59497/acc-op/hw/csr_mgr.sv Line: 33
Info (16884): Verilog HDL info at csr_mgr.vh(34): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-if/cci_csr_if.vh File: /home/u59497/acc-
op/hw/csr_mgr.vh Line: 34
Info (13230): Verilog HDL or VHDL information at csr_mgr.vh(34): back to file '/home/
u59497/acc-op/hw/csr_mgr.vh' File: /home/u59497/acc-op/hw/csr_mgr.vh Line: 34
Info (13230): Verilog HDL or VHDL information at csr_mgr.sv(33): back to file '/home/
u59497/acc-op/hw/csr_mgr.sv' File: /home/u59497/acc-op/hw/csr_mgr.sv Line: 33
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Info (16884): Verilog HDL info at hal.sv(44): analyzing included file /home/u59497/
intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/u59497/
acc-op/hw/hal.sv Line: 44
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at hal.sv(44): back to file '/home/
u59497/acc-op/hw/hal.sv' File: /home/u59497/acc-op/hw/hal.sv Line: 44
Info (16884): Verilog HDL info at hal.sv(45): analyzing included file /home/u59497/
acc-op/hw/csr_mgr.vh File: /home/u59497/acc-op/hw/hal.sv Line: 45
Info (16884): Verilog HDL info at csr_mgr.vh(34): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-if/cci_csr_if.vh File: /home/u59497/acc-
op/hw/csr_mgr.vh Line: 34
Info (13230): Verilog HDL or VHDL information at csr_mgr.vh(34): back to file '/home/
u59497/acc-op/hw/csr_mgr.vh' File: /home/u59497/acc-op/hw/csr_mgr.vh Line: 34
Warning (16817): Verilog HDL warning at csr_mgr.vh(99): overwriting previous
definition of app_csrs interface File: /home/u59497/acc-op/hw/csr_mgr.vh Line: 99
Info (18437): Verilog HDL info at csr_mgr.vh(99): previous definition of module
app_csrs is here File: /home/u59497/acc-op/hw/csr_mgr.vh Line: 99
Info (13230): Verilog HDL or VHDL information at hal.sv(45): back to file '/home/
u59497/acc-op/hw/hal.sv' File: /home/u59497/acc-op/hw/hal.sv Line: 45
Info (16884): Verilog HDL info at ccip_std_afu.sv(45): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh File: /home/u59497/
acc-op/hw/ccip_std_afu.sv Line: 45
Info (16884): Verilog HDL info at cci_mpf_if.vh(8): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
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Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at cci_mpf_if.vh(8): back to file '/
home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if.vh Line: 8
Warning (16817): Verilog HDL warning at cci_mpf_if.vh(135): overwriting previous
definition of cci_mpf_if interface File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/
rtl/cci-mpf-if/cci_mpf_if.vh Line: 135
Info (18437): Verilog HDL info at cci_mpf_if.vh(135): previous definition of module
cci_mpf_if is here File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/
cci_mpf_if.vh Line: 135
Info (13230): Verilog HDL or VHDL information at ccip_std_afu.sv(45): back to file '/
home/u59497/acc-op/hw/ccip_std_afu.sv' File: /home/u59497/acc-op/hw/ccip_std_afu.sv
Line: 45
Info (16884): Verilog HDL info at ccip_std_afu.sv(46): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh File: /home/
u59497/acc-op/hw/ccip_std_afu.sv Line: 46
Info (13230): Verilog HDL or VHDL information at ccip_std_afu.sv(46): back to file '/
home/u59497/acc-op/hw/ccip_std_afu.sv' File: /home/u59497/acc-op/hw/ccip_std_afu.sv
Line: 46
Info (16884): Verilog HDL info at ccip_std_afu.sv(47): analyzing included file /home/
u59497/acc-op/hw/cci_mpf_app_conf_default.vh File: /home/u59497/acc-op/hw/
ccip_std_afu.sv Line: 47
Info (16884): Verilog HDL info at cci_mpf_app_conf_default.vh(32): analyzing included
file /home/u59497/acc-op/hw/cci_mpf_app_conf.vh File: /home/u59497/acc-op/hw/
cci_mpf_app_conf_default.vh Line: 32
Info (13230): Verilog HDL or VHDL information at cci_mpf_app_conf_default.vh(32): back
to file '/home/u59497/acc-op/hw/cci_mpf_app_conf_default.vh' File: /home/u59497/acc-
op/hw/cci_mpf_app_conf_default.vh Line: 32
Info (13230): Verilog HDL or VHDL information at ccip_std_afu.sv(47): back to file '/
home/u59497/acc-op/hw/ccip_std_afu.sv' File: /home/u59497/acc-op/hw/ccip_std_afu.sv
Line: 47
Info (16884): Verilog HDL info at ccip_std_afu.sv(48): analyzing included file /home/
u59497/acc-op/hw/csr_mgr.vh File: /home/u59497/acc-op/hw/ccip_std_afu.sv Line: 48
Info (16884): Verilog HDL info at csr_mgr.vh(34): analyzing included file /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-if/cci_csr_if.vh File: /home/u59497/acc-
op/hw/csr_mgr.vh Line: 34
Info (13230): Verilog HDL or VHDL information at csr_mgr.vh(34): back to file '/home/
u59497/acc-op/hw/csr_mgr.vh' File: /home/u59497/acc-op/hw/csr_mgr.vh Line: 34
Warning (16817): Verilog HDL warning at csr_mgr.vh(99): overwriting previous
definition of app_csrs interface File: /home/u59497/acc-op/hw/csr_mgr.vh Line: 99
Info (18437): Verilog HDL info at csr_mgr.vh(99): previous definition of module
app_csrs is here File: /home/u59497/acc-op/hw/csr_mgr.vh Line: 99
Info (13230): Verilog HDL or VHDL information at ccip_std_afu.sv(48): back to file '/
home/u59497/acc-op/hw/ccip_std_afu.sv' File: /home/u59497/acc-op/hw/ccip_std_afu.sv
Line: 48
Info (16884): Verilog HDL info at ccip_std_afu.sv(49): analyzing included file /home/
u59497/acc-op/hw/dma_if.vh File: /home/u59497/acc-op/hw/ccip_std_afu.sv Line: 49
Info (13230): Verilog HDL or VHDL information at ccip_std_afu.sv(49): back to file '/
home/u59497/acc-op/hw/ccip_std_afu.sv' File: /home/u59497/acc-op/hw/ccip_std_afu.sv
Line: 49
Info (16884): Verilog HDL info at ccip_std_afu.sv(50): analyzing included file /home/
u59497/acc-op/hw/mmio_if.vh File: /home/u59497/acc-op/hw/ccip_std_afu.sv Line: 50
Info (13230): Verilog HDL or VHDL information at ccip_std_afu.sv(50): back to file '/
home/u59497/acc-op/hw/ccip_std_afu.sv' File: /home/u59497/acc-op/hw/ccip_std_afu.sv
Line: 50
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Info (16884): Verilog HDL info at ccip_std_afu.sv(51): analyzing included file ../hw/
afu_json_info.vh File: /home/u59497/acc-op/hw/ccip_std_afu.sv Line: 51
Info (13230): Verilog HDL or VHDL information at ccip_std_afu.sv(51): back to file '/
home/u59497/acc-op/hw/ccip_std_afu.sv' File: /home/u59497/acc-op/hw/ccip_std_afu.sv
Line: 51
Warning (16818): Verilog HDL warning at mem_ctrl.sv(85): block identifier is required
on this block File: /home/u59497/acc-op/hw/mem_ctrl.sv Line: 85
Warning (16818): Verilog HDL warning at accelerators.sv(186): block identifier is
required on this block File: /home/u59497/acc-op/hw/accelerators.sv Line: 186
Warning (16818): Verilog HDL warning at csa.sv(12): block identifier is required on
this block File: /home/u59497/acc-op/hw/csa.sv Line: 12
Info (16884): Verilog HDL info at green_bs.sv(30): analyzing included file platform/
fpga_defines.vh File: /home/u59497/acc-op/hw/synth/build/platform/green_bs.sv Line: 30
Warning (13228): Verilog HDL or VHDL warning at fpga_defines.vh(70): ignoring re-
definition of command line macro 'INCLUDE_DDR4' File: /home/u59497/acc-op/hw/synth/
build/platform/fpga_defines.vh Line: 70
Info (13230): Verilog HDL or VHDL information at green_bs.sv(30): back to file
'platform/green_bs.sv' File: /home/u59497/acc-op/hw/synth/build/platform/green_bs.sv
Line: 30
Info (16884): Verilog HDL info at green_bs.sv(40): analyzing included file /usr/share/
opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/acc-op/hw/synth/build/
platform/green_bs.sv Line: 40
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at green_bs.sv(40): back to file
'platform/green_bs.sv' File: /home/u59497/acc-op/hw/synth/build/platform/green_bs.sv
Line: 40
Info (16884): Verilog HDL info at green_bs.sv(43): analyzing included file platform/
pr_hssi_if.vh File: /home/u59497/acc-op/hw/synth/build/platform/green_bs.sv Line: 43
Info (13230): Verilog HDL or VHDL information at green_bs.sv(43): back to file
'platform/green_bs.sv' File: /home/u59497/acc-op/hw/synth/build/platform/green_bs.sv
Line: 43
Warning (13228): Verilog HDL or VHDL warning at green_bs.sv(45): parameter declared
inside compilation unit '$unit_platform_green_bs_sv' shall be treated as localparam
File: /home/u59497/acc-op/hw/synth/build/platform/green_bs.sv Line: 45
Warning (13228): Verilog HDL or VHDL warning at green_bs.sv(46): parameter declared
inside compilation unit '$unit_platform_green_bs_sv' shall be treated as localparam
File: /home/u59497/acc-op/hw/synth/build/platform/green_bs.sv Line: 46
Warning (13228): Verilog HDL or VHDL warning at green_bs_resync.v(142): generate block
is allowed only inside loop and conditional generate in SystemVerilog mode File: /
home/u59497/acc-op/hw/synth/build/platform/lib/common/green_bs_resync.v Line: 142
Warning (13228): Verilog HDL or VHDL warning at fpga_defines.vh(70): ignoring re-
definition of command line macro 'INCLUDE_DDR4' File: /home/u59497/acc-op/hw/synth/
build/platform/fpga_defines.vh Line: 70
Info (16884): Verilog HDL info at cci_mpf_prim_ram_dualport_byteena.sv(43): analyzing
included file /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/
cci_mpf_platform.vh File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-
prims/cci_mpf_prim_ram_dualport_byteena.sv Line: 43
```

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Info (16884): Verilog HDL info at cci_mpf_platform.vh(39): analyzing included file /
usr/share/opae/platform/platform_if/rtl/platform_if.vh File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(39): analyzing included file ./
platform/platform_afu_top_config.vh File: /usr/share/opae/platform/platform_if/rtl/
platform_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(39): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 39
Info (16884): Verilog HDL info at platform_if.vh(41): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (16884): Verilog HDL info at device_if.vh(39): analyzing included file /usr/
share/opae/platform/platform_if/rtl/device_if/avalon_mem_if.vh File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at device_if.vh(39): back to file '/usr/
share/opae/platform/platform_if/rtl/device_if/device_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/device_if/device_if.vh Line: 39
Info (13230): Verilog HDL or VHDL information at platform_if.vh(41): back to file '/
usr/share/opae/platform/platform_if/rtl/platform_if.vh' File: /usr/share/opae/
platform/platform_if/rtl/platform_if.vh Line: 41
Info (13230): Verilog HDL or VHDL information at cci_mpf_platform.vh(39): back to file
'/home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh'
File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_platform.vh
Line: 39
Info (13230): Verilog HDL or VHDL information at
cci_mpf_prim_ram_dualport_byteena.sv(43): back to file '/home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-prims/cci_mpf_prim_ram_dualport_byteena.sv' File: /home/
u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-prims/
cci_mpf_prim_ram_dualport_byteena.sv Line: 43
Info: Elaborating from top-level entity "dcp_top"
Info (19272): Using dcp.qdb to replace the root partition.
Info (19534): Using dcp.qdb to replace the partition root_partition_2cedade0.
Warning (13469): Verilog HDL assignment warning at csr_mgr.sv(418): truncated value
with size 17 to match size of target (16) File: /home/u59497/acc-op/hw/csr_mgr.sv
Line: 418
Warning (13469): Verilog HDL assignment warning at csr_mgr.sv(426): truncated value
with size 17 to match size of target (16) File: /home/u59497/acc-op/hw/csr_mgr.sv
Line: 426
Warning (13469): Verilog HDL assignment warning at cci_mpf_prim_fifo_lutram.sv(250):
truncated value with size 5 to match size of target (4) File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-prims/cci_mpf_prim_fifo_lutram.sv Line: 250
Warning (13469): Verilog HDL assignment warning at cci_mpf_prim_fifo_lutram.sv(266):
truncated value with size 5 to match size of target (4) File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-prims/cci_mpf_prim_fifo_lutram.sv Line: 266
Warning (13469): Verilog HDL assignment warning at cci_mpf_shim_edge_fiu.sv(411):
truncated value with size 3 to match size of target (2) File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_edge/cci_mpf_shim_edge_fiu.sv Line:
411
Warning (13469): Verilog HDL assignment warning at cci_mpf_shim_edge_fiu.sv(412):
truncated value with size 32 to match size of target (2) File: /home/u59497/intel-
fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_edge/cci_mpf_shim_edge_fiu.sv
Line: 412
Warning (13469): Verilog HDL assignment warning at cci_mpf_shim_csr.sv(850): truncated
value with size 108 to match size of target (6) File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_csr.sv Line: 850
Warning (13469): Verilog HDL assignment warning at cci_mpf_shim_csr.sv(961): truncated
value with size 32 to match size of target (6) File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_csr.sv Line: 961
Warning (13469): Verilog HDL assignment warning at cci_mpf_prim_fifo_lutram.sv(250):
truncated value with size 7 to match size of target (6) File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-prims/cci_mpf_prim_fifo_lutram.sv Line: 250
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Warning (13469): Verilog HDL assignment warning at cci_mpf_prim_fifo_lutram.sv(266):
truncated value with size 7 to match size of target (6) File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-prims/cci_mpf_prim_fifo_lutram.sv Line: 266
Warning (13469): Verilog HDL assignment warning at cci_mpf_prim_fifo_lutram.sv(250):
truncated value with size 5 to match size of target (4) File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-prims/cci_mpf_prim_fifo_lutram.sv Line: 250
Warning (13469): Verilog HDL assignment warning at cci_mpf_prim_fifo_lutram.sv(266):
truncated value with size 5 to match size of target (4) File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-prims/cci_mpf_prim_fifo_lutram.sv Line: 266
Warning (13469): Verilog HDL assignment warning at cci_mpf_prim_fifo_lutram.sv(250):
truncated value with size 3 to match size of target (2) File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-prims/cci_mpf_prim_fifo_lutram.sv Line: 250
Warning (13469): Verilog HDL assignment warning at cci_mpf_prim_fifo_lutram.sv(266):
truncated value with size 3 to match size of target (2) File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-prims/cci_mpf_prim_fifo_lutram.sv Line: 266
Warning (13469): Verilog HDL assignment warning at cci_mpf_prim_fifo_lutram.sv(250):
truncated value with size 5 to match size of target (4) File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-prims/cci_mpf_prim_fifo_lutram.sv Line: 250
Warning (13469): Verilog HDL assignment warning at cci_mpf_prim_fifo_lutram.sv(266):
truncated value with size 5 to match size of target (4) File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-prims/cci_mpf_prim_fifo_lutram.sv Line: 266
Warning (13469): Verilog HDL assignment warning at cci_mpf_svc_vtp_tlb.sv(520):
truncated value with size 4 to match size of target (3) File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_svc_vtp_tlb.sv Line: 520
Warning (13469): Verilog HDL assignment warning at cci_mpf_svc_vtp_tlb.sv(520):
truncated value with size 4 to match size of target (3) File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_svc_vtp_tlb.sv Line: 520
Warning (13416): Verilog HDL warning at cci_mpf_svc_vtp_pt_walk.sv(495): ignoring
unsupported system task "fatal" File: /home/u59497/intel-fpga-bbb/BBB_cci_mpf/hw/rtl/
cci-mpf-shims/cci_mpf_shim_vtp/cci_mpf_svc_vtp_pt_walk.sv Line: 495
Warning (13469): Verilog HDL assignment warning at cci_mpf_prim_lutram.sv(448):
truncated value with size 10 to match size of target (9) File: /home/u59497/intel-
fpga-bbb/BBB_cci_mpf/hw/rtl/cci-mpf-prims/cci_mpf_prim_lutram.sv Line: 448
Warning (13469): Verilog HDL assignment warning at cci_mpf_prim_fifo_lutram.sv(250):
truncated value with size 6 to match size of target (5) File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-prims/cci_mpf_prim_fifo_lutram.sv Line: 250
Warning (13469): Verilog HDL assignment warning at cci_mpf_prim_fifo_lutram.sv(266):
truncated value with size 6 to match size of target (5) File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-prims/cci_mpf_prim_fifo_lutram.sv Line: 266
Warning (13469): Verilog HDL assignment warning at cci_mpf_prim_rob.sv(219): truncated
value with size 9 to match size of target (8) File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-prims/cci_mpf_prim_rob.sv Line: 219
Warning (13469): Verilog HDL assignment warning at cci_mpf_prim_lutram.sv(448):
truncated value with size 9 to match size of target (8) File: /home/u59497/intel-fpga-
bbb/BBB_cci_mpf/hw/rtl/cci-mpf-prims/cci_mpf_prim_lutram.sv Line: 448
Warning (13469): Verilog HDL assignment warning at cci_mpf_if_pkg.sv(371): truncated
value with size 148 to match size of target (77) File: /home/u59497/intel-fpga-bbb/
BBB_cci_mpf/hw/rtl/cci-mpf-if/cci_mpf_if_pkg.sv Line: 371
Warning (13469): Verilog HDL assignment warning at cpu_alu.sv(33): truncated value
with size 64 to match size of target (32) File: /home/u59497/acc-op/hw/cpu_alu.sv
Line: 33
Warning (13469): Verilog HDL assignment warning at cpu.sv(248): truncated value with
size 17 to match size of target (16) File: /home/u59497/acc-op/hw/cpu.sv Line: 248
Warning (13469): Verilog HDL assignment warning at cpu.sv(253): truncated value with
size 17 to match size of target (16) File: /home/u59497/acc-op/hw/cpu.sv Line: 253
Warning (13469): Verilog HDL assignment warning at cpu.sv(309): truncated value with
size 9 to match size of target (8) File: /home/u59497/acc-op/hw/cpu.sv Line: 309
Warning (13469): Verilog HDL assignment warning at cpu.sv(343): truncated value with
size 9 to match size of target (8) File: /home/u59497/acc-op/hw/cpu.sv Line: 343
Warning (13469): Verilog HDL assignment warning at cpu.sv(422): truncated value with
size 32 to match size of target (16) File: /home/u59497/acc-op/hw/cpu.sv Line: 422
Warning (13469): Verilog HDL assignment warning at cpu.sv(464): truncated value with
size 32 to match size of target (16) File: /home/u59497/acc-op/hw/cpu.sv Line: 464
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Warning (13469): Verilog HDL assignment warning at cpu.sv(476): truncated value with size 32 to match size of target (4) File: /home/u59497/acc-op/hw/cpu.sv Line: 476
Warning (13469): Verilog HDL assignment warning at cpu.sv(484): truncated value with size 32 to match size of target (4) File: /home/u59497/acc-op/hw/cpu.sv Line: 484
Warning (13469): Verilog HDL assignment warning at cpu.sv(487): truncated value with size 32 to match size of target (4) File: /home/u59497/acc-op/hw/cpu.sv Line: 487
Warning (13469): Verilog HDL assignment warning at cpu.sv(490): truncated value with size 32 to match size of target (4) File: /home/u59497/acc-op/hw/cpu.sv Line: 490
Warning (16788): Net "EXMEM_in[159]" does not have a driver at cpu.sv(168) File: /home/u59497/acc-op/hw/cpu.sv Line: 168
Warning (13469): Verilog HDL assignment warning at mem_ctrl.sv(197): truncated value with size 5 to match size of target (4) File: /home/u59497/acc-op/hw/mem_ctrl.sv Line: 197
Warning (13469): Verilog HDL assignment warning at mem_ctrl.sv(217): truncated value with size 2 to match size of target (1) File: /home/u59497/acc-op/hw/mem_ctrl.sv Line: 217
Warning (16735): Verilog HDL warning at accelerators.sv(148): actual bit length 16 differs from formal bit length 32 for port "mem_read_addr" File: /home/u59497/acc-op/hw/accelerators.sv Line: 148
Warning (16735): Verilog HDL warning at accelerators.sv(151): actual bit length 16 differs from formal bit length 32 for port "mem_write_addr" File: /home/u59497/acc-op/hw/accelerators.sv Line: 151
Warning (13469): Verilog HDL assignment warning at acc_control_unit.sv(471): truncated value with size 8 to match size of target (7) File: /home/u59497/acc-op/hw/acc_control_unit.sv Line: 471
Warning (13469): Verilog HDL assignment warning at acc_control_unit.sv(482): truncated value with size 3 to match size of target (2) File: /home/u59497/acc-op/hw/acc_control_unit.sv Line: 482
Warning (16735): Verilog HDL warning at accelerators.sv(177): actual bit length 32 differs from formal bit length 16 for port "mem_acc_read_addr" File: /home/u59497/acc-op/hw/accelerators.sv Line: 177
Warning (16735): Verilog HDL warning at accelerators.sv(180): actual bit length 32 differs from formal bit length 16 for port "mem_acc_write_addr" File: /home/u59497/acc-op/hw/accelerators.sv Line: 180
Warning (13469): Verilog HDL assignment warning at acc_control_unit.sv(471): truncated value with size 8 to match size of target (7) File: /home/u59497/acc-op/hw/acc_control_unit.sv Line: 471
Warning (13469): Verilog HDL assignment warning at acc_control_unit.sv(482): truncated value with size 3 to match size of target (2) File: /home/u59497/acc-op/hw/acc_control_unit.sv Line: 482
Warning (16735): Verilog HDL warning at accelerators.sv(177): actual bit length 32 differs from formal bit length 16 for port "mem_acc_read_addr" File: /home/u59497/acc-op/hw/accelerators.sv Line: 177
Warning (16735): Verilog HDL warning at accelerators.sv(180): actual bit length 32 differs from formal bit length 16 for port "mem_acc_write_addr" File: /home/u59497/acc-op/hw/accelerators.sv Line: 180
Warning (13469): Verilog HDL assignment warning at acc_control_unit.sv(471): truncated value with size 8 to match size of target (7) File: /home/u59497/acc-op/hw/acc_control_unit.sv Line: 471
Warning (13469): Verilog HDL assignment warning at acc_control_unit.sv(482): truncated value with size 3 to match size of target (2) File: /home/u59497/acc-op/hw/acc_control_unit.sv Line: 482
Warning (16735): Verilog HDL warning at accelerators.sv(177): actual bit length 32 differs from formal bit length 16 for port "mem_acc_read_addr" File: /home/u59497/acc-op/hw/accelerators.sv Line: 177
Warning (16735): Verilog HDL warning at accelerators.sv(180): actual bit length 32 differs from formal bit length 16 for port "mem_acc_write_addr" File: /home/u59497/acc-op/hw/accelerators.sv Line: 180
Warning (13469): Verilog HDL assignment warning at acc_control_unit.sv(471): truncated value with size 8 to match size of target (7) File: /home/u59497/acc-op/hw/acc_control_unit.sv Line: 471
Warning (13469): Verilog HDL assignment warning at acc_control_unit.sv(482): truncated value with size 3 to match size of target (2) File: /home/u59497/acc-op/hw/acc_control_unit.sv Line: 482
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Warning (16735): Verilog HDL warning at accelerators.sv(177): actual bit length 32 
differs from formal bit length 16 for port "mem_acc_read_addr" File: /home/u59497/acc-
op/hw/accelerators.sv Line: 177
Warning (16735): Verilog HDL warning at accelerators.sv(180): actual bit length 32 
differs from formal bit length 16 for port "mem_acc_write_addr" File: /home/u59497/
acc-op/hw/accelerators.sv Line: 180
Warning (13469): Verilog HDL assignment warning at acc_control_unit.sv(471): truncated 
value with size 8 to match size of target (7) File: /home/u59497/acc-op/hw/
acc_control_unit.sv Line: 471
Warning (13469): Verilog HDL assignment warning at acc_control_unit.sv(482): truncated 
value with size 3 to match size of target (2) File: /home/u59497/acc-op/hw/
acc_control_unit.sv Line: 482
Warning (16735): Verilog HDL warning at accelerators.sv(177): actual bit length 32 
differs from formal bit length 16 for port "mem_acc_read_addr" File: /home/u59497/acc-
op/hw/accelerators.sv Line: 177
Warning (16735): Verilog HDL warning at accelerators.sv(180): actual bit length 32 
differs from formal bit length 16 for port "mem_acc_write_addr" File: /home/u59497/
acc-op/hw/accelerators.sv Line: 180
Warning (13469): Verilog HDL assignment warning at acc_control_unit.sv(471): truncated 
value with size 8 to match size of target (7) File: /home/u59497/acc-op/hw/
acc_control_unit.sv Line: 471
Warning (13469): Verilog HDL assignment warning at acc_control_unit.sv(482): truncated 
value with size 3 to match size of target (2) File: /home/u59497/acc-op/hw/
acc_control_unit.sv Line: 482
Warning (16735): Verilog HDL warning at accelerators.sv(177): actual bit length 32 
differs from formal bit length 16 for port "mem_acc_read_addr" File: /home/u59497/acc-
op/hw/accelerators.sv Line: 177
Warning (16735): Verilog HDL warning at accelerators.sv(180): actual bit length 32 
differs from formal bit length 16 for port "mem_acc_write_addr" File: /home/u59497/
acc-op/hw/accelerators.sv Line: 180
Warning (13469): Verilog HDL assignment warning at acc_control_unit.sv(471): truncated 
value with size 8 to match size of target (7) File: /home/u59497/acc-op/hw/
acc_control_unit.sv Line: 471
Warning (13469): Verilog HDL assignment warning at acc_control_unit.sv(482): truncated 
value with size 3 to match size of target (2) File: /home/u59497/acc-op/hw/
acc_control_unit.sv Line: 482
Warning (16735): Verilog HDL warning at accelerators.sv(177): actual bit length 32 
differs from formal bit length 16 for port "mem_acc_read_addr" File: /home/u59497/acc-
op/hw/accelerators.sv Line: 177
Warning (16735): Verilog HDL warning at accelerators.sv(180): actual bit length 32 
differs from formal bit length 16 for port "mem_acc_write_addr" File: /home/u59497/
acc-op/hw/accelerators.sv Line: 180
Warning (13469): Verilog HDL assignment warning at acc_control_unit.sv(471): truncated 
value with size 8 to match size of target (7) File: /home/u59497/acc-op/hw/
acc_control_unit.sv Line: 471
Warning (13469): Verilog HDL assignment warning at acc_control_unit.sv(482): truncated 
value with size 3 to match size of target (2) File: /home/u59497/acc-op/hw/
acc_control_unit.sv Line: 482
Warning (16735): Verilog HDL warning at accelerators.sv(177): actual bit length 32 
differs from formal bit length 16 for port "mem_acc_read_addr" File: /home/u59497/acc-
op/hw/accelerators.sv Line: 177
Warning (16735): Verilog HDL warning at accelerators.sv(180): actual bit length 32 
differs from formal bit length 16 for port "mem_acc_write_addr" File: /home/u59497/
acc-op/hw/accelerators.sv Line: 180
Warning (16788): Net "csrs.afu_id[127]" does not have a driver at ccip_std_afu.sv(150) 
File: /home/u59497/acc-op/hw/ccip_std_afu.sv Line: 150
Warning (287013): Variable or input pin "byteena_b" is defined but never used. File: /
home/u59497/acc-op/hw/synth/build/tmp-clearbox/afu_default/71792/altsyncram_d1b2.tdf 
Line: 33
Warning (287013): Variable or input pin "data_b" is defined but never used. File: /
home/u59497/acc-op/hw/synth/build/tmp-clearbox/afu_default/71792/altsyncram_d1b2.tdf 
Line: 36
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Warning (287013): Variable or input pin "wren_b" is defined but never used. File: /
home/u59497/acc-op/hw/synth/build/tmp-clearbox/afu_default/71792/altsyncram_d1b2.tdf
Line: 40
Warning (287013): Variable or input pin "rden_a" is defined but never used. File: /
home/u59497/acc-op/hw/synth/build/tmp-clearbox/afu_default/71792/altsyncram_clf1.tdf
Line: 35
Warning (287013): Variable or input pin "rden_a" is defined but never used. File: /
home/u59497/acc-op/hw/synth/build/tmp-clearbox/afu_default/71792/altsyncram_gof1.tdf
Line: 35
Warning (287013): Variable or input pin "rden_a" is defined but never used. File: /
home/u59497/acc-op/hw/synth/build/tmp-clearbox/afu_default/71792/altsyncram_hof1.tdf
Line: 35
Warning (287013): Variable or input pin "rden_a" is defined but never used. File: /
home/u59497/acc-op/hw/synth/build/tmp-clearbox/afu_default/71792/altsyncram_cof1.tdf
Line: 35
Warning (287013): Variable or input pin "rden_a" is defined but never used. File: /
home/u59497/acc-op/hw/synth/build/tmp-clearbox/afu_default/71792/altsyncram_0uf1.tdf
Line: 35
Warning (287013): Variable or input pin "rden_a" is defined but never used. File: /
home/u59497/acc-op/hw/synth/build/tmp-clearbox/afu_default/71792/altsyncram_elf1.tdf
Line: 35
Warning (287013): Variable or input pin "rden_a" is defined but never used. File: /
home/u59497/acc-op/hw/synth/build/tmp-clearbox/afu_default/71792/altsyncram_aof1.tdf
Line: 35
Warning (287013): Variable or input pin "rden_a" is defined but never used. File: /
home/u59497/acc-op/hw/synth/build/tmp-clearbox/afu_default/71792/altsyncram_grf1.tdf
Line: 35
Warning (287013): Variable or input pin "rden_a" is defined but never used. File: /
home/u59497/acc-op/hw/synth/build/tmp-clearbox/afu_default/71792/altsyncram_eof1.tdf
Line: 35
Info: Found 231 design entities
Info: There are 368 partitions after elaboration.
Info: Creating instance-specific data models and dissolving soft partitions
Info (18299): Expanding entity and wildcard assignments.
Info (18300): Expanded entity and wildcard assignments. Elapsed time: 00:00:02
Warning (14284): Synthesized away the following node(s):
    Warning (14285): Synthesized away the following RAM node(s):
        Warning (14320): Synthesized away node "fpga_top|inst_green_bs|
platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|rspOrder|wr_heap|mem|ram|data|
auto_generated|q_b[0]" File: /home/u59497/acc-op/hw/synth/build/tmp-clearbox/
afu_default/71792/altsyncram_aof1.tdf Line: 39
        Warning (14320): Synthesized away node "fpga_top|inst_green_bs|
platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|rspOrder|wr_heap|mem|ram|data|
auto_generated|q_b[1]" File: /home/u59497/acc-op/hw/synth/build/tmp-clearbox/
afu_default/71792/altsyncram_aof1.tdf Line: 69
        Warning (14320): Synthesized away node "fpga_top|inst_green_bs|
platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|rspOrder|wr_heap|mem|ram|data|
auto_generated|q_b[2]" File: /home/u59497/acc-op/hw/synth/build/tmp-clearbox/
afu_default/71792/altsyncram_aof1.tdf Line: 99
        Warning (14320): Synthesized away node "fpga_top|inst_green_bs|
platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|rspOrder|wr_heap|mem|ram|data|
auto_generated|q_b[3]" File: /home/u59497/acc-op/hw/synth/build/tmp-clearbox/
afu_default/71792/altsyncram_aof1.tdf Line: 129
        Warning (14320): Synthesized away node "fpga_top|inst_green_bs|
platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|rspOrder|wr_heap|mem|ram|data|
auto_generated|q_b[4]" File: /home/u59497/acc-op/hw/synth/build/tmp-clearbox/
afu_default/71792/altsyncram_aof1.tdf Line: 159
        Warning (14320): Synthesized away node "fpga_top|inst_green_bs|
platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|rspOrder|wr_heap|mem|ram|data|
auto_generated|q_b[5]" File: /home/u59497/acc-op/hw/synth/build/tmp-clearbox/
afu_default/71792/altsyncram_aof1.tdf Line: 189
        Warning (14320): Synthesized away node "fpga_top|inst_green_bs|
platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|rspOrder|wr_heap|mem|ram|data|
```

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auto_generated|q_b[6]" File: /home/u59497/acc-op/hw/synth/build/tmp-clearbox/
afu_default/71792/altsyncram_aof1.tdf Line: 219
        Warning (14320): Synthesized away node "fpga_top|inst_green_bs|
platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|rspOrder|wr_heap|mem|ram|data|
auto_generated|q_b[7]" File: /home/u59497/acc-op/hw/synth/build/tmp-clearbox/
afu_default/71792/altsyncram_aof1.tdf Line: 249
        Warning (14320): Synthesized away node "fpga_top|inst_green_bs|
platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|rspOrder|wr_heap|mem|ram|data|
auto_generated|q_b[8]" File: /home/u59497/acc-op/hw/synth/build/tmp-clearbox/
afu_default/71792/altsyncram_aof1.tdf Line: 279
        Warning (14320): Synthesized away node "fpga_top|inst_green_bs|
platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|rspOrder|wr_heap|mem|ram|data|
auto_generated|q_b[9]" File: /home/u59497/acc-op/hw/synth/build/tmp-clearbox/
afu_default/71792/altsyncram_aof1.tdf Line: 309
        Warning (14320): Synthesized away node "fpga_top|inst_green_bs|
platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|rspOrder|wr_heap|mem|ram|data|
auto_generated|q_b[10]" File: /home/u59497/acc-op/hw/synth/build/tmp-clearbox/
afu_default/71792/altsyncram_aof1.tdf Line: 339
        Warning (14320): Synthesized away node "fpga_top|inst_green_bs|
platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|rspOrder|wr_heap|mem|ram|data|
auto_generated|q_b[11]" File: /home/u59497/acc-op/hw/synth/build/tmp-clearbox/
afu_default/71792/altsyncram_aof1.tdf Line: 369
        Warning (14320): Synthesized away node "fpga_top|inst_green_bs|
platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|rspOrder|wr_heap|mem|ram|data|
auto_generated|q_b[12]" File: /home/u59497/acc-op/hw/synth/build/tmp-clearbox/
afu_default/71792/altsyncram_aof1.tdf Line: 399
        Warning (14320): Synthesized away node "fpga_top|inst_green_bs|
platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|rspOrder|wr_heap|mem|ram|data|
auto_generated|q_b[13]" File: /home/u59497/acc-op/hw/synth/build/tmp-clearbox/
afu_default/71792/altsyncram_aof1.tdf Line: 429
        Warning (14320): Synthesized away node "fpga_top|inst_green_bs|
platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|rspOrder|wr_heap|mem|ram|data|
auto_generated|q_b[14]" File: /home/u59497/acc-op/hw/synth/build/tmp-clearbox/
afu_default/71792/altsyncram_aof1.tdf Line: 459
        Warning (14320): Synthesized away node "fpga_top|inst_green_bs|
platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|rspOrder|wr_heap|mem|ram|data|
auto_generated|q_b[15]" File: /home/u59497/acc-op/hw/synth/build/tmp-clearbox/
afu_default/71792/altsyncram_aof1.tdf Line: 489
        Warning (14320): Synthesized away node "fpga_top|inst_green_bs|
platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|rspOrder|gen_rd_rob.rd_rob|
genMeta.memMeta|ram|data|auto_generated|q_b[9]" File: /home/u59497/acc-op/hw/synth/
build/tmp-clearbox/afu_default/71792/altsyncram_eof1.tdf Line: 309
        Warning (14320): Synthesized away node "fpga_top|inst_green_bs|
platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|rspOrder|gen_rd_rob.rd_rob|
genMeta.memMeta|ram|data|auto_generated|q_b[10]" File: /home/u59497/acc-op/hw/synth/
build/tmp-clearbox/afu_default/71792/altsyncram_eof1.tdf Line: 339
        Warning (14320): Synthesized away node "fpga_top|inst_green_bs|
platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|rspOrder|gen_rd_rob.rd_rob|
genMeta.memMeta|ram|data|auto_generated|q_b[11]" File: /home/u59497/acc-op/hw/synth/
build/tmp-clearbox/afu_default/71792/altsyncram_eof1.tdf Line: 369
Critical Warning (20580): Imported Partition 'green_region' has type
'PARTIAL_RECONFIGURATION_PARTITION' but it is not specified in the current project.
Info: found pre-synthesis snapshots for 3 partition(s)
Info: Synthesizing partition "root_partition"
Info: Successfully synthesized partition
Info: Synthesizing partition "root_partition_2cedade0"
Info: Successfully synthesized partition
Info: Synthesizing partition "green_region"
```

```
Warning (276020): Inferred RAM node "fpga_top|inst_green_bs|
platform_shim_ccip_std_afu|ccip_std_afu|hal|dma_ctrl|rd_fifo|mem_rtl_0" from
synchronous design logic.  Pass-through logic has been added to match the read-during-
write behavior of the original design.
Info (19000): Inferred 29 megafunctions from design logic
    Info (276038): Inferred altdpram megafunction from the following logic: "fpga_top|
inst_green_bs|platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_edge_fiu|b|c0_fifo|fifo|
data|data_rtl_0"
        Info (286033): Parameter WIDTH set to 51
        Info (286033): Parameter WIDTHAD set to 4
        Info (286033): Parameter NUMWORDS set to 16
        Info (286033): Parameter WRADDRESS_REG set to INCLOCK
        Info (286033): Parameter WRADDRESS_ACLR set to OFF
        Info (286033): Parameter WRCONTROL_REG set to INCLOCK
        Info (286033): Parameter WRCONTROL_ACLR set to OFF
        Info (286033): Parameter RDADDRESS_REG set to OUTCLOCK
        Info (286033): Parameter RDADDRESS_ACLR set to OFF
        Info (286033): Parameter RDCONTROL_REG set to UNREGISTERED
        Info (286033): Parameter RDCONTROL_ACLR set to OFF
        Info (286033): Parameter INDATA_REG set to INCLOCK
        Info (286033): Parameter INDATA_ACLR set to OFF
        Info (286033): Parameter OUTDATA_REG set to UNREGISTERED
        Info (286033): Parameter OUTDATA_ACLR set to OFF
        Info (286033): Parameter LPM_FILE set to UNUSED
        Info (286033): Parameter RAM_BLOCK_TYPE set to LUTRAM
    Info (276038): Inferred altdpram megafunction from the following logic: "fpga_top|
inst_green_bs|platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_edge_fiu|b|c1_fifo|fifo|
data|data_rtl_0"
        Info (286033): Parameter WIDTH set to 58
        Info (286033): Parameter WIDTHAD set to 4
        Info (286033): Parameter NUMWORDS set to 16
        Info (286033): Parameter WRADDRESS_REG set to INCLOCK
        Info (286033): Parameter WRADDRESS_ACLR set to OFF
        Info (286033): Parameter WRCONTROL_REG set to INCLOCK
        Info (286033): Parameter WRCONTROL_ACLR set to OFF
        Info (286033): Parameter RDADDRESS_REG set to OUTCLOCK
        Info (286033): Parameter RDADDRESS_ACLR set to OFF
        Info (286033): Parameter RDCONTROL_REG set to UNREGISTERED
        Info (286033): Parameter RDCONTROL_ACLR set to OFF
        Info (286033): Parameter INDATA_REG set to INCLOCK
        Info (286033): Parameter INDATA_ACLR set to OFF
        Info (286033): Parameter OUTDATA_REG set to UNREGISTERED
        Info (286033): Parameter OUTDATA_ACLR set to OFF
        Info (286033): Parameter LPM_FILE set to UNUSED
        Info (286033): Parameter RAM_BLOCK_TYPE set to LUTRAM
    Info (276038): Inferred altdpram megafunction from the following logic: "fpga_top|
inst_green_bs|platform_shim_ccip_std_afu|ccip_std_afu|mpf|csr|req_fifo|fifo|data|
data_rtl_0"
        Info (286033): Parameter WIDTH set to 15
        Info (286033): Parameter WIDTHAD set to 6
        Info (286033): Parameter NUMWORDS set to 64
        Info (286033): Parameter WRADDRESS_REG set to INCLOCK
        Info (286033): Parameter WRADDRESS_ACLR set to OFF
        Info (286033): Parameter WRCONTROL_REG set to INCLOCK
        Info (286033): Parameter WRCONTROL_ACLR set to OFF
        Info (286033): Parameter RDADDRESS_REG set to OUTCLOCK
        Info (286033): Parameter RDADDRESS_ACLR set to OFF
        Info (286033): Parameter RDCONTROL_REG set to UNREGISTERED
        Info (286033): Parameter RDCONTROL_ACLR set to OFF
        Info (286033): Parameter INDATA_REG set to INCLOCK
        Info (286033): Parameter INDATA_ACLR set to OFF
        Info (286033): Parameter OUTDATA_REG set to UNREGISTERED
        Info (286033): Parameter OUTDATA_ACLR set to OFF
```

```
        Info (286033): Parameter LPM_FILE set to UNUSED
        Info (286033): Parameter RAM_BLOCK_TYPE set to LUTRAM
    Info (276038): Inferred altdpram megafunction from the following logic: "fpga_top|
inst_green_bs|platform_shim_ccip_std_afu|ccip_std_afu|mpf|v_to_p.vtp|inp[0].in_fifo|
fifo|data|data_rtl_0"
        Info (286033): Parameter WIDTH set to 40
        Info (286033): Parameter WIDTHAD set to 4
        Info (286033): Parameter NUMWORDS set to 16
        Info (286033): Parameter WRADDRESS_REG set to INCLOCK
        Info (286033): Parameter WRADDRESS_ACLR set to OFF
        Info (286033): Parameter WRCONTROL_REG set to INCLOCK
        Info (286033): Parameter WRCONTROL_ACLR set to OFF
        Info (286033): Parameter RDADDRESS_REG set to OUTCLOCK
        Info (286033): Parameter RDADDRESS_ACLR set to OFF
        Info (286033): Parameter RDCONTROL_REG set to UNREGISTERED
        Info (286033): Parameter RDCONTROL_ACLR set to OFF
        Info (286033): Parameter INDATA_REG set to INCLOCK
        Info (286033): Parameter INDATA_ACLR set to OFF
        Info (286033): Parameter OUTDATA_REG set to UNREGISTERED
        Info (286033): Parameter OUTDATA_ACLR set to OFF
        Info (286033): Parameter LPM_FILE set to UNUSED
        Info (286033): Parameter RAM_BLOCK_TYPE set to LUTRAM
    Info (276038): Inferred altdpram megafunction from the following logic: "fpga_top|
inst_green_bs|platform_shim_ccip_std_afu|ccip_std_afu|mpf|v_to_p.vtp|inp[1].in_fifo|
fifo|data|data_rtl_0"
        Info (286033): Parameter WIDTH set to 40
        Info (286033): Parameter WIDTHAD set to 4
        Info (286033): Parameter NUMWORDS set to 16
        Info (286033): Parameter WRADDRESS_REG set to INCLOCK
        Info (286033): Parameter WRADDRESS_ACLR set to OFF
        Info (286033): Parameter WRCONTROL_REG set to INCLOCK
        Info (286033): Parameter WRCONTROL_ACLR set to OFF
        Info (286033): Parameter RDADDRESS_REG set to OUTCLOCK
        Info (286033): Parameter RDADDRESS_ACLR set to OFF
        Info (286033): Parameter RDCONTROL_REG set to UNREGISTERED
        Info (286033): Parameter RDCONTROL_ACLR set to OFF
        Info (286033): Parameter INDATA_REG set to INCLOCK
        Info (286033): Parameter INDATA_ACLR set to OFF
        Info (286033): Parameter OUTDATA_REG set to UNREGISTERED
        Info (286033): Parameter OUTDATA_ACLR set to OFF
        Info (286033): Parameter LPM_FILE set to UNUSED
        Info (286033): Parameter RAM_BLOCK_TYPE set to LUTRAM
    Info (276038): Inferred altdpram megafunction from the following logic: "fpga_top|
inst_green_bs|platform_shim_ccip_std_afu|ccip_std_afu|mpf|v_to_p.vtp|merged_fifo|fifo|
data|data_rtl_0"
        Info (286033): Parameter WIDTH set to 41
        Info (286033): Parameter WIDTHAD set to 2
        Info (286033): Parameter NUMWORDS set to 4
        Info (286033): Parameter WRADDRESS_REG set to INCLOCK
        Info (286033): Parameter WRADDRESS_ACLR set to OFF
        Info (286033): Parameter WRCONTROL_REG set to INCLOCK
        Info (286033): Parameter WRCONTROL_ACLR set to OFF
        Info (286033): Parameter RDADDRESS_REG set to OUTCLOCK
        Info (286033): Parameter RDADDRESS_ACLR set to OFF
        Info (286033): Parameter RDCONTROL_REG set to UNREGISTERED
        Info (286033): Parameter RDCONTROL_ACLR set to OFF
        Info (286033): Parameter INDATA_REG set to INCLOCK
        Info (286033): Parameter INDATA_ACLR set to OFF
        Info (286033): Parameter OUTDATA_REG set to UNREGISTERED
        Info (286033): Parameter OUTDATA_ACLR set to OFF
        Info (286033): Parameter LPM_FILE set to UNUSED
        Info (286033): Parameter RAM_BLOCK_TYPE set to LUTRAM
```

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    Info (276038): Inferred altdpram megafunction from the following logic: "fpga_top|
inst_green_bs|platform_shim_ccip_std_afu|ccip_std_afu|mpf|v_to_p.vtp|pipe|active_reqs|
fifo|data|data_rtl_0"
        Info (286033): Parameter WIDTH set to 41
        Info (286033): Parameter WIDTHAD set to 4
        Info (286033): Parameter NUMWORDS set to 16
        Info (286033): Parameter WRADDRESS_REG set to INCLOCK
        Info (286033): Parameter WRADDRESS_ACLR set to OFF
        Info (286033): Parameter WRCONTROL_REG set to INCLOCK
        Info (286033): Parameter WRCONTROL_ACLR set to OFF
        Info (286033): Parameter RDADDRESS_REG set to OUTCLOCK
        Info (286033): Parameter RDADDRESS_ACLR set to OFF
        Info (286033): Parameter RDCONTROL_REG set to UNREGISTERED
        Info (286033): Parameter RDCONTROL_ACLR set to OFF
        Info (286033): Parameter INDATA_REG set to INCLOCK
        Info (286033): Parameter INDATA_ACLR set to OFF
        Info (286033): Parameter OUTDATA_REG set to UNREGISTERED
        Info (286033): Parameter OUTDATA_ACLR set to OFF
        Info (286033): Parameter LPM_FILE set to UNUSED
        Info (286033): Parameter RAM_BLOCK_TYPE set to LUTRAM
    Info (276038): Inferred altdpram megafunction from the following logic: "fpga_top|
inst_green_bs|platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|eop|c0_tracker|
flit_cnt|ram|m[0].ram|data_rtl_0"
        Info (286033): Parameter WIDTH set to 2
        Info (286033): Parameter WIDTHAD set to 8
        Info (286033): Parameter NUMWORDS set to 256
        Info (286033): Parameter WRADDRESS_REG set to INCLOCK
        Info (286033): Parameter WRADDRESS_ACLR set to OFF
        Info (286033): Parameter WRCONTROL_REG set to INCLOCK
        Info (286033): Parameter WRCONTROL_ACLR set to OFF
        Info (286033): Parameter RDADDRESS_REG set to UNREGISTERED
        Info (286033): Parameter RDADDRESS_ACLR set to OFF
        Info (286033): Parameter RDCONTROL_REG set to UNREGISTERED
        Info (286033): Parameter RDCONTROL_ACLR set to OFF
        Info (286033): Parameter INDATA_REG set to INCLOCK
        Info (286033): Parameter INDATA_ACLR set to OFF
        Info (286033): Parameter OUTDATA_REG set to UNREGISTERED
        Info (286033): Parameter OUTDATA_ACLR set to OFF
        Info (286033): Parameter LPM_FILE set to UNUSED
        Info (286033): Parameter RAM_BLOCK_TYPE set to LUTRAM
    Info (276038): Inferred altdpram megafunction from the following logic: "fpga_top|
inst_green_bs|platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|eop|c0_tracker|
flit_cnt|ram|m[1].ram|data_rtl_0"
        Info (286033): Parameter WIDTH set to 2
        Info (286033): Parameter WIDTHAD set to 8
        Info (286033): Parameter NUMWORDS set to 256
        Info (286033): Parameter WRADDRESS_REG set to INCLOCK
        Info (286033): Parameter WRADDRESS_ACLR set to OFF
        Info (286033): Parameter WRCONTROL_REG set to INCLOCK
        Info (286033): Parameter WRCONTROL_ACLR set to OFF
        Info (286033): Parameter RDADDRESS_REG set to UNREGISTERED
        Info (286033): Parameter RDADDRESS_ACLR set to OFF
        Info (286033): Parameter RDCONTROL_REG set to UNREGISTERED
        Info (286033): Parameter RDCONTROL_ACLR set to OFF
        Info (286033): Parameter INDATA_REG set to INCLOCK
        Info (286033): Parameter INDATA_ACLR set to OFF
        Info (286033): Parameter OUTDATA_REG set to UNREGISTERED
        Info (286033): Parameter OUTDATA_ACLR set to OFF
        Info (286033): Parameter LPM_FILE set to UNUSED
        Info (286033): Parameter RAM_BLOCK_TYPE set to LUTRAM
    Info (276038): Inferred altdpram megafunction from the following logic: "fpga_top|
inst_green_bs|platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|eop|c1_tracker|
flit_cnt|ram|m[0].ram|data_rtl_0"
        Info (286033): Parameter WIDTH set to 2
```

```
        Info (286033): Parameter WIDTHAD set to 8
        Info (286033): Parameter NUMWORDS set to 256
        Info (286033): Parameter WRADDRESS_REG set to INCLOCK
        Info (286033): Parameter WRADDRESS_ACLR set to OFF
        Info (286033): Parameter WRCONTROL_REG set to INCLOCK
        Info (286033): Parameter WRCONTROL_ACLR set to OFF
        Info (286033): Parameter RDADDRESS_REG set to OUTCLOCK
        Info (286033): Parameter RDADDRESS_ACLR set to OFF
        Info (286033): Parameter RDCONTROL_REG set to UNREGISTERED
        Info (286033): Parameter RDCONTROL_ACLR set to OFF
        Info (286033): Parameter INDATA_REG set to INCLOCK
        Info (286033): Parameter INDATA_ACLR set to OFF
        Info (286033): Parameter OUTDATA_REG set to UNREGISTERED
        Info (286033): Parameter OUTDATA_ACLR set to OFF
        Info (286033): Parameter LPM_FILE set to UNUSED
        Info (286033): Parameter RAM_BLOCK_TYPE set to LUTRAM
    Info (276038): Inferred altdpram megafunction from the following logic: "fpga_top|
inst_green_bs|platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|eop|c1_tracker|
flit_cnt|ram|m[1].ram|data_rtl_0"
        Info (286033): Parameter WIDTH set to 2
        Info (286033): Parameter WIDTHAD set to 8
        Info (286033): Parameter NUMWORDS set to 256
        Info (286033): Parameter WRADDRESS_REG set to INCLOCK
        Info (286033): Parameter WRADDRESS_ACLR set to OFF
        Info (286033): Parameter WRCONTROL_REG set to INCLOCK
        Info (286033): Parameter WRCONTROL_ACLR set to OFF
        Info (286033): Parameter RDADDRESS_REG set to OUTCLOCK
        Info (286033): Parameter RDADDRESS_ACLR set to OFF
        Info (286033): Parameter RDCONTROL_REG set to UNREGISTERED
        Info (286033): Parameter RDCONTROL_ACLR set to OFF
        Info (286033): Parameter INDATA_REG set to INCLOCK
        Info (286033): Parameter INDATA_ACLR set to OFF
        Info (286033): Parameter OUTDATA_REG set to UNREGISTERED
        Info (286033): Parameter OUTDATA_ACLR set to OFF
        Info (286033): Parameter LPM_FILE set to UNUSED
        Info (286033): Parameter RAM_BLOCK_TYPE set to LUTRAM
    Info (276038): Inferred altdpram megafunction from the following logic: "fpga_top|
inst_green_bs|platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|vtp.v_to_p|c0_vtp|
l1tlb|fifo|fifo|data|data_rtl_0"
        Info (286033): Parameter WIDTH set to 92
        Info (286033): Parameter WIDTHAD set to 5
        Info (286033): Parameter NUMWORDS set to 19
        Info (286033): Parameter WRADDRESS_REG set to INCLOCK
        Info (286033): Parameter WRADDRESS_ACLR set to OFF
        Info (286033): Parameter WRCONTROL_REG set to INCLOCK
        Info (286033): Parameter WRCONTROL_ACLR set to OFF
        Info (286033): Parameter RDADDRESS_REG set to OUTCLOCK
        Info (286033): Parameter RDADDRESS_ACLR set to OFF
        Info (286033): Parameter RDCONTROL_REG set to UNREGISTERED
        Info (286033): Parameter RDCONTROL_ACLR set to OFF
        Info (286033): Parameter INDATA_REG set to INCLOCK
        Info (286033): Parameter INDATA_ACLR set to OFF
        Info (286033): Parameter OUTDATA_REG set to UNREGISTERED
        Info (286033): Parameter OUTDATA_ACLR set to OFF
        Info (286033): Parameter LPM_FILE set to UNUSED
        Info (286033): Parameter RAM_BLOCK_TYPE set to LUTRAM
    Info (276038): Inferred altdpram megafunction from the following logic: "fpga_top|
inst_green_bs|platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|vtp.v_to_p|c0_vtp|
l2tlb|heap_ctrl|lr.fl|freeList|data_rtl_0"
        Info (286033): Parameter WIDTH set to 4
        Info (286033): Parameter WIDTHAD set to 4
        Info (286033): Parameter NUMWORDS set to 16
        Info (286033): Parameter WRADDRESS_REG set to INCLOCK
        Info (286033): Parameter WRADDRESS_ACLR set to OFF
```

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        Info (286033): Parameter WRCONTROL_REG set to INCLOCK
        Info (286033): Parameter WRCONTROL_ACLR set to OFF
        Info (286033): Parameter RDADDRESS_REG set to OUTCLOCK
        Info (286033): Parameter RDADDRESS_ACLR set to OFF
        Info (286033): Parameter RDCONTROL_REG set to UNREGISTERED
        Info (286033): Parameter RDCONTROL_ACLR set to OFF
        Info (286033): Parameter INDATA_REG set to INCLOCK
        Info (286033): Parameter INDATA_ACLR set to OFF
        Info (286033): Parameter OUTDATA_REG set to UNREGISTERED
        Info (286033): Parameter OUTDATA_ACLR set to OFF
        Info (286033): Parameter LPM_FILE set to UNUSED
        Info (286033): Parameter RAM_BLOCK_TYPE set to LUTRAM
    Info (276038): Inferred altdpram megafunction from the following logic: "fpga_top|
inst_green_bs|platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|vtp.v_to_p|c0_vtp|
l2tlb|heap_ctx|data_rtl_0"
        Info (286033): Parameter WIDTH set to 53
        Info (286033): Parameter WIDTHAD set to 4
        Info (286033): Parameter NUMWORDS set to 16
        Info (286033): Parameter WRADDRESS_REG set to INCLOCK
        Info (286033): Parameter WRADDRESS_ACLR set to OFF
        Info (286033): Parameter WRCONTROL_REG set to INCLOCK
        Info (286033): Parameter WRCONTROL_ACLR set to OFF
        Info (286033): Parameter RDADDRESS_REG set to OUTCLOCK
        Info (286033): Parameter RDADDRESS_ACLR set to OFF
        Info (286033): Parameter RDCONTROL_REG set to UNREGISTERED
        Info (286033): Parameter RDCONTROL_ACLR set to OFF
        Info (286033): Parameter INDATA_REG set to INCLOCK
        Info (286033): Parameter INDATA_ACLR set to OFF
        Info (286033): Parameter OUTDATA_REG set to UNREGISTERED
        Info (286033): Parameter OUTDATA_ACLR set to OFF
        Info (286033): Parameter LPM_FILE set to UNUSED
        Info (286033): Parameter RAM_BLOCK_TYPE set to LUTRAM
    Info (276038): Inferred altdpram megafunction from the following logic: "fpga_top|
inst_green_bs|platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|vtp.v_to_p|c0_vtp|
l2tlb|tlb_fifo_out|fifo|data|data_rtl_0"
        Info (286033): Parameter WIDTH set to 41
        Info (286033): Parameter WIDTHAD set to 4
        Info (286033): Parameter NUMWORDS set to 16
        Info (286033): Parameter WRADDRESS_REG set to INCLOCK
        Info (286033): Parameter WRADDRESS_ACLR set to OFF
        Info (286033): Parameter WRCONTROL_REG set to INCLOCK
        Info (286033): Parameter WRCONTROL_ACLR set to OFF
        Info (286033): Parameter RDADDRESS_REG set to OUTCLOCK
        Info (286033): Parameter RDADDRESS_ACLR set to OFF
        Info (286033): Parameter RDCONTROL_REG set to UNREGISTERED
        Info (286033): Parameter RDCONTROL_ACLR set to OFF
        Info (286033): Parameter INDATA_REG set to INCLOCK
        Info (286033): Parameter INDATA_ACLR set to OFF
        Info (286033): Parameter OUTDATA_REG set to UNREGISTERED
        Info (286033): Parameter OUTDATA_ACLR set to OFF
        Info (286033): Parameter LPM_FILE set to UNUSED
        Info (286033): Parameter RAM_BLOCK_TYPE set to LUTRAM
    Info (276038): Inferred altdpram megafunction from the following logic: "fpga_top|
inst_green_bs|platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|vtp.v_to_p|c1_vtp|
l1tlb|fifo|fifo|data|data_rtl_0"
        Info (286033): Parameter WIDTH set to 99
        Info (286033): Parameter WIDTHAD set to 5
        Info (286033): Parameter NUMWORDS set to 19
        Info (286033): Parameter WRADDRESS_REG set to INCLOCK
        Info (286033): Parameter WRADDRESS_ACLR set to OFF
        Info (286033): Parameter WRCONTROL_REG set to INCLOCK
        Info (286033): Parameter WRCONTROL_ACLR set to OFF
        Info (286033): Parameter RDADDRESS_REG set to OUTCLOCK
        Info (286033): Parameter RDADDRESS_ACLR set to OFF
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        Info (286033): Parameter RDCONTROL_REG set to UNREGISTERED
        Info (286033): Parameter RDCONTROL_ACLR set to OFF
        Info (286033): Parameter INDATA_REG set to INCLOCK
        Info (286033): Parameter INDATA_ACLR set to OFF
        Info (286033): Parameter OUTDATA_REG set to UNREGISTERED
        Info (286033): Parameter OUTDATA_ACLR set to OFF
        Info (286033): Parameter LPM_FILE set to UNUSED
        Info (286033): Parameter RAM_BLOCK_TYPE set to LUTRAM
    Info (276038): Inferred altdpram megafunction from the following logic: "fpga_top|
inst_green_bs|platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|vtp.v_to_p|c1_vtp|
l2tlb|heap_ctrl|lr.fl|freeList|data_rtl_0"
        Info (286033): Parameter WIDTH set to 4
        Info (286033): Parameter WIDTHAD set to 4
        Info (286033): Parameter NUMWORDS set to 16
        Info (286033): Parameter WRADDRESS_REG set to INCLOCK
        Info (286033): Parameter WRADDRESS_ACLR set to OFF
        Info (286033): Parameter WRCONTROL_REG set to INCLOCK
        Info (286033): Parameter WRCONTROL_ACLR set to OFF
        Info (286033): Parameter RDADDRESS_REG set to OUTCLOCK
        Info (286033): Parameter RDADDRESS_ACLR set to OFF
        Info (286033): Parameter RDCONTROL_REG set to UNREGISTERED
        Info (286033): Parameter RDCONTROL_ACLR set to OFF
        Info (286033): Parameter INDATA_REG set to INCLOCK
        Info (286033): Parameter INDATA_ACLR set to OFF
        Info (286033): Parameter OUTDATA_REG set to UNREGISTERED
        Info (286033): Parameter OUTDATA_ACLR set to OFF
        Info (286033): Parameter LPM_FILE set to UNUSED
        Info (286033): Parameter RAM_BLOCK_TYPE set to LUTRAM
    Info (276038): Inferred altdpram megafunction from the following logic: "fpga_top|
inst_green_bs|platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|vtp.v_to_p|c1_vtp|
l2tlb|heap_ctx|data_rtl_0"
        Info (286033): Parameter WIDTH set to 60
        Info (286033): Parameter WIDTHAD set to 4
        Info (286033): Parameter NUMWORDS set to 16
        Info (286033): Parameter WRADDRESS_REG set to INCLOCK
        Info (286033): Parameter WRADDRESS_ACLR set to OFF
        Info (286033): Parameter WRCONTROL_REG set to INCLOCK
        Info (286033): Parameter WRCONTROL_ACLR set to OFF
        Info (286033): Parameter RDADDRESS_REG set to OUTCLOCK
        Info (286033): Parameter RDADDRESS_ACLR set to OFF
        Info (286033): Parameter RDCONTROL_REG set to UNREGISTERED
        Info (286033): Parameter RDCONTROL_ACLR set to OFF
        Info (286033): Parameter INDATA_REG set to INCLOCK
        Info (286033): Parameter INDATA_ACLR set to OFF
        Info (286033): Parameter OUTDATA_REG set to UNREGISTERED
        Info (286033): Parameter OUTDATA_ACLR set to OFF
        Info (286033): Parameter LPM_FILE set to UNUSED
        Info (286033): Parameter RAM_BLOCK_TYPE set to LUTRAM
    Info (276038): Inferred altdpram megafunction from the following logic: "fpga_top|
inst_green_bs|platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|vtp.v_to_p|c1_vtp|
l2tlb|tlb_fifo_out|fifo|data|data_rtl_0"
        Info (286033): Parameter WIDTH set to 41
        Info (286033): Parameter WIDTHAD set to 4
        Info (286033): Parameter NUMWORDS set to 16
        Info (286033): Parameter WRADDRESS_REG set to INCLOCK
        Info (286033): Parameter WRADDRESS_ACLR set to OFF
        Info (286033): Parameter WRCONTROL_REG set to INCLOCK
        Info (286033): Parameter WRCONTROL_ACLR set to OFF
        Info (286033): Parameter RDADDRESS_REG set to OUTCLOCK
        Info (286033): Parameter RDADDRESS_ACLR set to OFF
        Info (286033): Parameter RDCONTROL_REG set to UNREGISTERED
        Info (286033): Parameter RDCONTROL_ACLR set to OFF
        Info (286033): Parameter INDATA_REG set to INCLOCK
        Info (286033): Parameter INDATA_ACLR set to OFF
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        Info (286033): Parameter OUTDATA_REG set to UNREGISTERED
        Info (286033): Parameter OUTDATA_ACLR set to OFF
        Info (286033): Parameter LPM_FILE set to UNUSED
        Info (286033): Parameter RAM_BLOCK_TYPE set to LUTRAM
    Info (276038): Inferred altdpram megafunction from the following logic: "fpga_top|
inst_green_bs|platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|rspOrder|
gen_rd_rob.rd_rob|r[0].validBits|ram|m[0].ram|data_rtl_0"
        Info (286033): Parameter WIDTH set to 1
        Info (286033): Parameter WIDTHAD set to 6
        Info (286033): Parameter NUMWORDS set to 64
        Info (286033): Parameter WRADDRESS_REG set to INCLOCK
        Info (286033): Parameter WRADDRESS_ACLR set to OFF
        Info (286033): Parameter WRCONTROL_REG set to INCLOCK
        Info (286033): Parameter WRCONTROL_ACLR set to OFF
        Info (286033): Parameter RDADDRESS_REG set to OUTCLOCK
        Info (286033): Parameter RDADDRESS_ACLR set to OFF
        Info (286033): Parameter RDCONTROL_REG set to UNREGISTERED
        Info (286033): Parameter RDCONTROL_ACLR set to OFF
        Info (286033): Parameter INDATA_REG set to INCLOCK
        Info (286033): Parameter INDATA_ACLR set to OFF
        Info (286033): Parameter OUTDATA_REG set to UNREGISTERED
        Info (286033): Parameter OUTDATA_ACLR set to OFF
        Info (286033): Parameter LPM_FILE set to UNUSED
        Info (286033): Parameter RAM_BLOCK_TYPE set to LUTRAM
    Info (276038): Inferred altdpram megafunction from the following logic: "fpga_top|
inst_green_bs|platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|rspOrder|
gen_rd_rob.rd_rob|r[0].validBits|ram|m[1].ram|data_rtl_0"
        Info (286033): Parameter WIDTH set to 1
        Info (286033): Parameter WIDTHAD set to 6
        Info (286033): Parameter NUMWORDS set to 64
        Info (286033): Parameter WRADDRESS_REG set to INCLOCK
        Info (286033): Parameter WRADDRESS_ACLR set to OFF
        Info (286033): Parameter WRCONTROL_REG set to INCLOCK
        Info (286033): Parameter WRCONTROL_ACLR set to OFF
        Info (286033): Parameter RDADDRESS_REG set to OUTCLOCK
        Info (286033): Parameter RDADDRESS_ACLR set to OFF
        Info (286033): Parameter RDCONTROL_REG set to UNREGISTERED
        Info (286033): Parameter RDCONTROL_ACLR set to OFF
        Info (286033): Parameter INDATA_REG set to INCLOCK
        Info (286033): Parameter INDATA_ACLR set to OFF
        Info (286033): Parameter OUTDATA_REG set to UNREGISTERED
        Info (286033): Parameter OUTDATA_ACLR set to OFF
        Info (286033): Parameter LPM_FILE set to UNUSED
        Info (286033): Parameter RAM_BLOCK_TYPE set to LUTRAM
    Info (276038): Inferred altdpram megafunction from the following logic: "fpga_top|
inst_green_bs|platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|rspOrder|
gen_rd_rob.rd_rob|r[0].validBits|ram|m[2].ram|data_rtl_0"
        Info (286033): Parameter WIDTH set to 1
        Info (286033): Parameter WIDTHAD set to 6
        Info (286033): Parameter NUMWORDS set to 64
        Info (286033): Parameter WRADDRESS_REG set to INCLOCK
        Info (286033): Parameter WRADDRESS_ACLR set to OFF
        Info (286033): Parameter WRCONTROL_REG set to INCLOCK
        Info (286033): Parameter WRCONTROL_ACLR set to OFF
        Info (286033): Parameter RDADDRESS_REG set to OUTCLOCK
        Info (286033): Parameter RDADDRESS_ACLR set to OFF
        Info (286033): Parameter RDCONTROL_REG set to UNREGISTERED
        Info (286033): Parameter RDCONTROL_ACLR set to OFF
        Info (286033): Parameter INDATA_REG set to INCLOCK
        Info (286033): Parameter INDATA_ACLR set to OFF
        Info (286033): Parameter OUTDATA_REG set to UNREGISTERED
        Info (286033): Parameter OUTDATA_ACLR set to OFF
        Info (286033): Parameter LPM_FILE set to UNUSED
        Info (286033): Parameter RAM_BLOCK_TYPE set to LUTRAM
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    Info (276038): Inferred altdpram megafunction from the following logic: "fpga_top|
inst_green_bs|platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|rspOrder|
gen_rd_rob.rd_rob|r[0].validBits|ram|m[3].ram|data_rtl_0"
        Info (286033): Parameter WIDTH set to 1
        Info (286033): Parameter WIDTHAD set to 6
        Info (286033): Parameter NUMWORDS set to 64
        Info (286033): Parameter WRADDRESS_REG set to INCLOCK
        Info (286033): Parameter WRADDRESS_ACLR set to OFF
        Info (286033): Parameter WRCONTROL_REG set to INCLOCK
        Info (286033): Parameter WRCONTROL_ACLR set to OFF
        Info (286033): Parameter RDADDRESS_REG set to OUTCLOCK
        Info (286033): Parameter RDADDRESS_ACLR set to OFF
        Info (286033): Parameter RDCONTROL_REG set to UNREGISTERED
        Info (286033): Parameter RDCONTROL_ACLR set to OFF
        Info (286033): Parameter INDATA_REG set to INCLOCK
        Info (286033): Parameter INDATA_ACLR set to OFF
        Info (286033): Parameter OUTDATA_REG set to UNREGISTERED
        Info (286033): Parameter OUTDATA_ACLR set to OFF
        Info (286033): Parameter LPM_FILE set to UNUSED
        Info (286033): Parameter RAM_BLOCK_TYPE set to LUTRAM
    Info (276038): Inferred altdpram megafunction from the following logic: "fpga_top|
inst_green_bs|platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|rspOrder|
gen_rd_rob.rd_rob|r[1].validBits|ram|m[0].ram|data_rtl_0"
        Info (286033): Parameter WIDTH set to 1
        Info (286033): Parameter WIDTHAD set to 6
        Info (286033): Parameter NUMWORDS set to 64
        Info (286033): Parameter WRADDRESS_REG set to INCLOCK
        Info (286033): Parameter WRADDRESS_ACLR set to OFF
        Info (286033): Parameter WRCONTROL_REG set to INCLOCK
        Info (286033): Parameter WRCONTROL_ACLR set to OFF
        Info (286033): Parameter RDADDRESS_REG set to OUTCLOCK
        Info (286033): Parameter RDADDRESS_ACLR set to OFF
        Info (286033): Parameter RDCONTROL_REG set to UNREGISTERED
        Info (286033): Parameter RDCONTROL_ACLR set to OFF
        Info (286033): Parameter INDATA_REG set to INCLOCK
        Info (286033): Parameter INDATA_ACLR set to OFF
        Info (286033): Parameter OUTDATA_REG set to UNREGISTERED
        Info (286033): Parameter OUTDATA_ACLR set to OFF
        Info (286033): Parameter LPM_FILE set to UNUSED
        Info (286033): Parameter RAM_BLOCK_TYPE set to LUTRAM
    Info (276038): Inferred altdpram megafunction from the following logic: "fpga_top|
inst_green_bs|platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|rspOrder|
gen_rd_rob.rd_rob|r[1].validBits|ram|m[1].ram|data_rtl_0"
        Info (286033): Parameter WIDTH set to 1
        Info (286033): Parameter WIDTHAD set to 6
        Info (286033): Parameter NUMWORDS set to 64
        Info (286033): Parameter WRADDRESS_REG set to INCLOCK
        Info (286033): Parameter WRADDRESS_ACLR set to OFF
        Info (286033): Parameter WRCONTROL_REG set to INCLOCK
        Info (286033): Parameter WRCONTROL_ACLR set to OFF
        Info (286033): Parameter RDADDRESS_REG set to OUTCLOCK
        Info (286033): Parameter RDADDRESS_ACLR set to OFF
        Info (286033): Parameter RDCONTROL_REG set to UNREGISTERED
        Info (286033): Parameter RDCONTROL_ACLR set to OFF
        Info (286033): Parameter INDATA_REG set to INCLOCK
        Info (286033): Parameter INDATA_ACLR set to OFF
        Info (286033): Parameter OUTDATA_REG set to UNREGISTERED
        Info (286033): Parameter OUTDATA_ACLR set to OFF
        Info (286033): Parameter LPM_FILE set to UNUSED
        Info (286033): Parameter RAM_BLOCK_TYPE set to LUTRAM
    Info (276038): Inferred altdpram megafunction from the following logic: "fpga_top|
inst_green_bs|platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|rspOrder|
gen_rd_rob.rd_rob|r[1].validBits|ram|m[2].ram|data_rtl_0"
        Info (286033): Parameter WIDTH set to 1
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        Info (286033): Parameter WIDTHAD set to 6
        Info (286033): Parameter NUMWORDS set to 64
        Info (286033): Parameter WRADDRESS_REG set to INCLOCK
        Info (286033): Parameter WRADDRESS_ACLR set to OFF
        Info (286033): Parameter WRCONTROL_REG set to INCLOCK
        Info (286033): Parameter WRCONTROL_ACLR set to OFF
        Info (286033): Parameter RDADDRESS_REG set to OUTCLOCK
        Info (286033): Parameter RDADDRESS_ACLR set to OFF
        Info (286033): Parameter RDCONTROL_REG set to UNREGISTERED
        Info (286033): Parameter RDCONTROL_ACLR set to OFF
        Info (286033): Parameter INDATA_REG set to INCLOCK
        Info (286033): Parameter INDATA_ACLR set to OFF
        Info (286033): Parameter OUTDATA_REG set to UNREGISTERED
        Info (286033): Parameter OUTDATA_ACLR set to OFF
        Info (286033): Parameter LPM_FILE set to UNUSED
        Info (286033): Parameter RAM_BLOCK_TYPE set to LUTRAM
    Info (276038): Inferred altdpram megafunction from the following logic: "fpga_top|
inst_green_bs|platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|rspOrder|
gen_rd_rob.rd_rob|r[1].validBits|ram|m[3].ram|data_rtl_0"
        Info (286033): Parameter WIDTH set to 1
        Info (286033): Parameter WIDTHAD set to 6
        Info (286033): Parameter NUMWORDS set to 64
        Info (286033): Parameter WRADDRESS_REG set to INCLOCK
        Info (286033): Parameter WRADDRESS_ACLR set to OFF
        Info (286033): Parameter WRCONTROL_REG set to INCLOCK
        Info (286033): Parameter WRCONTROL_ACLR set to OFF
        Info (286033): Parameter RDADDRESS_REG set to OUTCLOCK
        Info (286033): Parameter RDADDRESS_ACLR set to OFF
        Info (286033): Parameter RDCONTROL_REG set to UNREGISTERED
        Info (286033): Parameter RDCONTROL_ACLR set to OFF
        Info (286033): Parameter INDATA_REG set to INCLOCK
        Info (286033): Parameter INDATA_ACLR set to OFF
        Info (286033): Parameter OUTDATA_REG set to UNREGISTERED
        Info (286033): Parameter OUTDATA_ACLR set to OFF
        Info (286033): Parameter LPM_FILE set to UNUSED
        Info (286033): Parameter RAM_BLOCK_TYPE set to LUTRAM
    Info (276038): Inferred altdpram megafunction from the following logic: "fpga_top|
inst_green_bs|platform_shim_ccip_std_afu|ccip_std_afu|mpf|mpf_pipe|mpf_edge_afu|
afu_edge|wr_heap_ctrl|lr.fl|freeList|data_rtl_0"
        Info (286033): Parameter WIDTH set to 7
        Info (286033): Parameter WIDTHAD set to 7
        Info (286033): Parameter NUMWORDS set to 128
        Info (286033): Parameter WRADDRESS_REG set to INCLOCK
        Info (286033): Parameter WRADDRESS_ACLR set to OFF
        Info (286033): Parameter WRCONTROL_REG set to INCLOCK
        Info (286033): Parameter WRCONTROL_ACLR set to OFF
        Info (286033): Parameter RDADDRESS_REG set to OUTCLOCK
        Info (286033): Parameter RDADDRESS_ACLR set to OFF
        Info (286033): Parameter RDCONTROL_REG set to UNREGISTERED
        Info (286033): Parameter RDCONTROL_ACLR set to OFF
        Info (286033): Parameter INDATA_REG set to INCLOCK
        Info (286033): Parameter INDATA_ACLR set to OFF
        Info (286033): Parameter OUTDATA_REG set to UNREGISTERED
        Info (286033): Parameter OUTDATA_ACLR set to OFF
        Info (286033): Parameter LPM_FILE set to UNUSED
        Info (286033): Parameter RAM_BLOCK_TYPE set to LUTRAM
    Info (276029): Inferred altsyncram megafunction from the following design logic:
"fpga_top|inst_green_bs|platform_shim_ccip_std_afu|ccip_std_afu|hal|dma_ctrl|rd_fifo|
mem_rtl_0"
        Info (286033): Parameter OPERATION_MODE set to DUAL_PORT
        Info (286033): Parameter WIDTH_A set to 512
        Info (286033): Parameter WIDTHAD_A set to 9
        Info (286033): Parameter NUMWORDS_A set to 512
        Info (286033): Parameter WIDTH_B set to 512
```

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        Info (286033): Parameter WIDTHAD_B set to 9
        Info (286033): Parameter NUMWORDS_B set to 512
        Info (286033): Parameter ADDRESS_ACLR_A set to NONE
        Info (286033): Parameter OUTDATA_REG_B set to UNREGISTERED
        Info (286033): Parameter ADDRESS_ACLR_B set to NONE
        Info (286033): Parameter OUTDATA_ACLR_B set to NONE
        Info (286033): Parameter ADDRESS_REG_B set to CLOCK0
        Info (286033): Parameter INDATA_ACLR_A set to NONE
        Info (286033): Parameter WRCONTROL_ACLR_A set to NONE
```