Portland State University

ECE571 – Intro to SystemVerilog

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AXI4 LITE

VERIFICATION PLAN

Group 1

Pradeep Reddy M

Narendra Srinivas R

Naveen Manivannan

Introduction:-

The AMBA AXI-Lite protocol is the traditional version and subset of AXI(Advance eXtensible Interface used for communication with simpler control register style interfaces within components. It can have multiple masters and slaves which are synchronous has high performance and frequency. It is mainly used for on-chip communication.

In our project we are using a single master and slave environment which communicates using five channels to ensure there are successful transactions(Read and Writes) between the master and slave. We need to make sure that the Reads and writes of this master slave system is working as expected. The five channels being used here are Write Address Channel, Write Data Channel, Write Response Channel, Read Address Channel, Read Data Channel.

Each channel has its own VALID/READY and uses the same for handshake, in order to transfer control and data information Each channel uses specific signals which are listed in the upcoming slides. The functionalities, description and direction of the signals in each channel and who drives the signal is listed in upcoming tables. We have also listed the Testcases using which we intend to find the bugs in the Design.

Signals used:-

NO	SIGNAL NAME	DESCRIPTION	DIRECTION	CHANNEL
1	ARESETN	SYSTEM RESET (ACTIVE LOW)	NONE	ALL CHANNEL
2	ACLK	SYSTEM CLOCK	NONE	ALL CHANNEL
3	AWADDR	WRITE ADDRESS VALID, ADDRESS TO BE WRITTEN INTO	NONE	WRITE ADDRESS CHANNEL
4	AWVALID	WRITE ADDRESS VALID, SETS HIGH IF ADDRESS IS VALID	MASTER → SLAVE	WRITE ADDRESS CHANNEL

5	AWREADY	WRITE ADDRESS READY, WHEN SLAVE IS READY TO ACCEPT	SLAVE → MASTER	WRITE ADDRESS CHANNEL
6	WDATA	WRITE DATA, DATA TO BE WRITTEN INTO	NONE	WRITE DATA CHANNEL
7	WVALID	WRITE VALID, SETS HIGH IF DATA IS VALID	MASTER → SLAVE	WRITE DATA CHANNEL
8	WREADY	WRITE READY, WHEN SLAVE IS READY TO ACCEPT	SLAVE → MASTER	WRITE DATA CHANNEL
9	BVALID	WRITE RESPONSE VALID, SLAVE GENERATES WHEN WRITE RESPONSE ON BUS VALID	SLAVE → MASTER	WRITE RESPONSE CHANNEL
10	BREADY	READ ADDRESS READY, WHEN MASTER CAN ACCEPT WRITE RESPONSE	MASTER → SLAVE	WRITE RESPONSE CHANNEL
11	ARADDR	READ ADDRESS, ADDRESS TO BE READ	NONE	READ ADDRESS CHANNEL
12	ARVALID	READ ADDRESS VALID, SETS HIGH IF READ ADDRESS AND CONTROL SIGNALS ARE VALID	MASTER → SLAVE	READ ADDRESS CHANNEL
13	ARREADY	READ ADDRESS READY, WHEN SLAVE IS READY TO ACCEPT READ ADDRESS AND CONTROL SIGNAL	SLAVE → MASTER	READ ADDRESS CHANNEL
14	RDATA	READ DATA, DATA TO BE READ	NONE	READ DATA CHANNEL
15	RVALID	READ VALID, SETS HIGH IF READ DATA IS VALID	SLAVE → MASTER	READ DATA CHANNEL
16	RREADY	READ READY, WHEN MASTER CAN ACCEPT READ DATA	MASTER → SLAVE	READ DATA CHANNEL
17	rd_en	READ ENABLE, SETS HIGH TO ACCESS ALL READ CHANNEL	NONE	CONTROL SIGNAL
18	wr_en	WRITE ENABLE, SETS HIGH TO ACCESS ALL WRITE CHANNEL	NONE	CONTROL SIGNAL

Unit Level Testing and Test cases:-

We will be testing the 5 channels of AXI4-LITE namely Write Address channel, Write Data channel, Write Response channel, Read Address channel, Read Data channel. We will be writing directed test cases to cover the functionality of each unit by simulating the behavior of these channels using assertions and checkers.

Write Address Channel:-

- Assert wr_en and toggle AWVALID signal to check the behavior of AWREADY signal.
- Deassert wr_en and toggle AWVALID signal to check the behavior of AWREADY signal.

Signals	Expected behaviour	Outcome (Pass/Fail)
wr_en, AWVALID	AWREADY	Pass
wr_en, !AWVALID	AWREADY	Fail
wr_en, AWVALID	!AWREADY	Fail
wr_en, !AWVALID	!AWREADY	Pass
!wr_en, AWVALID	AWREADY	Fail
!wr_en, !AWVALID	AWREADY	Fail
!wr_en, AWVALID	!AWREADY	Fail
!wr_en, !AWVALID	!AWREADY	Pass

Write Data Channel:-

- Assert AWVALID and toggle WVALID signal to check the behavior of WREADY signal.
- Deassert AWVALID and toggle WVALID signal to check the behavior of WREADY signal.

Signals	Expected behaviour	Outcome (Pass/Fail)
AWVALID, WVALID	WREADY	Pass
!AWVALID, WVALID	WREADY	Fail
AWVALID, WVALID	!WREADY	Fail
!AWVALID, WVALID	!WREADY	Pass
AWVALID, !WVALID	!WREADY	Pass
AWVALID, !WVALID	WREADY	Fail
!AWVALID, !WVALID	WREADY	Fail
!AWVALID, !WVALID	!WREADY	Pass

Write Response Channel:-

- Assert BREADY and toggle the other handshake signals to check the behavior of BVALID signal.
- Deassert BREADY to check the behavior of BVALID signal.

Signals	Expected behaviour	Outcome (Pass/Fail)
BREADY, AWVALID, WVALID, AWREADY, WREADY	BVALID	Pass
BREADY, AWVALID, WVALID, AWREADY, WREADY	!BVALID	Fail
BREADY, !(AWVALID, WVALID, AWREADY, WREADY)	BVALID	Fail
BREADY, !(AWVALID, WVALID, AWREADY, WREADY)	!BVALID	Pass
!BREADY, AWVALID, WVALID, AWREADY, WREADY	BVALID	Fail
!BREADY, AWVALID, WVALID, AWREADY, WREADY	!BVALID	Pass

Read Address Channel:-

- Assert rd_en and toggle ARVALID signal to check the behavior of ARREADY signal.
- Deassert rd_en and toggle ARVALID signal to check the behavior of ARREADY signal.

Signals	Expected behaviour	Outcome (Pass/Fail)
rd_en, ARVALID	ARREADY	Pass
rd_en, ARVALID	!ARREADY	Fail
rd_en, !ARVALID	ARREADY	Fail
rd_en, !ARVALID	!ARREADY	Pass
!rd_en, ARVALID	ARREADY	Fail
!rd_en, ARVALID	!ARREADY	Pass
!rd_en, !ARVALID	ARREADY	Fail
!rd_en, !ARVALID	!ARREADY	Pass

Read Data Channel:-

- Assert RREADY and toggle ARREADY signal to check the behavior of RVALID signal.
- Deassert RREADY and toggle ARREADY signal to check the behavior of RVALID signal.

Signals	Expected behaviour	Outcome (Pass/Fail)
RREADY,ARREADY	RVALID	Pass
RREADY,ARREADY	!RVALID	Fail
RREADY,!ARREADY	RVALID	Fail
RREADY,!ARREADY	!RVALID	Pass
!RREADY,ARREADY	RVALID	Fail
!RREADY,ARREADY	!RVALID	Pass

Global Test cases:-

- When ARESETN is low, all handshake signals should be low.
- Testing the address and data bus for 32 bit width.
- Check validity of ACLK before applying stimulus.

Test Case Name	Description
Test_WR_Location	Write to a given location in the memory
Test_RD_Location	Read from a given location in the memory
Test_WR_Last	Write to the last location in the memory
Test_RD_Last	Read from the last location in the memory
Test_WR_Outofrange	Write to the location not in memory
Test_RD_Outofrange	Read from a location not in memory
Test_WR_RD	Write and then read that from the same location to make sure that the data is written correctly
Test_RD_WR	Read and then write that location in the memory
Test_WR_Successive	Multiple writes to the memory to check for any issues in the system
Test_RD_Successive	Multiple reads to the memory to check for any issues in the system

Assertions Used:

Various assertions are written and deployed in each channel to verify the AXI-4 lite design and identify bugs.

The names of the assertions and their description is given below.

Assertion Name	Description	Channel
AWADDR_STABLE_a	AWADDR remains stable when AWVALID is asserted and AWREADY is LOW	Write address channel
AWVALID_STABLE_a	When AWVALID is asserted, then it remains asserted until AWREADY is HIGH	Write address channel
AWADDR_xcheck_a	A value of X on AWADDR is not permitted when AWVALID is HIGH	Write address channel

WDATA_stable_a	WDATA remains stable when WVALID is asserted and WREADY is LOW	Write Data Channel
WVALID_stable_a	When WVALID is asserted, then it must remain asserted until WREADY is HIGH	Write Data Channel
WDATA_xcheck_a	A value of X on WDATA valid byte lanes is not permitted when WVALID is HIGH	Write Data Channel
ARADDR_stable_a	ARADDR remains stable when ARVALID is asserted and ARREADY is LOW	Read Address Channel
ARVALID_stable_a	When ARVALID is asserted, then it remains asserted until ARREADY is HIGH	Read Address Channel
ARADDR_xcheck_a	A value of X on ARADDR is not permitted when ARVALID is HIGH	Read Address Channel
RDATA_stable_a	RDATA remains stable when RVALID is asserted, and RREADY is LOW	Read Data Channel
RVALID_stable_a	When RVALID is asserted, then it must remain asserted until RREADY is HIGH	Read Data Channel
RDATA_xcheck_a	A value of X on RDATA is not permitted when RVALID is HIGH	Read Data Channel

Work Split-up:-

Responsibilities	Members
Environment Setup and Makefile	Pradeep,Srinivas,Naveen
Simulation	Pradeep,Srinivas
Unit level testing for Write Address,Write data Channel	Srinivas,Naveen
Unit level testing for Read Address,Read data Channel	Pradeep,Srinivas
Unit level testing for Write Response Channel and Global Coverage	Naveen,Pradeep