MIPS16 verification Draft

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Work Split up:

Person 1-5: Unit level testing, Writing assertions at unit level.
Person 1, 2, 5: CPU level testing, assemble code, log expected result
Person 3, 4: Emulation
Person 1-5: Makefile, Environment setup.
Person 5: Packaging the RTL, Run unit level and CPU level test.

Unit level Testing and the testcases and assertions for Unit level

We will be testing all 8 units naming IF, ID, EXE, MEM, WB (involved in the 5 stage MIPS16 pipeline), Hazard, register_file and CPU with 8 test benches. For unit level testing, we will be writing directed test cases by simulating the behavior of the neighboring blocks to cover functionality of each unit. Assertions will be used as checkers for unit level testing. A brief test plan for each unit is provided below.

Instruction Fetch:

Strategy: - Load the instruction memory through a memory map file, simulate the output behavior from the ID stage (branch, imm offset) and Hazard (fetch enable), check for valid output.

Test	Description
Test_reset	Assert reset, check PC=0 (assertions)
Test_instruction_enable	De assert instruction fetch enable, simulate for branch taken and branch not taken
Test_branch_taken	Assert instruction fetch enable and branch, test for + and – immediate displacement, zero displacement, +/- max displacement (assertions)
Test_branch_not_taken	Assert instruction fetch enable, de assert branch
Test_pc_rollover	Assert instruction fetch enable, assert branch, keep incrementing PC by giving + immediate displacement till it roll over from last address

Assertions

Assertion	Description
IF_inst_nx_assert	Check if the instruction from Instruction memory is not unknown, and instruction[15:12] is a valid code
IF_inst_valid_nop_assert	Check if the NOP instruction is valid, if instruction[15:12] = 0 then instruction = 0
IF_inst_valid_rtype_assert	Check for valid R- Type instruction, instruction [2:0]=0
IF_inst_valid_bz_assert	Check for valid Branch instruction, instruction [11:9]=0
IF_pc_inc_assert	Check if the PC is incremented, based on branch taken/immediate offset

Instruction Decode:

Strategy: - Send a valid instruction, valid data for the register read access request to simulate the behavior of IF (instruction), Hazard (decode_enable) and register file (reg_read_addr1/2). Check for the expected decoded output (write_back_enable, source/destination address, immediate field value, ALU command).

Test	Description
Test_reset	Assert reset, check instruction_reg = 0 (assertions)
Test_decode_en	De assert decode enable, send a valid instruction and check if it is executed or not
Test_register_instruction_decode	Assert decode enable, send valid R-type instructions and check a valid/corresponding ALU command and register address is decoded at the output (assertions)
Test_immediate_instruction_decode	Assert decode enable, send valid I-type instructions and check a valid/corresponding ALU command and register address and immediate field is decoded at the output
Test_branch_instruction_decode	Assert decode enable, send a branch instruction, test for branch taken/not taken
Test_invalid_instructions	Assert decode enable, send an invalid instruction and check if its not decoded.

Assertions:

Assertion	Description
ID_alu_cmd_nop_assert	To check if instruction is OP_NOP and alu_cmd is ALU_NOP and write_back_enable is 0 and mux_sel is X.
ID_alu_cmd_add_assert	To check if instruction is OP_ADD and alu_cmd is ALU_ADD and write_back_enable is 1 and mux_sel is 0.
ID_alu_cmd_sub_assert	To check if instruction is OP_SUB and alu_cmd is ALU_SUB and write_back_enable is 1 and mux_sel is 0.
ID_alu_cmd_and_assert	To check if instruction is OP_AND and alu_cmd is ALU_AND and write_back_enable is 1 and mux_sel is 0.

ID_alu_cmd_or_assert	To check if instruction is OP_OR and alu_cmd is ALU_OR and write_back_enable is 1 and mux_sel is 0.
ID_alu_cmd_xor_assert	To check if instruction is OP_XOR and alu_cmd is ALU_XOR and write_back_enable is 1 and mux_sel is 0. a
ID_alu_cmd_sl_assert	To check if instruction is OP_SL and alu_cmd is ALU_SL and write_back_enable is 1 and mux_sel is 0.
ID_alu_cmd_sr_assert	To check if instruction is OP_SR and alu_cmd is ALU_SR and write_back_enable is 1 and mux_sel is 0.
ID_alu_cmd_sru_assert	To check if instruction is OP_SRU and alu_cmd is ALU_SRU and write_back_enable is 1 and mux_sel is 0.
ID_alu_cmd_addi_assert	To check if instruction is OP_ADDI and alu_cmd is ALU_ADDI and write_back_enable is 1 and mux_sel is 0.
ID_alu_cmd_ld_assert	To check if instruction is OP_LD and alu_cmd is ALU_LD and write_back_enable is 1 and mux_sel is 1.
ID_alu_cmd_st_assert	To check if instruction is OP_ST and alu_cmd is ALU_ST and write_back_enable is 0 and mux_sel is x.
ID_alu_cmd_bz_assert	To check if instruction is OP_BZ and alu_cmd is ALU_BZ and write_back_enable is 0 and mux_sel is x.
ID_forward_rd1_op1_assert	Check read_data_1 is forwarded to operand1
ID_forward_rd2_mem_wr_data_assert	Check read_data_2 is forwarded to memory_write_data
ID_mem_wr_en_assert	Check if mem_write_en is asserted for ST instruction
ID_reg_addr_1_assert	Check if reg_read_address_1 is extracted from instruction
ID_reg_addr_2_assert	Check if reg_read_address_2 is extracted from instruction

Execute:

Strategy: This unit will be tested in conjunction with the ID (after ID unit level is clean), we will use the ID test stimulus to get a valid input to the EXE stage. Check for expected ALU operation result, and rest of the signals like write_back, memory write are forwarded to the next stage. We will be using assertions to check the ALU results.

Test	Description
Test_reset	Assert reset, check pipeline_reg_out = 0 (assertions)
Test_alu_operation	Send valid ALU command and operands, check for expected results (Assertions)
Test_invalid_alu_operation	Send invalid ALU command and check results

Assertions for Execute Stage:

Assertion	Description
alu_result_assert	To check if selected part of output is evaluated one clock tick after the ALU result ends when reset is disabled.
pipeline_reg_write_data_assert	To check if selected part of output is evaluated one clock tick after the pipeline_reg_in result ends when reset is disabled.

Assertions for ALU:

Assertion	Description
alu_nc_assert	Checking the result for the corresponding command ALU_NC and checking the bits a and b contain X or Z.
alu_add_assert	Checking the result for the corresponding command ALU_ADD and checking the bits a and b contain X or Z.
alu_sub_assert	Checking the result for the corresponding command ALU_SUB and checking the bits a and b contain X or Z.
alu_and_assert	Checking the result for the corresponding command ALU_AND and checking the bits a and b contain X or Z.
alu_or_assert	Checking the result for the corresponding command ALU_OR and checking the bits a and b contain X or Z.
alu_xor_assert	Checking the result for the corresponding command ALU_XOR and checking the bits a and b contain X or Z.
alu_sl_assert	Checking the result for the corresponding command ALU_SL and checking the bits a and b contain X or Z.
alu_sr_assert	Checking the result for the corresponding command ALU_SR and checking the bits a and b contain X or Z.
alu_sru_assert	Checking the result for the corresponding command ALU_SRU and checking the bits a and b contain X or Z.

Memory Stage:

Strategy: - We are going to test the data memory in this unit testing. Load the data memory with random values/memory map file (same memory image will be loaded to checker memory), drive valid address, toggle write enable and perform read/write. Check the read data with the checker memory copy. Assertion for checking data_in [4:0] == data_out[4:0]

Test	Description
Test_reset	Assert reset, check pipeline_reg_out = 0 (assertions)
Test_write_operation	Assert write enable, send valid address and data, check the data_out is same as data provided for write
Test_read_operation	De-assert write enable, send valid address and check whether data out is same as checker memory copy.

Assertions:

Assertion	Description
pipeline_reg_addr_assert	To check if selected part of pipeline_reg_out is evaluated one clock tick after the selected part of pipeline_reg_in ends and when reset is disabled.
pipeline_reg_write_data_assert	To check if selected part of pipeline_reg_out is evaluated one clock tick after the selected part of pipeline_reg_in ends and when reset is disabled.
pipeline_reg_in_out_assert	To check if selected part of pipeline_reg_out is evaluated one clock tick after the selected part of pipeline_reg_in ends and when reset is disabled.

Write Back Stage:

Strategy: - In this unit we will be testing the ALU result/Data write back mux. Toggle write back mux control to switch between data to be written to register file, drive valid alu result/memory read data, drive destination register address and check corresponding data/address/write_en appears at the output. Use assertions to check all the outputs.

Test	Description
Test_toggle_mux	Toggle write back mux control and check if reg_write_data is selected based on selection input Write to all destination registers

Assertions:

Assertion	Description
Write_back_result_mux1_assert	To check if pipeline_reg_in[20:5] is taken by reg_write_data when write_back_result_mux is 1.
Write_back_result_mux0_assert	To check if pipeline_reg_in[36:21] is taken by reg_write_data when write_back_result_mux is 0.

Register file:

Strategy: - We are testing the behavior of simultaneous single write, dual read memory in this unit. Drive the inputs to valid address/data check for read/write behavior. A checker memory array will be used to compare the results of read/write.

Test	Description
Test_reset	Assert reset, check all register values = 0 (assertions)
Test_write_operation	Assert write enable, send valid address and data, do a read to same address and check if the data was written successfully
Test_read_operation	De-assert write enable, send valid address to both the read port, check if the data received matches the checker memory De-assert write enable, send same address to both the read port, check if the data received matches the checker memory De assert write enable, read to destination register 000 and check the result of read is zero
Test_read_write_same_address	Assert write enable, make read and write address same. Check data written appears on read port.

Assertions:

Assertion	Description
Wb_reset_assert	Check all the registers are reset to 0
Wb_write_nx	Check if the data written to register on write_en is valid (no x's)
wb_read_r0	Check if the read to R0 always returns 0

Hazard:

Strategy: - Drive valid source register address (ID stage) and destination register address (EXE/MEM/WB). Check for pipeline stall condition. Assertions will be used to monitor active low pipeline stall signal.

Test	Description
Test_source_zero	Source1/source2 register address = 0
Test_source_non_zero_stall	Source1/source2 register address!=0, but source1 = EXE/MEM/WB destination address Source1/source2 register address!=0, but source2 = EXE/MEM/WB destination address
Test_source_non_zero_no_stall	Source1/source2 register address!=0, but source1 != EXE/MEM/WB destination address Source1/source2 register address!=0, but source2 != EXE/MEM/WB destination address

Assertions:

Assertion	Description
Hz_src1_hazzard	Check if the pipeline_stall_n is asserted for RAW hazzard from operand 1
Hz_src2_hazzard	Check if the pipeline_stall_n is asserted for RAW hazzard from operand 2

CPU level verification and Test plan:

For top level testing we will be writing code snippets in MIPS16 assembly, use the software model to get the instruction code. Load the Instruction memory and monitor the Registers.

The expected result (Register values) for each test will be logged in a file, and the results after each simulation will be compared against it

Test	Description
Test_reset	Assert reset, check registers
Test_ISA	Test each instruction individually, checks expected result from the register file. R-type instruction: Test involving access to all 8 registers, for each instruction Test the access to R0 special register. I-type Instruction: Test LD/ST instruction Test for branch instructions, +/- displacement, rollover from last accessible address. Test for +/-/0 immediate values
Test_snippets	Write a MIPS16 assembly code snippets and test for expected behavior
Test_Hazard	Write a assembly code with RAW pipeline hazards and check for pipeline stalls.

Unit level assertions will be binded for top CPU level verification.

Emulation:

We have to setup the design for emulation. For this setup, we should create a design directory on our compile host or file server. After adding HDL, HVL and source files, we should setup and map analysis libraries and create veloce.config file. Now, when the veloce.config file with all the compilation options is in the current design directory, we should run the velcomp from the top level of our design directory.

Packaging of RTL and Verify:

Replace the interconnections between the pipeline stages with interface/mod ports. Individually test each unit using the test bench created for the RTL released. The RTL from git will be used as a reference model for the testing. Stitch all the units together and run CPU level testing on the top module.

Find any chance of parameterizing/encapsulation in the RTL

Makefile, Environment Setup, project package:

All the unit level test/CPU level testing will have its own Makefile, the make file is capable of reading the Assembly code, load the instruction memory and chose test to be run. Individual who owns the unit level test will create their own Makefile and environment setup.

Setup for Emulator is done by person who owns emulation part of the project.