Verification of AMBA AXI4-Lite protocol

Fall 2021
ECE 571 Project Option 2
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AXI4 Lite Protocol

The Advanced eXtensible Interface (AXI), part of the ARM Advanced Microcontroller Bus Architecture is a parallel high-performance, synchronous, high-frequency, multi-master, multi-slave communication interface, mainly designed for on-chip communication.

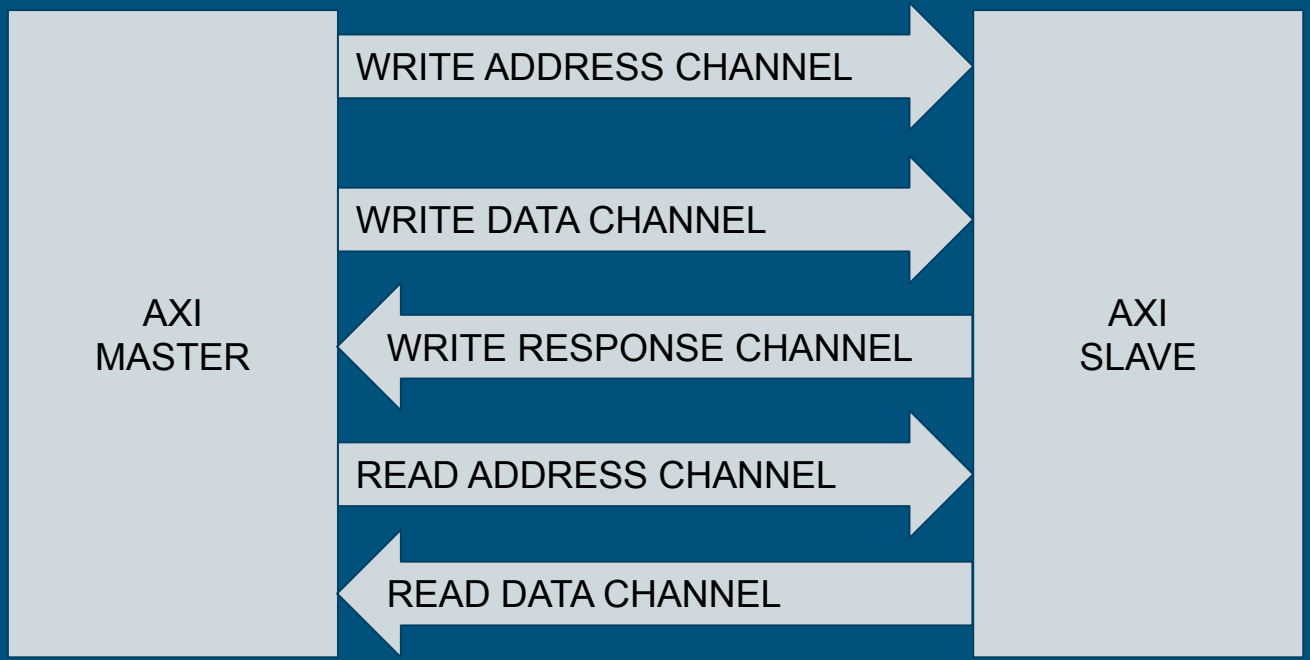
The AMBA specification defines three AXI4 protocols:

- AXI4

- AXI4-Lite: A subset of AXI, lacking burst access capability. Has a simpler interface than the full AXI4 interface. Main features are that the address is a traditional Address/Data (single address, single data) and supports only 32 or 64 bits data width.

- AXI4-Stream

Block Diagram



What will be provided with?

Master model, Slave model and an interface.

The slave writes the data received from master to a memory.

The memory range supported for the slave is parameterised.

The signals are encapsulated using an interface.

Slave and master modports are defined in the interface specify direction of signals.

axi4lite_master.sv	Drives address/data and controls to the slave via interface.	Encrypted
axi4lite_slave.sv	Sends data from the requested address to the master. Writes data received from master to a memory.	Encrypted
axi4lite_pkg.sv	Contains shared parameters/structures/enum used in DUV	Visible
axi4lite_bfm.sv	Bus Functional Model Includes all the signals required by the DUV.	Visible
design.sv	The instantiation of master, slave and bus functional model	Visible

Expectation

Understanding the protocol, developing verification strategy and proposing a solid verification plan.

Perform unit level testing. Then building a complete verification environment with appropriate SV constructs ie, assertions, checkers, covergroups, etc. for system level testing.

Using OOP constructs, performing directed test cases and randomised test cases.

Capture the induced bugs/logic errors in the design and explain them during the presentation.

Generating a coverage report using questaSim tool.

During 20 minute presentation, mention individual contributions and include it in Verification report as well.

Verification report showing results, bugs found, conclusions, lessons learned, future scope given more time and individual contribution

Do not forget to submit everything that reproduces your result on MAKEFILE along with source code (DUT, TB, SIM).

Additional: 4th team member - needs to submit 1-2 page proposal by email to Professor

References:

Introduction to AXI4-Lite:

https://www.realdigital.org/doc/a9fee931f7a172423e1ba73f66ca4081

Specification:

http://www.gstitt.ece.ufl.edu/courses/fall15/eel4720_5721/labs/refs/AXI4_specification.pdf

Reminder

Join the github classroom and self assign as group of 3 (4 with approval).

Wed, 10-Nov: AXI4 lite project details release on d2l

Mon, 15-Nov: Decide on project of choice and inform TA

Sun, 28-Nov: Verification plan turn in on d2l

Mon, 29-Nov: AXI4 lite broken encrypted code release.

Mon, Tue 06,07-Dec: Final project presentations - day 1,2

Wed, 08-Dec: Final project deliverables due to D2L and GitHub by 10:00pm