Mask-Design for the Fabrication of Memristive $BiFeO_3$ Crossbar Arrays

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***Abstract*—In this work, a layout of a crossbar design has been proposed. This layout is tailored for characterization purpose of resistive switching behaviour of $BiFeO_3$ (BFO) memristors formed in a crossbar structure. The ideal crossbar structure should have a footprint of $4F^2$ with F is the allowed minimum structure width at the technology at which the crossbar is implemented.Topic like the optical-mechanical pattern generator and issues on the fabricated bottom electrodes are discussed.**

***Index Terms*—Resistive Switching, Memristor, $BiFeO_3$ (BFO), Crossbar, Nanowire Resistance.**

I. Introduction

MOORE's Law has been a guidance in the development of microelectronics industries for more than 50 years. Through the development of this field, there has been some challenges that could have ended the Moore's Law e.g. conventional scaling, power wall, and the limitation of von Neumann architecture. The technical challenges which might eventually increase the production cost can negatively affect the self-fulfilling virtuous circle which reflects the innovation and development in this industry. For these, several device alternatives and computing architecture have been proposed. One of them is memristor and architectures which utilizing crossbar structures.

Memristor was predicted theoretically the first time in 1971 as the missing element that links charge and flux [1]. The very first paper described also the unique circuit behaviors that are impossible to be produced by RLC circuit [1]. 37 years after the prediction, the passive two-terminal memristor device was discovered [2]. Since this discovery, the research have been done from the fundamental physics of the memristive materials [3] to circuit and system level [4] [5], including many of the potential applications [6] [7] [8] [9]. The device can be be utilized as a single device [10] [11] in a circuit or in the form of array that is called memristor crossbar array [12].

The memristive material that has been under investigation is $BiFeO_3$ (BFO). Until now, it is utilized only as a single device. [10]. The purpose of this work is to check how it will work in a crossbar array, i.e. with patterned top and bottom electrodes.

The work has to proposed mask layout with varied crossbar array, i.e. different geometrical parameters and different number of bit-line and word-line. The design also have to be optimized for 1 x 1 cm^2 cell on 6" wafer.

The rest of this report is structuctured as follows. In Section II, The basic theories and knowledges which are related and helpful to understand the resistive switching in BFO is explained. Section III gives some information about optical mechanical pattern generator. Section IV discusses some problems of fabrication result of the bottom electrodes. The work is ended by a summary.

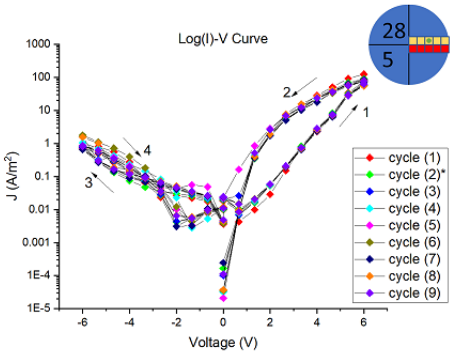


Fig. 1. wafer_28_S_5: (a) IV curve (b) Log(I)-V curve. The circles describing the sample naming convention used in this work is a courtesy of A. Aleisa/D.Bürger.

II. Resistive Swicthing in BFO

The switching mechanism in BFO memristors is shortly discussed here. The plot of IV characteristics and all derivatives are taken from one samples: wafer_28_S_5_2_20_30mm (wafer_28_S_5). Figure 1 show the IV curve of wafer_28_S_5.

The mechanism of the resistive switching behavior can be understood easier if we keep the understanding of Schottky contact in mind. When BFO makes contact with the top electrodes made of Au, the electrons from the BFO will move to Au layer to make the Fermi level flat. This will produce ionized area under the Schottky contact in the BFO layer. On the other side, the bottom interface is Ohmic type. The detail mechanism of the switching is discussed in [13]. The proposed mechanism is the electron trapping/detrapping mechanism which explain how the space charge region shifts due to the reduction(oxidation) process on Fe^{3+}(Fe^{2+}) ions.

Another possible switching mechanism based on the OV (Oxygen Vacancy) movement during writing bias was suggested in [14]. This mechanism suggests that the migration of OV changes the barrier height and contact type of the bottom interface [14]. The non-volatility is caused by the trapped mobile ion among immobile Ti^{4+} donors [14]. Figure 2 describes this mechanism. In forward bias, the OV is pushed toward the bottom interface leaving the top interface with higher barrier height. Due to the increase of the donor

concentration around the bottom interface, the potential barrier at the bottom contact decreases. The device is in LRS now. After losing the bias, the OV will stay put because they are trapped by the potential from the Ti^{4+} ions and only the electric field from the writing voltage is strong enough to move these OVs. During the reverse bias, the OVs will drift closer to the top electrode lowering the barrier height of the top interface. The top and bottom interface will act like two rectifying diode with BFO layer as their cathode. The barrier height of the top contact is higher than the one at the bottom.

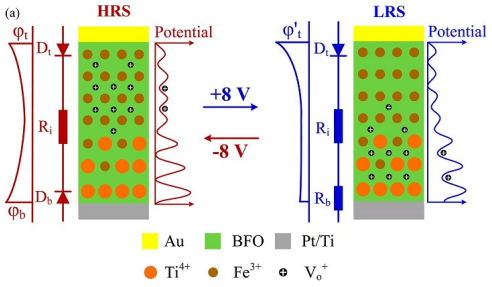


Fig. 2. Switching mechanism of the BFO memristor. Reprinted with permission from (ACS Appl. Mater. Interfaces 2014, 6, 22, 19758-19765). Copyright (2014) American Chemical Society. [14]

The memristor in Au/BFO/Pt/Ti/SiO_2/Si structure has following characteristics: self-select [15], eightwise [13], asymmetric (rectifying) [13] [15], bipolar [13], nonlinear *IV* characteristic [13], nonvolatile [13] [14], multilevel resistive switching possible [15] [14].

III. Crossbar Layout and Optical Mechanical Pattern Generator

Figure 3 shows the layout of 3 x 3 crossbar. The layout of crossbars with other sizes (e.g., 1 x 1, 6 x 6, 10 x 10) have also been made with the LayoutEditor. All of these crossbar are planned to be patterned on a single wafer. A macro has been written to generate the layouts so some parameters (e.g., track distance and width, pad size, etc.) of the layout can be easily changed. This layouts are later translated into a pattern generator file by the optical mechanical pattern generator.

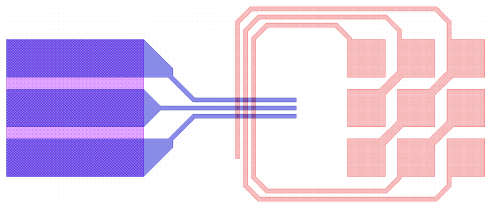
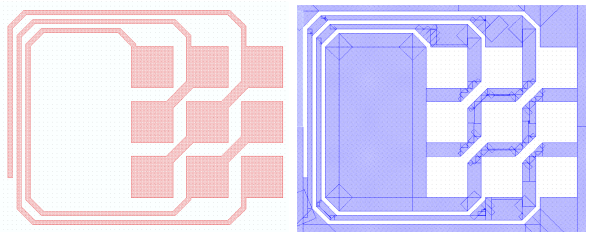


Fig. 3. The layout of 3 x 3 Crossbar.

The optical mechanical pattern generator transfers the layout by exposing the photoresist on the blank reticle repetitively with the light source which have been shaped into a smaller structure like rectangular. This repetition makes the final result consists of many smaller patches. Figure 4b shows an example of a pattern generator file. It can be seen how it build a larger pattern from many small patterns if it is not possible to form such large pattern from single large block.



(a) (b)

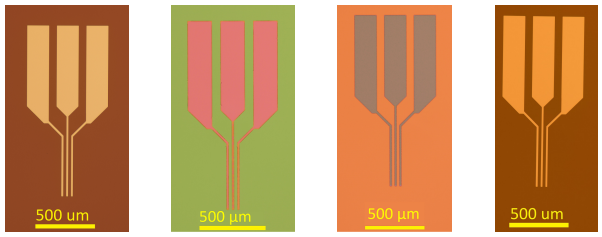
Fig. 4. (a) Layout of top electrode of 3 x 3 crossbar made using LayoutEditor. (b) Part of pattern generator file for (a) received from Nanostructuring Department of Fraunhofer ENAS. The pattern generator file is a courtesy of M. Pleuel/J. Wienandt. [16]

IV. Pattern Generation for the Mask and Fabricated Bottom Electrode

The process for the final mask fabrication was done involving persons in charge both from the mask fabrication and process technology. The pattern generation file need to be checked for the last confirmation before mask fabrication. For this, a macro was made to detect and locate unwanted artifacts on the pattern generator file.

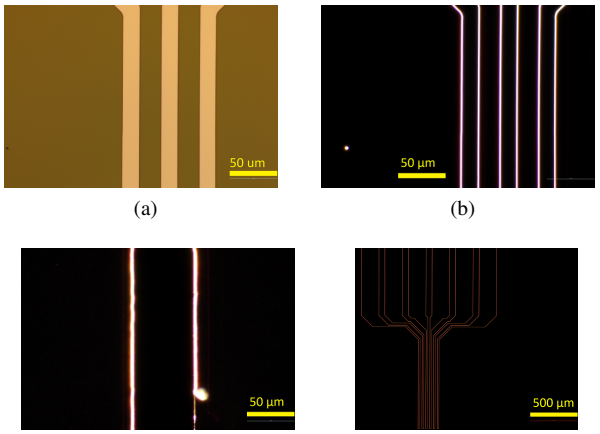
For the layouts designed in this work, the fabricated bottom electrode have been received. Wafer 01 and wafer 20 have considerably good result, while wafer 02 and wafer 19 have some problems. Figure 5 shows the fabricated bottom electrodes (BE) of the crossbar (XB) of 3 x 3. Actually, wafer 01 also has an issue which is an unwanted artifact, even though the structure of interest looks good. From those pictures, it might be a little bit difficult to see the bad structure edges on the wafer 02 and wafer 19. Dark field microscopy makes this edge detection easy by utilizing the optical path length difference between structures with different height. The result of this techniques can be seen in Figure 6. Dark field images give high contrast images which are beneficial during topography analysis. As mentioned before, the fabricated bottom electrodes from wafer 01 has one small artifact which shown in 6a. It might be dust or other small residue. For this instance, it still can be seen easily but still dark field microscopy can make it easier to detect level differences as shown in 6b. For the case of bad edge like in Figure 6c, it is much more difficult to gauge the patterning quality if we depend only on bright field image (not shown). This is when dark field technique is really helpful. Figure 6d shows an example of a good patterning result seen by dark field technique.

In addition to two issue above, there is another one which are experienced by all four wafers. The problem is the metal tracks are over etched laterally. The metal tracks are designed to have 20 µm width and 20 µm distance between tracks while the patterning result shows the width is 16.76 µm. This is shown in Figure 7. Simple calculation can show that the underetch is about 1.77 µm. This value is too large considering the total thickness is only 180 nm (Ti: 30 nm, Pt: 150 nm). So it is less probable to be the cause of this issue. Two other potential reason are (1) the resist was not cured and developed properly and (2) the mask has wrong dimensions, considering it happens in all four wafers. Usually, there is one step that



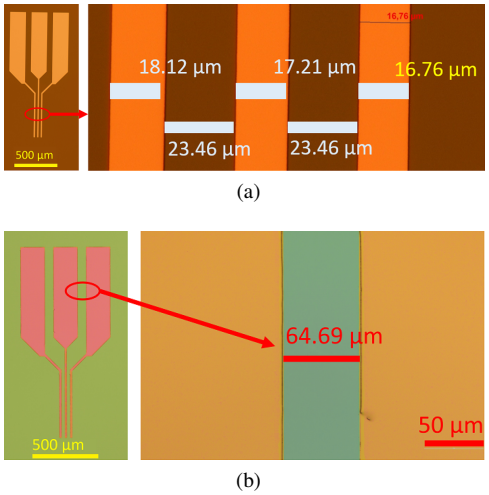
(a) (b) (c) (d)

Fig. 5. The fabricated bottom electrodes from wafer (a) 1, (b) 2, (c) 19, (d) 20, respectively. It might be a little bit difficult to see the bad structure edges on wafer 02 and wafer 19. In case of printing problem, the scale bar shown in each picture is 500 µm.



(a) (b) (c) (d)

Fig. 6. (a) The fabricated bottom electrodes from wafer 01 which shows one small artifact. (b) The dark field image of (a) shows more contrast to detect the artifact. (c) Wafer 02 shows bad structure edge which detected in its dark field image. Wafer 20 have shows good patterning result of the bottom electrode. Its dark field image is shown in (d).



(a)

(b)

Fig. 7. The lateral over etched issue on wafer 20 and wafer 2. (a) The lateral over etched issue on wafer 20 around the crossbar track area. The length of all short and long scale bars are 16.76 µm and 23.46 µm. It can be seen that the (widest) track on the most left position is wider than the track on the most right while the width of the middle track is between those two values. The distance between tracks in the layout is 20 µm while in the fabricated bottom electrode of 3 x 3 crossbar is 23.25 µm and 23.40 µm. (b) The lateral over etched issue on wafer 2 around the area between pads. The pad distance in the layout is 60 µm while in the fabricated bottom electrode is 64.69 µm. On both (a) and (b), (1) the full bottom electrode pictures and red circles are used just to help us get the bigger picture of the area of interest e.g., pad distance area and track distance area, not necessarily give us the information about the exact location of the problem shown like in the enlarged versions of the pictures. So, the information on the enlarged pictures on the right does not necessarily originated from the instances of the bottom electrodes shown in the full bottom electrode pictures on the left. (2) The original scale bars are the ones which length of 16.76 µm, 50 µm, and 500 µm. The other scale bars and length information are obtained through scaling.

bridges between layout making and mask fabrication. Depend on the technology and maybe working flow, this step might deal with ensuring the pattern on the wafer to resemblance the layout as much as possible, i.e., by implementing optical proximity correction (OPC) and design for manufacturability (DFM) techniques to suppress variations. But for 40 µm pitch, the issue of lacking of these DFM techniques seems less relevant. So, as long as the masks have correct dimensions, most probably they do, potential reason (2) is almost not possible to happen. This left us with potential reason number (1) but, still, without more information or effort, e.g., measuring the mask, measuring the patterned resist before and after etching, etc., the main reason for this problem is hard to be determined.

V. Summary

A design of crossbar layout has been suggested in this work in order to investigate the resistive switching behavior of the $BiFeO_3$ (BFO) when it is assembled into a crossbar, i.e., with patterned top and bottom electrodes. The layout is parameterized so it can stand some design changes to a certain extent.

For the layouts designed in this work, the fabricated bottom electrodes have been received. The dark field microscopy is used for topography analysis in addition to bright field technique. Wafer 01 and wafer 20 have considerably good result, while wafer 02 and wafer 19 have some problems. In addition of bad structure edges on wafer 02 and wafer 19, all wafers experience over etch-like problem laterally.

Underetch is probably not the reason for this issue because the underetch value (1.77 µm) is too large for the films thickness of 180 nm in total. Two other potential reason are (1) the resist was not cured and developed properly and (2) the mask has wrong dimensions, considering it happens in all four wafers. However, without more information or effort, e.g., etching selectivity information, measuring the mask, measuring the patterned resist before and after etching, etc., the main reason for this problem is hard to be determined.

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