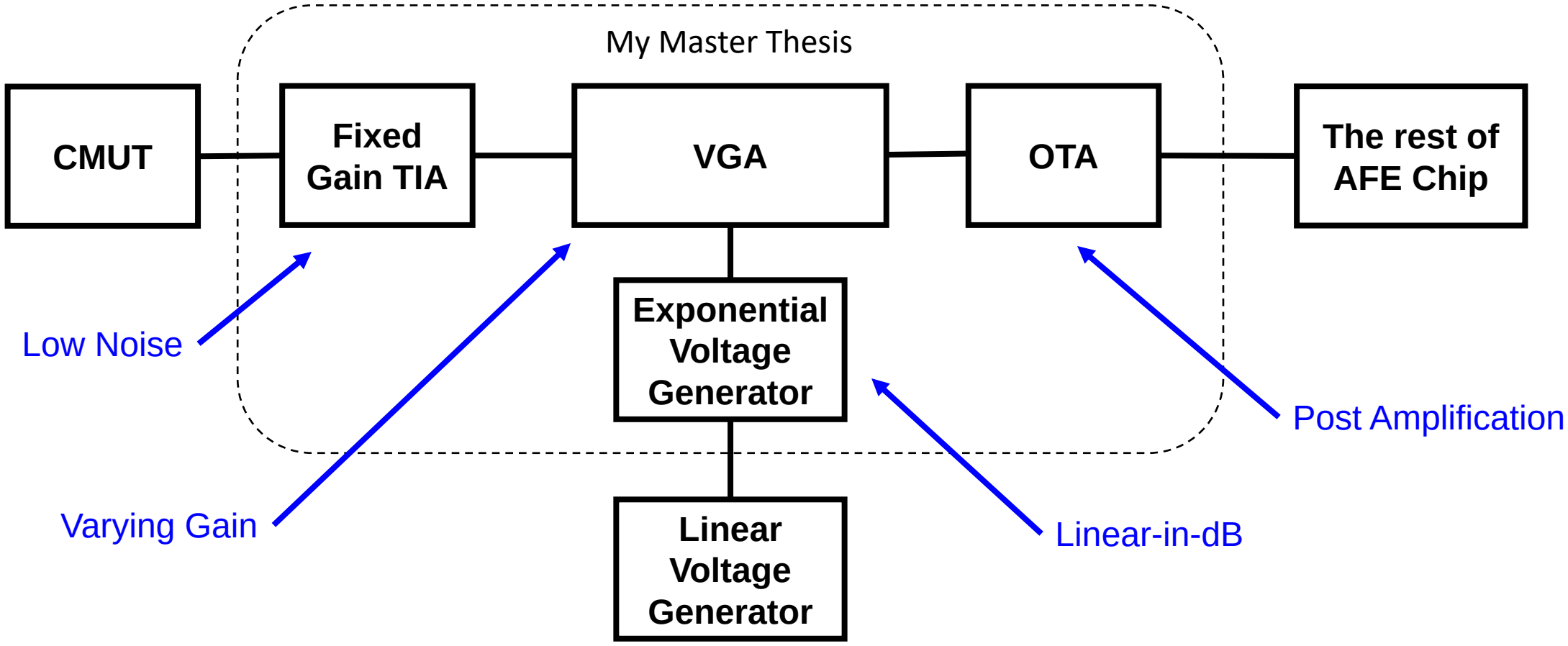
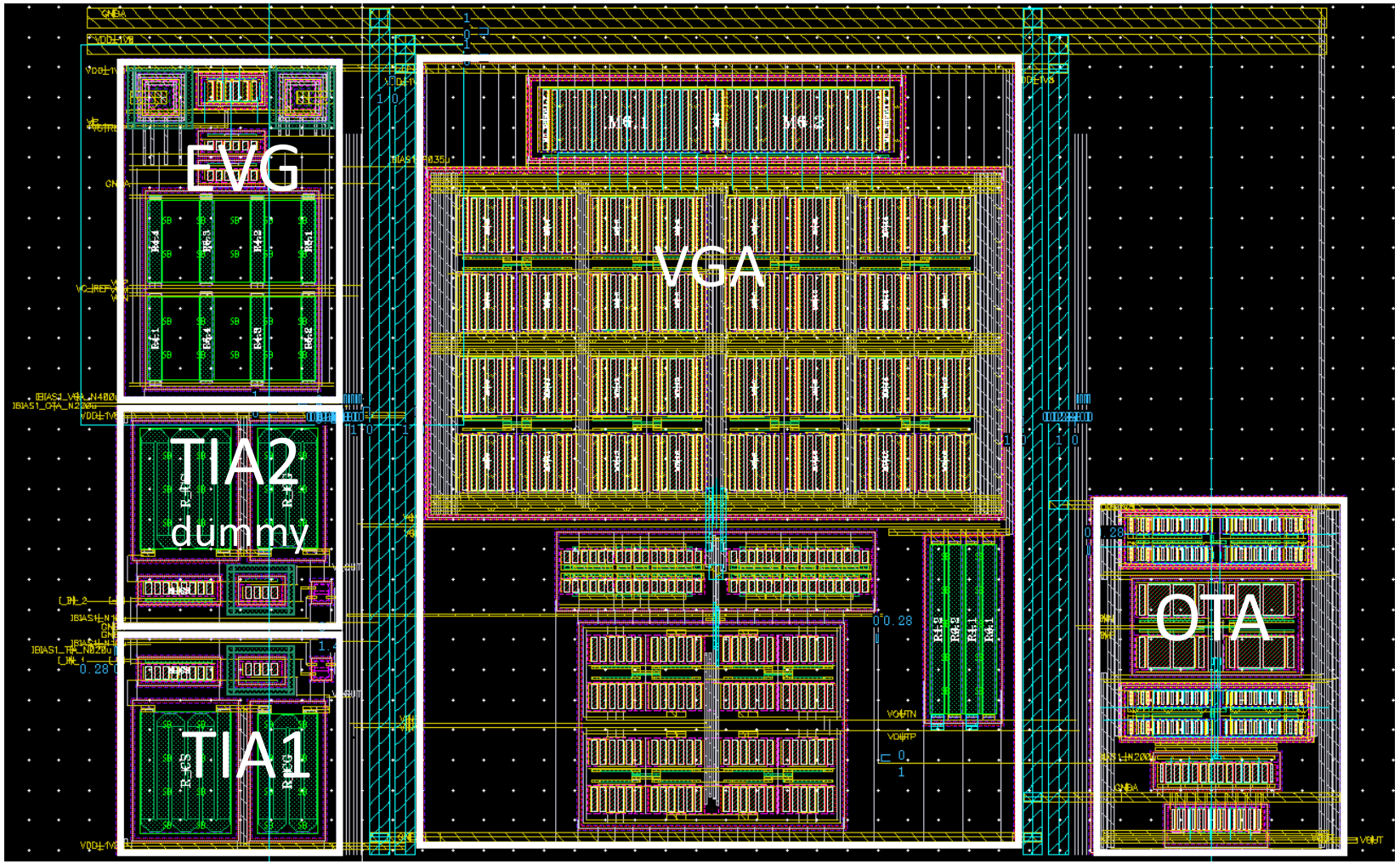
Top Level Circuit : Time Gain Compensation (TGC) Transimpedance Amplifier

Proposed Block Diagram



More simulation results and topology reviews will be included after my thesis defense at the university.

Top Level Circuit : Time Gain Compensation (TGC) Transimpedance Amplifier



The project is realized using 0.18 µm Silicon on Insulator (SOI) process technology from X-FAB.
The simulation is done using Spectre in the Cadence Virtuoso with BSIM4v4.70 as the transistor model.

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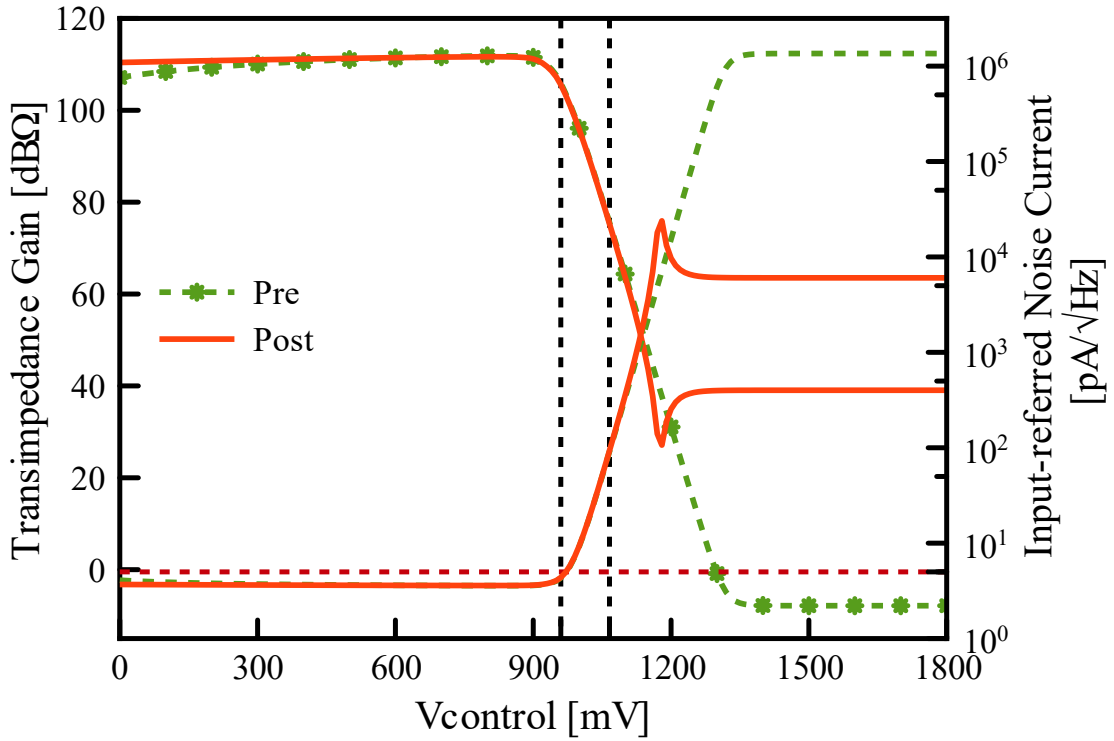
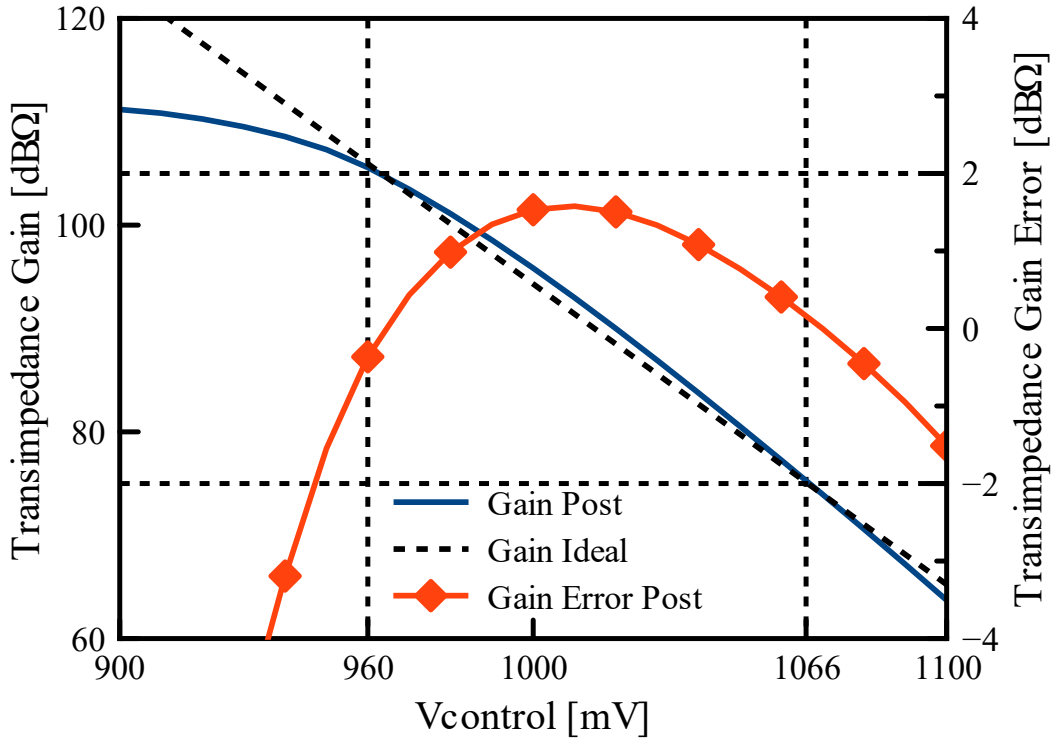
Parameter	Unit	Target	This work	[3]	[40]	[41]
Gain Range	[dBΩ]	≥ 30	30	33	18	36
Maximum Gain	[dBΩ]	≥ 106	108	107	97	41.6
Gain Error	[dBΩ]	-	±2	±1	-	±0.5
Gain Control Type	[-]	-	Analog	Analog	Discrete	Discrete
Control Voltage Range	[mV]	-	960 – 1066	800	-	-
3dB Bandwidth	[MHz]	≥ 5	5	7	7.5	10-25
Input-referred Current Noise @5MHz	[pA/√Hz]	≤ 5	4.5 - 99	1.7	4.8	-
Transducer Capacitance	[pF]	10	10	15	5.5	-
Load Capacitance	[pF]	5	2*	1.7	-	-
Power Consumption	[mW]	≤ 6	5.35	5.2	0.18	3.6
Area	[μm^2]	-	210 x 141	400 x 400	76 x 50	320000
Process Technology	-	0.18 µm SOI	0.18 µm SOI	0.18 µm	65 nm	0.18 µm

[3] 10.1109/ISSCC19947.2020.9063052
[40] 10.1109/TBCAS.2017.2716836
[41] 10.1109/VLSID49098.2020.00034

Top Level Circuit : Time Gain Compensation (TGC) Transimpedance Amplifier

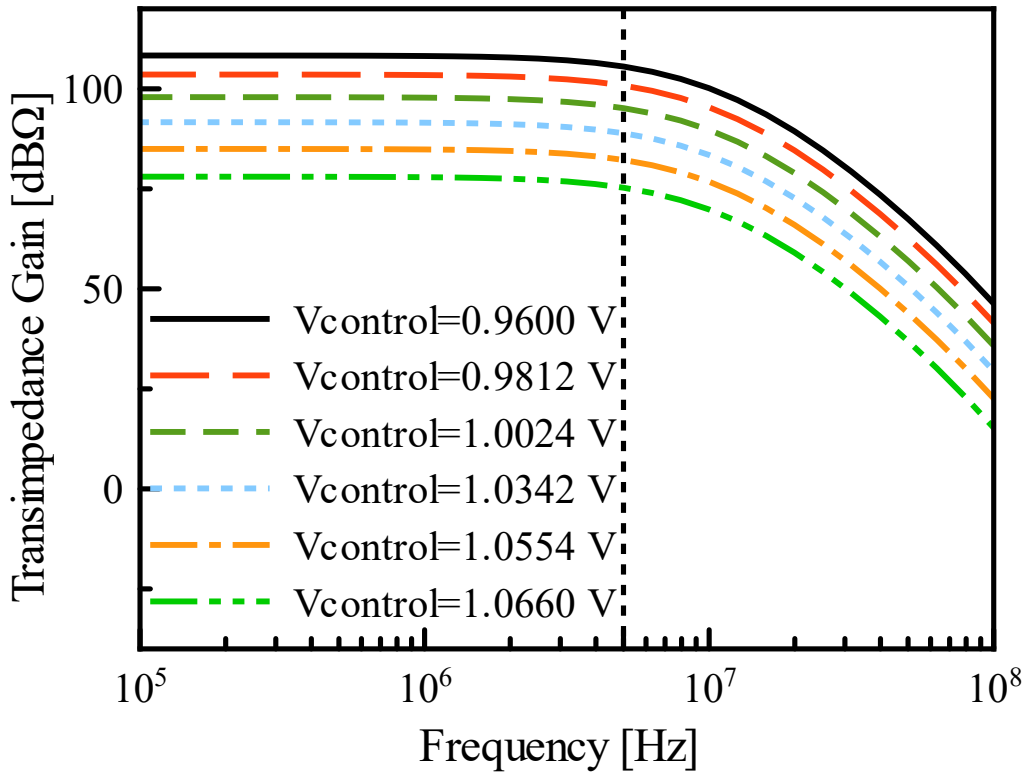
Post Layout DC Simulation

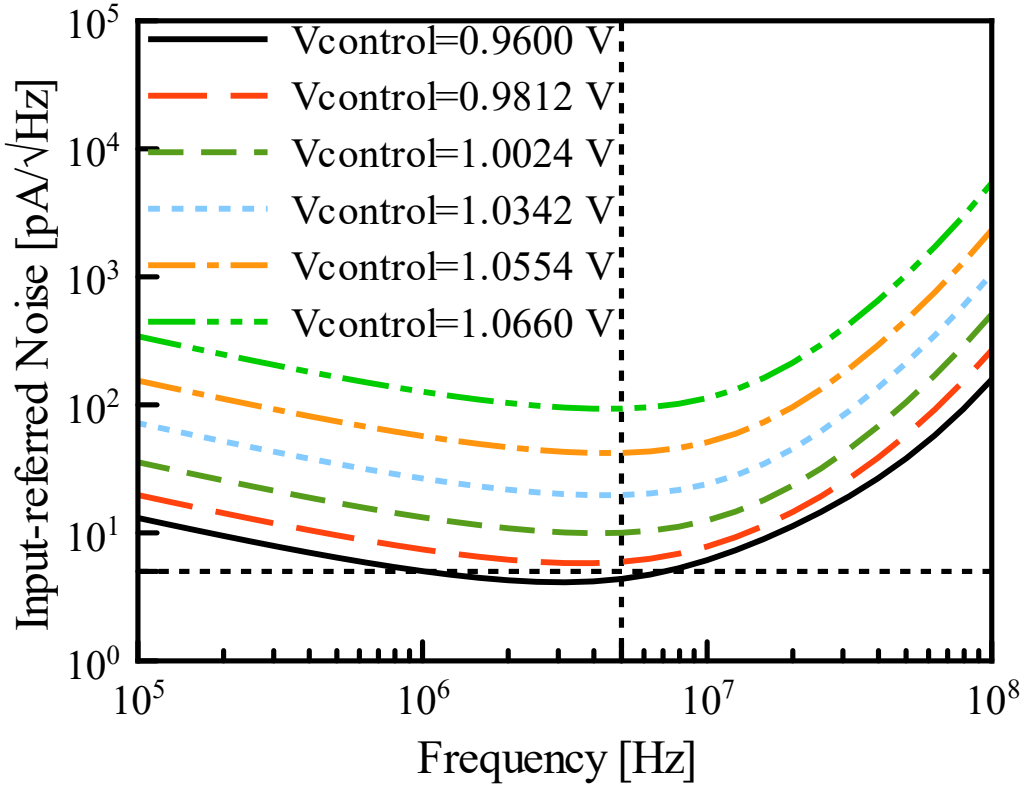




Top Level Circuit : Time Gain Compensation (TGC) Transimpedance Amplifier

Post Layout AC Simulation





Top Level Circuit : Time Gain Compensation (TGC) Transimpedance Amplifier

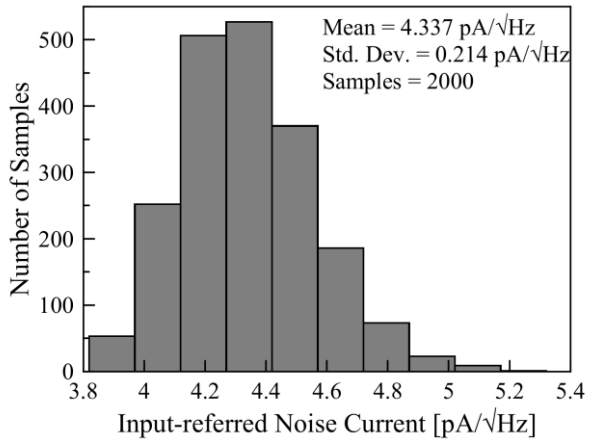
Post Layout Corner Simulation

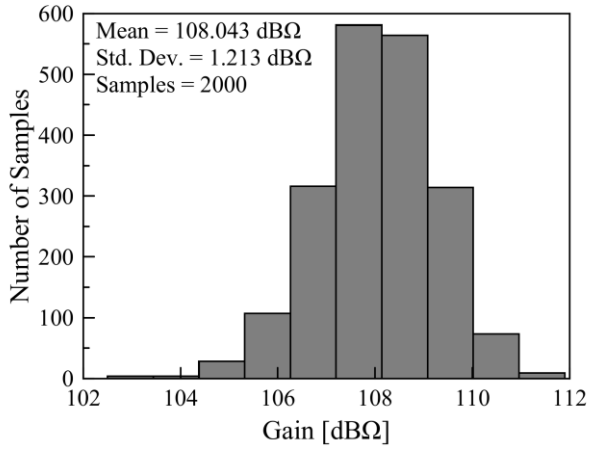
Corner	Current	Noise_@MaxGain	Noise_@MinGain	Bandwidth	Gain@10KHz	Gain Range
Unit	mA	$pA/\sqrt{Hz}$	$pA/\sqrt{Hz}$	MHz	dBΩ	dBΩ
tm	2.780	4.366	93.36	5.263	108.3	30.30
wo	2.780	4.307	92.26	5.441	108.2	30.28
wp	2.971	4.505	99.96	5.803	106.8	30.14
ws	2.618	4.420	91.30	4.788*	109.2	30.27
wz	2.780	4.440	94.72	5.087	108.4	30.31

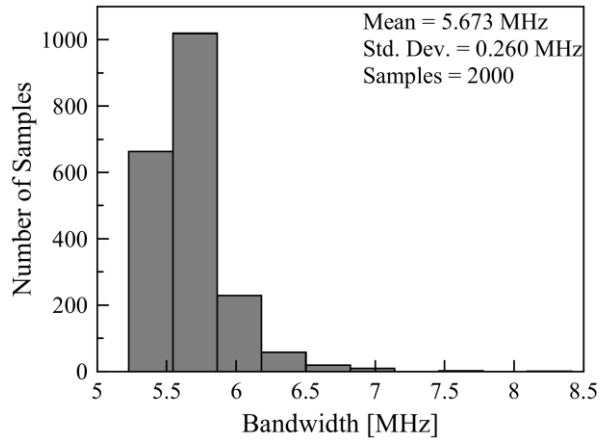
Summary of post-layout corner simulation of the top level circuit at 27 °C. Noise simulation was done at 5 MHz. * lower than the target value.

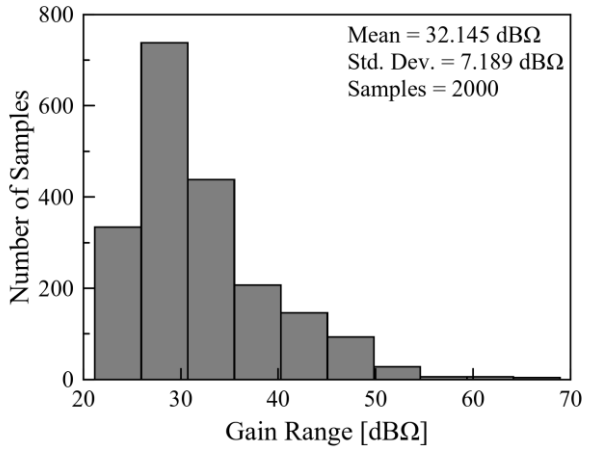
Top Level Circuit : Time Gain Compensation (TGC) Transimpedance Amplifier

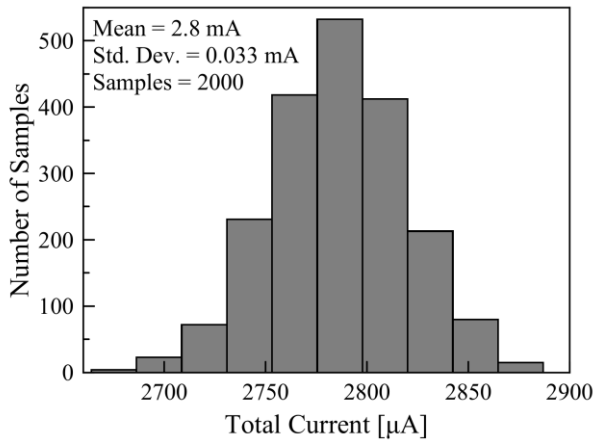
Pre Layout Monte Carlo Simulation





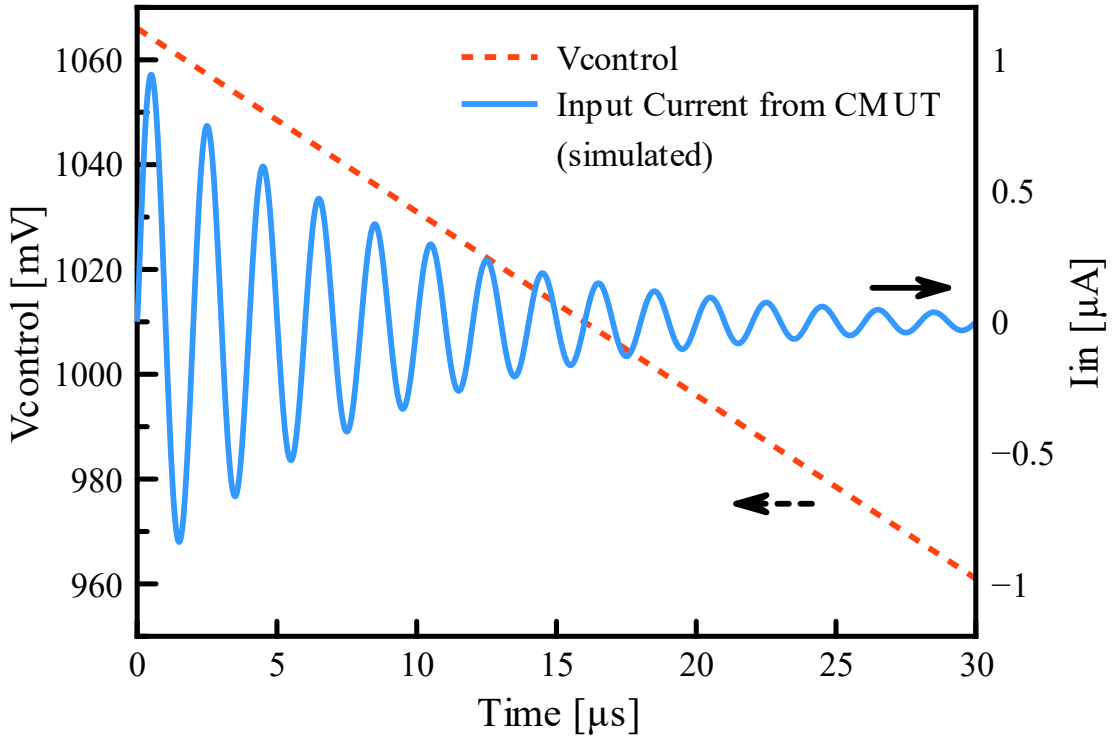


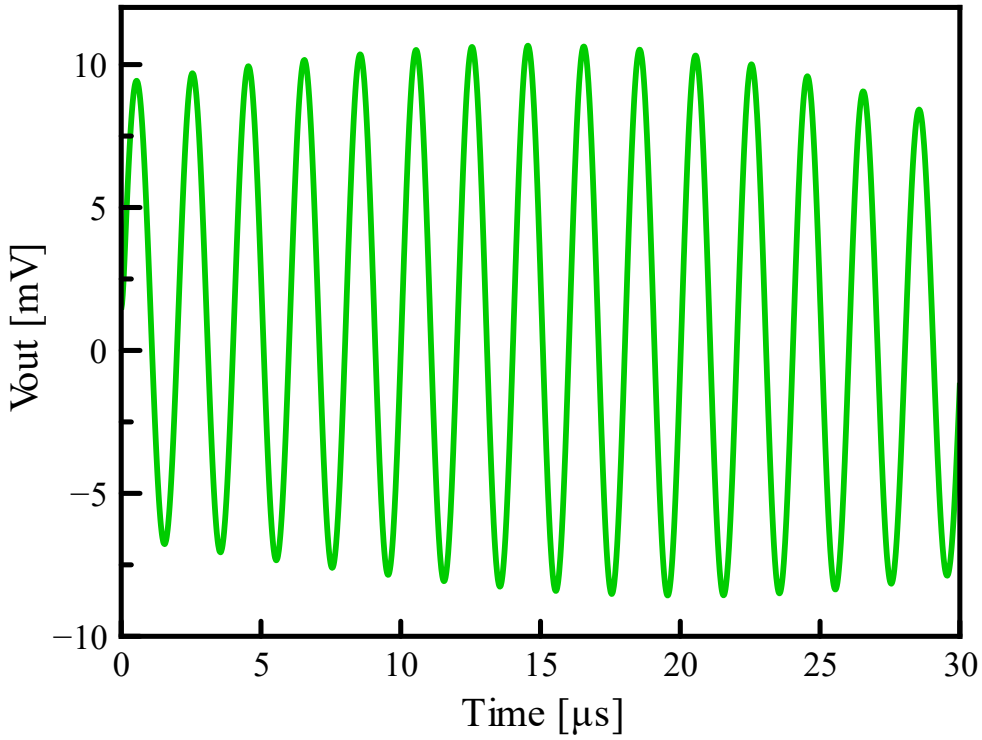




Top Level Circuit : Time Gain Compensation (TGC) Transimpedance Amplifier

Post Layout Transient Simulation





Top Level Circuit : Time Gain Compensation (TGC) Transimpedance Amplifier

Thank You!

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