Design of a Time Gain Compensation Amplifier for an Ultrasound Analog Receiver Front End Using 0.18 µm SOI Process

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- CMUT and Measurement Principle of Ultrasound Systems
- System Level Considerations
- Top Level Simulation Results
- Suggested Improvements

Capacitive Micromachined Ultrasonic Transducers

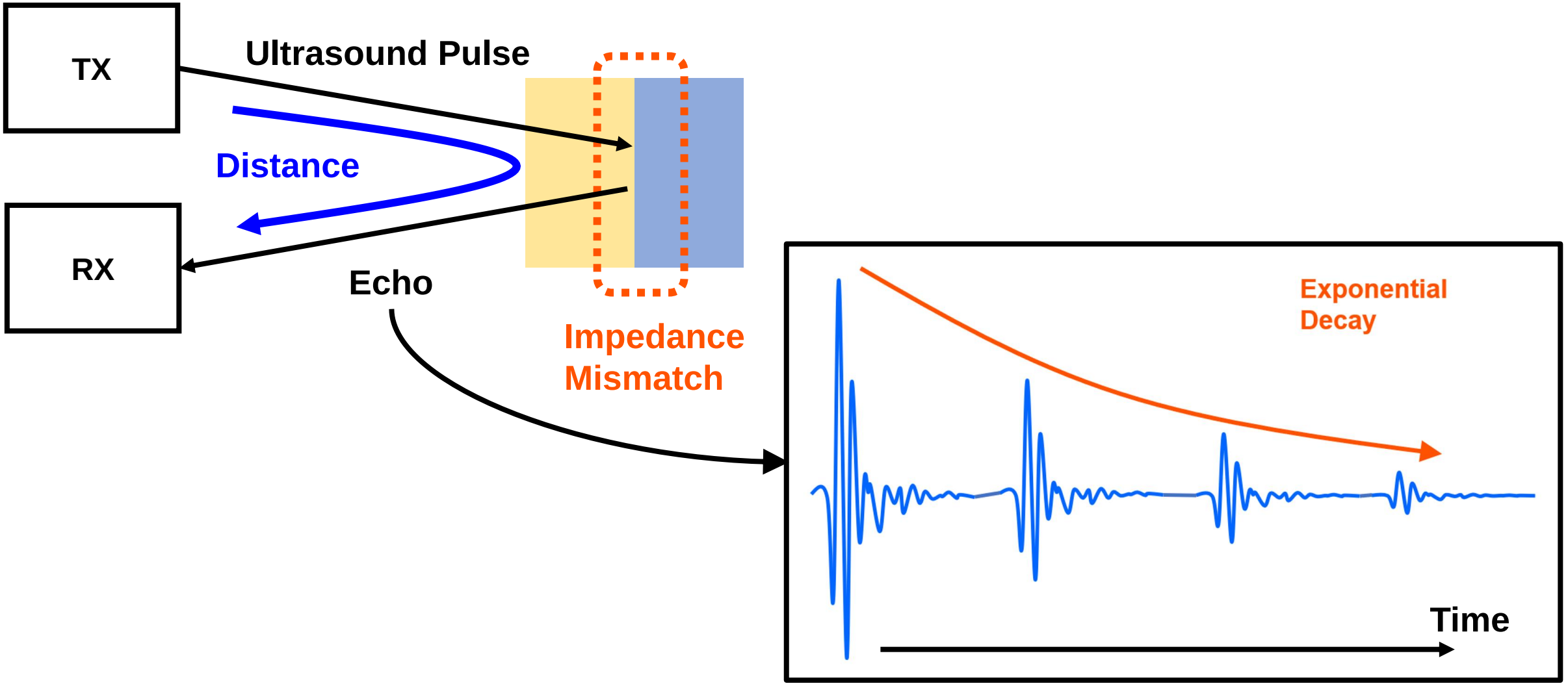
$$C = \epsilon_0 \frac{A}{d}$$

The impinging echoes change the distance

$$\frac{dCV}{dt} = C\frac{dV}{dt} + V\frac{dC}{dt} = \frac{dQ}{dt} = i_{CMUT}$$

We want to measure this.

Measurement Principle and Time-Gain Compensation



Block Diagram

Single stage, including variable gain and linear-in-dB features [1]

- **Interpolation technique**
- complex analog controller to steer the biasing current.

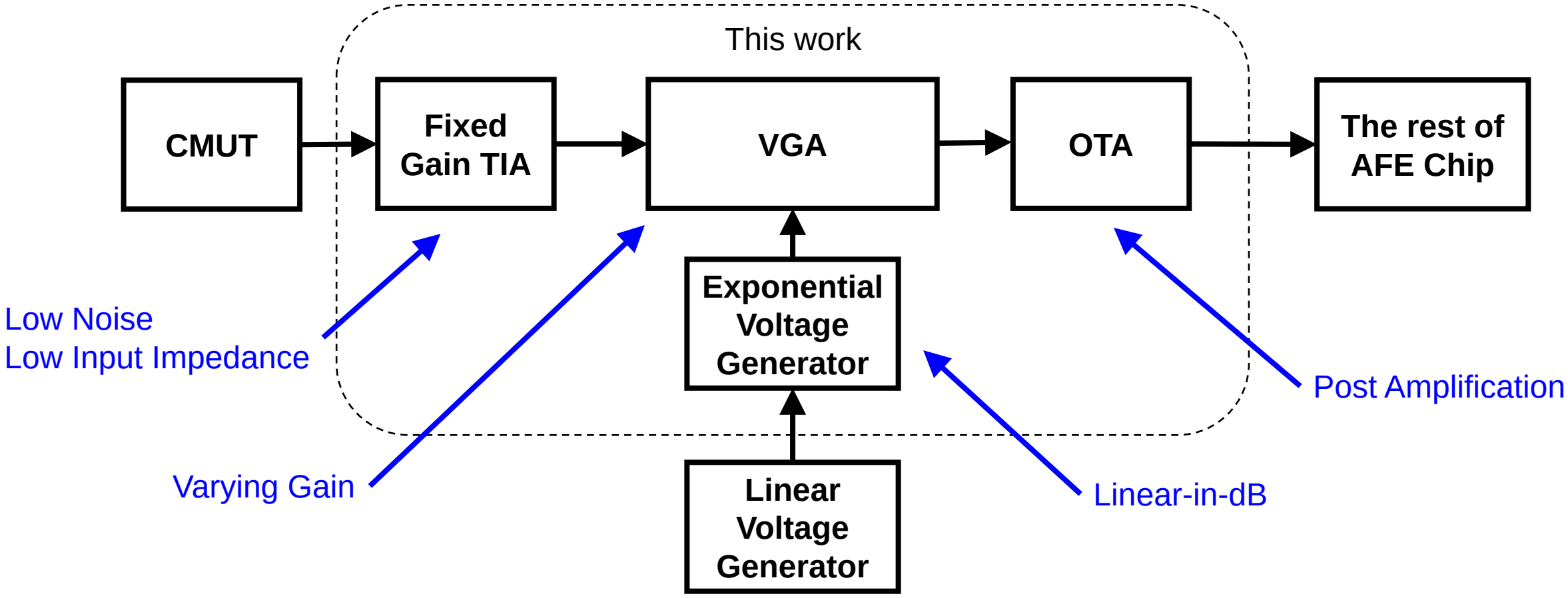
[1] 10.1109/ISSCC19947.2020.9063052

System Level Considerations

Challenges	Solutions	Circuits
Echo attenuation	Variable gain	VGA : Folded Gilbert Cell
Exponential attenuation profile	Exponential gain variation	Exponential Voltage Generator
High (output) impedance sensor	Low input impedance front end	Common gate topology (and its derivatives)
Low noise is expected	Allocate high gain at the first stage	LNA : Regulated Cascode
Low VGA gain	Post amplifier	Post Amp : Symmetrical OTA

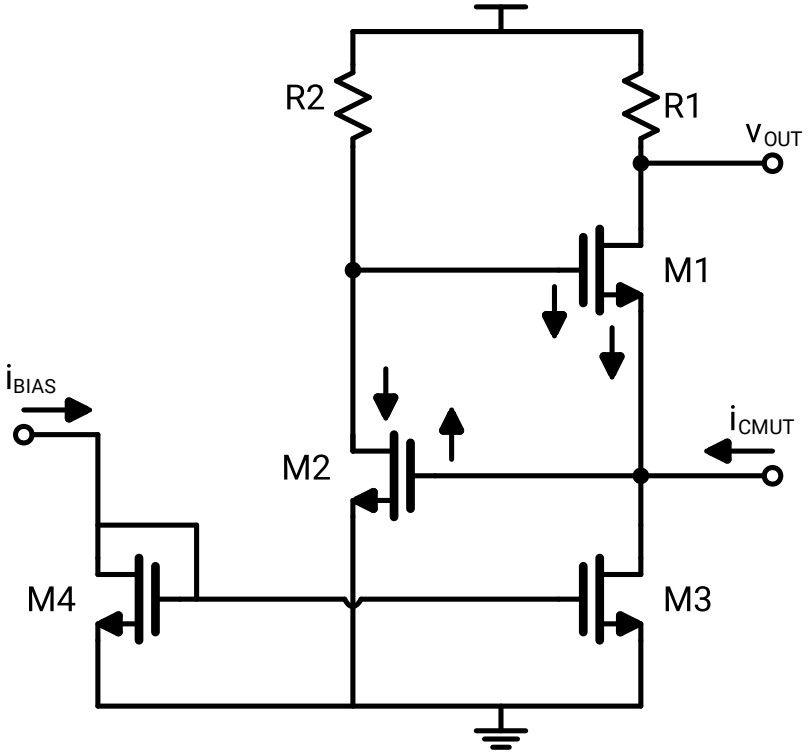
Block Diagram

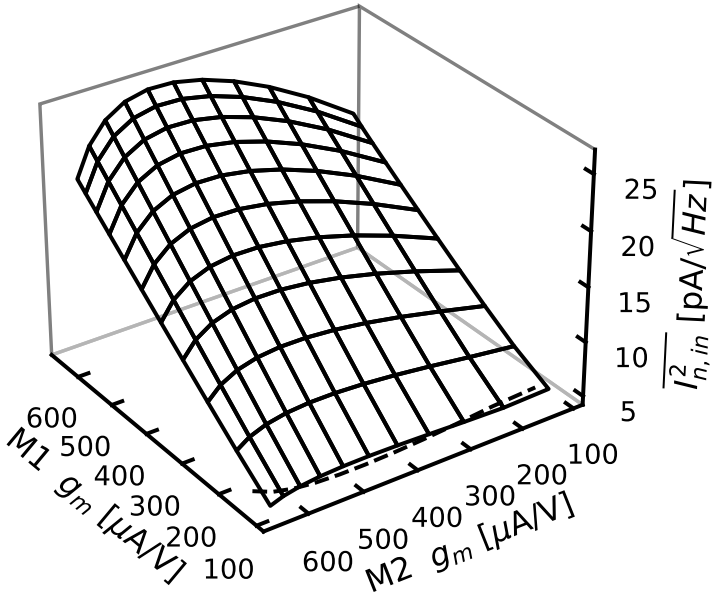
Proposed Block Diagram

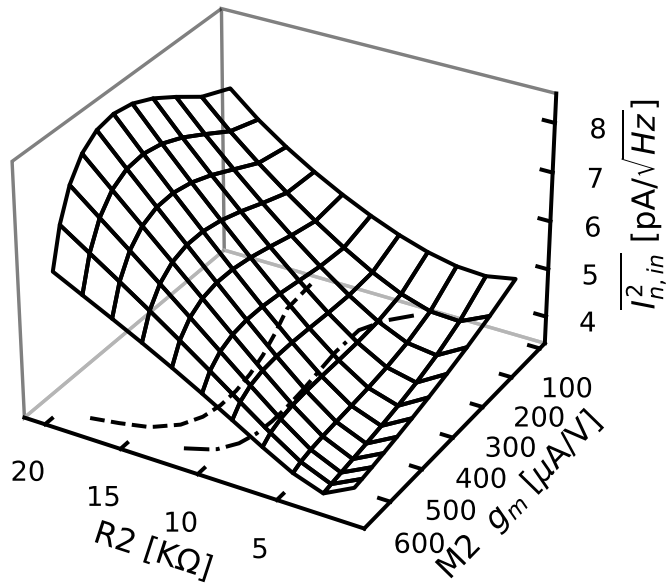


After determining the block diagram…

- Literature research for each block
- Device characterization using gm/ID method
- Detail hand calculation and circuit performance exploration, if necessary
- Complete design workflow until post layout simulation

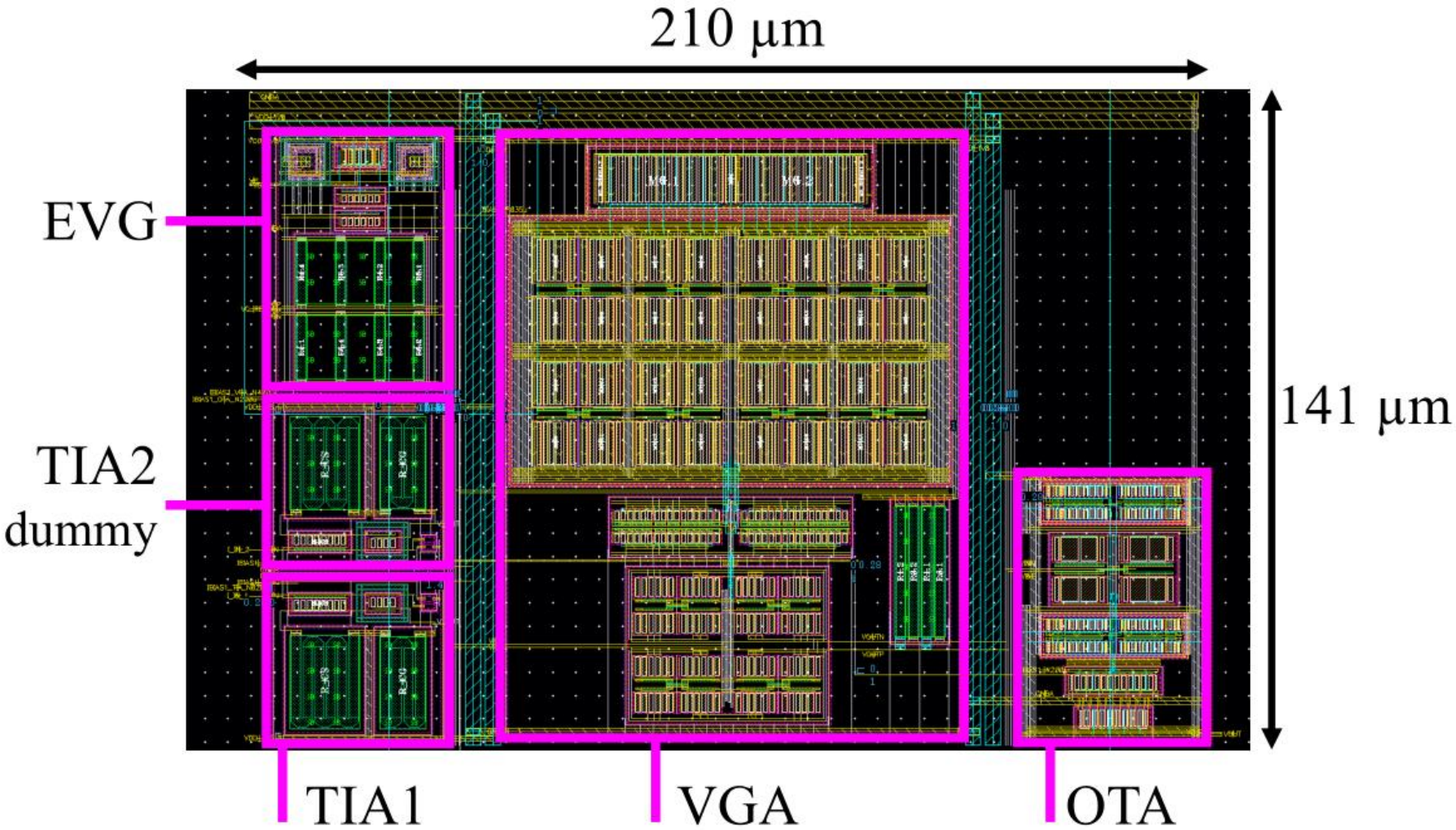






It helps me to optimize the circuit

Top Level Circuit : Time Gain Compensation (TGC) Transimpedance Amplifier

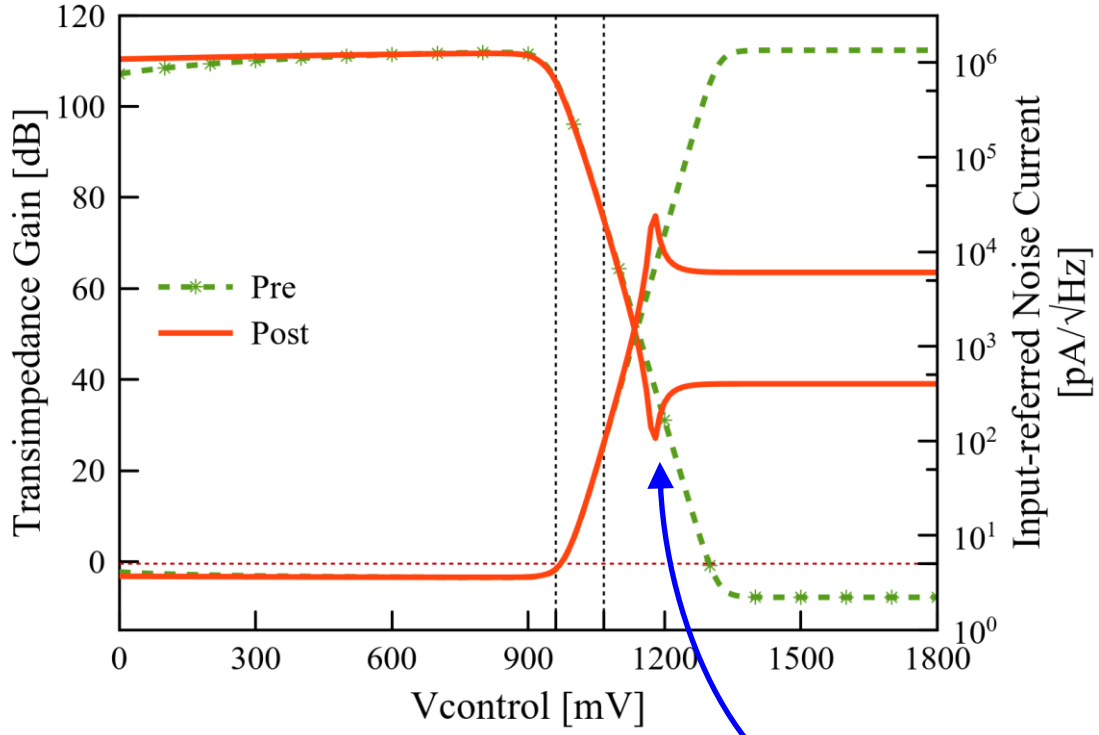


This concludes the design phase.

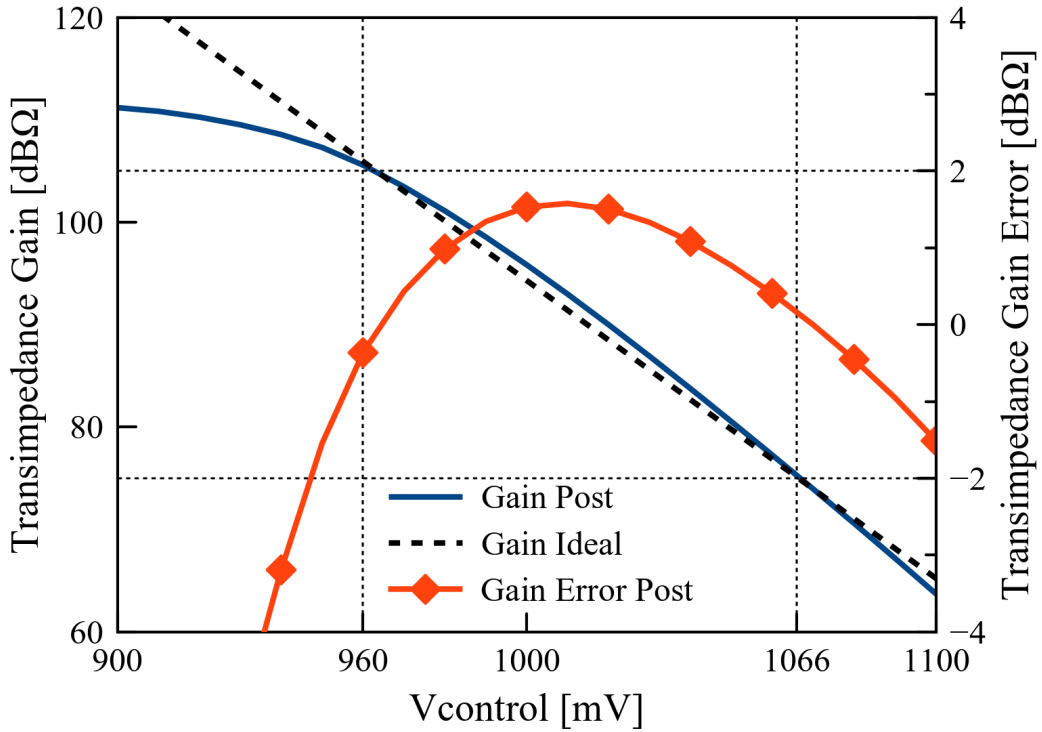
The next part will be about
the **simulation results** and **proposed improvements**.

Top Level Circuit : Time Gain Compensation (TGC) Transimpedance Amplifier

Post Layout DC Simulation

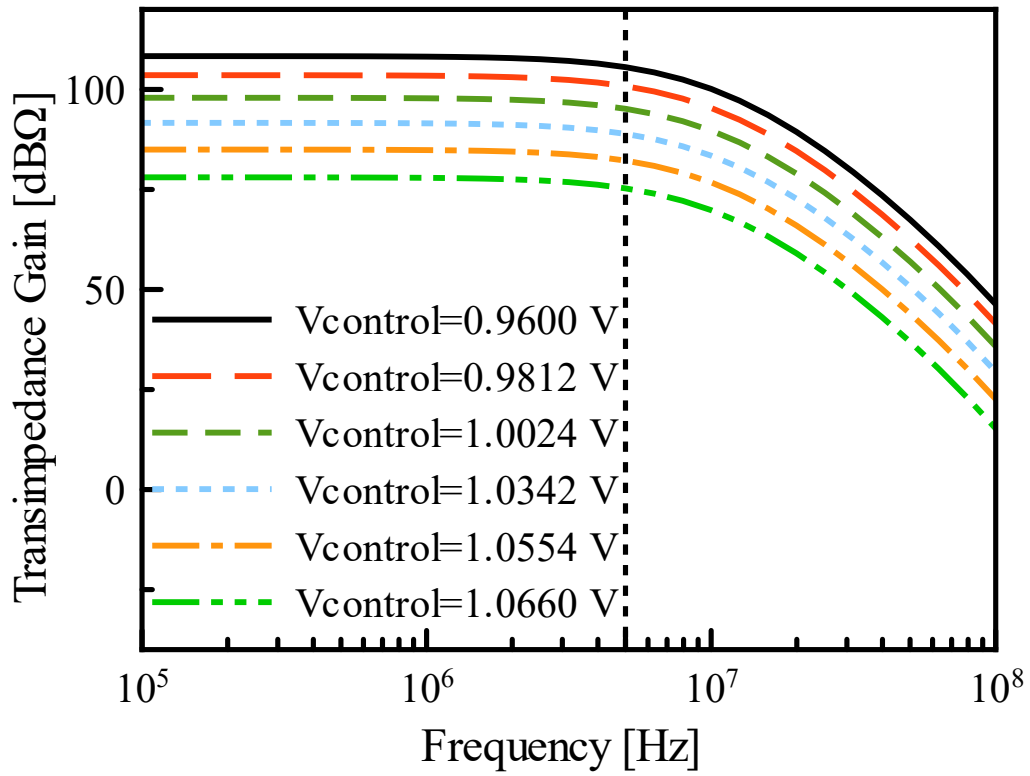


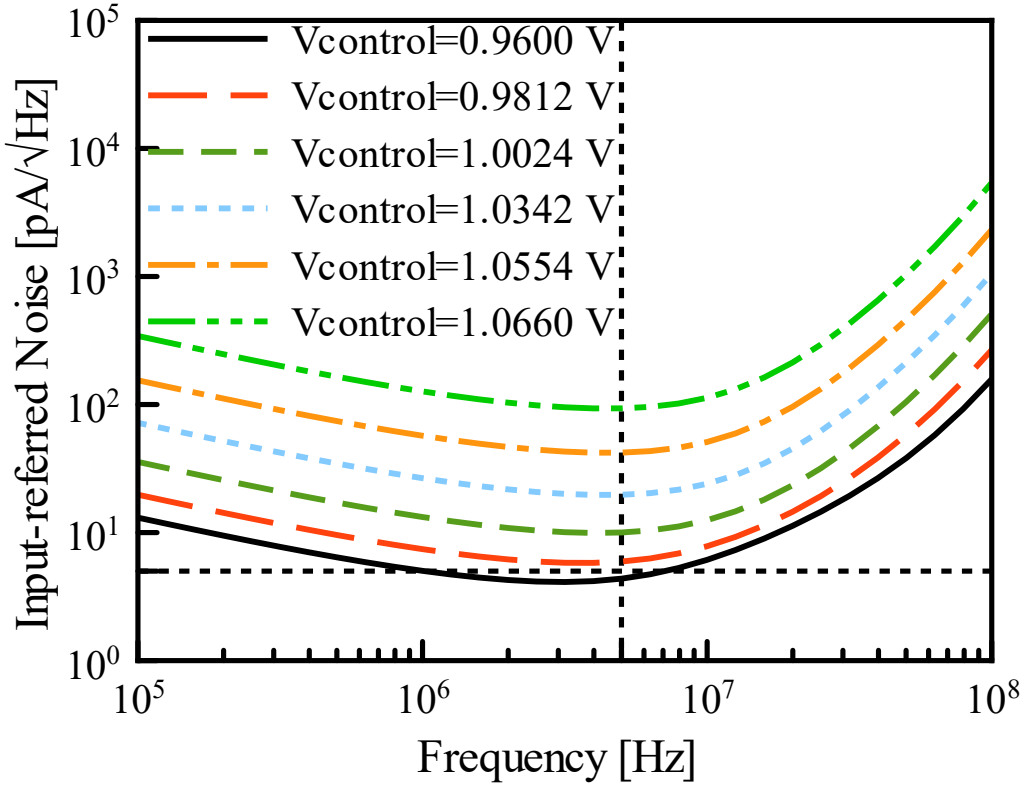
Due to parasitic components



Top Level Circuit : Time Gain Compensation (TGC) Transimpedance Amplifier

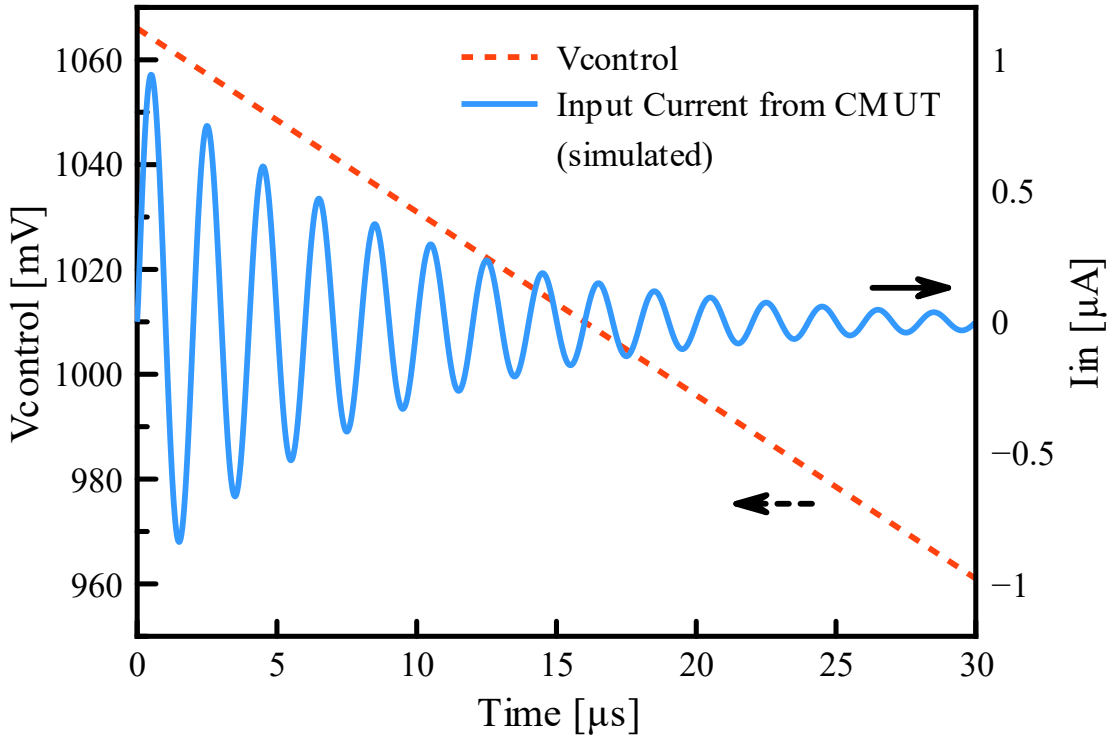
Post Layout AC Simulation

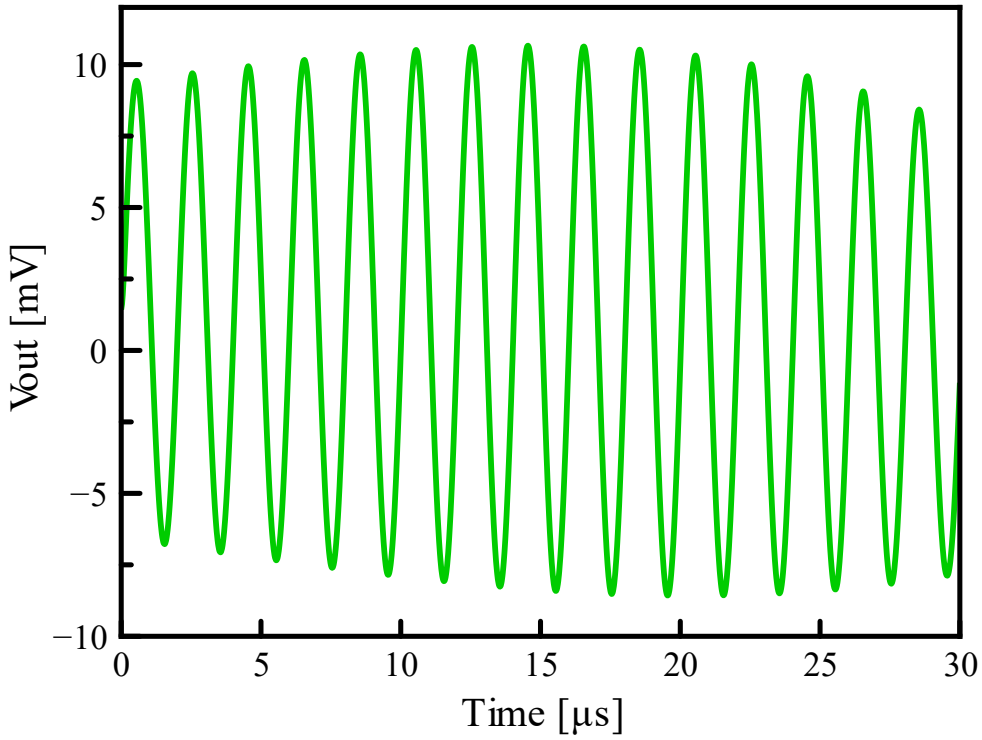




Top Level Circuit : Time Gain Compensation (TGC) Transimpedance Amplifier

Post Layout Transient Simulation



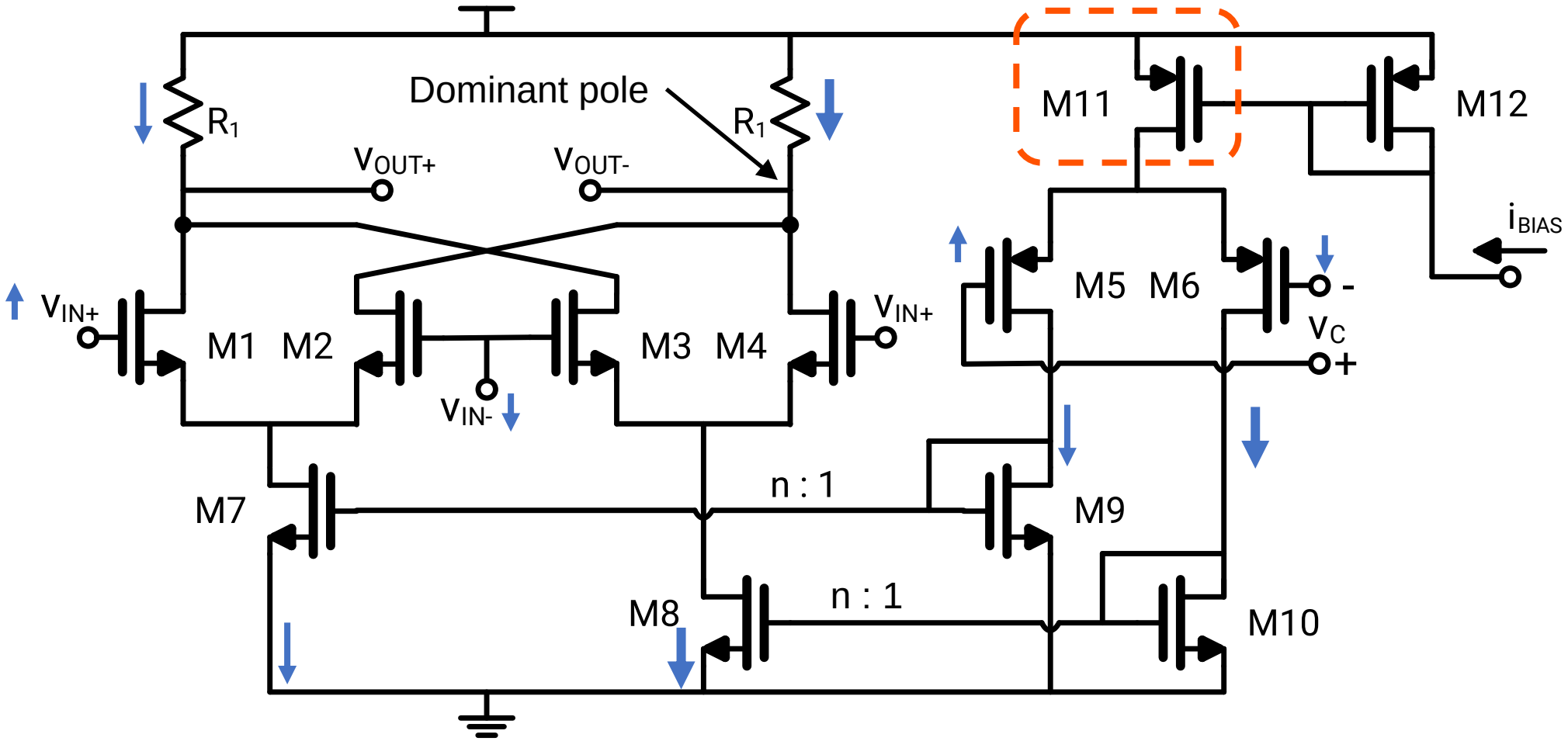


Top Level Circuit : Time Gain Compensation (TGC) Transimpedance Amplifier

Parameter	Unit	Target	This work	ISSCC2020 [3]	TBCAS2017 [40]	VLSID2020 [41]
Gain Range	[dBΩ]	≥ 30	30	33	18	36
Maximum Gain	[dBΩ]	≥ 106	108	107	97	41.6
Gain Error	[dBΩ]	-	±2	±1	-	±0.5
Gain Control Type	[-]	-	Analog	Analog	Discrete	Discrete
Control Voltage Range	[mV]	-	960 – 1066	800	-	-
3dB Bandwidth	[MHz]	≥ 5	5	7	7.5	10-25
Input-referred Current Noise @5MHz	[pA/√Hz]	≤ 5	4.5 - 99	1.7	4.8	-
Transducer Capacitance	[pF]	10	10	15	5.5	-
Load Capacitance	[pF]	5	2*	1.7	-	-
Power Consumption	[mW]	≤ 6	5.35	5.2	0.18	3.6
Area	[μm^2]	-	210 x 141	400 x 400	76 x 50	320000
Process Technology	-	0.18 µm SOI	0.18 µm SOI	0.18 µm	65 nm	0.18 µm

[3] 10.1109/ISSCC19947.2020.9063052
[40] 10.1109/TBCAS.2017.2716836
[41] 10.1109/VLSID49098.2020.00034

Suggested Improvement #1 : Reduce Bias Current on M11



Suggested Improvement #2 : Use PMOS input for the Symmetrical OTA

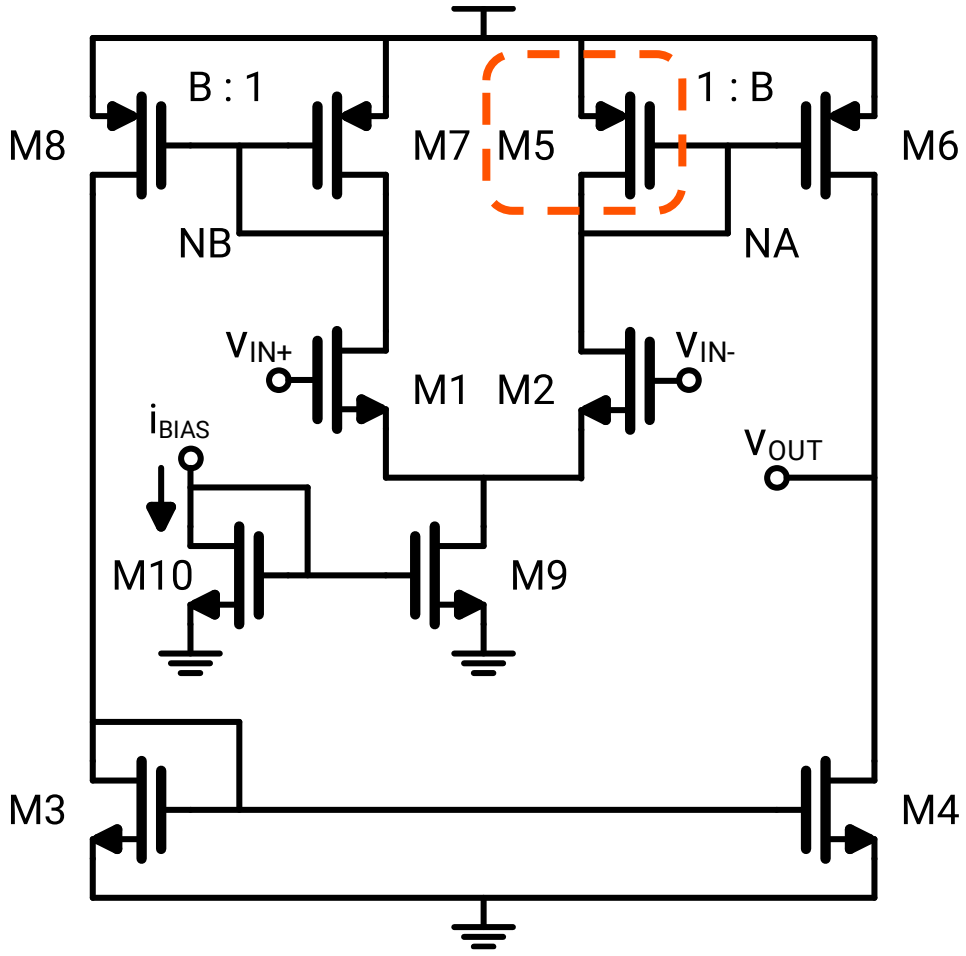
Post Layout Corner Simulation of the Top Level Circuit

Corner	Current	Noise_@MaxGain	Noise_@MinGain	Bandwidth	Gain_@10KHz	Gain Range
Unit	[mA]	[pA/√Hz]	[pA/√Hz]	[MHz]	[dBΩ]	[dBΩ]
tm	2.780	4.366	93.36	5.263	108.3	30.30
wo	2.780	4.307	92.26	5.441	108.2	30.28
wp	2.971	4.505	99.96	5.803	106.8	30.14
ws	2.618	4.420	91.30	4.788*	109.2	30.27
wz	2.780	4.440	94.72	5.087	108.4	30.31

The noise was evaluated at 5 MHz.

* Lower than the target value.

Suggested Improvement #2 : Use PMOS input for the Symmetrical OTA



In addition to suggestion #1 to improve bandwidth, we also need to increase **second** pole frequency.

$$f_{2p} \approx \frac{f_{T5}}{B+3} = 3 \times GBW$$

$$f_{T_{\mathrm{PMOS}}} \approx \frac{1}{5} \times f_{T_{\mathrm{NMOS}}}$$

Thank You!