Switchable Counter & Variable Pulse Generator

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Abstract— This document presents the design, simulation, and implementation of a digital system composed of a switchable counter and a variable pulse generator. The project incorporates two distinct 1-bit data generators operating at different frequencies, a 2-by-2 CMOS-configured multiplexer, and a duty-cycle-variable pulse generator synchronized with a user-defined control logic. Additionally, the system features a multivibrator-based clock generator, a frequency divider, and a control mechanism that toggles between counting modes and pulse duty configurations.

The switchable counter receives a selected clock input and increments its value either by 1 or 2 depending on the control signal, displaying the result on a two-digit 7-segment display. The duty-cycle controller adjusts the pulse width of the output waveform dynamically, ranging from 0% to 50%, based on analog control input.

Key challenges addressed include the stable generation of clock signals, design of a CMOS-level multiplexer for signal routing, and synchronization of sequential logic components under variable clock conditions. The project demonstrates an integrated approach to digital system design by aligning low-level circuit construction with high-level timing and control strategies.

Keywords—component, formatting, style, styling, insert (key words)

I. Introduction

In the field of digital system design, the creation of modular and configurable logic circuits is fundamental to advancing applications in timing control, signal modulation, and automated counting systems. This project focuses on the design, simulation, and implementation of a fully functional digital system combining a switchable binary-coded decimal (BCD) counter and a duty-cycle-variable pulse generator. The system is built through a multi-stage development process incorporating oscillator-based signal generation, CMOS-level signal selection, and gate-level computation, offering a comprehensive exploration of both low- and high-level digital design principles.

The project consists of three main modules. First, a 1-bit signal generator is constructed using an astable multivibrator circuit to produce a stable square wave at approximately 2 Hz. This waveform acts as a timing reference for the rest of the system. Second, a 2x2 multiplexer (MUX) is designed using CMOS logic, utilizing PMOS and NMOS transistors to route input signals (A1 and A0) to outputs (B1 and B0) based on control inputs (SM1, SM0), ensuring energy efficiency and high-speed switching. Third, a switchable BCD counter and a variable pulse-width modulation (PWM) generator are developed using flip-flops, logic gates, and comparator-based analog-digital interfacing. The counter can increment by either one or two depending on a control input, while the PWM generator adjusts the duty cycle of a 1 Hz pulse (from B0) via a user-controlled potentiometer, ranging from 0% to 50%.

Through LTspice simulations and physical design practices, the project aims to demonstrate proficiency in digital logic implementation, circuit timing synchronization, and the integration of analog control into digital systems. This design not only fulfills the requirements of a reconfigurable timing and counting system but also emphasizes scalability, component-level precision, and real-world applicability in embedded systems and signal control environments.

Description of the Entire System

The system developed in this project is designed to integrate several key modules, including a 1-bit signal generator, a 2x2 multiplexer (MUX), a switchable BCD counter, and a duty-cycle-variable pulse generator. These components work together to provide a complete digital control system capable of generating precise time intervals, performing counting operations, and modulating signal pulse widths. Each module is constructed with careful attention to both functional accuracy and efficiency, utilizing CMOS technology for logic design and analog techniques for signal manipulation.

1. 1-Bit Signal Generator

The core of the system begins with the generation of square wave signals by the 1-bit signal generator. This is accomplished using an astable multivibrator circuit made from BC547B transistors, resistors, and capacitors. The circuit is designed to generate square wave pulses at a frequency of approximately 2 Hz, which serves as the primary timing reference for other components in the system. The output waveform, verified through LTspice simulations, has a duty cycle close to 50%, satisfying the required specifications. The frequency and waveform stability are crucial for ensuring reliable synchronization across the entire system.

2. 2x2 CMOS Multiplexer (MUX)

To manage and route the signals generated by the 1-bit generators, the system includes a 2x2 multiplexer (MUX) designed with CMOS logic. The MUX allows for the selection between two different input signals (A1 and A0) based on the values of the selection control inputs (SM0 and SM1). The multiplexer is designed using PMOS and NMOS transistors, providing both low power consumption and high-speed switching. The control inputs determine which of the two clock signals (A0 or A1) is directed to the outputs (B0 or B1). This selection mechanism allows for flexible clock signal routing based on the desired operational mode of the system. The outputs of the MUX are fed into subsequent stages of the system, including the counter and pulse generator.

3. Switchable BCD Counter

The switchable BCD counter receives a clock signal from the MUX output (B1) and produces a binary-coded decimal (BCD) output that is used for counting. The counter can increment its value by 1 or 2 based on the Switch Control (SC) input. This is achieved through a combination of D flip-flops and combinational logic gates. The counter is designed to increment correctly, with overflow detection ensuring that the counter wraps around and updates the next most significant digit when necessary. The two 4-bit outputs (D1 and D0) are displayed on a 2-digit 7-segment display to show the current count. The system's counter functionality allows for precise and configurable counting operations.

4. Duty-Cycle-Variable Pulse Generator

The duty-cycle-variable pulse generator utilizes the B0 output from the MUX as the base clock for generating a pulse-width modulated (PWM) signal. This signal is modulated through a potentiometer, op-amps, and resistors to adjust the duty cycle between 0% and 50%. The duty cycle of the pulse is a key parameter in applications requiring precise control of signal power or timing, such as in motor speed control or LED brightness modulation. The op-amp circuit compares input voltages to modulate the on-time and off-time of the output signal, allowing for smooth adjustment of the duty cycle.

5. Control Interface and Output Display

The system includes a user-friendly control interface consisting of three slide switches (SM0, SM1, SC) that allow the user to manipulate the counting behavior and signal generation. The SM0 and SM1 switches control the MUX selection between different clock signals (A0 and A1), while the SC switch determines whether the counter increments by 1 or 2. The output of the system is displayed through five LEDs (A1, A0, B1, B0, O0) and a two-digit 7-segment display, which shows the current value of the switchable counter. This output system provides real-time feedback, making it easy to observe the system’s operation and adjust the parameters accordingly.

6. System Integration and Operation

The entire system is integrated to provide a seamless digital control mechanism where the MUX routes clock signals to the counter and pulse generator, the counter handles variable counting based on user input, and the pulse generator adjusts signal timing with varying duty cycles. The modular design of the system, with each component serving a specific function, allows for easy expansion or modification of the system in the future.

By simulating the system in LTspice and physically implementing the circuits, the entire design has been tested to ensure proper functionality. The simulations have verified that the system meets the specifications for frequency, duty cycle control, and counter operation. This design serves as a versatile platform for various digital control applications, from basic counting to more complex signal manipulation tasks.

TASK 1

DATA GENERATOR (A1 and A0)

Data Generator for A1 and A0

In the design of this system, the primary function of the data generator is to produce stable, oscillating clock signals (square waves) that serve as timing references for the rest of the system. The two clock signals, A1 and A0, are generated with different frequencies, providing flexibility in controlling the speed and synchronization of the system’s operations.

A1 - 2 Hz Signal Generator

The A1 signal is generated using an astable multivibrator circuit, which produces a square wave signal oscillating at a frequency of approximately 2 Hz. This circuit is designed to continuously switch between high and low states, creating the desired waveform. The frequency of A1 is determined by the RC time constant (where R is resistance and C is capacitance). By adjusting the values of the resistors and capacitors, the time it takes for the capacitor to charge and discharge is controlled, which ultimately sets the frequency of the oscillations.

Since A1 operates at a 2 Hz frequency, it provides a faster timing reference compared to A0, making it ideal for operations that require more frequent updates or faster timing cycles. This higher frequency allows A1 to play a crucial role in modulating faster counting and timing operations within the system.

A0 - 1 Hz Signal Generator

In contrast, the A0 signal is generated with a frequency of 1 Hz, using a similar astable multivibrator circuit but with different resistor and capacitor values to achieve the slower oscillation. The circuit operates in the same manner as A1,

switching between high and low states to produce a square wave. The lower frequency of A0 is important for tasks that require slower timing intervals, providing a steady, low-frequency clock signal that is useful for operations that don't need high-speed updates.

The A0 signal, oscillating at 1 Hz, serves as a timing reference when slower counting or signal manipulation is needed. This lower frequency provides stability for slower processes, making A0 suitable for controlling more gradual or less frequent updates.

Operational Behaviour of A1 and A0

- A1 oscillates at a 2 Hz frequency and serves as a faster timing reference for quicker counting or signal manipulation tasks.
- A0 oscillates at 1 Hz and provides a slower, stable clock for operations that require longer timing intervals.

Both signals are routed through the 2x2 multiplexer (MUX), where the system can select between the two signals (A1 or A0) based on the SM1 and SM0 control inputs. This selection mechanism allows the system to adjust the speed of operations dynamically, providing flexibility for both rapid and slow processing tasks.

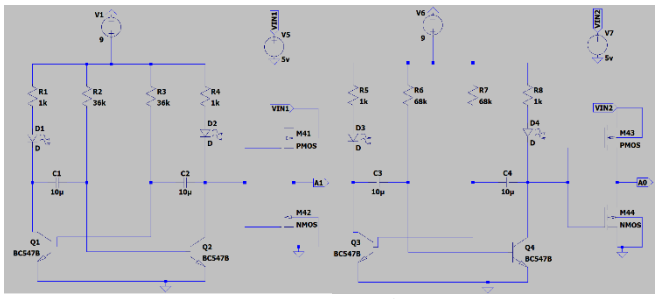


Figure 1: The whole period of the circuit A1 and A0

$$v_C(t) = v_{max}\left(1 - e^{-\frac{t}{RC}}\right) \quad (1)$$

In an oscillator circuit, half of a period is determined by the capacitor reaching a voltage level of 50%.

$$0.5v_{max} = v_{max}\left(1 - e^{-\frac{t}{RC}}\right) \quad 0.5 = \left(1 - e^{-\frac{t}{RC}}\right) \quad (2)$$

$$e^{-\frac{t}{RC}} = 0.5 \quad -\frac{t}{RC} = \ln(0.5) \quad (3)$$

$$\frac{t}{RC} = \ln(0.5) \quad \ln(0.5) \approx -0.69 * RC \quad (4)$$

Equation 1: The Charging Voltage Equation of The RC Circuit

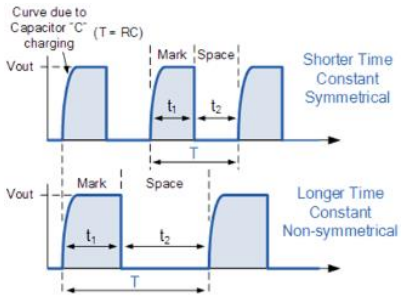


Figure 2: Astable Multivibrator Waveforms

$$T = t_1 + t_2 \quad (5)$$

$$t_1 = 0.69 * C_1 R_2 \quad (6)$$

$$t_2 = 0.69 * C_2 R_3 \quad (7)$$

$$f = \frac{1}{T} = \frac{1}{1.38*R*C} \quad (8)$$

$$f = \frac{1}{1.38*36k*10uF} = 2Hz \quad (9)$$

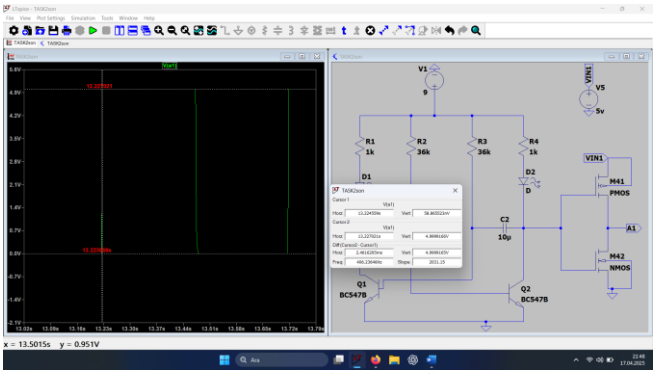


Figure 3: Time of the T rise for A1

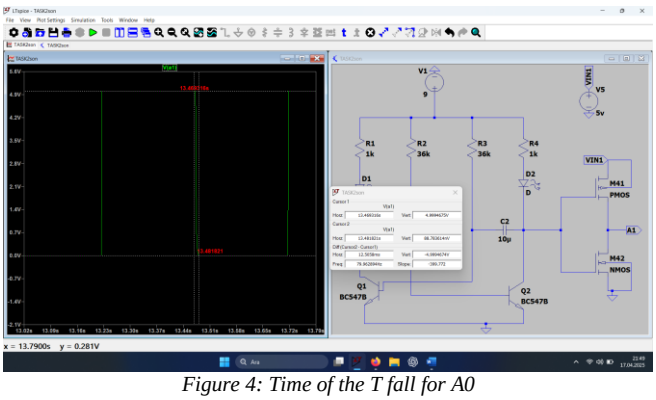


Figure 4: Time of the T fall for A0

$$\text{Ratio of the Flatness} = \left(1 - \frac{T_{rise} + T_{fall}}{T_{total}}\right) * 100 = 97\% \quad (10)$$

Equation 4.1: For the Flatness Ratio

Duty Cycle Calculation for A1

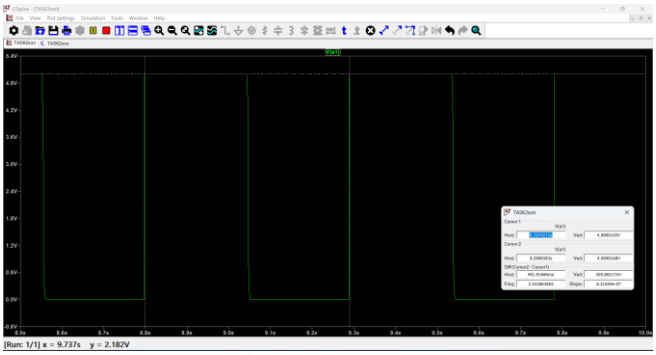


Figure 5: The Full Period of the Circuit

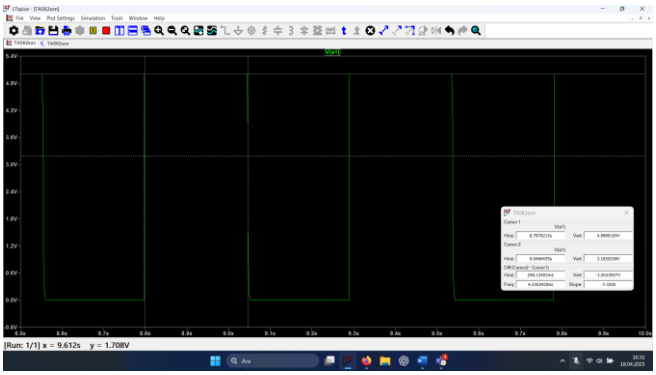


Figure 6: The half Period of the Circuit

Difference between the cursors in

9.0460455s-8.7979215s=0.252221 (11)

Equation 6.1: Time of the Half Period

9.2891658s-8.7938245s=0.4953413 (12)

Equation 6.2: Time of the Full Period

$$\text{Duty Cycle} = \frac{0.252221}{0.4953413} = 50.922\ \% \quad (13)$$

Equation 6.3: Equation for the Duty Cycle

And Real Part and Oscilloscope Part Photographs

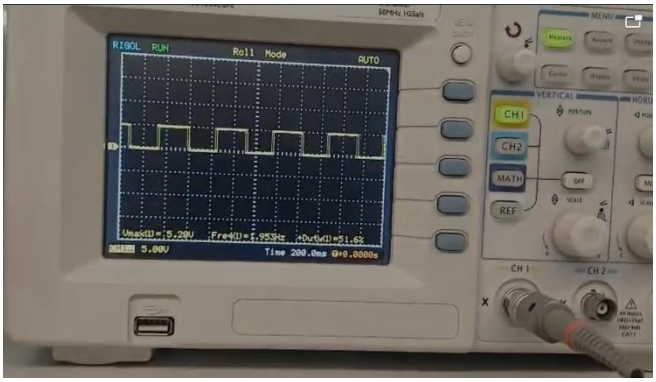


Figure 7: Oscilloscope Photograph for A1

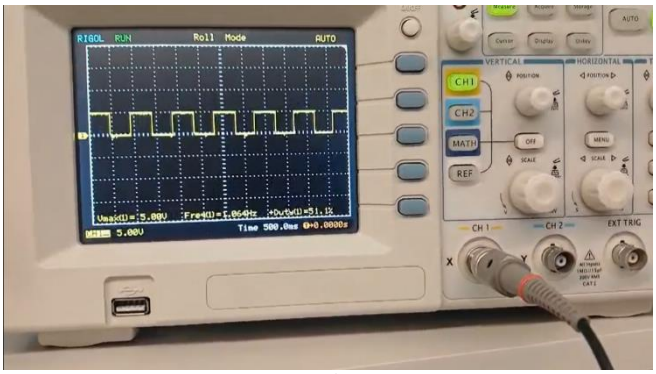
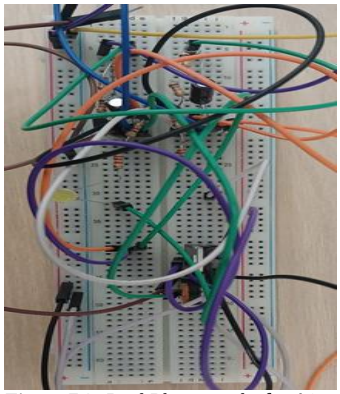


Figure 7.1: Oscilloscope Photograph for A1



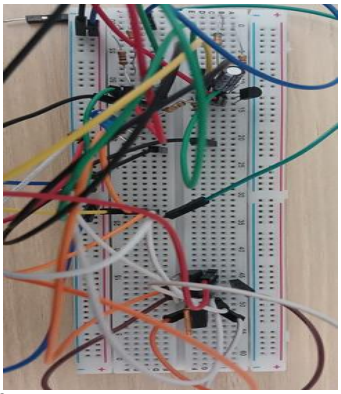


Figure 7.2: Real Photographs for A1 and A0

TASK 2- Operational Behavior of MUX

In this project, a 2x2 multiplexer (MUX) is designed using CMOS logic to control the routing of two different clock signals, A0 and A1. The MUX selects which signal to pass to the B0 and B1 outputs based on the values of the SM0 and SM1 selection inputs. This configuration provides dynamic switching between the different timing sources required to control the operating speed of the counter and the duty cycle generator. The CMOS implementation provides low power consumption and high speed signal switching, making it suitable for digital system integration.

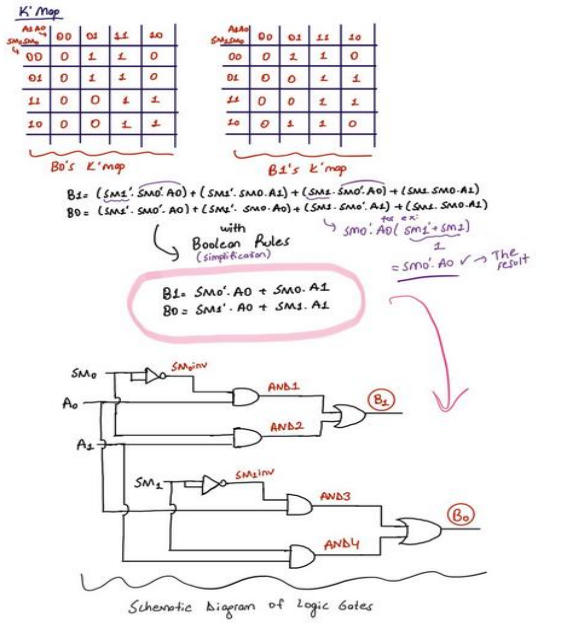


Figure 8: KMAP for the 2 by 2 MUX

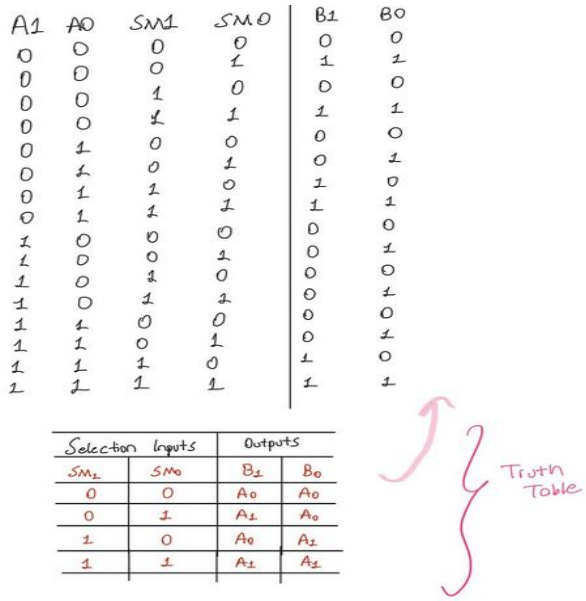


Figure 8.1: Truth Table for the 2 by 2 MUX

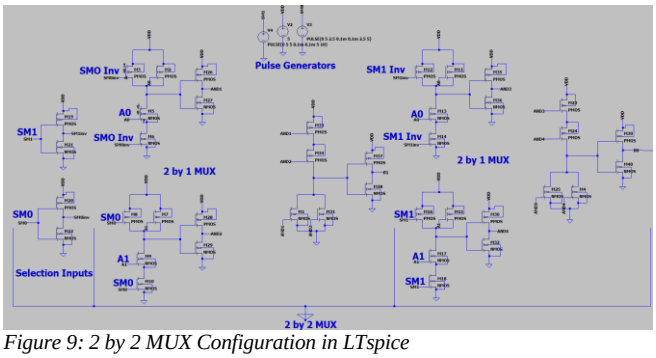


Figure 9: 2 by 2 MUX Configuration in LTspice

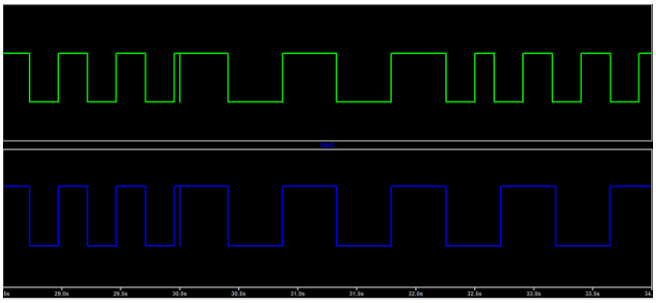


Figure 10: Output of the 2 by 2 MUX Configuration

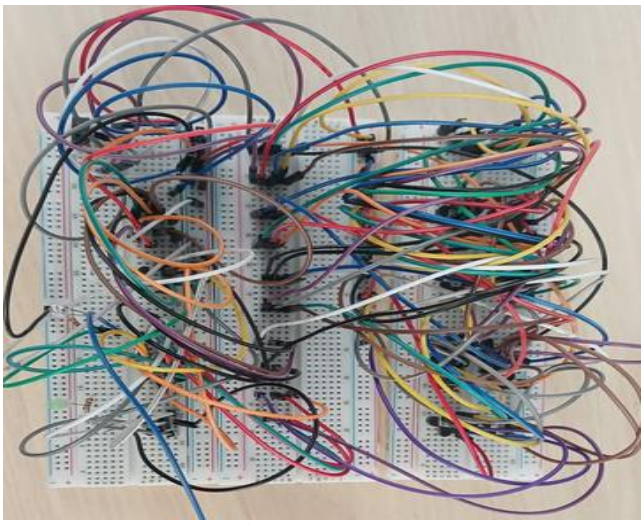


Figure 11: 2 by 2 MUX Configuration on Breadboard

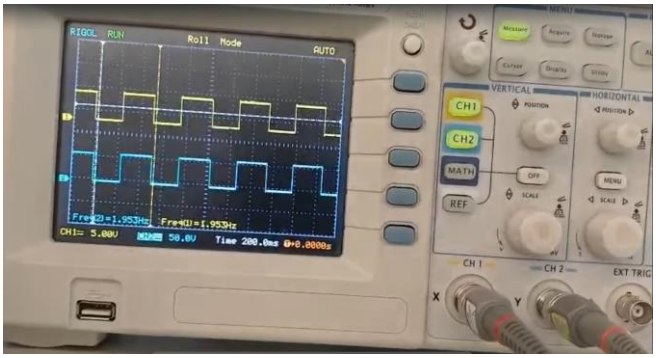


Figure 12: Oscilloscope Photograph 2 by 2 MUX for SM1 and SM0 are 0

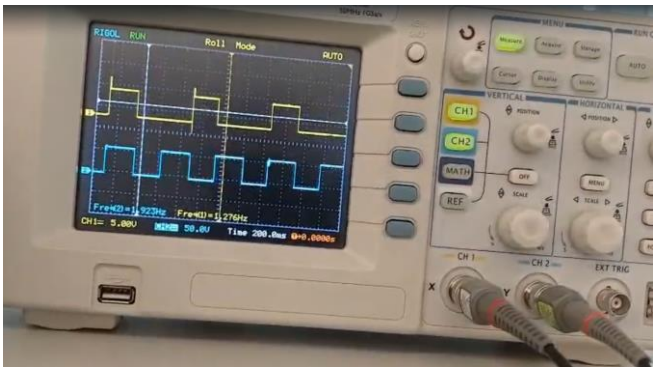


Figure 12.1: Oscilloscope Photograph 2 by 2 MUX for SM1 =1 and SM0=0

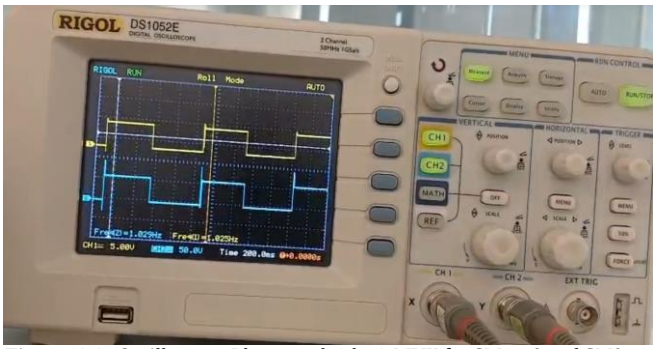


Figure 12.2: Oscilloscope Photograph 2 by 2 MUX for SM1 =0 and SM0=1

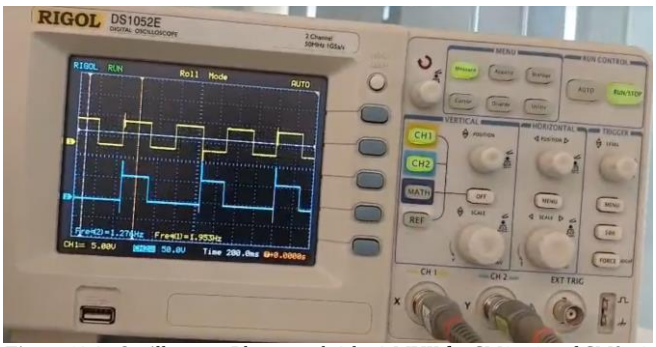


Figure 12.3: Oscilloscope Photograph 2 by 2 MUX for SM1 =1 and SM0=1

Logical Foundation and Truth Table Construction

The logical behaviour of the 2x2 MUX is initially modelled using truth tables and Karnaugh maps (K-maps). Each output (B1 and B0) operates as an independent 2-to-1 multiplexer: B1 is selected via SM0 and receives either A0 or A1. B0 is selected via SM1 and also switches between A0 and A1. From the truth table, Boolean expressions are derived and simplified using Karnaugh maps:

- $B1 = SM0' \cdot A0 + SM0 \cdot A1$ (14)
- $B0 = SM1' \cdot A0 + SM1 \cdot A1$ (15)

These expressions are then translated into a logic gate level schematic using NOT, AND and OR gates as shown in the handwritten diagram. This simplified logic forms the basis of the CMOS transistor level implementation.

Transistor-Level CMOS Implementation in LTspice

The next step involved implementing the logic with real transistors. Using BS170 (NMOS) and BS250 (PMOS) transistors, the logic gates were built in LTspice. The circuit consists of: Two clock signal generators (A0 ~1Hz, A1 ~2Hz), Four inverters to generate the control signal complements (SM0' and SM1'), Four AND gates and two OR gates implemented with CMOS configurations, two separate 2x1 multiplexers that internally form a 2x2 MUX. The schematic shows clear labelling of each functional block, including inverters, selectors, pulse generators, and output routing. Voltages and logic levels are appropriately modelled to mimic real-world transistor behaviour.

Simulation Results

LTspice simulation results confirm the logical correctness and timing accuracy of the 2x2 CMOS multiplexer circuit. As observed in the simulation waveform, the output signals B1 and B0 correctly follow either A0 or A1 depending on the select inputs SM0 and SM1. When the select inputs are changed, the outputs dynamically switch between the two input frequencies, reflecting the behavior predicted by the Boolean logic and truth table. The transitions are clean and stable, and the timing of the square waves is almost 100% consistent with the expected frequencies of the input signals. These results confirm that the CMOS-based implementation performs as intended and that the selection logic is implemented properly at the transistor level, indicating that the operations are performed as intended.

Physical Implementation and Oscilloscope Results

To verify the circuit beyond simulation, the 2x2 MUX was implemented on a physical breadboard using discrete NMOS and PMOS transistors along with external pulse generators and selector switches. Despite the complexity of the wiring, it was pleasing to see that it accurately reproduced the logic defined in the prototype schematic. The output signals were observed using a RIGOL DS1052E digital oscilloscope, where both channels B0 and B1 displayed the expected square waveforms. Multiple measurements were made under varying combinations of selector inputs, and it was observed that the outputs switched correctly between 1 Hz (A0) and 2 Hz (A1) signals. The frequencies displayed on the oscilloscope matched the simulation results with precise transitions and clean waveform shapes, thus verifying the successful operation of the CMOS-based multiplexer in the real world.

The 2x2 CMOS multiplexer designed in this project was successfully developed, simulated and implemented both virtually and physically. This process began with truth table analysis and Karnaugh map simplification, and the circuit was built at the transistor level in LTspice using complementary MOSFET logic. Simulation results confirmed functional correctness and clean switching behaviour. Hardware implementation further validated the design, with oscilloscope measurements closely matching theoretical and simulated expectations. This multiplexer provides dynamic and reliable clock signal selection, which plays a vital role in the larger system architecture and demonstrates the practical applicability of CMOS-based logic design in digital systems.

A. Switchable Counter

The switchable counter receives the output from the MUX, either B1 or B0, depending on the selection made. This counter is designed to increment by 1 or 2 based on the state of the control signal SC. When SC = 0, the counter increments by 1 per clock pulse; when SC = 1, the counter increments by 2. The counter's outputs, D1 and D0, are 4-bit binary values representing the current count, which are used to drive a 7-segment display. This display shows the current count in Binary Coded Decimal (BCD) format. The switchable nature of the counter allows for flexible control of the counting step size. Additionally, overflow detection is built into the design to handle cases where the counter reaches its maximum value and needs to reset or cascade to the next stage.

B. Pulse Generator with Variable Duty Cycle

The pulse generator in this system is designed to produce a PWM signal with an adjustable duty cycle. It receives the signal from B0 (the output from the MUX) and adjusts the duty cycle of the generated signal according to a control input, typically via a potentiometer. The potentiometer allows for the variation of the duty cycle, controlling the time the signal is high (on) versus low (off). The output of the pulse generator is denoted as O0, which is a PWM signal. This output can be used to control devices like motors, LEDs, or other systems that require varying power delivery based on the PWM signal's duty cycle. The duty cycle can be adjusted within a range from 0% to 50%, offering flexibility in power modulation.

TASK 3- Switchable Counter and Duty-Cycle-Variable Pulse Generator

The objective of Task 3 was to develop an entire digital system made up of a switchable counter and duty-cycle variable pulse generator. Unlike Task 2, which was a transistor-level CMOS implementation, the task was a gate-level implementation at a higher level of abstraction using simple digital logic building elements such as AND, OR, NOT gates, and D flip-flops. The goal was to design a binary counter and generate a PWM (Pulse Width Modulation) signal in order to control the duty cycle of the signal. LTspice, a well-known digital and analog circuit analysis simulation tool, was employed in the design and functional test.

The task was divided into two primary parts:
Switchable Counter: A binary counter capable of incrementing by 1 or 2 based on the control input

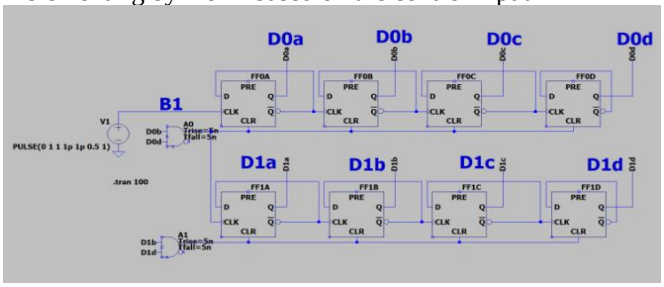


Figure 13: Circuit Diagram of One Unit Increment

Duty-Cycle-Variable Pulse Generator: A pulse generator that produces a PWM signal with a variable duty cycle, controlled through a potentiometer.

1) Switchable Counter

The switchable counter is the most important component in the system to be used to generate the count in binary format. The counter was implemented with D flip-flops to get a 4-bit binary counter. The counter was implemented to increment its value based on the SC control signal. Exactly, the counter was used to increment by 1 when SC = 0 and 2 when SC = 1.

The counter was implemented using four D flip-flops, and each of them latched one bit of the binary count. The D flip-flops were triggered by a signal that was generated from the MUX (Multiplexer), which alternates between the two clocks (A1 and A0). The counter is a synchronous counter, where all flip-flops transition at the same instant with each clock pulse.

Overflow Handling:

The counter has been designed with the ability to handle overflow conditions. When the counter exceeds its maximum value (i.e., 1111 in binary, or 15 in decimal), it overflows to 0000. In other cases, an overflow can make another counter handle larger values, so that even after reaching the maximum count, the system continues to function.

The counter output, D1D0, was displayed on a 2-digit 7-segment display. The display shows the binary count in Binary Coded Decimal (BCD) format. The 7-segment display allows users to view the current count clearly and provides a visual representation of the counter operation.

Switchable counter in Task 3 gives a BCD (Binary-Coded Decimal) output using the D flip-flops. The two outputs (D1 and D0) of the counter are applied to drive the seven-segment display. They are the binary representation of the count, which gets decoded and ultimately displayed on the 2-digit seven-segment display.
D1 and D0 are the tens and ones place value of the counter. The seven-segment display lights up the respective segments to show these values in BCD form.

Assume that the counter produces a count of 5:
D1 would be 0000 (0 in binary in tens place).
D0 would be 0101 (5 in binary for ones place).
The seven-segment display would show the digit 5 for the digit 0 (the ones place) and 0 for the digit 1 (the tens place).

Therefore, the seven-segment display plays a very significant role in showing the current value of the switchable counter to enable users to see the count.

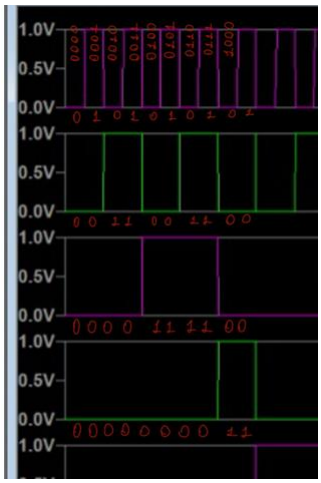


Figure 14: D Flip Flop Outputs in One Unit Increment

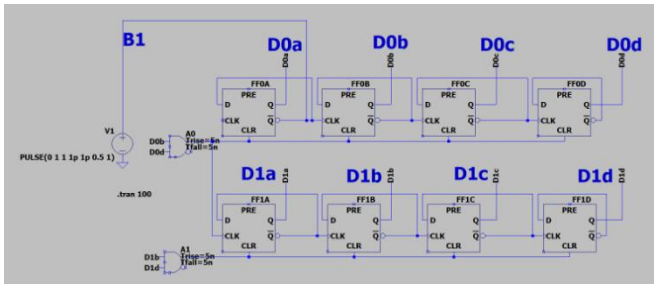


Figure 15: Circuit Diagram of Two Unit Increment

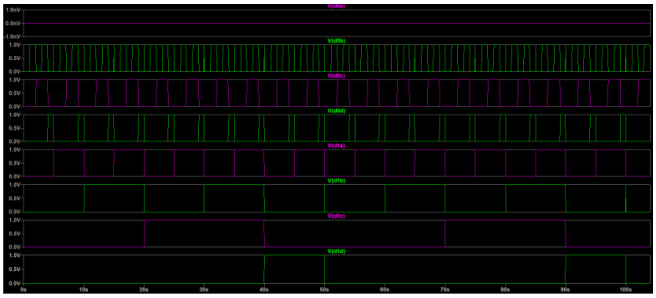


Figure 16: D Flip Flop Outputs in Two Unit Increments

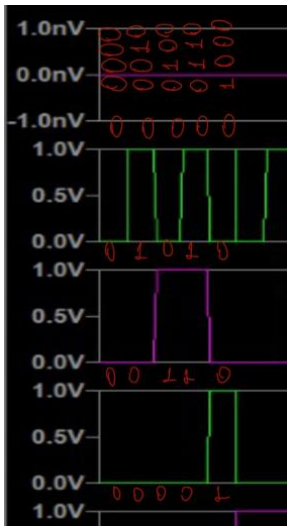


Figure 17: Representation of Two Unit Increase

2) Duty-Cycle-Variable Pulse Generator

The duty cycle is the ratio of the time for which a signal is high (on) to the total time period of the signal. It is an important principle of PWM (Pulse Width Modulation) systems, where the on time of a signal is varied to control different aspects of a system, for example, to control motor speeds or adjust LED brightness. In this circuit, the duty cycle is controlled by comparing a triangle wave with a reference voltage. Here's how it works:

a) Triangle Wave Generation (Integrator Op-Amp)
The input square wave (B0) is first run through an integrator op-amp. This stage creates a triangle wave.

The triangle wave is nothing but the integral of the input square wave, and it typically oscillates between 0V and Vs (supply voltage).

The triangle wave is employed as the reference signal for the PWM signal generation through comparison with the reference voltage.

b) Comparator Op-Amp with Reference Voltage Comparison
A comparator op-amp compares the triangle wave with the reference voltage. The reference voltage is maintained at some level, and the moment the triangle wave intersects the reference voltage, the comparator output goes HIGH.

The triangle wave is HIGH for as long as it remains greater than the reference voltage.

When the triangle wave becomes lower than the reference voltage, the output becomes LOW.

c) Duty Cycle and PWM Output

The duty cycle is directly proportional to the reference voltage. When the reference voltage is raised, the triangle wave remains high for a longer duration, which boosts the PWM signal's HIGH time and thereby raises the duty cycle.

Decreasing the reference voltage lowers the duration that the triangle wave remains high, decreasing the HIGH time of the PWM signal, which reduces the duty cycle.

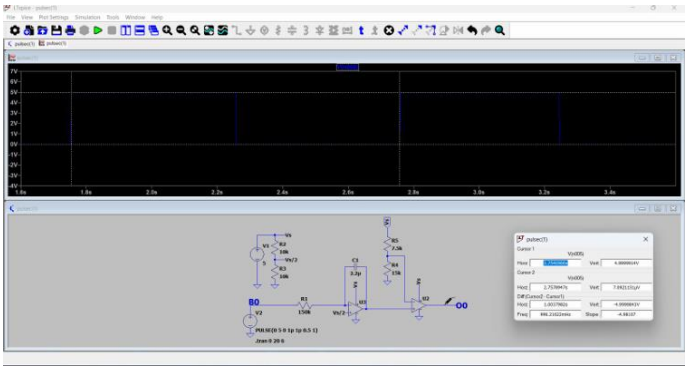


Figure 18: Duty Cycle ≅ 50% - R5 = 7.5kΩ Graph

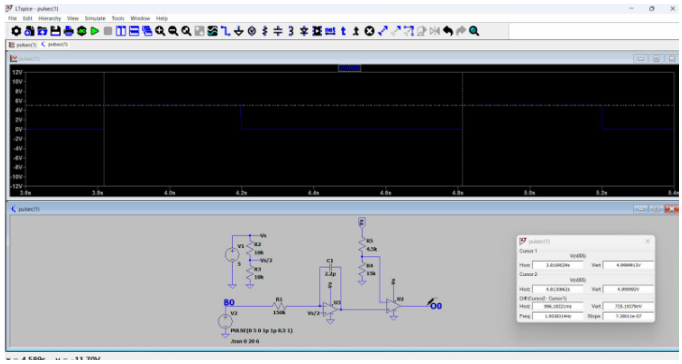


Figure 19 : Duty Cycle ≅34.5% - R5 = 4.5kΩ Graph

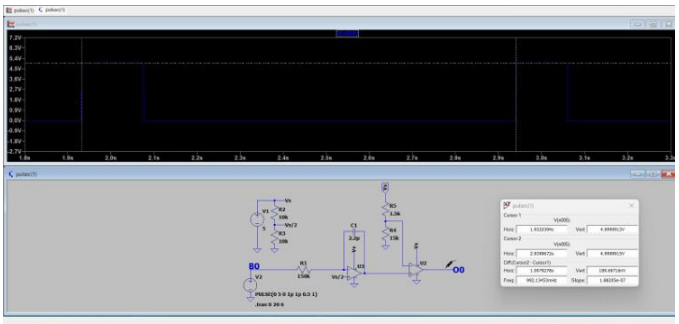


Figure 20: Duty Cycle ≅14.5% - R5 = 1.5kΩ Graph

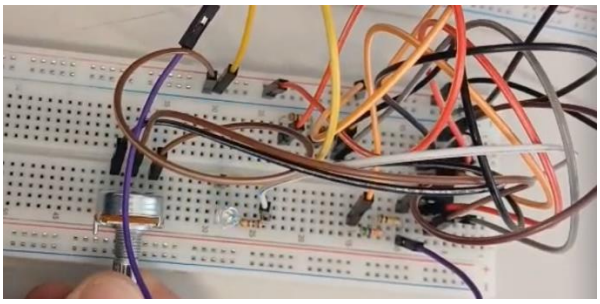


Figure 21: Duty Cycle Circuit on Breadboard

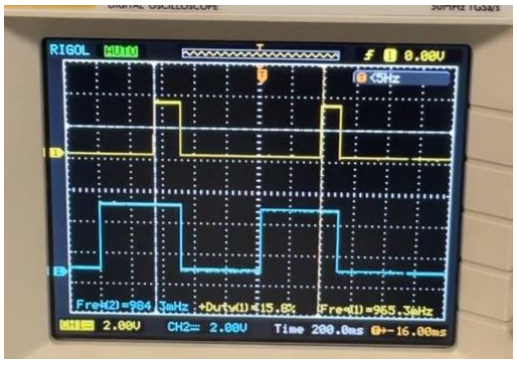


Figure 22: Oscilloscope Image of 15% Duty Cycle

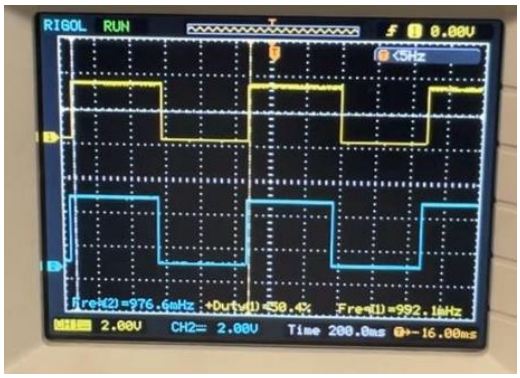


Figure 23: Oscilloscope Image of 50% Duty Cycle

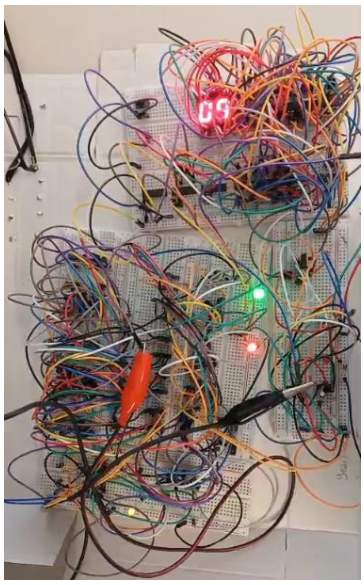


Figure 24: Image of the Entire System on Breadboard

CONCLUSION

This project consisted of a successful design, simulation, and integration of the Switchable Counter and Variable Pulse Generator system under three different tasks. Each task equally contributed to building an entire digital system capable of counting in binary and generating a PWM (Pulse Width Modulation) signal with an adjustable duty cycle. These tasks were not only meant to explore different aspects of digital design, but also to impart considerable hands-on experience with circuit simulation and integration.

Task 1 dealt with the design and simulation of a 1-bit generator circuit built with BC547B transistors, which produced a stable square wave of frequency 2 Hz and a duty cycle of about 50%. With the knowledge of using astable multivibrators, we were able to gain deep insight into oscillator circuits, and this circuit met the specifications to produce the required frequency and duty cycle. The theoretical and simulated results validated the operation of the multivibrator in producing a square wave signal fit for use in the later tasks.

Task 2 included designing and implementing at the transistor level a 2x2 multiplexer (MUX) in CMOS technology. The MUX selected between two input signals of A1 and A0 based on two control signals, SM1 and SM0. The MUX was designed using basic logic gates (AND, OR &

NOT), which were simulated using LTspice for testing the correct switching operation. The output of the MUX served as the clock input for the switchable counter as well as for the pulse generator. The simulation output confirmed the MUX was operating as intended, with the control signals selecting the correct input to be routed to the outputs.

Integrating the circuits developed in Task 1 and Task 2 into a complete digital system, the switchable counter was designed with D flip-flops to count by either 1 or 2 depending upon a control input (SC). The counter's output was visible on a 7-segment display. The duty-cycle-variable pulse generator produces a PWM signal with the duty cycle being adjustable from 0% to 50% by a potentiometer. The system was also simulated in LTspice for functional verification, where the PWM signal came into practical use in controlling brightness of LEDs or speed of motors.

The entire system, that is, the switchable counter and PWM pulse generator, was verified by simulation, with the results confirming that the system operates as required, meaning the counter works as intended, and the PWM signal is adjustable in terms of duty cycle.

In summary, the project provided ample demonstration of the role of digital logic design and system integration. Concentrating on the simplest building blocks of digital electronics, such as logic gates, flip-flops, and op-amps, has enabled one to realistically envision a modular and scannable implementation system. The simulations carried out in LTspice have offered important insights, while successful delivery of each task will set the stage for hardware implementation ahead.

SUPPORTING MATERIALS

https://youtu.be/m2DhtiDODto

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[3] GeeksforGeeks, “MUX in digital logic,” GeeksforGeeks, Aug.

[4] Wikipedia contributors, “Multivibrator,” Wikipedia, Mar. 11, 2024.https://en.wikipedia.org/wiki/Multivibrator