CS223 Laboratory Assignment 2

Adders on FPGA

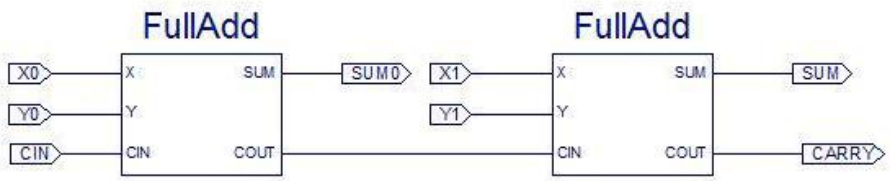
Lab dates and times:
Section 1: 19.2.2018 Monday 08:40-12:25
Section 2: 21.2.2018 Wednesday 08:40-12:25
Section 3: 20.2.2018 Tuesday 08:40-12:25
Section 4: 22.2.2018 Thursday 08:40-12:25

Location: EA Z04 (in the EA building, straight ahead past the elevators)
Groups: Each student will do the lab individually. Group size = 1

Preliminary Report (30 points)

In the previous lab, you implemented a 1-bit half-adder and full-adder using gates on the bread board. In this lab you will implement very similar circuits, but this time on the FPGA. Today's lab needs considerable advance preparation. You need to learn how to work with Xilinx's design tool set before attending the lab. Besides, Systemverilog models and testbenches should be prepared in advance, and assembled neatly into a Preliminary Report with a printed cover page and printed pages for the Systemverilog codes. Each page should have a proper heading. The content of the report is as follows:

a) A cover page which includes the following: course name and code number, the number of the lab, your name and student ID, date, number of your trainer pack.
b) Schematic for a 1-bit fulladder, made from 2-input XOR, AND and OR gates (you can refer to figures in Lab1).
c) Dataflow Systemverilog modules for a 1-bit fulladder, This means modeling with Boolean equations, using continuous assignment statements. Prepare a testbench.
d) Structural Systemverilog module for a 1-bit fulladder.
e) Using the dataflow description of the 1 bit adder design a Systemverilog modulefor the two bit adder as shown below. Prepare a testbench to test your two bit adder.



Additional pre-lab work:

You should study the following documents (available on Unilica/Documents/Resources) to be familiar with steps of design flow (Simulation, Synthesis, Implementation, Generation of Programming File, Downloading to FPGA board), using Xilinx Vivado tool. You can download, install and practice working with Xilinx Vivado on your own computer with free webpack license.

- Suggestions for Lab Success with Systemverilog, Vivado, and BASYS3.
- Basys3 Vivado Decoder Tutorial.
- Vivado Tutorial.
- BASYS-3 FPGA Board Reference Manual (just take a look, and later use it as reference when needed).

You will need a copy of your designs and Systemverilog programs with you in the lab to refer to or possibly correct and change it. The Preliminary Report will be turned in at the start of lab. Therefore, you must make a photocopy of it before you come to the lab, for your own use.

Implementation on FPGA (70 points)

In this step, you implement 1-bit adder/subtractor on FPGA. You don't need to connect your BASYS-3 board to the Beti board. Working with standalone BASYS-3 and having it connected to your computer is enough for this lab. There are some switches and LEDs available on BASYS-3 which you can use them.

- *Create a new Xilinx Vivado Project to do each part (one project for data-flow modeling and one for structural). Use appropriate names for files and folders, keeping the project in a directory where you can find it later and erase it (at the end of lab).*

a) Simulation: Give the Systemverilog codes for the preliminary part-c in the dataflow style. Then, using Systemverilog testbench code, verify in simulation that your circuit work correctly. Note that the testing should be complete, using all possible input combinations.
b) Simulation: Give the Systemverilog codes for the preliminary part-d , in the structural style. Then, using Systemverilog testbench code, verify in simulation that your circuit work correctly. Note that the testing should be complete, using all possible input combinations.
c) Simulation : Give the Systemverilog codes for preliminary part-e. Then, using Systemverilog testbench code, verify in simulation that your circuit work correctly. When you are convinced that your codes work correctly, show the simulation results to your TA. Be prepared to answer questions that you may be asked.
d) Program the FPGA: Now, follow the Xilinx design flow to synthesize, create programming file, and program your 1-bit adder to BASYS-3 FPGA board.
e) Test your design: Using the switches and LEDs (on BASYS-3) that you have assigned in constraint file, test your design. When you are convinced that they work correctly, show the physical implementation results to the TA. Be prepared to answer questions that you may be asked.
f) Program the FPGA: Now, follow the Xilinx design flow to synthesize, create programming file, and program your 2-bit adder to BASYS-3 FPGA board.

g) Test your design: Using the switches and LEDs (on BASYS-3) that you have assigned in constraint file, test your design. When you are convinced that they work correctly, show the physical implementation results to the TA. Be prepared to answer questions that you may be asked.

Submit your code for MOSS similarity testing

Finally, when you are done and before leaving the lab, you need to upload the file *StudentID_SVerilog.txt* created in the Implementation with FPGA part. Be sure that the file contains exactly and only the codes which are specifically detailed above. If you have multiple files, just copy and paste them in order, one after another inside text file. Check the specifications! Even if you didn't finish, or didn't get the Systemverilog part working, you must submit your code to the Unilica Assignment for similarity checking. Your codes will be compared against all the other codes in all sections of the class, by the MOSS program, to determine how similar it is (as an indication of plagiarism). So be sure that the code you submit is code that you actually wrote yourself! All students must upload their code to the 'Unilica>Assignment' specific for your section. Check submission time and don't miss it before leaving the lab. After taking a backup of your work, don't forget to delete it from computer. Because students of other sections will work with your system too.

Clean Up

1) Clean up your lab station, and return all the parts, wires, the Beti trainer board, etc. Leave your lab workstation for others the way you would like to find it.

2) CONGRATULATIONS! You are finished with Lab #2 and are one step closer to becoming a computer engineer.

NOTES

--Advance work on this lab, and all labs, is strongly suggested.
--Be sure to read and follow the Policies for CS223 labs, posted in Unilica.

LAB POLICIES

1. There are three computers in each row in the lab. Don't use middle computers, unless you are allowed by lab coordinator.
2. You borrow a lab-board containing the development board, connectors, etc. in the beginning. The lab coordinator takes your signature. When you are done, return it to his/her, otherwise you will be responsible and lose points.
3. Each lab-board has a number. You must always use the same board throughout the semester.
4. You must be in the lab, working on the lab, from the time lab starts until you finish and leave. (bathroom and snack breaks are the exception to this rule). Absence from the lab, at any time, is counted as absence from the whole lab that day.
5. No cell phone usage during lab. Tell friends not to call during the lab hours--you are busy learning how digital circuits work !
6. Internet usage is permitted only to lab-related technical sites. No Facebook, Twitter, email, news, video games, etc--you are busy learning how digital circuits work !

7. If you come to lab later than 20 minutes, you will lose that session completely.
8. When you are done, DO NOT return IC parts into the IC boxes where you've taken them first. Just put them inside your Lab-board box. Lab coordinator will check and return them later.