07.05.2020

Istanbul Technical University
Department of Computer Engineering

BLG 322E – Computer Architecture
Assignment 4

Due Date: 20.05.2020, **Wednesday,** 23.59.

QUESTION:

For the four cycles of a CPU, their durations are given below followed by their memory access requirements (if any):

1. Instruction Fetch (IF): 40 ns (Memory access)

2. Operand Fetch (OF): 60 ns (Memory access)

3. Execution (EX): 20 ns (No memory access)

4. Operand Write (OW): 40 ns (Memory access)

The memory access time and I/O interface access time are both 50 ns.

In this system, there are four 3-wire (BR, BG, BGACK) DMACs ($DMAC_1$, $DMAC_2$, $DMAC_3$, and $DMAC_4$), which are connected to the 68000-like processor over a bus arbiter (see lecture notes slide 5.23).

The order of precedence is $DMAC_1 > DMAC_2 > DMAC_3 > DMAC_4$.

1. Construct the truth table for the bus arbiter. BR_i represents the BR output of $DMAC_i$, and BG_i represents the BG input of $DMAC_i$. All signals are active low (0).

2. Write the minimized logical expressions for the outputs of the bus arbiter.

3. For all four DMACs, the DMAC type is **fly-by** (implicit) (i.e., data does not pass through the DMAC). $DMAC_1$, $DMAC_3$, and $DMAC_4$ work in **cycle-stealing** mode, and $DMAC_2$ works in **burst** mode. All DMACs are programmed to transfer 5 words. Assume that we start a clock (Clock = 0) when the CPU begins to run a program. $DMAC_1$, $DMAC_2$, $DMAC_3$, and $DMAC_4$ issue bus requests at the same time, when the processor is in the instruction fetch cycle. Write down step-by-step all operations performed by the DMACs and the CPU from the beginning of the instruction fetch until the end of the completion of the first instruction.

4. For all four DMACs, the DMAC type is **flow-through** (explicit) (i.e., data passes through the DMAC). $DMAC_1$ and $DMAC_3$ are in **cycle-stealing** mode, and $DMAC_2$ and $DMAC_4$ are in **burst** mode. Assume that we start a clock (Clock = 0) when the CPU begins to run a program and DMACs attempt to start data transfer for 5 words when Clock = 30 ns.

   i. When (Clock = ?) will $DMAC_2$ complete the transfer of the second word? Why?

   ii. When (Clock = ?) will the CPU complete the first instruction cycle? Why?

Submission: Write your answer using a computer program or by hand on a sheet of paper. Type your name and student ID at the top of the paper. Submit your homework in PDF format to the Ninova system before the due date.

Late submissions are not accepted.

Assignments have to be done individually. If any plagiarism is detected, disciplinary regulations of the University will be applied.

Note: If you have a problem about the homework, you may contact the research assistants of the course (esengun@itu.edu.tr).