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BLG 322E – Computer Architecture
Assignment 2

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INSTRUCTIONS	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
LDL $00(R3), R1	IF	DR	EX	ME	WB																		
LDL $04(R3), R2		IF	DR	EX	ME	WB																	
NOOP			IF	DR	EX	ME	WB																
NOOP				IF	DR	EX	ME	WB															
ADD R1, R2, R1					IF	DR	EX	ME	WB														
LDL $08(R3), R4						IF	DR	EX	ME	WB													
NOOP							IF	DR	EX	ME	WB												
NOOP								IF	DR	EX	ME	WB											
SUB R1, R4, R1									IF	DR	EX	ME	WB										
BRU LAST_OP										IF	DR	EX	ME	WB									
NOOP											IF	DR	EX	ME	WB								
NOOP												IF	DR	EX	ME	WB							
LDL $10(R3), R2													IF	DR	EX	ME	WB						
NOOP														IF	DR	EX	ME	WB					
NOOP															IF	DR	EX	ME	WB				
ADD R1, R2, R1																IF	DR	EX	ME	WB			
NOOP																	IF	DR	EX	ME	WB		
NOOP																		IF	DR	EX	ME	WB	
STL $104(R3), R1																			IF	DR	EX	ME	WB

a) Each NOOP instruction introduces 1 clock cycle penalty. Since there are 10 NOOP instructions, total amount of penalty is 10 clock cycles.

INSTRUCTIONS	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
LDL $00(R3), R1	IF	DR	EX	ME	WB													
LDL $04(R3), R2		IF	DR	EX	ME	WB												
LDL $08(R3), R4			IF	DR	EX	ME	WB											
NOOP				IF	DR	EX	ME	WB										
ADD R1, R2, R1					IF	DR	EX	ME	WB									
BRU LAST_OP						IF	DR	EX	ME	WB								
LDL $10(R3), R2							IF	DR	EX	ME	WB							
SUB R1, R4, R1								IF	DR	EX	ME	WB						
NOOP									IF	DR	EX	ME	WB					
NOOP										IF	DR	EX	ME	WB				
ADD R1, R2, R1											IF	DR	EX	ME	WB			
NOOP												IF	DR	EX	ME	WB		
NOOP													IF	DR	EX	ME	WB	
STL $104(R3), R1														IF	DR	EX	ME	WB

b) Total amount of penalty is reduced to 5 clock cycles after applying optimized software-based solutions.