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BLG 322E – Computer Architecture

Assignment 5

1. a. i.

- Since data is transferred in blocks of 16 words (bytes), 4 bits are enough to represent each word in a block and **w = 4 bits**.
- Cache memory has a capacity of 4 KB and this corresponds to 4 x 2^{10} = 2^{12} bytes of data. Each block is 16 bytes so that each frame also has to be 16 bytes = 2^4 bytes. If we divide total capacity of Cache by size of one frame, we can calculate the number of frames which is equal to 2^{12}/ 2^4 = 2^8 so that **f = 8 bits**.
- Since address bus is 20 bits wide, each address should be represented by 20 bits which makes **a = 20 bits**.
- Physical address from CPU is divided into three segments called tag bits, frame bits and word bits. Number of tag bits, frame bits and word bits should sum up to address bits so that a – (f + w) = 20 – (4 + 8) = **t = 8 bits**.

Physical Address (a) = 20 bits		
Tag (t)	Frame Number (f)	Word Number (w)
8 bits	8 bits	4 bits

1. a. ii.

Address (Hex)	Tag	Frame Number	Word Number	Event
$00050	0	5	0	**Miss**
$0005C	0	5	12	**Hit**
$01052	1	5	2	**Miss**
$00057	0	5	7	**Miss**
$01054	1	5	4	**Miss**

- A **miss** will occur for $00050 since initially cache memory is empty. After that, the memory block starting from $00050 and ending at $0005F will be copied into cache memory.
- $0005C will be **hit** since current tag number of fifth frame is equal to address tag number.
- A **miss** will occur for $01052 since tag numbers don't match. After that, content of frame five will be replaced with the memory block starting from $01050 and ending at $0105F.
- A **miss** will occur for $00057 since tag numbers don't match. Content of frame five will be replaced with the memory block starting from $00050 and ending at $0005F.
- A **miss** will occur for $01054 since tag numbers don't match. Content of frame five will be replaced with the memory block starting from $0105 and ending at $0105F.

1. b.

Physical Address (a) = 20 bits		
Tag (t)	Set Number (s)	Word Number (w)
9 bits	8 bits	3 bits

Address (Hex)	Tag	Set Number	Word Number	Event
$00050	0	10	0	**Miss**
$0005C	0	11	4	**Miss**
$01052	2	10	2	**Miss**
$00057	0	10	7	**Hit**
$01054	2	10	4	**Hit**

- A **miss** will occur for $00050 since initially cache memory is empty. After that, the memory block starting from $00050 and ending at $00057 will be copied into set 10 frame 0.
- A **miss** will occur for $0005C since initially set 11 of cache memory is empty. After that, the memory block starting from $00058 and ending at $0005F will be copied into set 11 frame 0.
- A **miss** will occur for $01052 since set 10 has a frame with tag number 0 but it doesn't have another with 2. Since set 10 is not full yet, the memory block starting from $01050 and ending at $01057 will be copied into set 10 frame 1. Now, both frames of set 10 are occupied.
- A **hit** will occur for $00057 since set 10 has the frame with tag number 0.
- A **hit** will occur for $01054 since set 10 has the frame with tag number 2.

2. Calculations

Main memory size = 2^{19} bytes → Physical address bits (a) = 19 bits
Cache memory size = 2^{14} bytes
Transfer block size = 2^4 bytes
frames = Cache memory size / Transfer block size = 2^{10}
sets = 2^8
Frames per set = # frames / # sets = 4

s = 8, w = 4, a = 19, t = a – (s + w) = 8

Physical Address (a) = 19 bits		
Tag (t)	Set Number (s)	Word Number (w)
7 bits	8 bits	4 bits

2. a. i.

Only array A is placed into the cache memory since **No Write Allocate** mode is used for missed write operations. Elements of B and C arrays are only reached for write operations

and because of the access mode, missed memory blocks are only updated in main memory and they are not transferred to cache.
Array A is placed in **three different sets**:

- The main memory block containing $0008E (Block 8), which is the block from $00080 to $0008F, is copied into **Set 8 Frame 0**.
- The main memory block containing $00090 (Block 9), which is the block from $00090 to $0009F, is copied into **Set 9 Frame 0**.
- The main memory block containing $000A0 (Block 10), which is the block from $000A0 to $000AF, is copied into **Set 10 Frame 0**.

2. a. ii.

	Read misses	Read hits	Write misses	Write hits	Write to main memory	Block transfers
LOOP 1	3	17	20	0	20	3
LOOP 2	0	10	10	0	10	0
TOTAL	3	27	30	0	30	3

2. a. iii.

All of the block transfers below are performed in order to preserve spatial locality besides temporal locality.

- The first block transfer happens when a miss occurs during reading from $0008E. The entire main memory block starting from $00080 and ending at $0008F (Block 8) is transferred to cache memory. After that, reading from $0008F results in a hit since this word was in Block 8.
- Reading from $00090 is a miss since this address doesn't exist in cache memory. The entire memory block starting from $00090 and ending at $0009F (Block 9) is transferred to cache memory. Following read operations until $000A0 are hits since these addresses are already moved to cache within the scope of Block 9 transfer.
- Reading from $000A0 is the final read miss since this address doesn't exist in cache memory. The entire memory block starting from $000A0 and ending at $000AF (Block 10) is transferred to cache memory. The following read operation of $000A1 is a hit since this address is in Block 10.

2. b. i.

	Read misses	Read hits	Write misses	Write hits	Write to main memory	Block transfers
LOOP 1	3	17	2	18	20	5
LOOP 2	0	10	1	9	10	1
TOTAL	3	27	3	27	30	6

2. b. ii.

There are **six block transfers** during the flow. Half of them are read transfers and the other half are write transfers. Read transfers are the same as a. iii. but they will be explained briefly again.

LOOP 1

- First block transfer occurs when read $0008E operation is missed. The block from $00080 to $0008F (Block 8) is copied into cache memory.
- Another miss occurs when write $00119 operation is being handled. The memory block containing this address (Block 17) is updated in main memory and then brought to cash. This block contains addresses from $00110 to $0011F.
- The third block transfer takes place when a miss occurs during reading $00090. The memory block starting from $00090 (Block 9) is transferred into cache.
- Another miss occurs during write $00120 operation. The main memory block (Block 18) is updated and then copied into cache memory. This block starts from $00120 and ends at $0012F.
- The fifth block transfer happens when read $000A0 operation is missed. The block starting from $000A0 (Block 10) is copied into cache memory.

LOOP 2

- The final block transfer during program run is at loop 2. A write miss occurs at $00212. The memory block from $00210 to $0021F (Block 33) is updated and brought to cache. Since the ten required elements of array C are in this block, there aren't any other block transfers during loop 2.