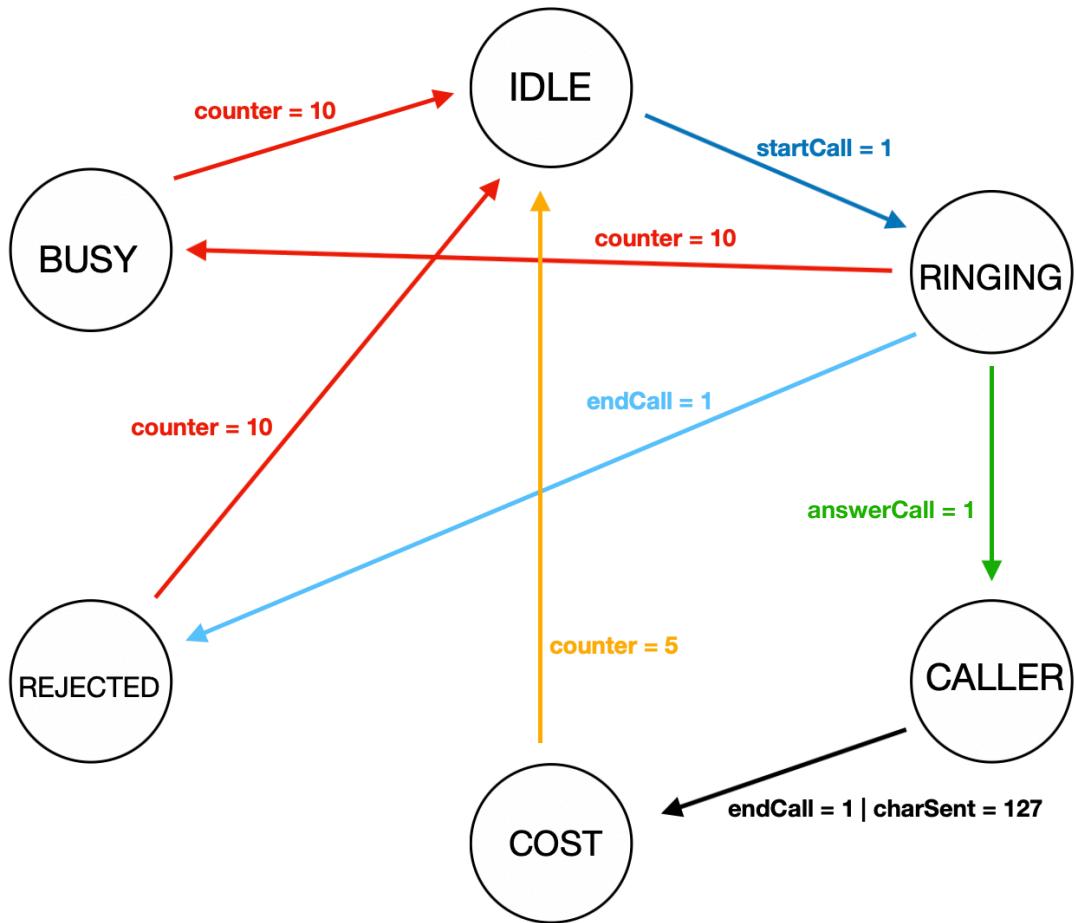
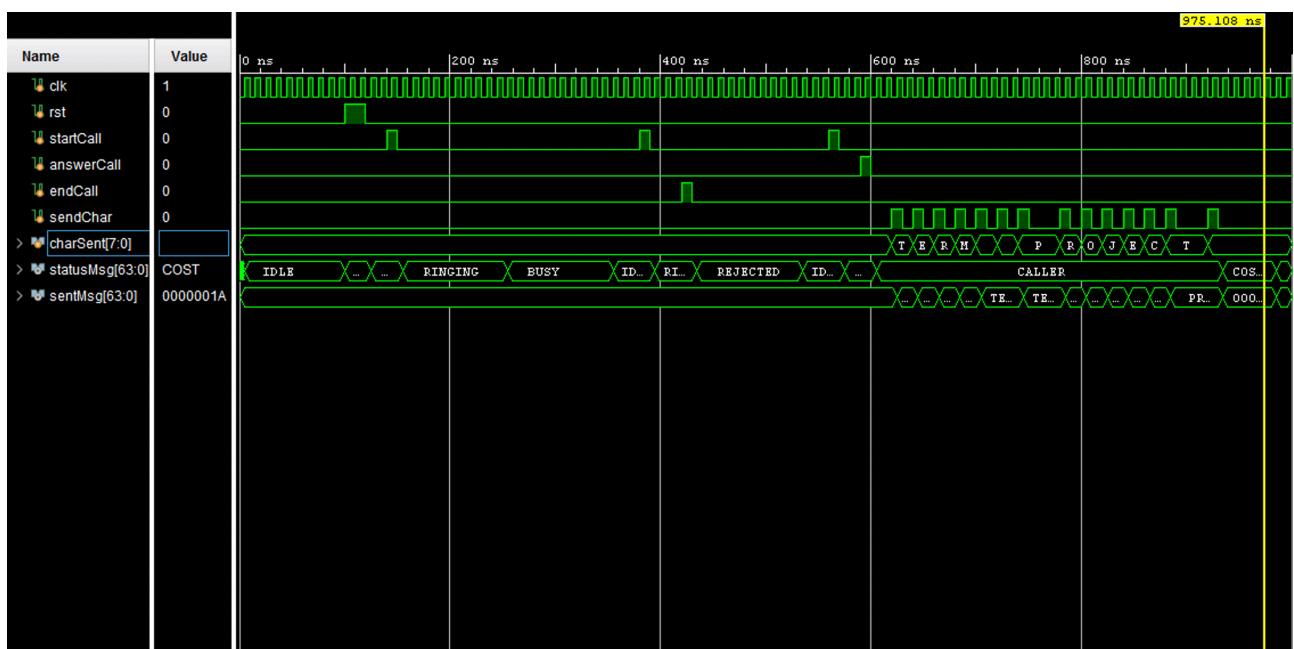


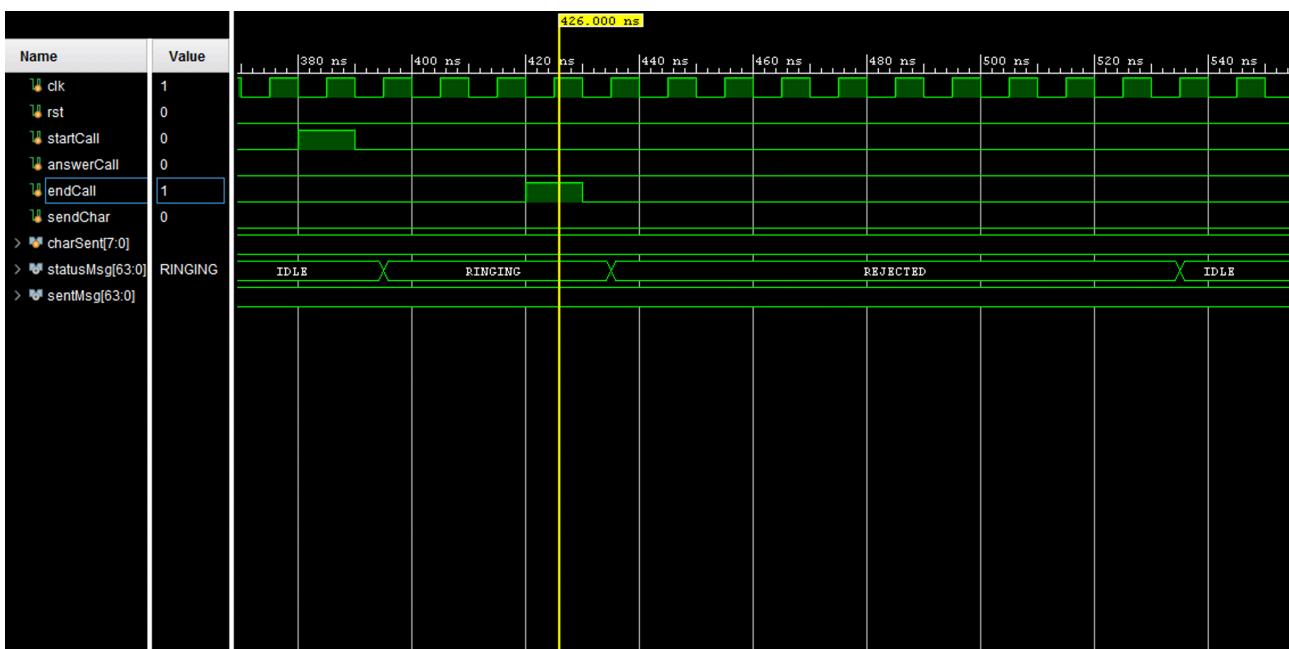
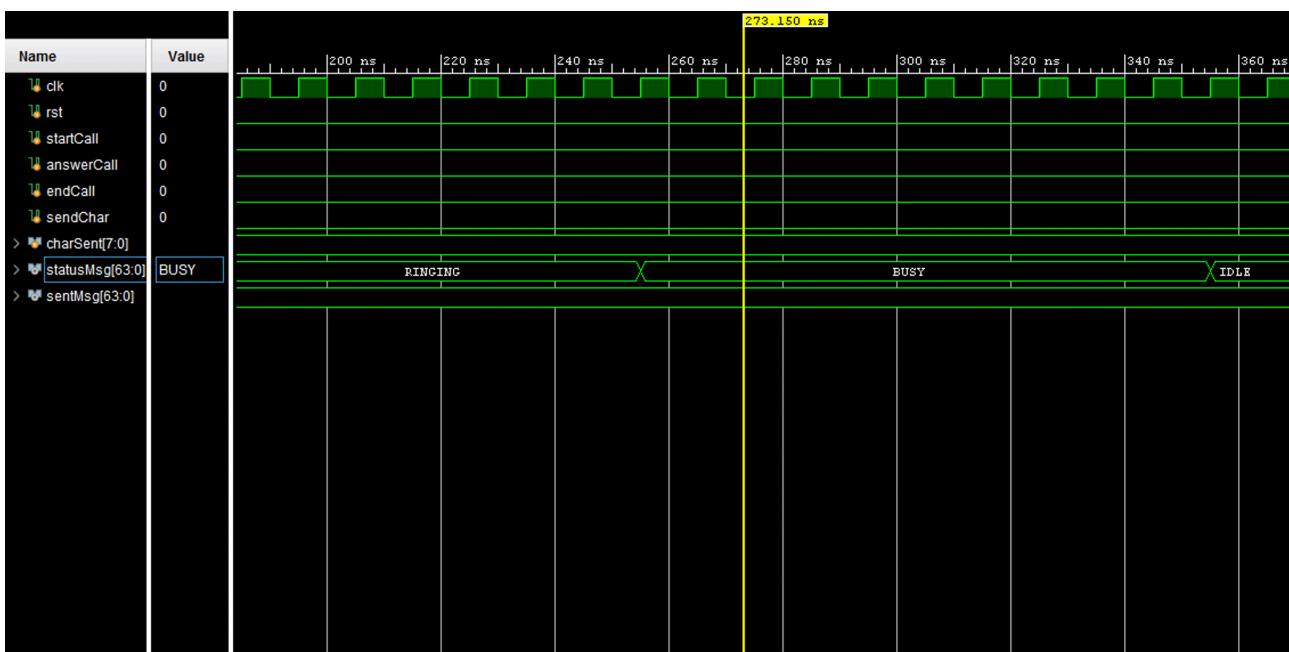
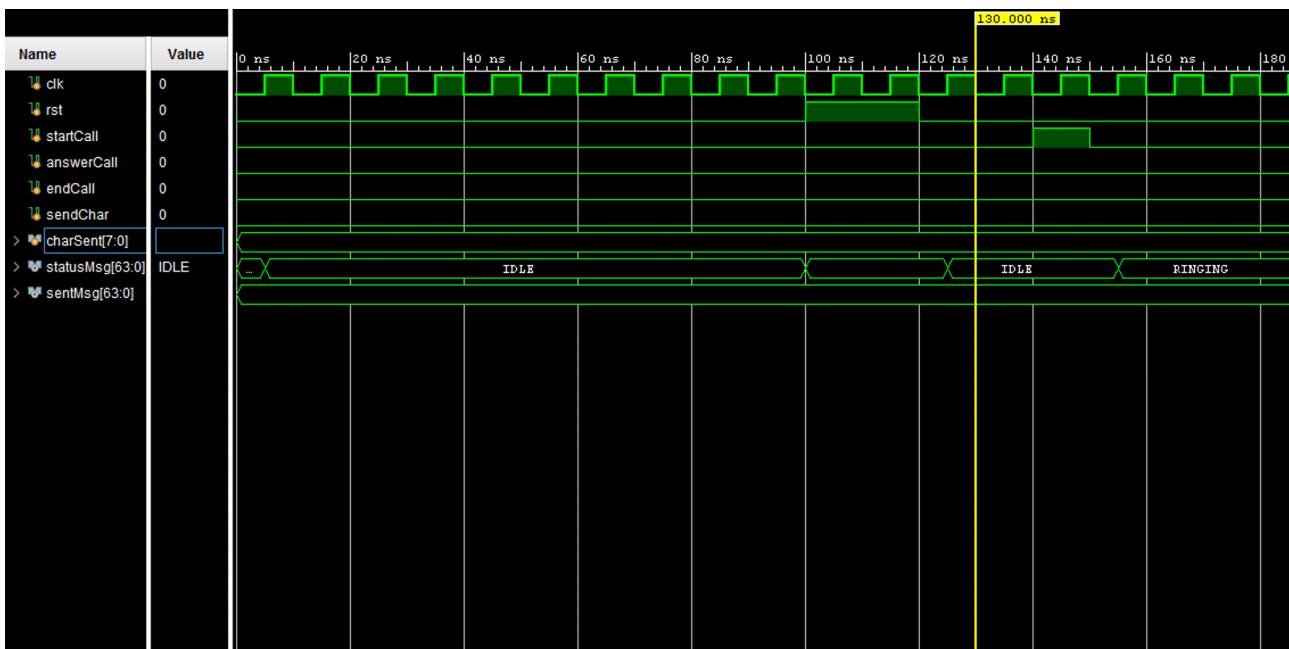
Term Project Report

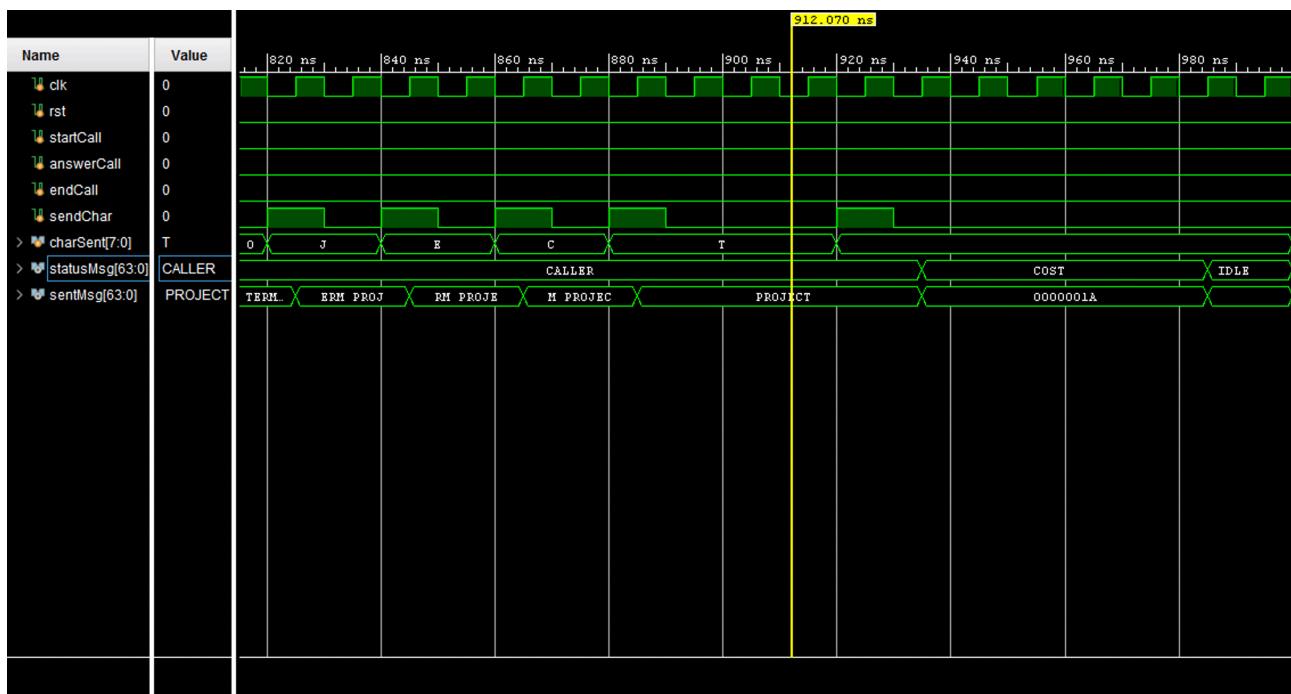
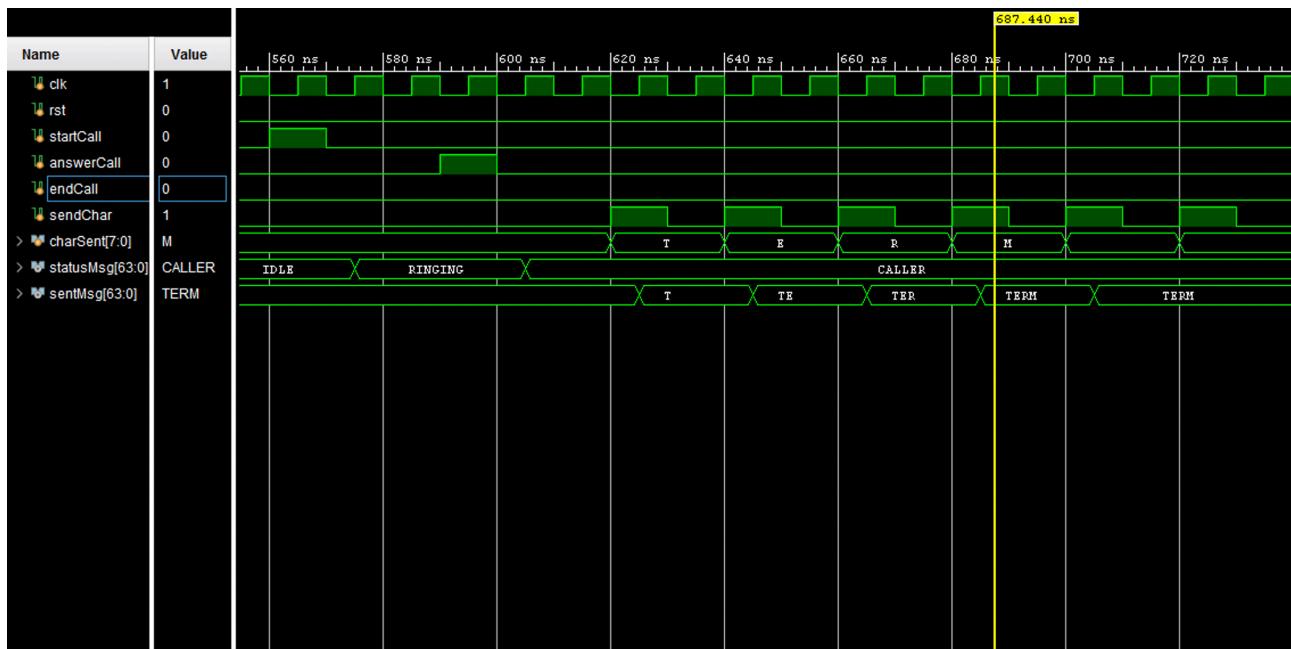
- An overview of the design with the states



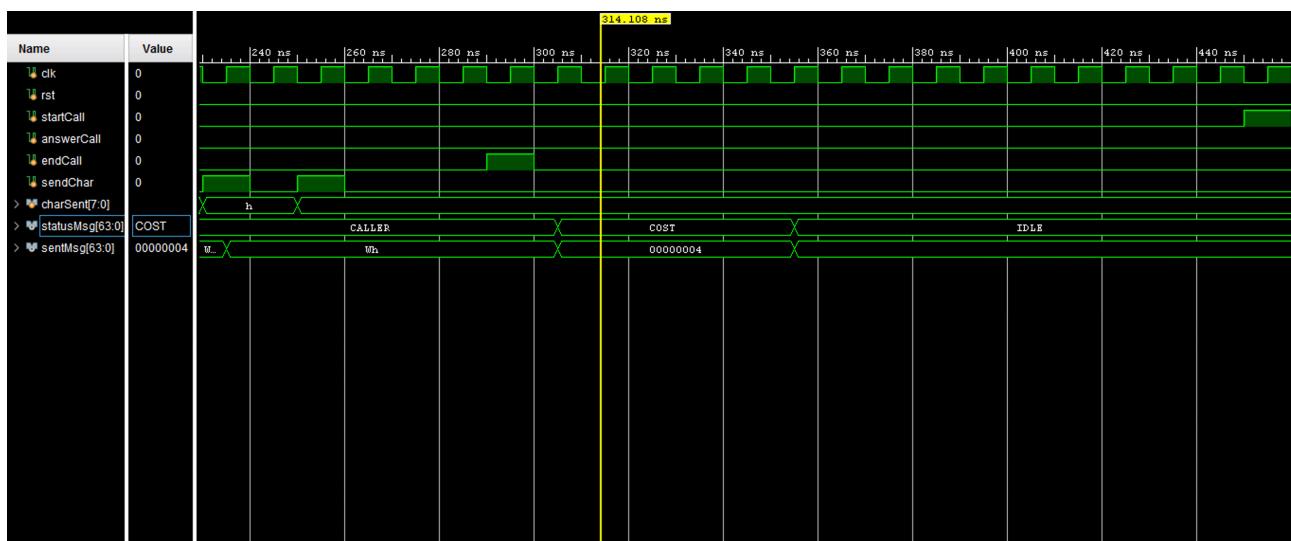
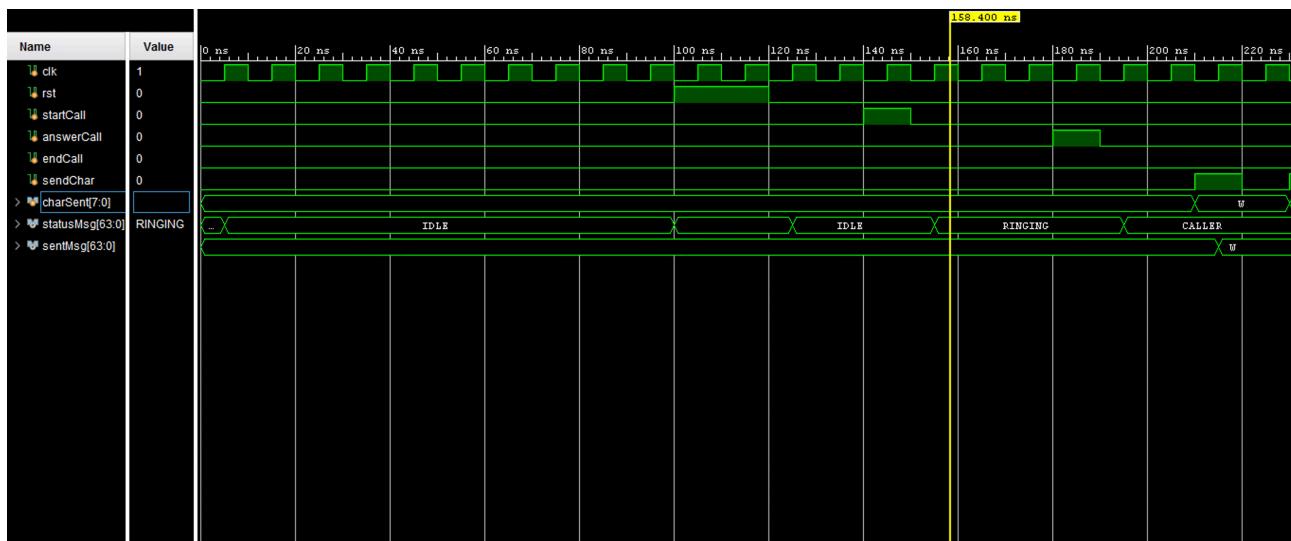
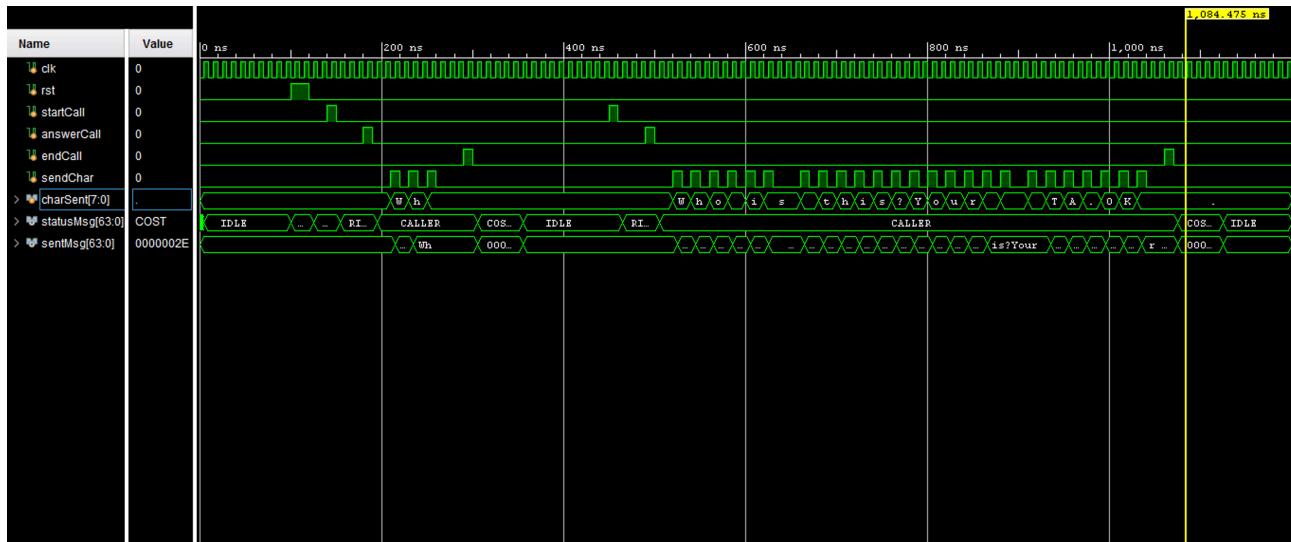
- Simulation results for tel_tb.v

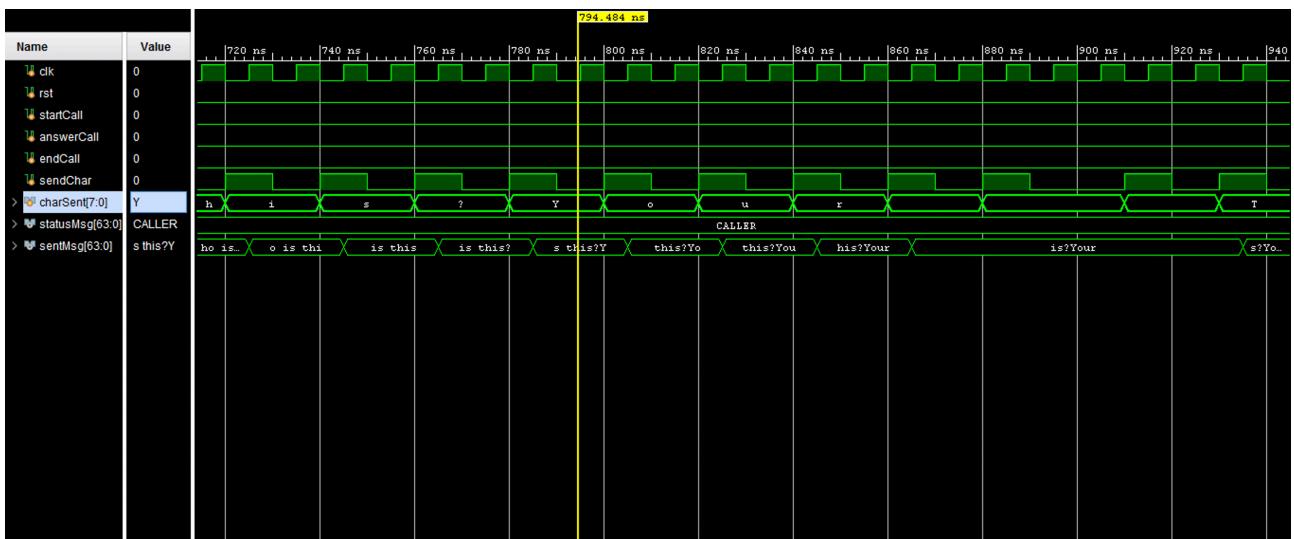






- Simulation results for tel_tb_2.v





- Synthesis results

Graph | **Table**

Resource	Estimation	Available	Utilization %
LUT	42	63400	0.07
FF	54	126800	0.04
IO	142	210	67.62
BUFG	1	32	3.13