Design of the *Nebula* Instruction Decoder

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1 Introduction

In the traditional five-stage RISC pipeline model, the purpose of the instruction decode (ID) stage is to translate the 32-bit instruction into smaller chunks of signals which can be passed to the control and execution units to direct and sequence the instruction's operations. Because the instruction decoder is directly responsible for translating the instruction encoding into "actionable" commands, it is here where the complexity of an instruction set is most felt. As such, it can range from a few basic constructions of look-up tables (LUTs) and multiplexers in RISC architectures to large, state machine-driven, microcoded instruction translators in CISC processors.

The RISC-V architecture is designed with the intent to be relatively simple to decode, and this feature is primarily expressed in the modularity of the instruction opcode layout.