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4/30/21
ECPE 136
Final Lab Report: 4-bit Synchronous Up Counter Design and Verification

INTRODUCTION

The objective of this lab is to successfully construct a 4-bit synchronous up counter using the Cadence software. The outline of this report will consist of the design approach to counter, the implementation of the counter in VLSI design, analysis of simulation results and performance measurements, and concluding remarks for the counter design.

The basic construction of a 4-bit synchronous up counter consists of 4 J-K Flip-Flops, each run on the same external clock pulse. 2-input AND gates are also used to feed in the input and output signals of previous J-k flip-flops and the output of the gates are fed as an input signal to successive J-K flip-flops. The block diagram for the 4-bit synchronous up counter is shown in figure 1. The output of each stage (J-K flip-flops) represents the bits. The least significant bit is the output of the 1st J-K flip-flop shown in figure 1. The most significant bit is the output of the last J-K flip-flop.

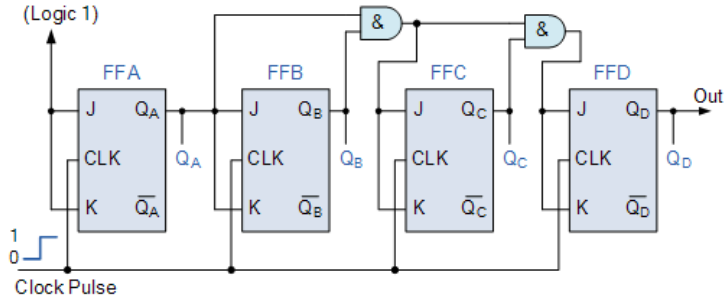

Figure 1: Block Diagram of a binary 4-bit synchronous up counter (electronics-tutorials 2018)

The typical waveform of the 4-bit synchronous up counter is shown in figure 2. Every positive edge of the clock signal results in the counter incrementing up 1 bit at a time. The 4-bit counter is expected to count from 0 to 15.

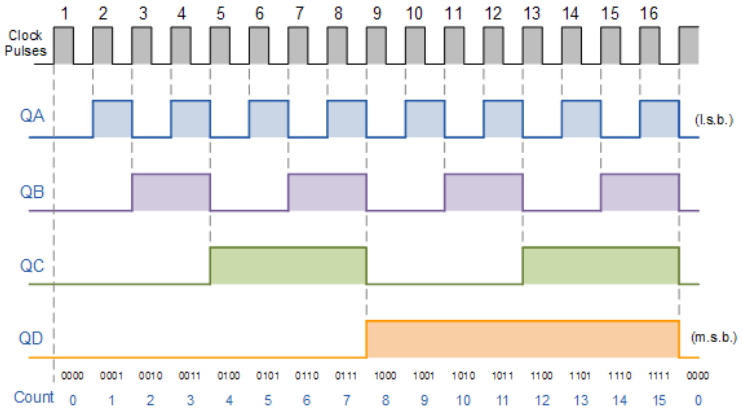

Figure 2: Expected Waveform Timing Diagram for 4-bit synchronous counter (electronics-tutorials 2018)

DESIGN

The design approach for the counter integrated circuit is to first construct the circuitry for a J-K Flip-Flop. Figure 3 shows the logic diagram that will be used for the construction a master-slave J-K Flip-Flop. The reason behind this design approach is that we want the outputs to change with the same clock edge that latches data in, hence this allows for a more controllable delay on the Master-Slave output. Ideally, the only delay that the IC experiences is in the internal propagation delay (Computer Science Simplified 2007). Also, the decision for a master-slave approach was the advantage of not worrying about making the proper adjustments to the threshold voltage of inverters and other gates (Analog, VLSI, and Devices Laboratory 2003). All of the previously mentioned reasons justify my decision to use the master-slave J-K Flip-Flop approach. The construction of a typical master-slave J-K Flip-Flop uses two 3-input NAND gates, six 2-input NAND gates, and two inverters attached in a feedback loop.

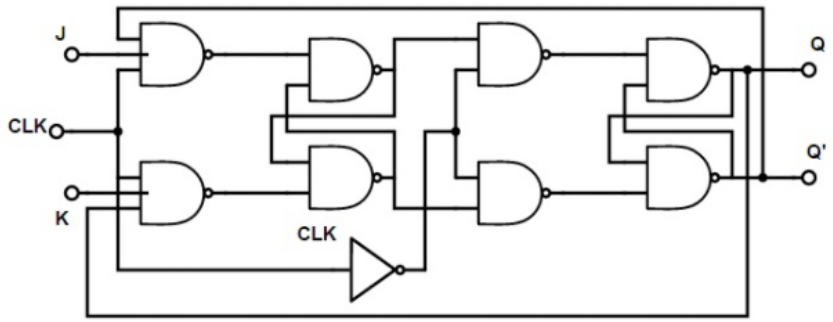

Figure 3: Logic Diagram of a master slave J-K Flip-Flop (Electronics Hub 2017)

To add an additional layer of complexity my design approach, I will incorporate RESET functionality to the construction of the J-K Flip-Flop. Figure 3 does not show the additional input logic required for the implementation of RESET; however, the modified schematic that does meet this specific requirement is shown and discussed in figure 4.

R	J	K	Q_{n+1}
0	0	0	Q_n
0	0	1	0
0	1	0	1
0	1	1	$\overline{Q_n}$
1	–	–	0

Table 1: Truth table for J-K Flip-Flop with RESET

The expected input-output combinations for the master-slave J-K Flip-Flop with a RESET function are tabulated in Table 1. The flip-flop operates normally when the RESET input signal R is a logic 0. If the input signal R is a logic 1, the output Q is forced to be 0 regardless of the input levels of J and K.

After the construction of the proposed J-K Flip-Flop design as shown in figure 4, we can then use 4 instances of the J-K flip-flops alongside three 2-input AND gates to create a functioning 4-bit synchronous up counter, similar to what is shown in figure 1, with the addition of a RESET input. Overall, the input signals driven into the IC will be the RESET and CLK signals. The CARRYOUT signal as well as the 4 Bit signals are all outputs of the IC. Table 2 shows the expected input-output combinations of the proposed counter design. The CARRYOUT signal can be used to drive additional J-K Flip-Flops if we wish to expand the number of bits that the counter can handle.

RESET	CARRYOUT	Bit 3	Bit 2	Bit 1	Bit 0	Number
0	0	0	0	0	0	0
					1	1
				1	0	2
					1	3
			1	0	0	4
					1	5
				1	0	6
					1	7
		1	0	0	0	8
					1	9
				1	0	10
					1	11
			1	0	0	12
					1	13
				1	0	14
	1				1	15
1	0	0	0	0	0	0

Table 2: Truth table for the 4-bit synchronous up counter with RESET and CARRYOUT

IMPLEMENTATION

The modified circuit shown in figure 4 includes two additional gates. The extra AND gate ties the J signal with the inverted RESET signal as inputs, which will then drive one of the inputs of the top 3-input NAND gate of the master-slave flip-flop. The extra OR gate ties the RESET signal with the K signal as inputs, which will drive one of the inputs of the bottom 3-input NAND gate. The addition of the extra gates ensures that that the J-K Flip-Flop operates normally whenever the RESET signal is low, else the output of the flip-flop is forced to the value of 0.

All of the gates in figure 4 use a sizing of $3\mu m$ for the n-MOS and p-MOS widths. The reasoning behind making all the widths $3\mu m$ across all transistors was because I already designed most of the logic gates with those specific widths in previous labs. The Inverters, 2-input NAND gates, 2-input AND gates, and 2-input OR gates were all previously designed with $3\mu m$ widths. For simplicity sake, I designed the 3-input NAND gates with those same widths in mind. As evidenced by successful simulation of the 4-bit counter in the Results section of this report, the decision to continue using $3\mu m$ widths do not negatively impact the functionality of the IC and helps in keeping the total size of the IC to a minimum.

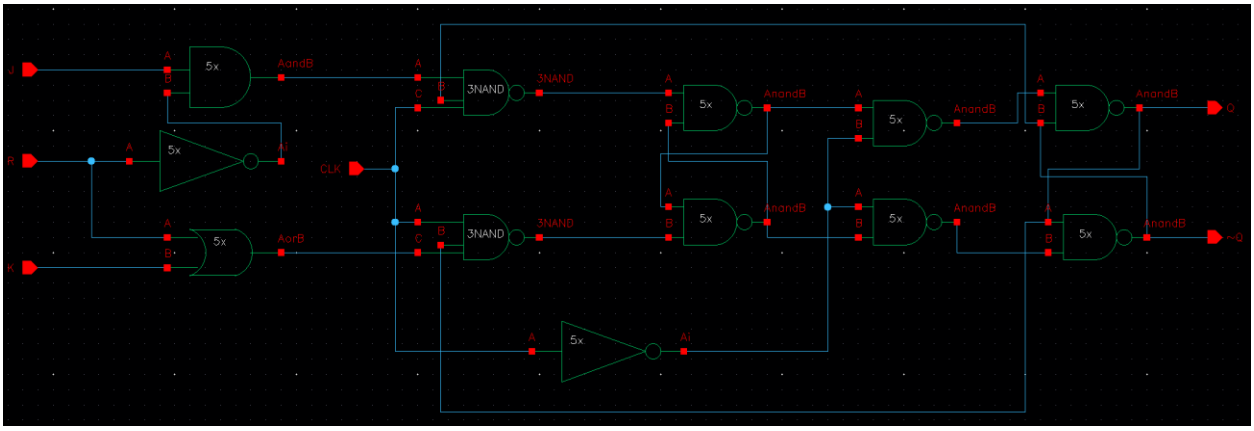

Figure 4: Schematic of J-K Flip-Flop

The layout view of the J-K Flip-Flop is shown in figure 5. The design used the AMI $0.6\mu m$ process with $3\mu m$ widths for the p-MOS and n-MOS. The height of the design is $30\mu m$ from the top of the n-tap to the bottom of the p-tap region, this provides a sufficient amount of space to wire connections between logic gates. Starting from the top-left of figure 5 to the top-right, the first NAND gate and inverter represents the 2-input AND gate, the second inverter ties the RESET signal with the input of the first AND gate, next is the 3-input NAND gate, followed by three 2-input NAND gates. Starting from the bottom-left to the bottom-right, the first NOR gate and inverter represents the 2-input OR gate, the second inverter ties the CLK signal to two 2-input NAND gates, next is the other 3-input NAND gate, followed by another three 2-input NAND gates. The overall layout shown in figure 5 does match the netlists of the schematic from figure 4, but there could be improvements to either placement of m1_poly vias or the wiring in general.

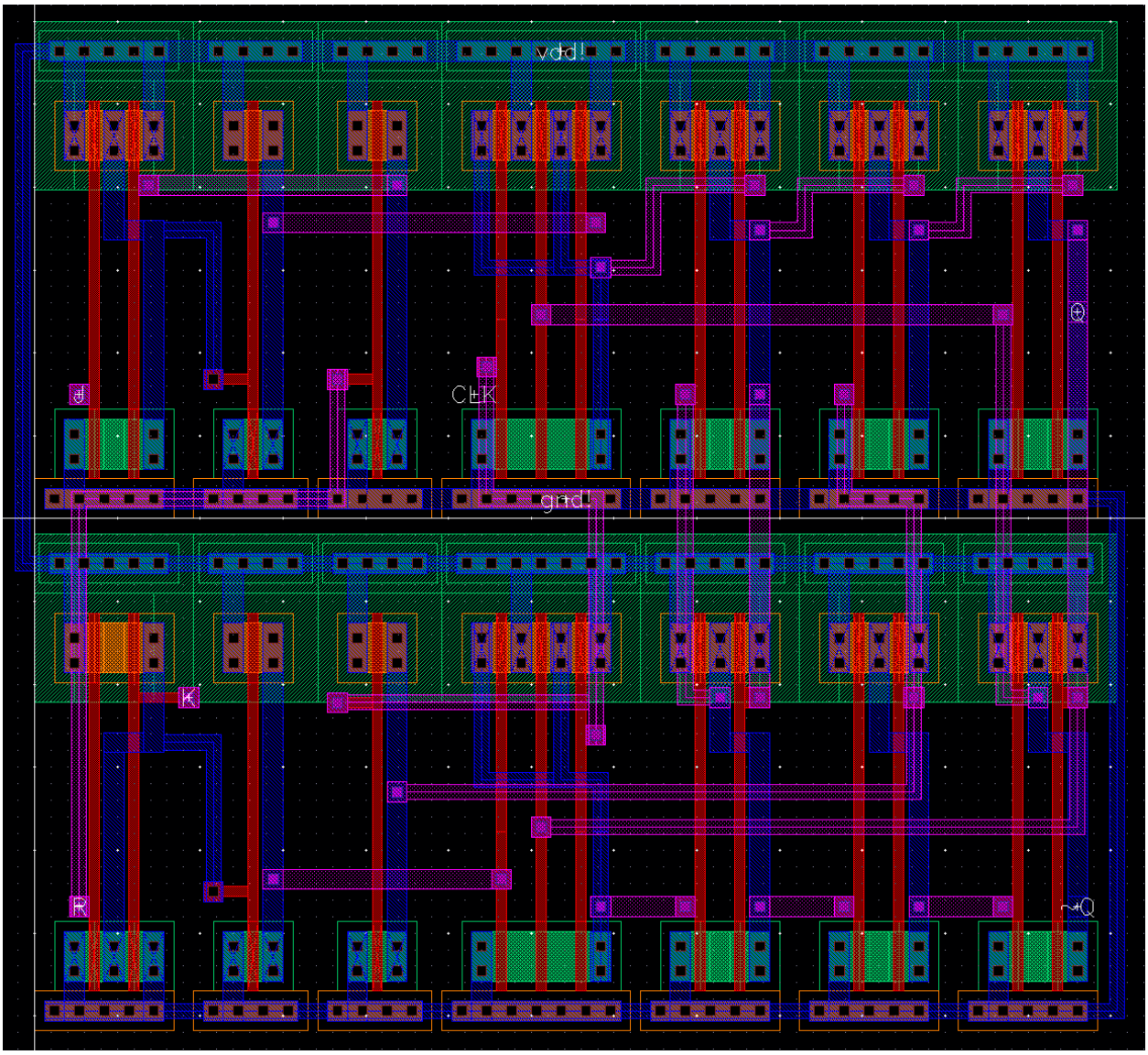

Figure 5: Layout of J-K Flip-Flop

The schematic used to simulate the functionality of the J-K Flip-Flop is shown in figure 6. The frequency of the CLK input signal was 200MHz. The RESET input signal had a pulse width of 10ns and a period of 80ns, this ensures that the J-K flip-flop has a sufficient amount of time to see most of the input-output combinations until the output Q_n is forced back to a 0. The frequency of the J input signal was 100MHz and the frequency of the K input signal was 50MHz. All of the input pulse signals have a peak voltage of 5V. The outputs Q_n and $\overline{Q_n}$ are both connected to 200fF capacitors each. A parametric sweep analysis was conducted on the value of the capacitors from 0fF to 200fF, but results showed that there were no noticeable differences in the output waveforms. This could have been a result of the latching characteristics of the master-slave flip-flop configuration that prevented any parasitic delays.

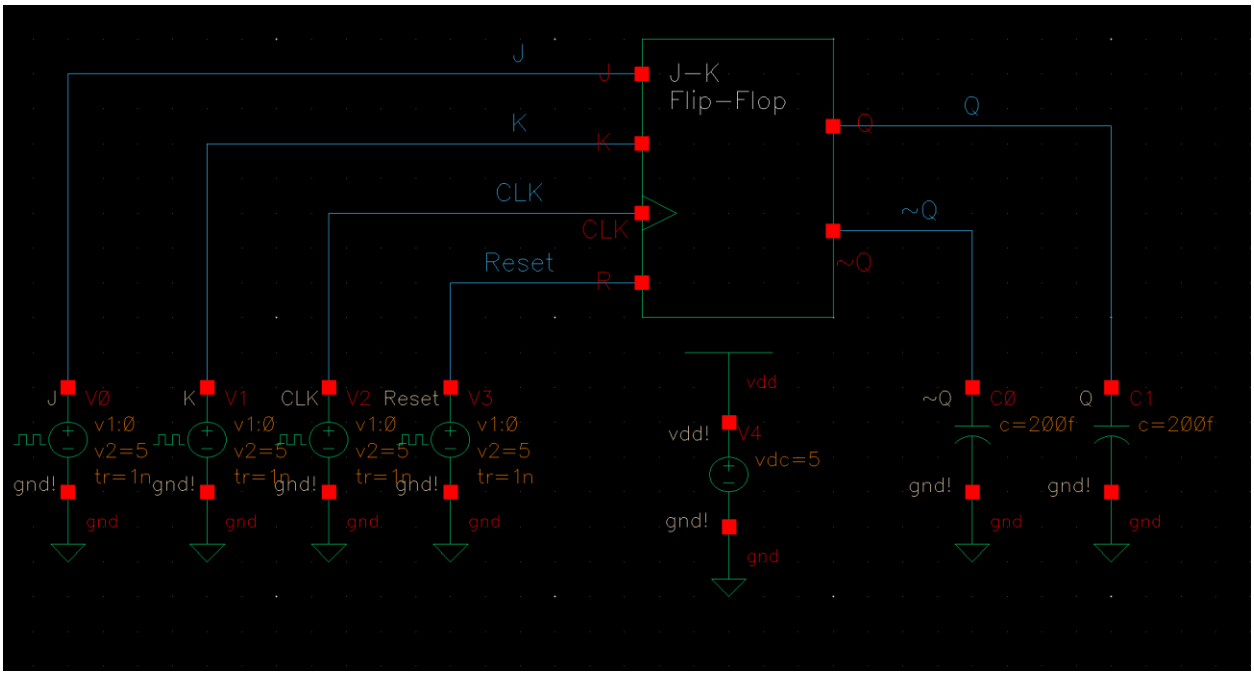

Figure 6: Schematic used to simulate the functionality of the J-K Flip-Flop

After the successful verification of the J-K Flip-Flop, the construction of the 4-bit synchronous up counter was finally possible. Figure 7 shows the schematic view of the proposed up-counter using 4 instances of the J-K flip-flop circuit. The CLK and RESET input signals are fed into each of the 4 flip-flops. Vdd is attached to the first flip-flop through inputs J and K; this flip-flop represents the least significant bit and is connected high to allow the flip-flop to toggle on every clock pulse. The addition of the 2-input AND gates are used to generate the required logic for the J and K inputs for each successive stage in the counter. Output pins B0, B1, B2, B3, and CARRYOUT are attached at the output of each stage; this allows us to see the bits toggling on and off during the transient analyses. The ~Q output signals are not used since the up-counter design only uses the Q signals. If our design was a down-counter, then the ~Q signals would be used instead.

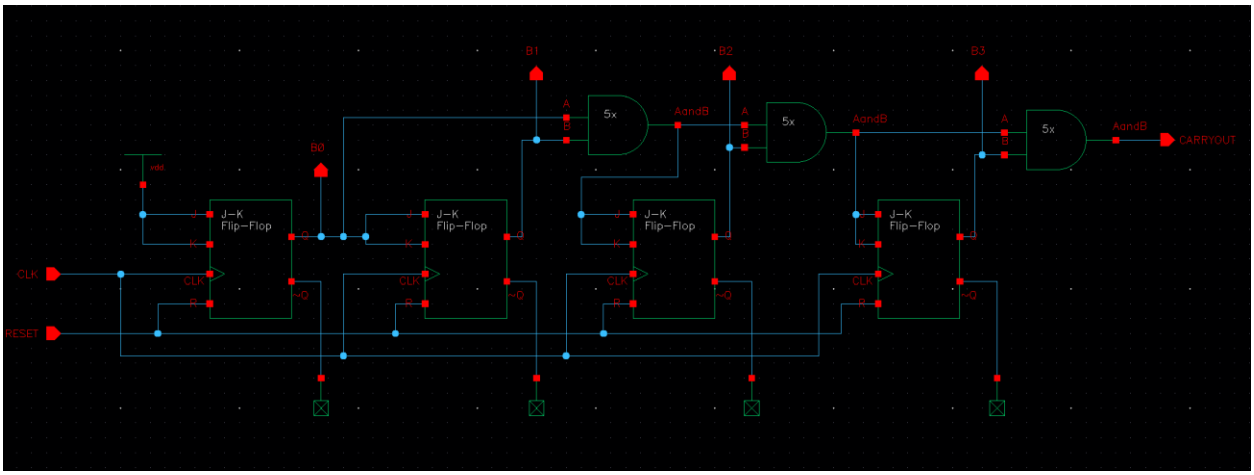

Figure 7: Schematic of 4-bit up counter

The layout design of the counter used 4 instances of the J-K flip-flop layouts as well as 3 instances of the 2-input AND gate layouts. Visually it may be difficult to tell in the layout shown in figure 8, but two of the AND gates are sandwiched in between the first 2 flip-flops and the last two flip-flops. The last AND gate is attached at the very end of the layout. Additional metal 2 wiring was necessary to tie the additional AND gates to make the logic work. Also, metal 3 was used in the layout to tie the CLK and RESET signals to all of the flip-flops. Metal 3 was also used to bridge any logic that metal 2 could not have; this ensured that there was no short circuiting of any of the metal 1 or 2 wiring.

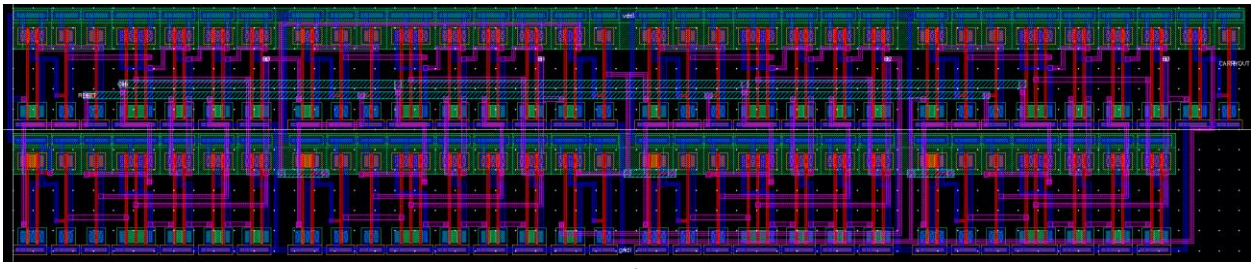
Figure 8: Layout of 4-bit up counter

The netlists of the extracted view and schematic view of the 4-bit synchronous up counter matched. An image of the ‘si.out’ file showing successful LVS verification is shown in figure 9.

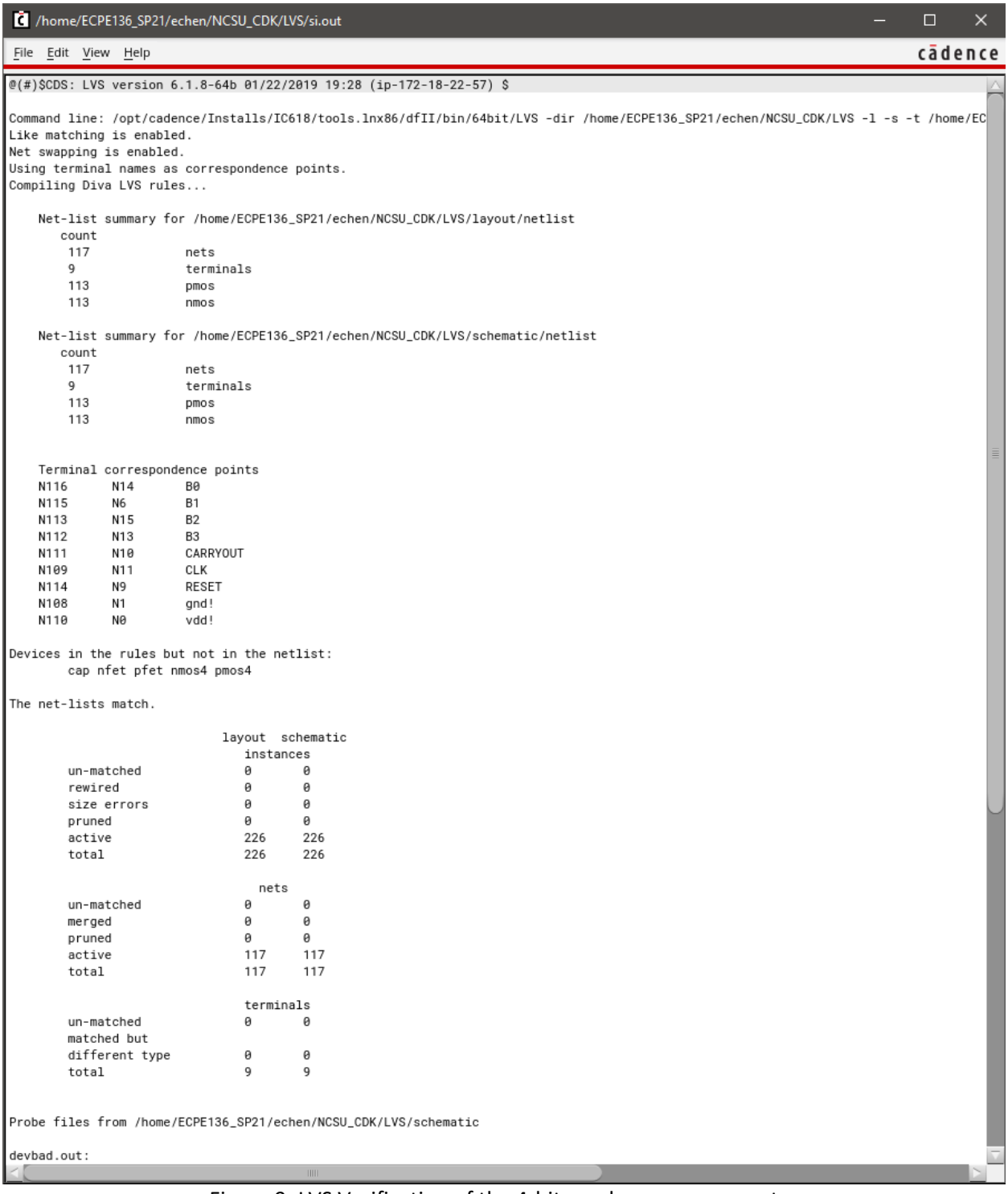

Figure 9: LVS Verification of the 4-bit synchronous up counter

Figure 10 shows the schematic used to simulate the functionality of the counter. The IC takes in two input signals, CLK and RESET. The output signals are labelled B0 to B3 and CARRYOUT. B0 is the least significant bit and B3 is the most significant bit. The CARRYOUT bit outputs a logic 1 whenever the counter exceeds 15 in decimal. Future expansion of the 4-bit counter can use this carryout signal as an input to more J-K Flip-Flops. The CLK signal runs at 50MHz and the RESET signal has a pulse width of 100ns but as a period of 800 ns to ensure there is a sufficient amount of time for the counter to reach a minimum count of 15 before the counter resets back to 0. The Load capacitances for all the output signals were kept at 200fF because the master-slave configuration of all the J-K flip-flops supposedly cause internal propagation delays and any parasitic delays may be negligible.

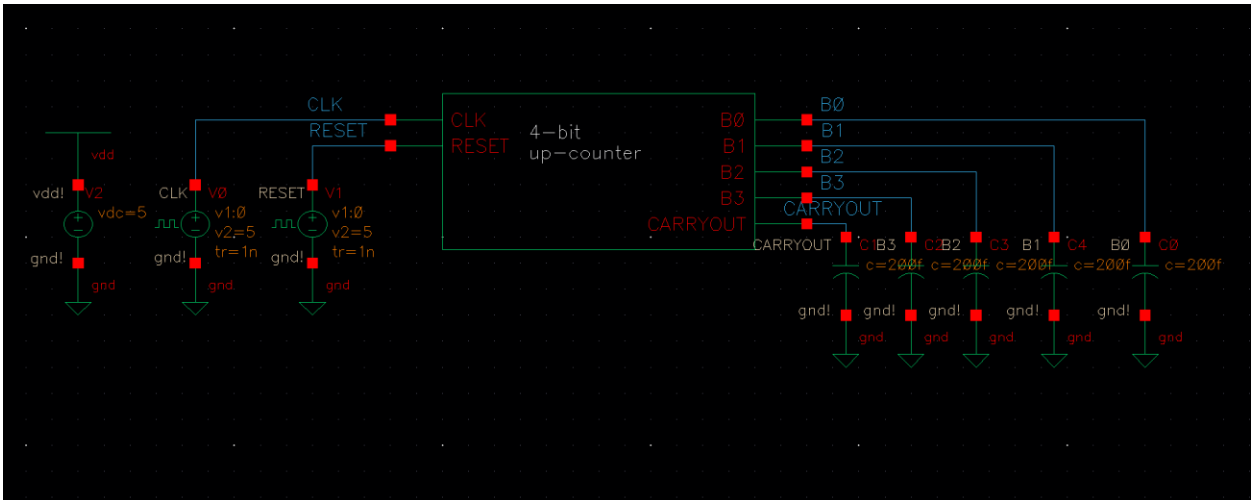

Figure 10: Schematic used to simulate the functionality of the 4-bit up counter

RESULTS

The output waveforms of the J-K Flip-Flop itself are shown in figure 11. The functionality of the J-K Flip-Flop has been validated since the input-output logic of the waveforms match the truth table from table 1. The only thing to note when trying to read the waveforms is that it takes one additional clock cycle for the design to actually switch as expected. For example, when RESET goes high around 80 ns, Output Q does not go low like expected. Not until one clock cycle later at around 90 ns will the flip-flop register the RESET signal and cause the output Q to go low. This scenario can be seen for all input-output combinations, as it takes around 10 ns for things to switch properly. The delay in switching is also evidenced by figure 12, in which the worst-case propagation delays can be seen visually.

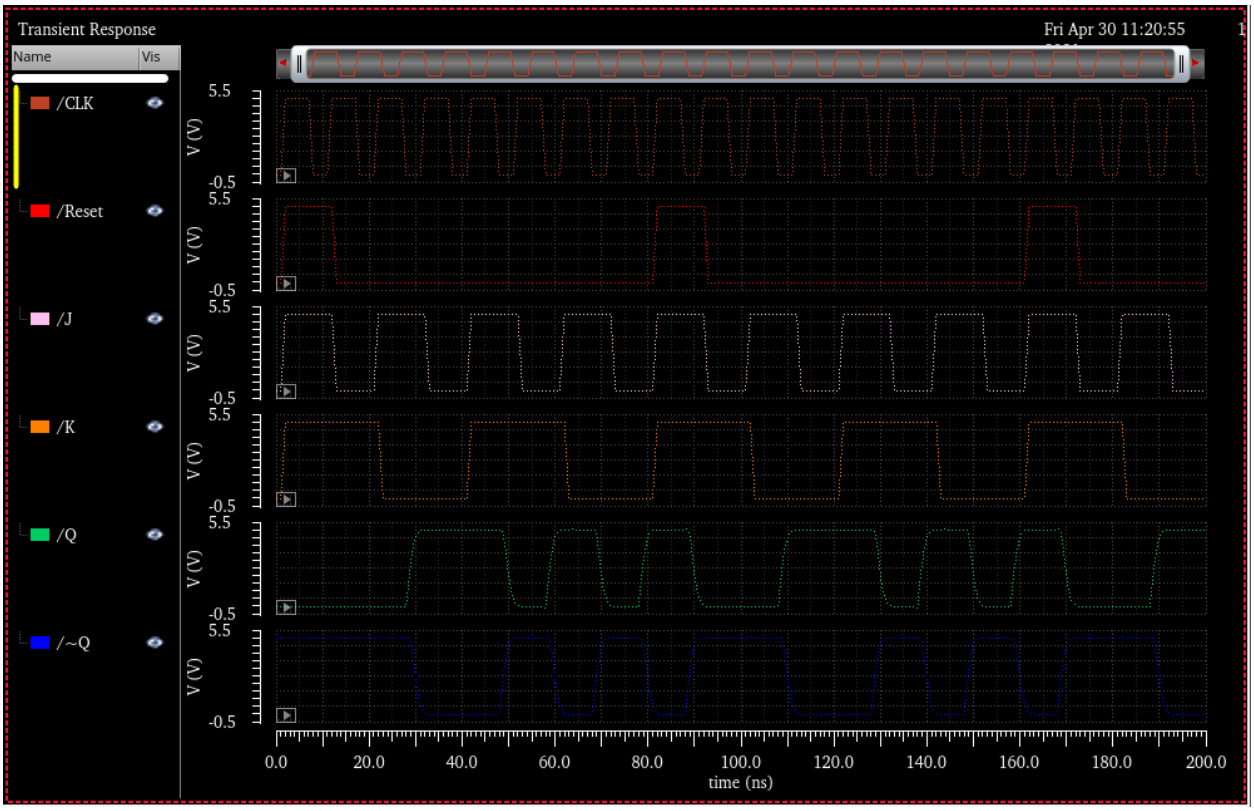

Figure 11: Waveforms of J-K flip-flop extracted view

The worst-case rising propagation delay of output Q seems to appear from roughly 20 ns to 30 ns of simulation time. The worst-case falling propagation delay of output Q seems to appear from 40 ns to 50 ns of simulation time. There was no particular reason behind using the K input signal over all other inputs to compare the propagation delay with output Q; all the input signals switch on the same clock pulse. I am also only looking at the propagation and switching times for the Q output signal and not ~Q output signal because ~Q will not be used in the design of the 4-bit synchronous up counter.

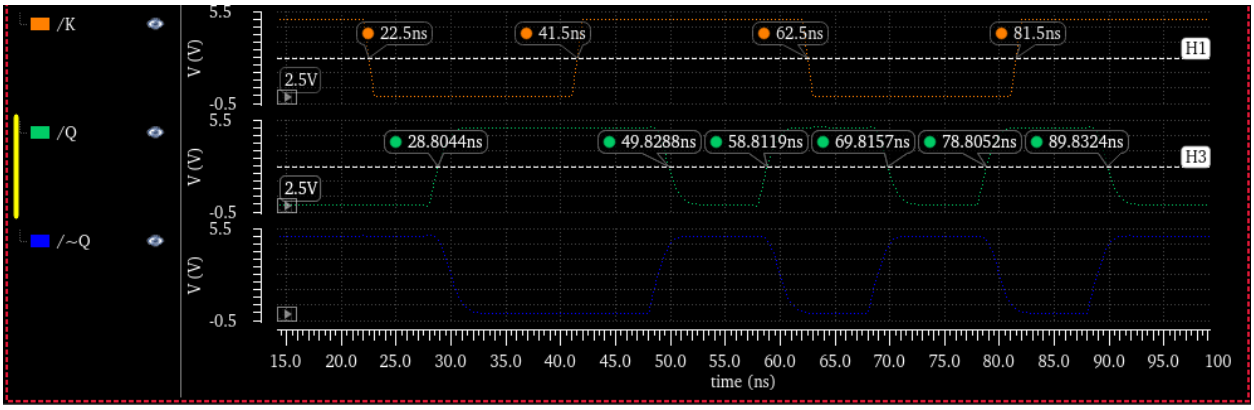

Figure 12: Comparison of Propagation Delay times between Input K signal and Output Q signal

The exact worst case rising and falling propagation delays are tabulated in table 3. The worst-case rising time for the output Q can be seen in figure 13 around 58 to 60 ns of simulation time. The worst-case falling time was around 48 to 51 ns of simulation time. The rising and falling times are tabulated in table 3 as well. The worst-case switching time appears to be roughly 2 ns for the J-K Flip-Flop.

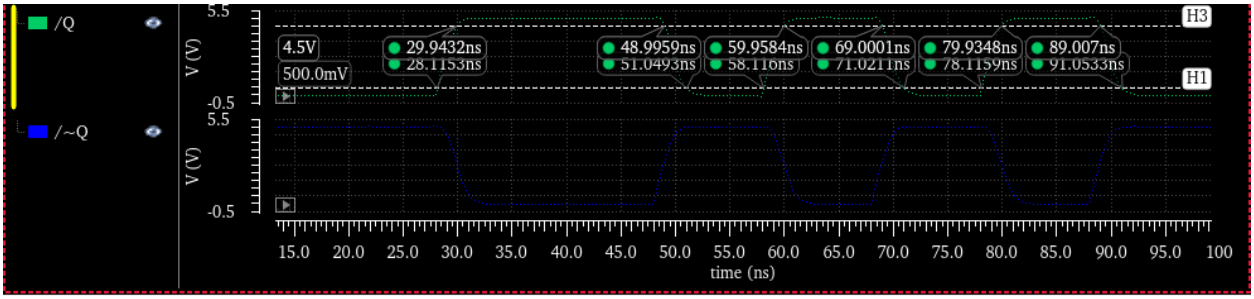

Figure 13: Comparison of Rise and Fall Delay times of Output Q signal

Rising Propagation Delay	6.3044 ns
Falling Propagation Delay	8.3324 ns
Rising Time	1.8424 ns
Falling Time	2.0534 ns
Switching Time	1.9479 ns

Table 3: List of Propagation and Switching Delays of output Q of the J-K Flip-Flop

Figure 14 shows the output waveforms for the 4-bit synchronous up counter. The input-output combinations shown in figure 14 agree with the expected input-output combinations listed in table 2. This means that the design of the counter was successful. Similar to the waveform from figure 11, figure 14 also shows that there is a delay, around 1 clock cycle in which there is no switching in the outputs; not until another cycle later do the signals change as expected.

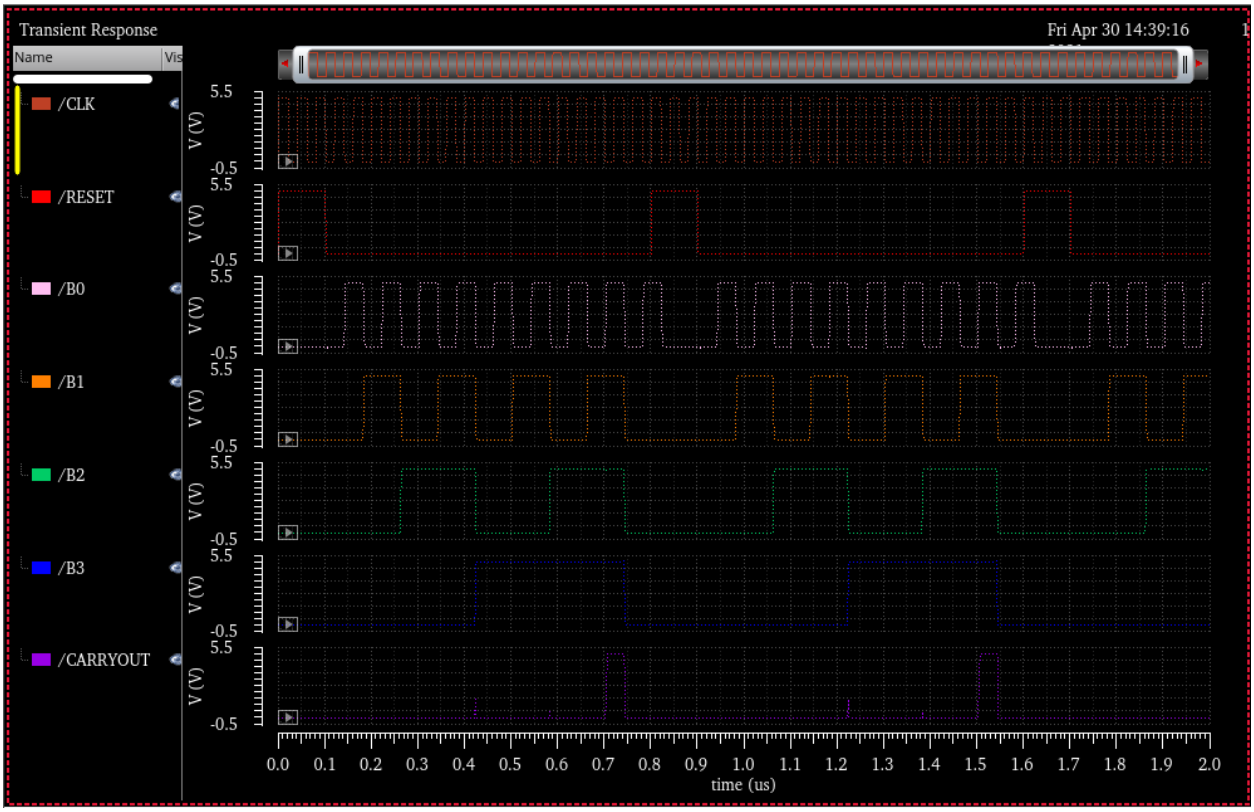

Figure 14: Waveforms of 4-bit synchronous up counter extracted view

Since there are lots of transitions between signals and the fact that we may have to account for all the various propagation delays and switching times of each bit (almost every output is chained to an input), it would be less intuitive to show a figure, and more intuitive to display the data in table 4. An interesting trend is that the more significant bits experience less of a propagation delay as well as a faster switching time than the less significant bits. Overall, these delays dwell in the nanoseconds, which I believe could be faster. There may be more underlying design decisions that could most likely improve the switching speed as well as lessen the propagation delay of the counter, but for the main purposes of building a functional counter in this lab, these results look decently promising.

	Bit 0	Bit 1	Bit 2	Bit 3	CARRYOUT
tdpr	1.416 ns	1.3515 ns	1.3509 ns	1.3512 ns	3.11195 ns
tdpf	1.5608 ns	1.5224 ns	1.5211 ns	1.4917 ns	2.39852 ns
trise	1.65607 ns	1.52812 ns	1.5279 ns	1.527 ns	1.8135 ns
tfall	2.1317 ns	1.9421 ns	1.9428 ns	1.943 ns	0.9633 ns
tswitch	1.8933885 ns	1.73511 ns	1.73535 ns	1.735 ns	1.3884 ns

Table 4: List of Propagation and Switching Delays for each bit of the 4-bit synchronous up counter

CONCLUSION

The design of the 4-bit synchronous up counter using Cadence was successful, and the functionality of the design was validated by simulations. The components that made up the counter were 4 instances of the J-K Flip-Flops and other logic gates consisting of: NAND, OR, AND, and inverters. Each of the logic gates were chosen with $3\mu m$ wide p-MOS and n-MOS transistors, which served as an adequate sizing for the design of the flip-flops and overall counter. Although the use of $3\mu m$ sizing was chosen, there a question that arose the analysis of the delay times of the counter. If I had used $6\mu m$ p-MOS transistors, how would this design decision affect the creation of the layout? Does the also cause a positive or a negative difference in the delay times? Another question that arose when verifying the functionality of the counter. It was seen in figures 11 and 14 that it takes around a full extra clock cycle for the output signals to switch when expected to. This could have been caused by the configuration of the master-slave J-K Flip-Flop configuration, in which the latching may have caused the delay. Despite all these issues and suggestions for further improvements to the design, the objective of this lab was met, as the design and verification of the proposed 4-bit synchronous up counter were accomplished.

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