ECPE 135 Project Report

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26 April 2022

Introduction

The objective of this project was to implement a $12V$ input $5V$ output, $0.75W$ buck converter with a switching frequency of $100kHz$. This report contains schematic diagrams of the system, calculations pertaining to expected buck converter behavior, discussion about component selection for the converter and 555 timer, and the results of circuit testing.

Schematic

The buck converter schematic in figure 1 shows the selection of R and C values needed to produce a ripple less than $0.1V$ under full load conditions. The schematic for the switch mechanism is shown in figure 2.

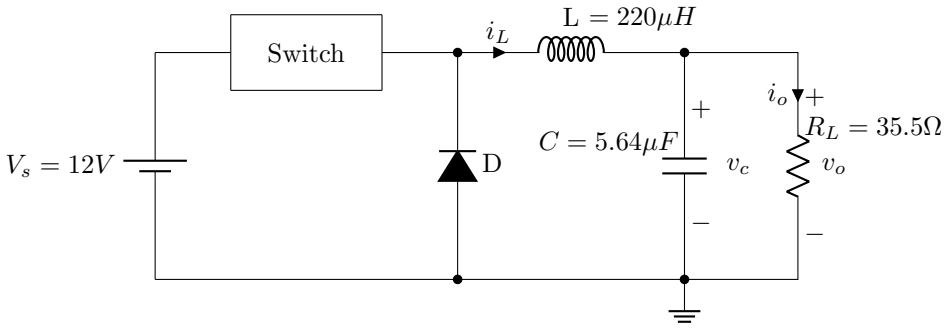

Figure 1: Buck Converter Schematic

The R and C values shown in figure 2 were used in the 555 Timer circuit to produce a $100kHz$ switching frequency and a duty cycle that results in an average $5V$ output from converter.

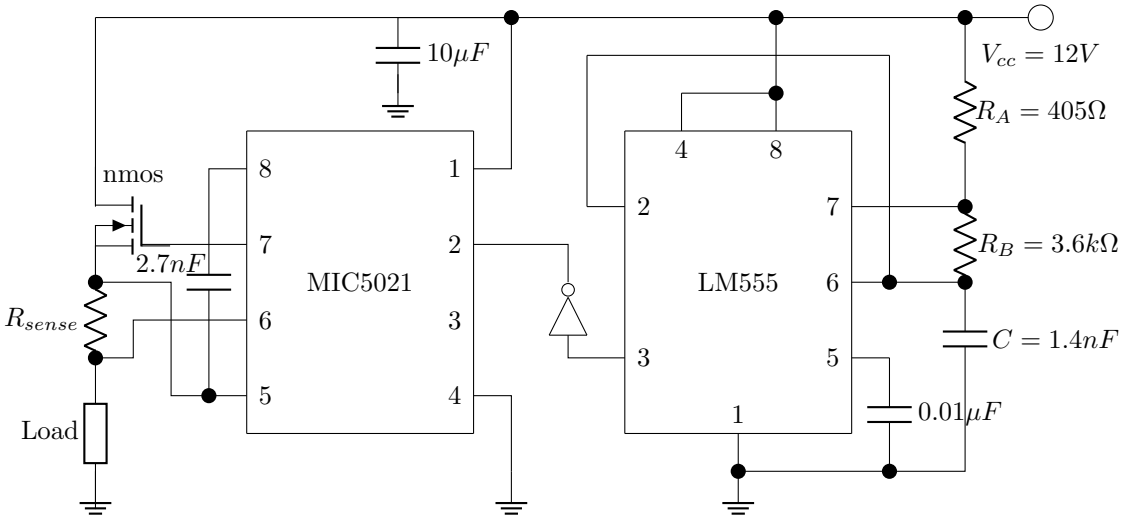

Figure 2: High-Side Driver and 555 Timer Schematic for MOSFET Switching

Calculations

Let the average output voltage $V_o = 5V$ and the source voltage $V_{in} = 12V$. The expected duty cycle of the ideal buck converter is

$$D = \frac{V_o}{V_{in}} = \frac{5V}{12V} \approx 0.417$$

The switching frequency of the converter is $F_s = 100kHz$. Let the switching period $T_s = \frac{1}{F_s} = 10\mu s$. Also let $220\mu H$ be the inductance. The expected ripple current value is

$$\Delta i_L = \frac{V_o(1-D)T_s}{L} = \frac{5V(1-0.417)(10\mu s)}{220\mu H} \approx 0.133A$$

The output voltage ripple of the converter needs to be limited to less than $0.1V$ under full load conditions. The equation for computing output voltage ripple is

$$\Delta V_o < \frac{T_s \Delta i_L}{8c} \qquad -(1)$$

This equation can be rewritten in terms of c to solve for the capacitance required to limit the voltage ripple. Let $V_o = 0.1V$ and solve the inequality for c.

$$c > \frac{T_s \Delta i_L}{8\Delta V_o} \Rightarrow c > \frac{(10\mu s)(0.133A)}{8(0.1V)} \Rightarrow c > 1.656\mu F$$

Buck Converter Component Selection

The Load resistor value that satisfies the $0.75W$ $5V$ output conditions can be calculated using the equation

$$R_L = \frac{{V_o}^2}{P_o} = \frac{(5V)^2}{0.75W} \approx 33.33\Omega$$

Since the expected output power is $0.75W$ and the resistors of choice are rated for a maximum $0.25W$, the load resistor was constructed using 3 12Ω resistors in series. The measured load resistance was 35.5Ω.

Recall that a capacitance $c > 1.656\mu F$ is required for the converter to sustain an output voltage ripple of less than $100mV$. The capacitors chosen for the build was a ceramic capacitor with a value $c_{ceramic} = 1.338\mu F$ and an electrolytic capacitor with a value $c_{electrolytic} = 3.302\mu F$. According to the Illinois Capacitor CKS/CKR series datasheet, both capacitors have a loss tangent value of $tan\delta = 0.1$. Let $\omega = 2\pi * 100kHz$ be the angular frequency. The ESR values for each capacitor is

$$ESR_{ceramic} = \frac{tan\delta}{\omega c} = \frac{0.1}{2\pi(100kHz)(1.338\mu F)} = 0.199\Omega$$

$$ESR_{electrolytic} = \frac{0.1}{2\pi(100kHz)(3.302\mu F)} = 0.036\Omega$$

The electrolytic and ceramic capacitors are in parallel, so the total ESR value is computed similar to resistors in parallel.

$$ESR_{total} = 0.199\Omega || 0.036\Omega = 27.6m\Omega$$

Voltage ripple due to ESR is computed using Ohm's law; the voltage ripple is the product of the inductor current ripple and the ESR of the capacitors. Let the inductor current ripple be $\Delta i_L = 0.133A$.

$$\Delta V_{c,ESR} = \Delta i_L ESR = 0.133A(27.6m\Omega) = 3.67mV$$

The total voltage ripple is the sum of the capacitor voltage ripple and the voltage ripple due to ESR. Capacitor voltage ripple is computed using equation 1. Let $c = c_{ceramic} + c_{electrolytic} = 5.64\mu F$ be the sum of both capacitors.

$$\Delta V_o = \frac{10\mu s(0.133A)}{8(5.64\mu F} = 29.477mV$$

$$\Delta V_{total} = \Delta V_o + \Delta V_{c,ESR} = 33.147mV$$

The total voltage ripple accounting for ESR is within the $100mV$ specification.

555 Timer Component Selection

The 555 timer generates the pwm signal that feeds into the MOSFET via the high-side driver. The switching frequency and the duty of the converter depends on the R and C values of the 555 timer circuit. According to the 555 timer datasheet, the duty cycle is set by the ratio of two resistors R_A and R_B; the capacitance of C affects the discharge time of the circuit, therefore affecting the frequency of the pwm signal. An R_A+2R_B value within the range of $1k\Omega$ and $10k\Omega$ is needed to achieve a free-running frequency of $100kHz$. Let $R_A + 2R_B = 8k\Omega$ to solve for the capacitance needed to generate a $100kHz$ output signal. Rearranging the equation for frequency in terms of C, the expected capacitance is

$$f = \frac{1.44}{(R_A + 2R_B)C} \Rightarrow C = \frac{1.44}{f(R_A + 2R_B)} \qquad -(2)$$

$$C = \frac{1.44}{100kHz(8k\Omega)} \Rightarrow C \approx 1.8\mu F$$

Recall the expected duty was $D \approx 0.417$. The value of R_B can be solved for using the following equation

$$R_B = D(R_A + 2R_B) = 0.417(8k\Omega) \Rightarrow R_B \approx 3.336k\Omega$$

Now that R_B is solved for and it is known that $8k\Omega$ was substituted into $R_A + 2R_B$, the value of R_A can be solved for using these relationships.

$$R_A + 2R_B = 8k\Omega \Rightarrow R_A = 8k\Omega - 2(3.336k\Omega) \Rightarrow R_A \approx 1.328k\Omega$$

When testing the 555 timer with the rest of the system, the calculated R and C values did not provide the expected $100kHz$ switching frequency and 42% duty cycle. An inverter was introduced to help correct the duty cycle and switching frequency of the 555 timer; figure 2 shows the inverter coupling the output of the timer to the high-side driver input. Since the calculated values of R and C did not provide the specified frequency and duty cycle, the selection of R and C values were achieved by using a potentiometer (variable resistance). The closest resistor configuration that provides a duty cycle close to 42% was

$$R_A = 405\Omega, R_B = 3.603K\Omega$$

The capacitance for this configuration can be solved using equation 2. From equation 2, the calculated capacitance value is $C = 1.9nF$. However, the actual capacitance value used in the final implementation of the 555 timer was

$$C = 1.4nF$$

MOSFET Overcurrent Protection

The R_{sense} current sensing resistor is tied to the sense pins of the high-side driver shown in figure 2. The driver trips its over-current protection when a certain threshold of current flows through the MOSFET. Let $R_{sense} = 0.2\Omega$ and let the trip voltage be $V_{trip} = 35mV$. The over-current trip value I_{trip} can be solved for using Ohm's law. The gating of the MOSFET will cease when the current exceeds the value of I_{trip}.

$$I_{trip} = \frac{V_{trip}}{R_{sense}} = \frac{35mV}{0.2\Omega} = 175mA$$

Summary of Components

555 Timer			Buck Converter		
R_A	=	405Ω	R_L	=	35.5Ω
R_B	=	$3.603k\Omega$	$C_{electrolytic}$	=	$3.302\mu F$
C	=	$1.4nF$	$C_{ceramic}$	=	$1.338\mu F$

Results of Circuit Testing

Using the R and C values calculated prior, the complete system was constructed by following the schematics from figures 1 and 2. Using a DMM to probe the output of the buck converter, shown in figure 3, the voltage reading stabilized near $4.89V$. The average voltage reading closely matched the $5V$ output specification.

Figure 3: DMM showing average output voltage is $4.89V$

The output of the converter was probed on the oscilloscope to measure the magnitude of the voltage ripple. The pwm signal generated by the 555 timer was also probed to verify its switching frequency and duty cycle. Figure 4 shows the output voltage waveform triggering off the pwm waveform. The horizontal scale shows $5\mu s$ per division. Figure 4 shows the pwm signal completes one full period within $10\mu s$, this measurement agrees with the calculated switching period. The measured duty cycle from figure 4 is 45.7%, which is slightly higher than the expected 41.7%, but is within a 10% margin of error.

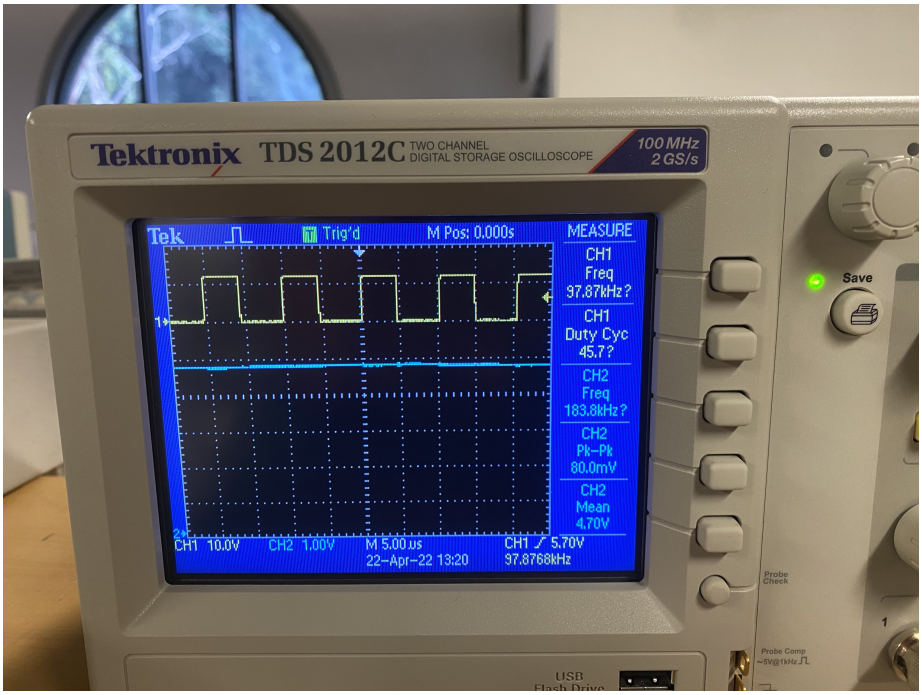

Figure 4: Output voltage waveform (blue) and pwm waveform (yellow) measurements. The oscilloscope shows pwm signal frequency is roughly $98kHz$ with a 45.7% duty cycle. Average output voltage of the converter is $4.7V$.

Figure 5 shows the output voltage waveform (blue) probed with AC coupling. The peak-to-peak value of the waveform lies in between one vertical division of $100mV$. This shows that the voltage ripple is within specifications.

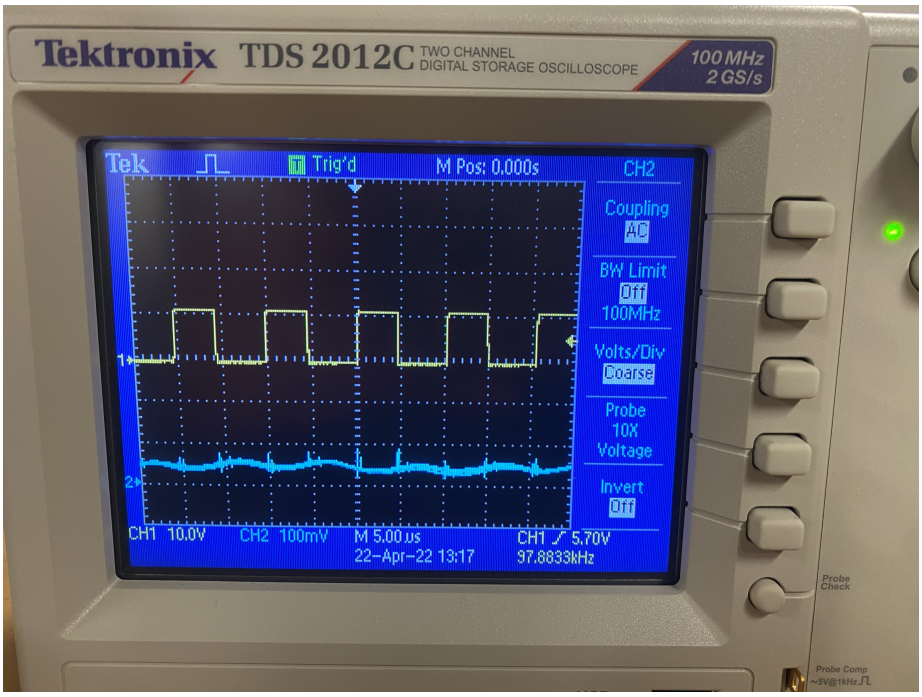

Figure 5: Oscilloscope measurements show the magnitude of the output voltage ripple is under $100mV$

The implementation of the buck converter was successful. The converter meets the $12V$ input, $0.75W$ $5V$ output specifications with a voltage ripple less than $100mV$ accounting for ESR. A worthwhile lesson from this project was understanding the effects of R and C values on charging and discharging times, which affected the switching period of the pwm signal, when designing the 555 timer circuit. Designing the 555 timer circuit to generate a pwm signal with the correct duty cycle requires consideration of resistor ratios and RC times, which proved to be the most challenging part of the buck converter build.