```
`timescale 1ns / 1ps
/**********************************************
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*
* Module: FunRegister
*
* Author: Eric Christie
* Class: ECEN 220, Section 1, Winter 2021
* Date: 3/2/21
*
* Description: Implementing 3 different
designs with Flip-Flop registers
*
*
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module FunRegister(
    input wire logic CLK, DIN, LOAD,
    output logic Q, NXT);

    FDCE my_ff (.Q(Q), .C(CLK), .CE(1'b1),
.CLR(1'b0), .D(NXT));
```

```
    assign NXT = LOAD?DIN:1'b0;

endmodule
```