```
`timescale 1ns / 1ps
/**********************************************
**********************************
*
* Module: Stopwatch
*
* Author: Eric Christie
* Class: ECEN 220, Section 1, Winter 2021
* Date: 3/9/21
*
* Description: Top layer for Stopwatch,
maps to board
*
*
**********************************************
**********************************/
`default_nettype none

module Stopwatch_top(
    input wire logic clk, btnc, sw,
    output logic [3:0] anode,
    output logic [7:0] segment);

    logic [15:0] data;
```

```
    //              clk, reset, run, [3:0]
digits 0-3
    Stopwatch Stpw(clk, btnc, sw,
data[3:0], data[7:4], data[11:8],
data[15:12]);
    //                              clk,
reset, DataIn, digitDisplay, digitPoint,
anode, segment
    SevenSegmentControl SSC( clk, btnc,
data, 4'b1111, 4'b0100, anode, segment);

endmodule
```