```
`timescale 1ns / 1ps
/**********************************************
**********************************
*
* Module: FunRegister
*
* Author: Eric Christie
* Class: ECEN 220, Section 1, Winter 2021
* Date: 3/2/21
*
* Description: Implementing 3 different
designs with Flip-Flop registers
*
*
**********************************************
**********************************/


module FunRegister(
    input wire logic CLK, CLR, INC,
    input wire logic [3:0] DIN,
    output logic [3:0] Q, NXT);

    FDCE ff0 (.Q(Q[0]), .C(CLK),
```

```
.CE(1'b1), .CLR(1'b0), .D(NXT[0]));
    FDCE ff1 (.Q(Q[1]), .C(CLK),
.CE(1'b1), .CLR(1'b0), .D(NXT[1]));
    FDCE ff2 (.Q(Q[2]), .C(CLK),
.CE(1'b1), .CLR(1'b0), .D(NXT[2]));
    FDCE ff3 (.Q(Q[3]), .C(CLK),
.CE(1'b1), .CLR(1'b0), .D(NXT[3]));

    assign NXT =(!CLR && INC)?(Q+1):
                (CLR && !INC)?4'b0000:
                Q;

endmodule
```