```
`timescale 1ns / 1ps
/**********************************************
**********************************
*
* Module: FullAdd
*
* Author: Eric Christie
* Class: ECEN 220, Section 1, Winter 2021
* Date: 2/9/21
*
* Description: FullAdder to combine to
amke a 9-bit adder
*
*
**********************************************
**********************************/

module FullAdd(
    input wire logic a, b, cin,
    output logic s, co);

    //internal wires from the 3 and gates
    logic a1, a2, a3;
```

```
    //gates
    xor(s, a, b, cin);

    and(a1,a, b);
    and(a2, b, cin);
    and(a3, a, cin);
    or(co, a1, a2, a3);
endmodule
```