```
`timescale 1ns / 1ps
/**********************************************
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*
* Module: Seven_segment_top
*
* Author: Eric Christie
* Class: ECEN 220, Section 1, Winter 2021
* Date: 2/23/21
*
* Description: Top level for seven_segment
module, links to board
*
*
**********************************************
**********************************/


module seven_segment_top(
    input wire logic [3:0] sw, //input
binary for numbers
    input wire logic btnc, //controls DP
    output logic [7:0] segment, //DP, CG -
CA
```

```
    output logic [3:0] anode);

    seven_segment SS0(.data(sw),
.segment(segment[6:0]));

    not(segment[7], btnc);

    assign anode = 4'b1110;

endmodule
```