```
`timescale 1ns / 1ps
/**********************************************
**********************************
*
* Module: uart top rx
*
* Author: Eric Christie
* Class: ECEN 220, Section 1, Winter 2021
* Date: 4/6/21
*
* Description: top-level module of the
uart receiver
*
*
**********************************************
**********************************/

`default_nettype none


module uart_rx_top(
    input wire logic clk, reset, ser_in,
//clk, btnu, rx_in
    output logic Receive, //led[11]
```

```
    input wire logic Received, //btnc
    output logic [7:0] rxData, //led[9:2]
    output logic parity); //led[0]

    //    clk, reset, serIn, Receive,
Received, Dout, parityError
    rx rx(clk, reset, ser_in, Receive,
Received, rxData, parity);

endmodule
```