```
`timescale 1ns / 1ps
/**********************************************
**********************************
*
* Module: Arithmetic_Top
*
* Author: Eric Christie
* Class: ECEN 220, Section 1, Winter 2021
* Date: 2/9/21
*
* Description: Instances Add9 to be the
control level
*
*
**********************************************
**********************************/
`default_nettype none


module arithmetic_top(
        input wire logic [15:0] sw,
        output logic [8:0] led);

    //wiring named after ports they
```

```
connect to and their size
    logic [8:0] a9, b9;
    logic co, cin;

    assign a9 = {sw[7], sw[7:0]};
    assign b9 = {sw[15], sw[15:8]};
    assign cin = 1'b0;

    //module
    Add9 Add(.a(a9), .b(b9), .cin(cin),
.co(co), .s(led));

endmodule
```