```
`timescale 1ns / 1ps
/**********************************************
**********************************
*
* Module: Add9
*
* Author: Eric Christie
* Class: ECEN 220, Section 1, Winter 2021
* Date: 2/9/21
*
* Description: Instances 9 FullAdders to
create a 9-bit adder
*
*
**********************************************
**********************************/


module Add9(
        input wire logic [8:0] a,
        input wire logic [8:0] b,
        input wire logic cin,
        output logic [8:0] s,
        output logic co);
```

```
    //internal wires
    logic [7:0] carry;

    //wiring
    FullAdd Add0(.a(a[0]), .b(b[0]),
.cin(cin), .s(s[0]), .co(carry[0]));
    FullAdd Add1(.a(a[1]), .b(b[1]),
.cin(carry[0]), .s(s[1]), .co(carry[1]));
    FullAdd Add2(.a(a[2]), .b(b[2]),
.cin(carry[1]), .s(s[2]), .co(carry[2]));
    FullAdd Add3(.a(a[3]), .b(b[3]),
.cin(carry[2]), .s(s[3]), .co(carry[3]));
    FullAdd Add4(.a(a[4]), .b(b[4]),
.cin(carry[3]), .s(s[4]), .co(carry[4]));
    FullAdd Add5(.a(a[5]), .b(b[5]),
.cin(carry[4]), .s(s[5]), .co(carry[5]));
    FullAdd Add6(.a(a[6]), .b(b[6]),
.cin(carry[5]), .s(s[6]), .co(carry[6]));
    FullAdd Add7(.a(a[7]), .b(b[7]),
.cin(carry[6]), .s(s[7]), .co(carry[7]));
    FullAdd Add8(.a(a[8]), .b(b[8]),
.cin(carry[7]), .s(s[8]), .co(co));
endmodule
```