```verilog
`timescale 1ns / 1ps
/**********************************
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*
* Module: Mod_Counter
*
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* Class: ECEN 220, Section 1, Winter 2021
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*
* Description: Basic Modulus Counter for
stopwatch project. Counts up to max value
*                      then rolls to 0
based on the input signals and clock.
*
*
********************************************
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`default_nettype none
module Mod_Counter #(parameter
MOD_VALUE=10, WID = 4)(
    input wire logic clk, reset, increment,
    output logic rolling_over,
```

```systemverilog
    output logic [WID-1:0] count);

    always_ff @(posedge clk) begin
        if(reset)
            count <= 0;
        else if((count == (MOD_VALUE - 1))
&& increment)
            count <= 0;
        else if(increment)
            count <= count + 1;
    end

    assign rolling_over = ((count ==
(MOD_VALUE - 1)) && increment); //1 when

endmodule
```