Appendix B: Design Journals

Team Design Journal

TEAM JOURNAL - CSSE232-03

MEMBERS: Alex Dripchak, Joshua Eckels, Bailey Morgan, Eric Tu

Milestone 1

MEETING 1.0 - 01/07/2019 - 12:40 pm [60 min]

Members Present: Alex, Josh, Bailey

(Eric not present due to miscommunication on members present's parts)

We decided to use a load/store architecture to build our processor. Part of the reason was it would be the easiest architecture to use in order to have 16-bit immediates. We could also use an accumulator style for math instructions using a dedicated register.

MEETING 1.1 - 01/08/2019 - 2:30 pm [50 min]

All members present & on time

Discussed how to construct instructions (ie how to divide bits to opcodes, regs, etc), registers. Decided that we would use more registers in favor of speed as opposed to using the stack. To account for this, we would have 128 function registers that would be represented by the first 16 "f" regs that could be all accessed by using (FCC * 16) + regs.

MEETING 1.2 - 01/08/2019 - 8:30 pm [90 min]

All members present

Began working on translating Euclid's Algorithm, relPrime, and other small algorithms to demonstrate operations. Also translated our instructions to machine code.

MEETING 1.3 - 01/09/2019 - 1:30 pm [120 min]

All members present

Finished Euclid's algorithm and relPrime. Translated the assembly language snippets to machine code. Polished the document. Completed Milestone 1. Pushed everything to git log in Design branch.

Milestone 2

MEETING 2.0 - 01/14/2019 - 5:10 pm [60 min]

Members Present: Josh, Bailey, Eric

Put the skeleton of the RTL in the table and mapped out what kind of registers we need for our RTL and what they do

MEETING 2.1 - 01/15/2019 - 5:30 pm [90 min]

All members present

Finished the RTL write-up for all instructions. Polished them.

Recorded a list of components that will be needed for the data path.

NOTE: REMEMBER TO REMOVE THE "MOV" INSTR!!!

MEETING 2.2 - 01/16/2019 - 1:30pm [120 min]

All members present

Polished up and translate RTL over to our design document. Developed shopping list for all hardware in our RTL.

Started describing our components. Added a comparator to the list, ALU now has 3 bit opcodes as we had 5 operations and needed 3 control wires to accomodate this.

Developed a "code-tracing thought experiment" in order to test our RTL, easier and quicker to develop than a simluation and less reliant on others than a survery from other groups.

Milestone 3

MEETING 3.1 - 01/20/2019 - 2:30pm [150 min]

All members present (Alex facetime)

Completed rough draft of datapath after walking through RTL for each instruction. Made changes to RTL based on our datapath.

We are still in need of documentation for each component and subsystem. Worked on defining and documenting control signals.

Will use a ROM for control unit. Meeting tomorrow to move a lot of the work from today into the design document.

MEETING 3.2 - 01/21/2019 - 5:10pm [120 min]:

All members present

Defining and describing every control signal. Working on ways to perform unit and integration testing on

our datapath. Started looking at Verilog and how to implement some components. Working on documention on Design document.

MEETING 3.3 - 01/22/2019 - 7:00pm [310 min]:

Updated datapath to reflect control unit, subsystems, and integration plan. Wrote/planned all unit and integrations tests. Wrote verilog modules and test benches for comparator, adder, and mux.

Updated list of hardware components, and reformatted into tables. Updated RTL, including plan for a simulation to verify RTL. Updated design document.

Milestone 4

MEETING 4.1 - 01/27/2019 - 6:00 pm [180 min]:

Members present: Bailey, Alex, Eric

Completed the finite state machine for the datapath control signals. Described different

testing methods for the finite state machine.

MEETING 4.2 - 01/28/2019 - 6:00 pm [300 min]:

All members present

Implemented most of the components in VHDL, except for memory, which still has some

reading problems. Planned to meet tomorrow to write up integration plans.

MEETING 4.3 - 01/30/2019 - 3:00 pm [300 min]:

All members present

Finished implementing register file and memory unit, along with their unit tests. Implemented some integration between the components

and finalized the multicycle FSM.

Milestone 5

MEETING 5.1 - 02/03/1029 - 1:00 pm [90 min]:

All members present

Formulated and discussed our plans for the week. Discussed a few issues with the data path that needed to be fixed and what solutions we

wanted to go with. Divided integration work up and assign parts to everyone to have done by Wednesday. Alex whooped Eric in smash.

MEETING 5.2 - 02/04/2019 - 10:50 pm [50 min]

Members present: Josh, Alex

Created base code for the control unit.

MEETING 5.3 - 02/05/2019 - 6:00 pm [150 min]:

Members present: Josh (60 min), Alex, Bailey, Eric (late)

Worked on integrating our systems. Control unit finished along with PMS and ALS. Still need FBS and RMS. Updated the design document

to reflect changes. Base code for the F Register Backup System has been created.

MEETING 5.4 - 02/06/2019 - 7:00 pm [60 min]:

All members present.

F Register Backup System has been tested. Realized there were some clock timing issues

that had to be noted whene using the system.

ALU System has been successfully implemented.

MEETING 5.5 - 02/07/2019 - 10:00 pm [180 minutes]

All members present

ALU System has been tested.

The Register Management System has been implemented. Fixed some bugs that

were in the original control unit and updated the design document accordingly

MEETING 5.6 - 02/08/2019 - 7:00 pm [180 minutes]

All members present

The Instruction Execution System and datapath has been implemented. The Instruction

Execution System is also tested.

MEETING 5.7 - 02/10/2019 - 4:00 pm [240 minutes]

All members present

The datapath has been tested and the design document has been updated according to the changes from the current milestone. Updates to the team journal and individual journals were made.

Milestone 6

MEETING 6.1 - 02/15/2019 - 11:00 am [60 minutes]

All members present

Demonstration day. Signed off on completed processor. Started work on presentation and final documentation

MEETING 6.2 - 02/16/2019 - 8:00 pm [180 minutes]

All members present

Finished and practiced presentation. Final documentation complete.

Alex Dripchak

Work log = Alex Dripchak

Milestone 1

01/07/2019 - Met with team to start M1, Started team journal [50 mins]

01/08/2019 - Met with team, discussed instructions, registers, wrote in team journal, helped develop small algorithms, exposed + fixed flaws in current model [3.5 hours]

Listened to Josh complain about git [30 mins]

01/09/2019 - Met to finish up milestone 1, others finished relPrime and Euclids, I worked on converting our code snippets to machine code. [2 hours]

Milestone 2

1/15/2019 - Met with the lads to finish up the RTL. Helped develop new components for the data path. [1.5 hours]

1/16/2019 - Helped write up the components, specifically the comparator and the F cache. Designed a test to use in order to make sure the RTL is correct, then exectured said test to look for errors. [2 hours]

Milestone 3

1/20/2019 - Helped make the datapath [2.5 hours]

1/21/2019 - Started working on Verilog components, wrote test bench for comparator [2 hours]

1/22/2019 - Went over document with team, developed components in Verilog, helped teammates learn Verilog and develop other components + tests [4.5 hours]

Milestone 4

1/26/2019 - Debugged Lab 6 and fixed slt [1.5 hours]

1/27/2019 - Finished control state machine, wrote-up control unit test plan [3 hours]

1/28/2019 - Finished making a register file and test cases [4 hours]

1/30/2019 - Finished rewriting some tests for comparator, helped make the memory unit [2 hours]

Milestone 5

2/3/2019 - Discussed current issues ie $ra reg not getting backed up, had the regFile handle input/output [1 hour]

2/4/2019 - Worked on the control unit w/ Josh. [1 hour]

2/5/2019 - Realize that we monumentally fricked up the control unit, phat rip in the chat. Josh rebuilt it correctly, I helped write the test case. Navigated as Bailey drove implementing the PMS [4 hours]

2/6/2019 - Helped debug the ALU test case [1.5 hours]

2/9/2019 - Provided moral support and insulted Josh for a little bit [~30 mins-ish]

2/10/2019 - Helped debug recursive calls not return properly and helped write the recursive test case [2.5 hours]

Joshua Eckels

CSSE232 - Activity Journal

Monday, January 7, 2019 [50 min]: Decisions on architecture type. Load-store with accumulators considered. Listing necessary functions to implement.

Tuesday, January 8, 2019 [50 min (1), 90 min (2)]: Assigning registers (Function regs, args, etc.). 2 instruction types (G and I). Began work on implementing Euclid's algorithm in our language. Worked on desgin document.

Wednesday, January 9, 2019 [120 min]: Finishing translation of relPrime into BAEJ and machine language. Reformatting document.

Monday, January 14, 2019 [60 min]: Working on RTL for milestone 2. Dividing up instructions into multiple cycles. Excel document made for RTL.

Tuesday, January 15, 2019 [90 min]: Finished RTL table, discussed shopping list and control signals

Wednesday, January 16, 2019 [120 min]: Finished M2, discussion of each item in shopping list, method for verifying our RTL. Wrote up description for all of the registers we used in our RTL.

Sunday, January 20, 2019 [150 min]: Working on M3. Walked through RTL and drew datapath on whiteboard appropriately. Just a rough draft. Needs a lot of work tomorrow. Still need to document all of our changes and new updates.

Monday, January 21, 2019 [150 min]: Working on control signals, bit sizes, purposes, and functionality in our datapath. Writing this up in the Design document as a table with complete list and description of all control signals.

Tuesday, January 22, 2019 [250 min]: Fixing formatting of hardware components in design document. Learning verilog. Created verilog modules for 16-bit adder, 1-bit mux, and comparator (including test benches for each).

Monday, January 28, 2019 [330 min]: Finished implementations and extensive test benches on 1-bit mux, 2-bit mux, adder, and ALU. ALU still has some bugs in it. Need to do regs as well.

Wednesday, January 30, 2019 [60 min]: ALU bugs fixed. Decided we don't need actual reg hardware; they can just be instantiated whenever we need them.

Sunday, February 3, 2019 [60 min]: Discussed rest of project. Divided up work. Began on control unit. Will begin working on ALU sub-system for integration plan.

Monday, February 4, 2019 [90 min]: Worked with Alex. Finished control unit and test bench. Noticed a lot of inconsistencies in naming conventions.

Tuesday, February 5, 2019 [50 min]: Realized issues with control unit. Needs to be implemented as finite state machine.

Wednesday, February 6, 2019 [200 min]: Multicycle control unit finished. Test bench completed and extensive. Working on Arithmetic logic implementation system.

Wednesday, February 6, 2019 [120 min]: Meeting number 2 today. Finished ALS integration system with extensive testing. Unclocked ALU (causing a cycle delay).

Thursday, February 7, 2019 [180 min]: Massive bug fix in the register management system. Comparator was broken lol. Will finish tomorrow.

Friday, February 8, 2019 [120 min]: Register management system is 100% functional with extensive testing. Had to fix bugs in the comparator and the reg file.

Saturday, February 9, 2019 [60 min]: Testing relPrime on our processor. Lot of debugging. Realizing more issues with control unit.

Sunday, February 10, 2019 [120 min]: Scanning through and updating design document with work over the past couple weeks. Control unit was updated and is working. Also was having more issues with RA that needed to be fixed with restoring and backing up. Updated FSM and RTL.

Tuesday, February 12, 2019 [100 min]: Added code to have program pauses after finishing execution. Memory can now read programs from a .mem file. Synthesis works. Working on benchmarking.

Friday, February 15, 2019 [60 min]: Demo day. Working on a template for final report. Writing a few more quick test programs.

Bailey Morgan

Work log = Bailey Morgan

Milestone 1

Monday, December 7, 2019 [60 min] - Met with team, discussed initial design decisions, load store vs stack and instruction design.

Tuesday, December 8, 2019 [240 min] - Finalized instructions and register designs, translated programs to asm and to machine code.

Wednesday, December 9, 2019 [120 min] - Finished asm and machine code changes. Final touches on language specification.

Milestone 2

Monday, January 14, 2019 [60 min] - Developed starting RTL for I types. Broke up instructions into cycles. Started RTL summary charts.

Tuesday, January 15, 2019 [90 min] - Finished RTL summary charts. Listed the needed hardware and logic units.

Wednesday, January 16, 2019 [120 min] - Finished hardware descriptions and methods for testing RTL description. Completed M2.

Milestone 3

Sunday, January 20, 2019 [150 min] - Worked on M3, developed datapath using rtl. Traced many instructions to verify they worked.

Monday, January 21, 2019 [180 min] - Created datapath svg and Makefile to convert both datapath diagram and design documents to pdfs. Touched up things in the data path.

Tuesday, January 21, 2019 [340 min] - Finished up datapath design and pdf conversions. Updated components list and created unit test plans and Integration test plans. Worked on subcomponents with Eric.

Milestone 4

Sunday, January 27, 2019 [180 min] - Worked on finite state machine design. Updated rtl and component descriptions based off of feedback

Monday, January 28, 2019 [300 min] - Finished Fcache and helped Alex with reg file, and Josh with alu. Made updates to the design doc.

Wednesday, January 30, 2019 [330 min] - Finished all parts and went over tests with everyone to make sure they were extensive enough. Made sure they also matched what was described in the design doc. Created PCS integration and wrote testbench with Eric

Milestone 5

Sunday, Febuary 3, 2019 [90 min] - Met to discuss what we need to do for the rest of the week. Discovered a few issues with our design and discussed fixes. Helped divide and assign integration work

Tuesday, Febuary 5, 2019 [150 min] - Updated PCS, integrated MMS and PMS

Wednesday, Febuary 6, 2019 [60 min] - Wrote test bench and tested FBS.

Thursday, Febuary 7, 2019 [180 min] - Helped with RMS integration. Helped debug control unit.

Friday, Febuary 8, 2019 [180 min] - With josh integrated IES and wrote test benches. After, integrated IES, PMS, and control unit to form the data path

Sunday, Febuary 10, 2019 [240 min] - Wrote some programs to test and debug datapath with including relprime. More control issues found and fixed. Processor seems to work fine. Added a reset input to the datapath to reset to processor to pc = 0.

Friday, February 15, 2019 [60 min] – Demo given to Micah

Saturday, February 16, 2019 [180 min] – optimizations and worked on presentation

Sunday, February 17, 2019 [20 min] – Recorded video demo

Eric Tu

Eric Tu

CSSE232 - Activity Journal

Monday, January 7, 2019 [20 min]:

Discussed implementation strategy for the BAEJ Assembly Language.

Tuesday, January 8, 2019 [50 min (1), 200 min (2)]:

Implementing modulus using BAEJ and helped with the summation function.

When challenges arose, I discussed certain implementations that were needed to satisfy

the requirements for the functions.

Began work on implementing Euclid's algorithm in our language.

Wednesday, January 9, 2019 [120 min]:

Finishing translation of relPrime into BAEJ and machine language. Reformatting document.

01/14/2019 - 5:10 pm [60 min]

Helped write the skeleton of the RTL table.

01/15/2019 - 5:30 pm [90 min]

Helped finish the RTL write-up for all instructions. Reviewed the instructions.

01/16/2019 - 1:30pm [120 min]

Wrote out the hardware component spec for the ALU. Reformated and reviewed the document.

01/20/2019 - 2:30pm [150 min]

Helped draw up a rough draft of datapath via RTL.

Discussed implementation method of backing of registers.

01/21/2019 - 5:10pm [120 min]:

Wrote up a rough draft of component unit testing methods.

01/22/2019 - 7:00 pm [270 min]:

Drew up and named subsystems for integration testing. Peer reviewed.

Rewrote methods of testing the RTL.

Milestone 4

01/27/2019 - 6:00 pm [180 min]:

Drafted the finite state machine for the datapath control signals. Described different

testing methods for the finite state machine with Alex.

01/28/2019 - 6:00 pm [240 min]:

Implemented the memory unit. Memory unit test still has bugs.

01/30/2019 - 3:00 pm [300 min]:

Finished implementing memory unit, along with its unit tests.

Milestone 5

02/03/2019 - 1:00 pm [90 min]:

Discussed the plans for the rest of the week. Communicated an issue about ra being lost upon nested function calls.

02/04/2019 - 8:00 pm [120 min]:

Worked on integrating and testing the F Register Backup System. Discovered that there were errors with the testbench and not the module itself.

02/05/2019 - 9:00 pm [120 min]:

Worked on integrating and testing the F Register Backup System. Bailey helped debug the test cases and found out that it was a timing issue. The FBS has been finalized.

02/06/2019 - 11:00 pm [150 min]:

Helped Josh debug the ALUS. Updated documentation and started the presentation powerpoint.

02/07/2019 - 8:00 pm [60 min]:

Helped Josh and Bailey debug the Register Management System.

02/08/2019 - 7:00 pm [60 min]:

Helped debug the datapath and discussed methods of I/O.

02/10/2019 - 4:00 pm [240 min]:

Updated the team journal and updated design document according to the current milestone with Josh.

Appendix C: Benchmarking

The following data was collected from the simulator when the relative prime algorithm was run with an input of 5040:

```
============================================================
                        METRICS
============================================================

Latency:
    Transfered from memory (bytes):  203944
    Transfered to memory   (bytes):  0
    Program size in memory (bytes):  70

Performance:
    Total instructions executed   :  50986
    Total cycles executed         :  163114
    Average cycles per instruction:  3.20
    Simulation clock rate    (MHz):  87.60
    Execution time            (ms):  1.86

Output:    11
```

Figure C.1: Benchmarking data on relPrime (5040)