Design Guide

Hardware Design Recommendations Of MX1081

May.2013

REVISION HISTORY

Version No.	Revised Date	Revised by	Description	Notes
1.0	**2012-10-22**	**Bruce**	**Hardware Design Guide released**	**Proposal**
1.1	2013-05-02	Bruce	Modify description about the external 32.768KHz of MCU	**Proposal**

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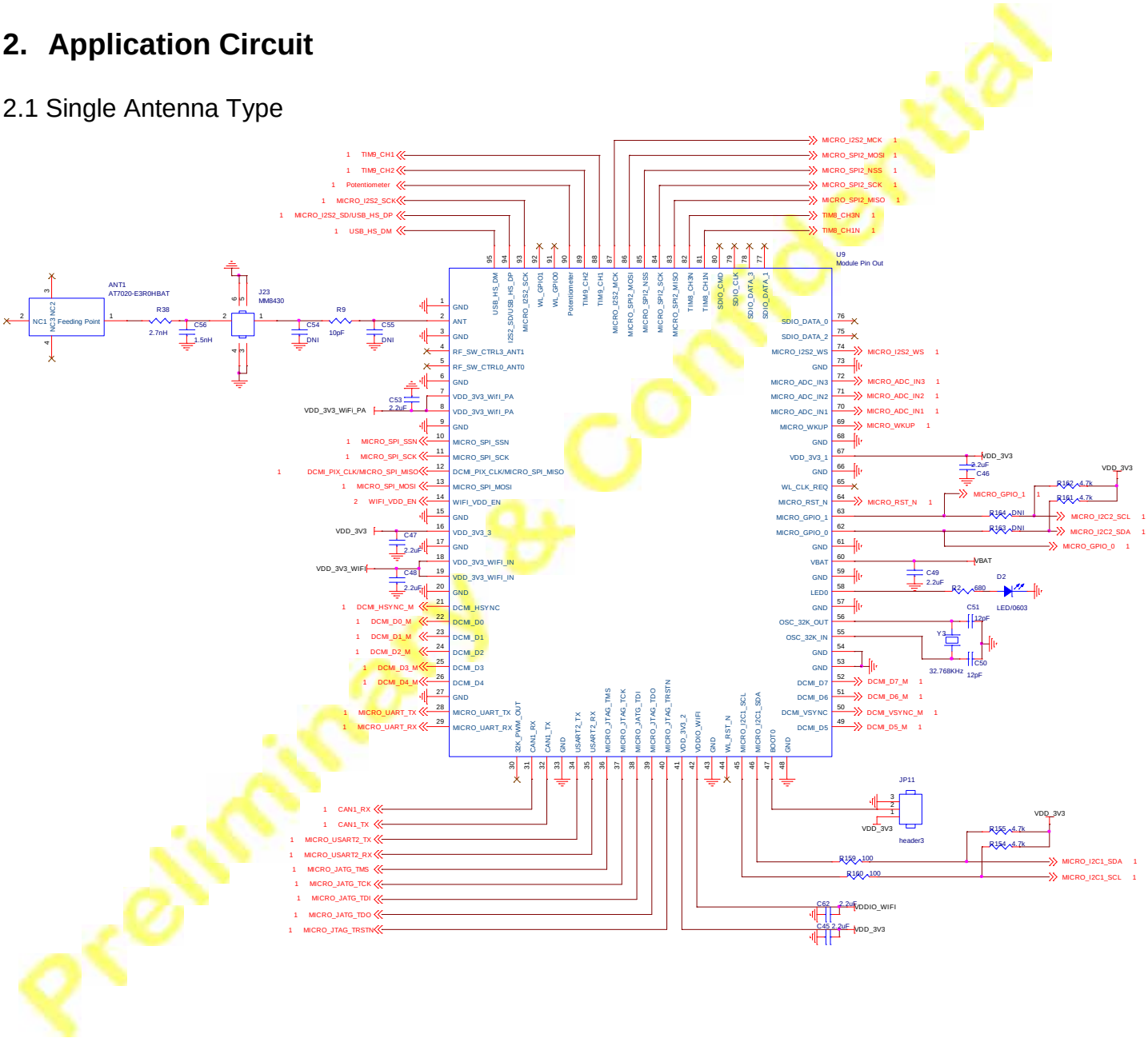
1. Purpose

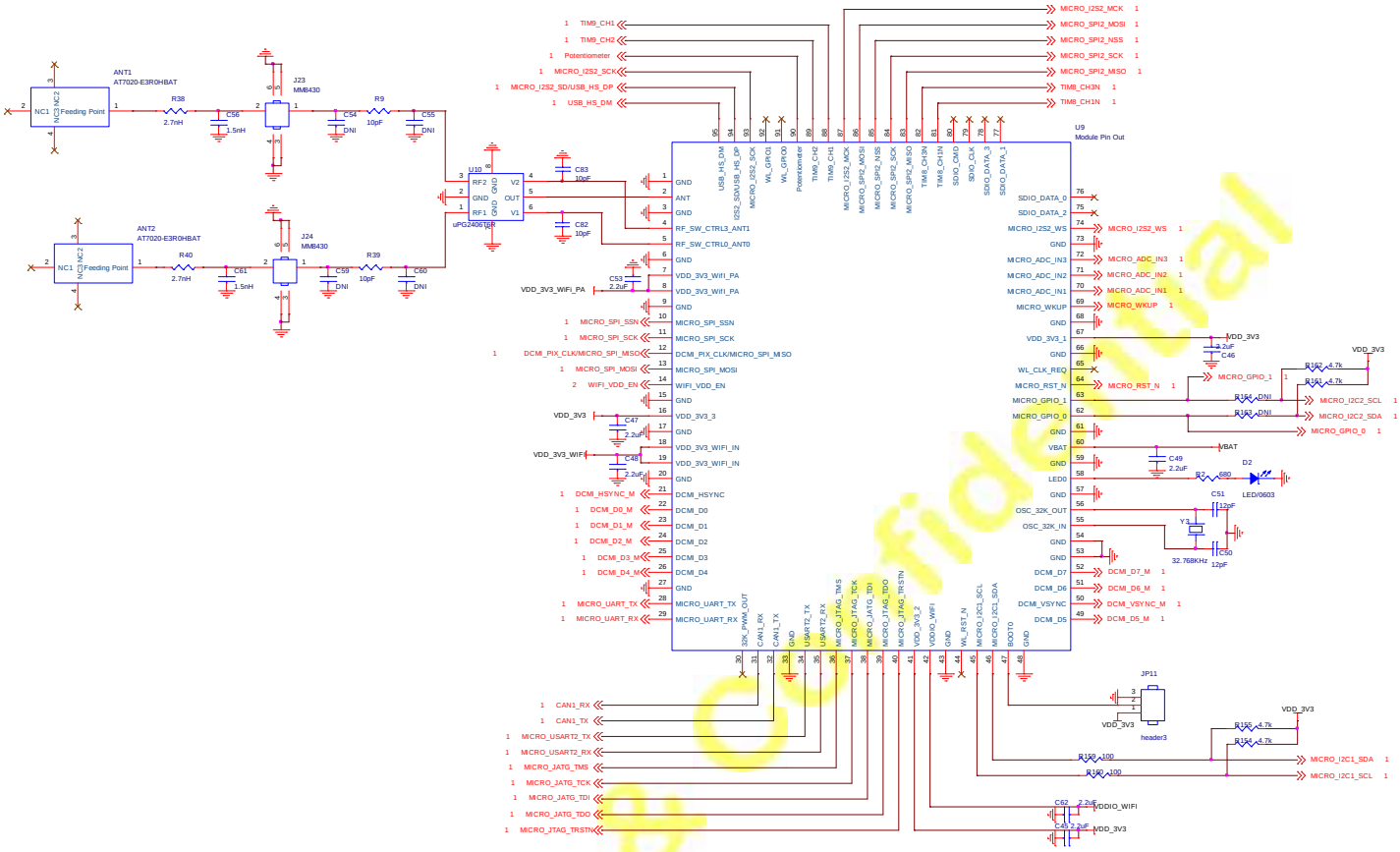
The purpose of this document is to define the hardware design recommendations for MX1081.

2. Application Circuit

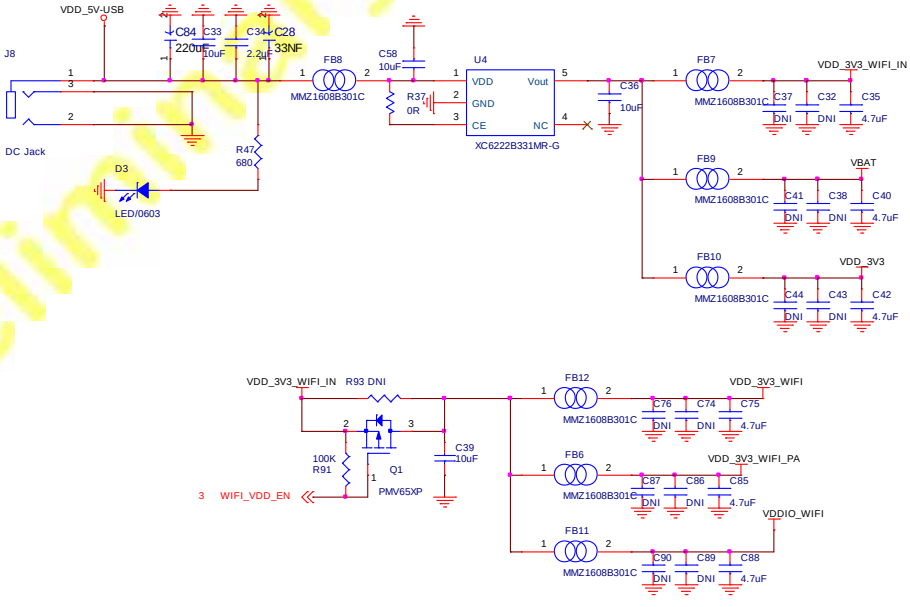
2.1 Single Antenna Type



2.2 Antenna Diversity Type



2.3 Power Supply Scheme



3. DC POWER CODITIONING AND DISTRIBUTION

Appropriate DC voltages are conditioned using the external power IC. Detailed performance specifications for the combo module and external power ICs are available in their respective device specifications as below.

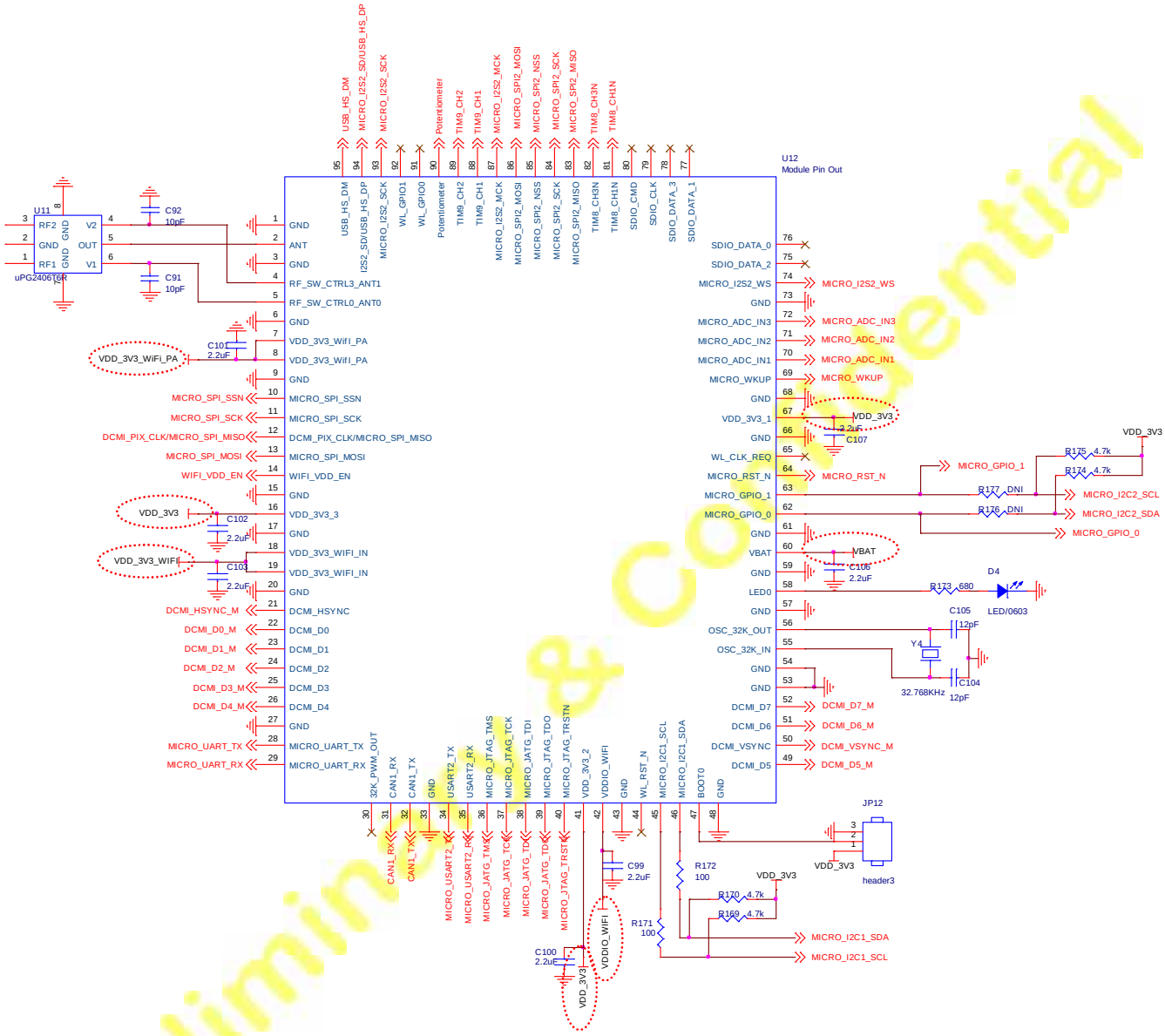
3.1 Power Conditioning

Symbol	Parameter	Min	Typ	Max	Unit
VBAT	MCU VBAT Voltage	2.0	3.3	3.6	V
VDD3V3_1	GPIO I/O Supply	2.4	3.3	3.6	V
VDD3V3_2	GPIO I/O Supply	2.4	3.3	3.6	V
VDD3V3_3	GPIO I/O Supply	2.4	3.3	3.6	V
VDD_3V3_WIFI	WiFi Voltage		3.3	3.6	V
VDD_3V3_WIFI_PA	WiFi PA Voltage		3.3	3.6	V
VDDIO_WIFI	MCU With WiFi		3.3	3.6	V
	Only WiFi Function	1.8	3.3	3.6	V

Each regulator output must be connected directly to its recommended output capacitor per the *Power source*. Additional filtering and bypassing of the RF supply voltages are described in the following sections

3.2 Power distribution to module

All the power supply pins should be decoupled as below.



4. CLOCK REQUIRE

4.1 MODULE EXTERNAL INPUT CLOCK _32.768KHZ SLEEP CLOCK of MCU

* Suggestion Crystal component list - Honsic: ETST32.768W070BMPZ

Electrical Specifications

Nominal Frequency:	32.768kHz
Operating Temperature Range:	-40 to +85 degC
Storage Temperature Range:	-55 to +125 degC
Frequency Tolerance:	+/- 20ppm Max. at 25 degC
Frequency Tolerance over:	Tumover Temp.: 25 +/- degC
Operating Temperature Range:	Temp.Coefficient: -0.034 +/- 0.006ppm/degC^2
Equivalent Series Resistance:	70k ohm Max. at 25 degC
Insulation Resistance:	500M ohm Min. / DC100V +/- 15V
Shunt Capacitance:	0.95pF Typ.
Load Capacitance:	7.0pF
Level of Drive:	1 Micro W Max.

Note: For C_{L1} and C_{L2} it is recommended to use high-quality external ceramic capacitors in the 5pF to 15pF range selected to match the requirements of the crystal or resonator (see Figure 4-1). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2} are Load capacitance C_L has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where C_{stray} is the pin capacitance and board or trace PCB – related capacitance. Typically, it is between 2pF and 7pF

Caution: To avoid exceeding the maximum value of C_{L1} and C_{L2} (15pF) it is strongly recommended to use a resonator with a load capacitance $C_L \leqq 7$pF. Never use a resonator with a load capacitance of 12.5pF.

Example: if you choose a resonator with a load capacitance of C_L = 6pF and C_{stray} = 2pF, then $C_{L1} = C_{L2}$ =8pF

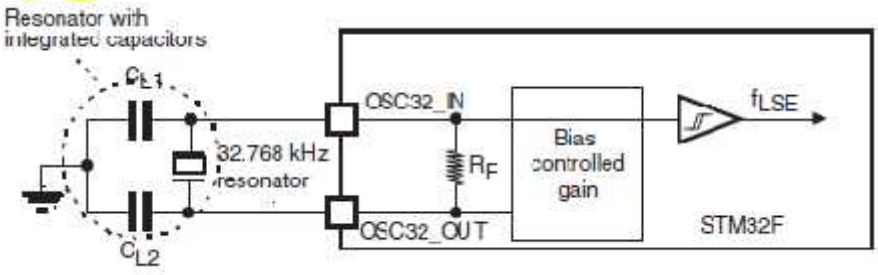


Figure 4-1. Typical application with a 32.768 kHz crystal

5. PCB LAYOUT GUIDELINES

5.1 DC Power

Use wide traces for power supply lines. Know the maximum currents being carried on each power supply trace, and make the trace widths proportionate to the current (especially for long trace lengths). Where possible, fill large areas with copper to distribute the highest currents. These measures minimize IR drops, line inductance, and switching transients.

- Use several plated via holes to connect power supply traces between layers. The number of vias used should be proportional to the current being routed.
- Avoid loops in the supply distribution traces. Current-carrying loops are essentially antennas radiating electromagnetic fields that may corrupt transceiver performance or cause regulatory electromagnetic interference (EMI) test failures.

Power amplifiers present particular concerns due to their high current draw and switching transients. In addition to the points listed above, traces distributing PA supply current and ground paths carrying its return current must follow these guidelines:

- High current traces should be kept as short as possible and devices on the same supply should be fed from a ‘star point’ rather than ‘daisy-chained’.
- Avoid loop in the PA supply and clock supply traces, PA supply traces and clock supply traces to be independent where possible.

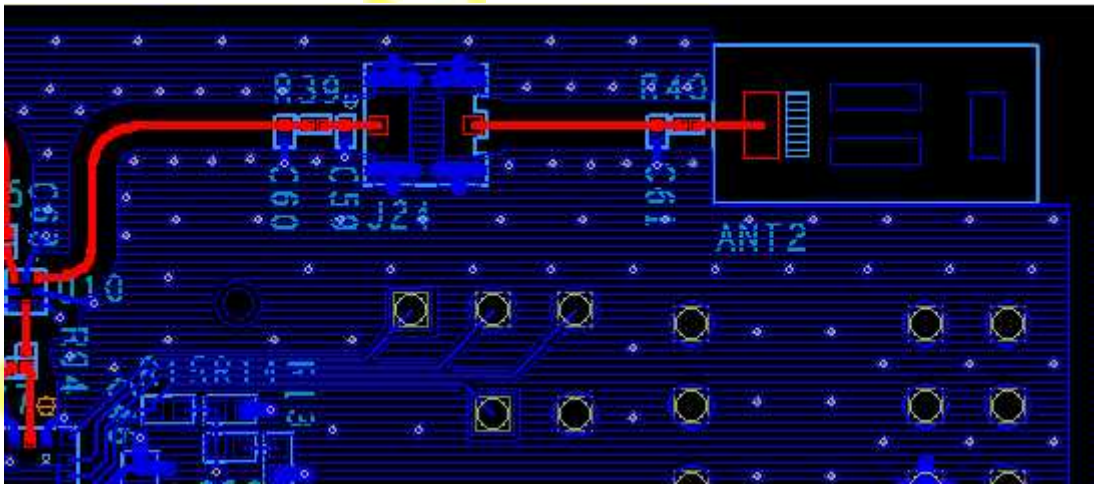
5.2 Antenna port RF signal

General guidelines for routing RF signals of WLAN antenna port. RF signals require controlled-impedance lines to minimize mismatch losses and efficiently transfer energy from source to load. The line impedance depends upon several variables — trace width and thickness, co-planar ground spacing, height of dielectric material between the trace and ground plane(s), and dielectric constant of the PCB material. Given the PCB material selected, the geometry of the micro-strip, strip-line, or co-planar grounded waveguide (CGW) elements must be designed properly to provide the desired 50-Ω impedance. Design of micro-strip, strip-line, and CGW elements is well documented and supported in many microwave software applications.

Additional RF-specific PCB design guidelines include:

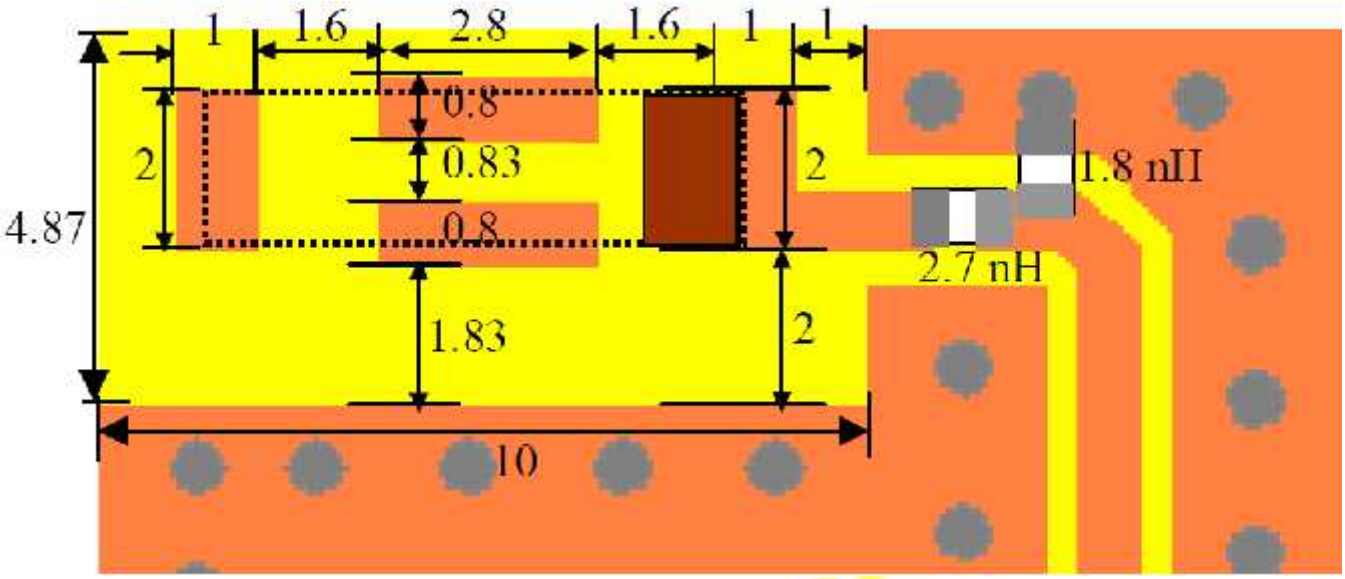
- Keep the RF traces on the component sides (top or bottom layer) using micro-strip or CGW techniques where possible.
- Screen these traces to avoid electromagnetic interference.
- Use internal layers with strip-line techniques if necessary.
- Maintain continuous ground below micro-strip traces, beside CGW traces, and above and below strip-line traces.
- Keep traces short and direct, to minimize loss and undesired coupling.
- Front-end losses increase the system noise figure — keep traces before the first gain stage as short as possible and use low-loss capacitors and inductors.
- Clear internal layer (or layers) of metal. This improves micro-strip, CGW, and strip-line geometries, allowing wider traces.
- Fill the areas along both sides of traces with ground to improve isolation, but provide adequate clearance to minimize co-planar capacitance and leakage. These ground-filled areas are integral to CGW designs.
- Use several ground vias along both sides of the signal traces to connect RF ground-fill areas to the internal RF ground plane.
- Avoid crossing RF traces if possible.

Example:



5.3 Chip Antenna Layout reference Design

- Layout reference design (Unit is mm)



* Matching circuit and component values will be different, depending on PCB Layout
* Line width should be designed to match 50ohm characteristic impedance, depending on PCB material and thickness.
* The Chip Antenna must put on the corner of PCB
* Suggestion Chip Antenna component list
  - ACX: AT7020-E3R0HBAT

5.4 Clock signal

Both supply variation and module external clock of signals onto this radio reference must be avoided. The clock signal traces, into the WICED Module, must be protected against corruption, by other clocks, power supply transients, and digital noise. These signals must be routed carefully using techniques similar to micro-strip and strip-line to maintain high isolation and signal purity.

Recommended orient the components to keep the clock signal lines from host as short and direct as possible.

Example: