Datasheet

MX1081

Embedded Wi-Fi MCU module

1.8 Date：2013-12-16 Datasheet

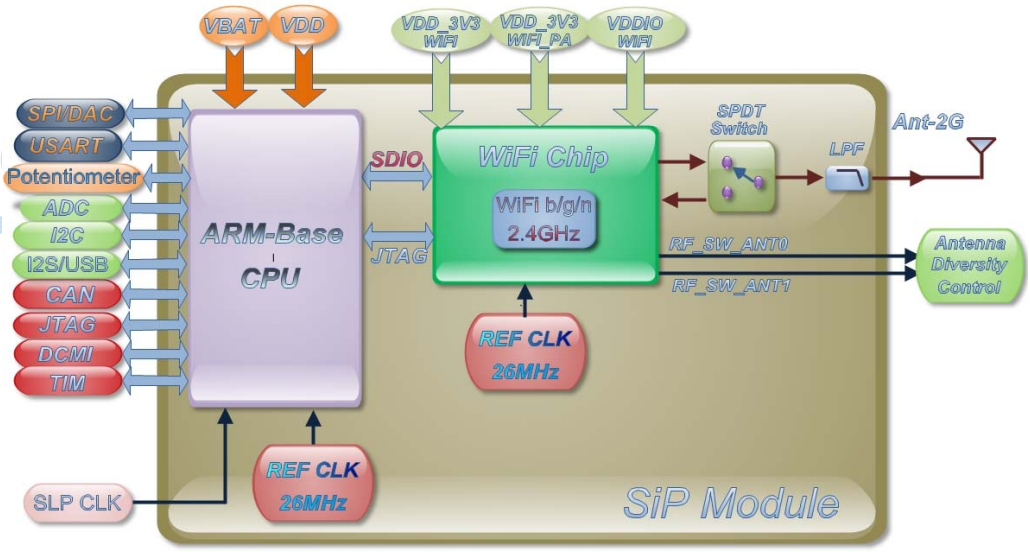
Overview

MX1081 is a complete WiFi MCU module which is designed for embedded wireless solution and a cost-effective, low power capabilities high performance MCU in M2M applications. It includes standards-based wired and wireless technologies to enable IP infrastructures for smart grid, smart home, security, building automation, toys, robots, remote health and wellness monitoring and other M2M applications.

The module integrates ARM Cortex™-M3 MCU, clock, WIFi and front end into a smallest form factor LGA package. It is based on Broadcom IEEE802.11 b/g/n antenna diversity single-stream Broadcom align technology. Thus, it can be used to enable wireless connectivity to the simplest existing sensor products with minimal engineering effort.

Applications

- Building Automation / Access Control
- Smart home appliances
- Medical/Health Care
- Industrial Automation Systems
- Point Of Sale system (POS)
- Auto electronics



REVISION HISTORY

Version No.	Revised Date	Revised by	Description	Notes
1.0	2012-03-28	William	Preliminary specification released	Proposal
1.1	2012-04-09	Bruce	1. Add Revision History information 2. Modify Pin Description of the Pin24, Pin25, &Pin26	Proposal
1.2	2012-04-20	Bruce	1. Update Block diagram (add DCMI Interface) 2. Modify Pin Out Counts (change from 51 to 58), Pin Description 3. Add DCMI Interface Characteristics 4. Modify Mechanical Dimension	Proposal
1.3	2012-06-27	Bruce	1. Update Block Diagram 2. Update Pin out counts & Pin Description 3. Update Mechanical Dimension	Proposal
1.4	2012-07-19	Bruce	1. Update Block Diagram (add Timer Function) 2. Update Pin out counts & Pin Description 3. Add TIM timer Interface Characteristics 4. Add pin definition Mapping to STM32F20x LQFP176 information.	Proposal
1.5	2012-08-08	Bruce	1. Update Block Diagram (add I2S/USB, Potentiometer Function) 2. Update Pin out counts & Pin Description 3. Add I2S Interface Characteristics 4. Modify Mechanical Dimension 5. Update Module Recommend Footprint & Stencil information	Proposal
1.6	2012-08-14	Bruce	1. Update Module Recommend Footprint & Stencil information	Proposal
1.7	2012-11-05	Bruce	1. Modify the Recommend footprint & Recommend Stencil 2. Add Alternate function mapping Table	Proposal
1.8	2012-11-23	Bruce	1. Modify current Consumption data of TX mode & RX mode.	Proposal

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1. Introduction

1.1 Description

This is a complete WiFi MCU module which is designed for embedded wireless solution and a cost-effective, low power capabilities high performance MCU in M2M applications. It includes standards-based wired and wireless technologies to enable IP infrastructures for smart grid, smart home, security, building automation, toys, robots, remote health and wellness monitoring and other M2M applications.

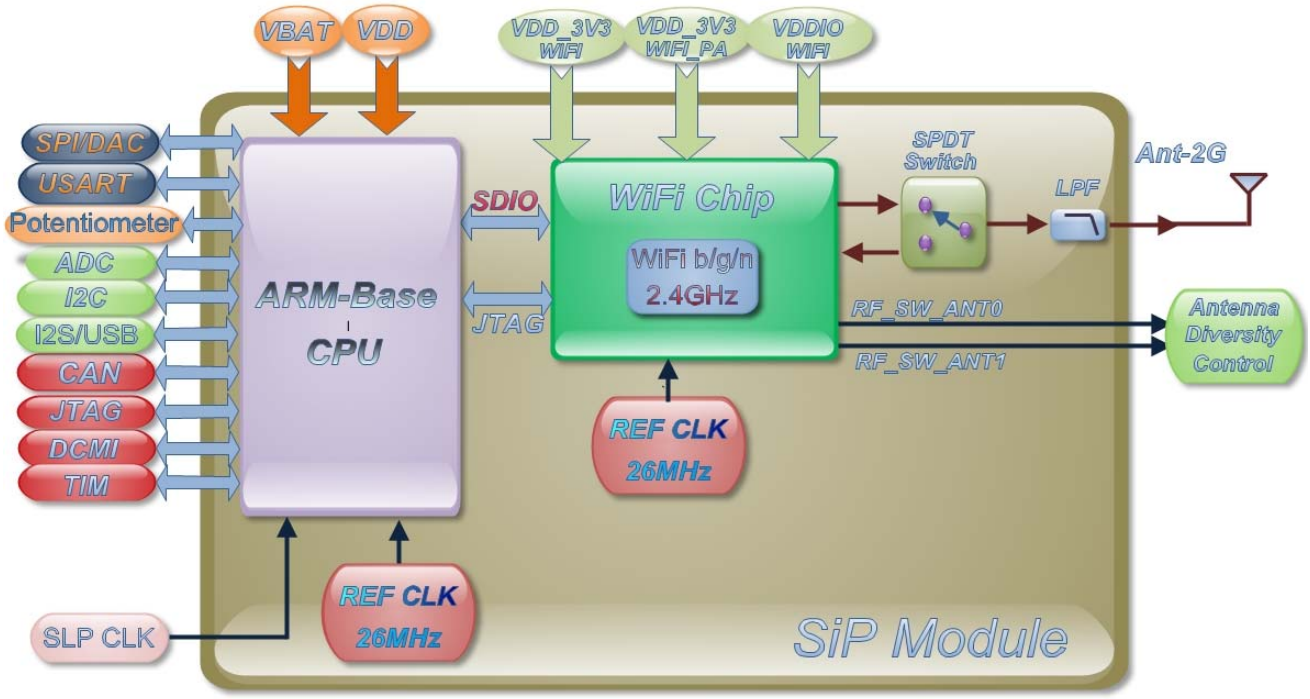
The module integrates ARM Cortex™-M3 MCU, clock, WIFi and front end into a smallest form factor LGA package. It is based on Broadcom IEEE802.11 b/g/n antenna diversity single-stream Broadcom align technology. Thus, it can be used to enable wireless connectivity to the simplest existing sensor products with minimal engineering effort.

The solution is provided as a module to reduce development time, lower manufacturing costs, save board space, ease certification, and minimize RF expertise required. Additionally it is provided as a complete platform solution including software drivers, sample applications, API guide, user documentation and a world-class support community.

1.2 Features

MCU	STM32 ARM 32-bit CortexTM-M3 Frequency up to 120 MHz
Diverse serial interface	SPI, USART
Sensor applications support	ADC, I2C, I2S,GPIO, CAN bus, 8-bit parallel camera interface, Timers,USB
Debug interface support	JTAG
On-chip functionality Single-chip	MAC/BB/RF
Frequency Band	2.4 GHz
Transmit Power	+17 dBm @b mode/11 Mbps
MIN Receiver Sensitivity	-96 dBm
Network Standard	802.11b, 802.11g, 802.11n (single stream)
Modulation Modes	CCK and OFDM with BPSK, QPSK, 16 QAM, 64QAM
Hardware Encryption	WEP, WPA/WPA2
Supported Data Rates	IEEE 802.11b 1 – 11 Mbps IEEE 802.11g 6 – 54 Mbps IEEE 802.11n (2.4 GHz) 7.2 – 72.2 Mbps
Advanced 1x1 802.11n features	Full/Half Guard Interval Frame Aggregation Space Time Block Coding (STBC) Low Density Parity Check (LDPC) Encoding
Two antenna configurations	Supported antenna diversity
Operating Temperature	-40℃ to 85℃
MSL level 3	
Certification	FCC and CE compliant

2. Block Diagram



ADC	Analog to Digital Converter
DAC	Digital to Analog Converter
I2C	Intelligent Interface Controller
SPI	Serial Peripheral Interface
CAN	Controller Area Network
USART	Universal synchronous/asynchronous receiver transmitters
DCMI	Digital Camera Interface (8-bit parallel)
TIM	Timers
I2S	Inter-integrated sound
Potentiometer	Thermal meter or sensor
USB	Universal serial bus on-the-go high-speed

3. Electrical Specification

3.1 Absolute Maximum Rating

Supply Power	Max +4.35 Volt		
Storage Temperature	- 40° to 85° Celsius		
Voltage ripple	+/- 2%	Max. Values not exceeding Operating voltage	
	Power	min	Max
Power Supply Absolute Maximum Ratings	VBAT	0	4
	VDD3V3_1	0	4
	VDD3V3_2	0	4
	VDD3V3_3	0	4
	VDD_3V3_WIFI	0	6
	VDD_3V3_WIFI_PA	0	6
	VDDIO_WIFI	0	4

3.2 Recommendable Operation Condition

3.2.1 Temperature, Humidity

The WiFi Network Controller module has to withstand the operational requirements as listed in the table below.

Operating Temperature	-40° to 85° Celsius	
Humidity range	Max 95%	Non condensing, relative humidity

3.2.2 Voltage

Power supply for the WiFi Network Controller module will be provided by the host via the power pins

Symbol	Parameter	Min	Typ	Max	Unit
VBAT	MCU VBAT Voltage	2.0	3.3	3.6	V
VDD3V3_1	GPIO I/O Supply	2.4	3.3	3.6	V
VDD3V3_2	GPIO I/O Supply	2.4	3.3	3.6	V
VDD3V3_3	GPIO I/O Supply	2.4	3.3	3.6	V
VDD_3V3_WIFI	WiFi Voltage		3.3	3.6	V
VDD_3V3_WIFI_PA	WiFi PA Voltage		3.3	3.6	V
VDDIO_WIFI	MCU With WiFi		3.3	3.6	V
	Only WiFi Function	1.8	3.3	3.6	V

3.3 Current Consumption

3.3.1 WLAN

Condition: Condition: 25deg.C, includes Both WiFi and Micro-Controller

Item	Condition	Min	Nom	Max	Unit
Tx mode(11b Max current)	11Mbps		345		mA
Tx mode(11g Max current)	54Mbps		250		mA
Tx mode(11n Max current)	MCS7		210		mA
Rx mode	11b (11Mbps)		115	150	mA
	11g (54Mbps)		115	150	mA
	11n (MCS7)		115	150	mA

4. RF Specification

4.1 wireless Specification

The WiFi Network Controller module complies with the following features and standards;

Features	Description
WLAN Standards	IEEE 802 Part 11b/g/n (802.11b/g/n single stream n)
Antenna Port	Support Single Antenna for WiFi
Frequency Band	2.400 – 2.484 GHz

The RF performance of WiFi Network Controller is given as follows. The default voltage is 3.3V.

Features	Description
Frequency Band	2.4000 – 2.497 GHz (2.4 GHz ISM Band)
Number of selectable Sub channels	14 channels
Modulation	OFDM, DSSS (Direct Sequence Spread Spectrum), DBPSK, DQPSK, CCK , 16QAM, 64QAM
Supported rates	1,2, 5.5,11,6,9,12,24,36,48,54 Mbps & HT20 MCS 0~7
Maximum receive input level	- 10dBm (with PER < 8%@11 Mbps) - 20dBm (with PER < 10%@54 Mbps) - 20dBm (with PER < 10%@MCS7)
Output Power	17dBm @ 802.11b 13dBm @ 802.11g 11dBm @ 802.11n
Carrier Frequency Accuracy	+/- 20ppm (crystal: 26MHz +/-10ppm in 250C)

4.2 WiFi RF Transmitter Specification

802.11b Transmit					
Item	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Transmit output power level	1M/2M/5.5M/11M		17		dBm
Transmit center frequency tolerance		-20		20	ppm
Transmit spectrum mask	Fc-22MHz<F<Fc-11MHz & Fc+11MHz<F<Fc+22MHz(1/2/5.5/11Mbps; channel 1~13)			-30*	dBr
	F<Fc-22MHz & F>Fc+22MHz(1/2/5.5/11Mbps; channel 1~13)			-50*	dBr
Transmit power -on	10% ~ 90 %		0.3	2*	us
Transmit power -down	90% ~ 10 %		1.5	2*	us
Transmit modulation accuracy	1/2/5.5/11 Mbps		-17	-10	dB

*” indicates IEEE802.11 specification

802.11g Transmit					
Item	Condition	Min.	Typ.	Max.	Unit
Transmit output power level	6M/9M/12M/18M/24M/36M/48M/54M		13		dBm dBm dBm
Transmit center frequency tolerance		-20	0	20	ppm
Transmit modulation accuracy	6Mbps			-5*	dB
	9Mbps			-8*	dB
	12Mbps			-10*	dB
	18Mbps			-13*	dB
	24Mbps			-16*	dB
	36Mbps			-19*	dB
	48Mbps			-22*	dB
	54Mbps			-25*	dB
Transmit spectrum mask	@ 11MHz			-20*	dBr
	@ 20MHz			-28*	dBr
	@ 30MHz			-40*	dBr

802.11n Transmit					
Item	Condition	Min.	Typ.	Max.	Unit
Transmit output power level	HT20 MCS 0~7		11		dBm dBm dBm
Transmit center frequency tolerance		-20	0	20	ppm
Transmit modulation accuracy	HT20, MCS0~7			-28*	dB dB
Transmit Spectrum mask	@ 11MHz			-20*	dBr
	@ 20MHz			-28*	dBr
	@ 30MHz			-40*	dBr

*” indicates IEEE802.11 specification

4.3 WIFi RF Receiver Specification

802.11 b Receiver					
Item	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Receiver minimum input level sensitivity (PER< 8 %)	1Mbps			-80*	dBm
	2Mbps			-80*	dBm
	5.5Mbps			-76*	dBm
	11Mbps			-76*	dBm
Receiver maximum input level sensitivity (PER< 8 %)	1/2/5.5/11 Mbps			-10*	dBm

"*" indicates IEEE802.11 specification

802.11g Receiver					
Item	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Receiver minimum input level sensitivity (PER<10 %)	6Mbps			-82*	dBm
	9Mbps			-81*	dBm
	12Mbps			-79*	dBm
	18Mbps			-77*	dBm
	24Mbps			-74*	dBm
	36Mbps			-70*	dBm
	48Mbps			-66*	dBm
	54Mbps			-65*	dBm
Receiver maximum input level (PER<10%)	6/9/12/18/24/36/48/54			-20*	dBm

"*" indicates IEEE802.11 specification

802.11n Receiver					
Item	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Receiver minimum input level sensitivity (PER<10 %)	HT20, MCS0			-82*	dBm
	HT20, MCS1			-79*	dBm
	HT20, MCS2			-77*	dBm
	HT20, MCS3			-74*	dBm
	HT20, MCS4			-70*	dBm
	HT20, MCS5			-66*	dBm
	HT20, MCS6			-65*	dBm
	HT20, MCS7			-64*	dBm
Receiver maximum input level (PER<10%)	MSC0~MSC7			-20*	dBm

"*" indicates IEEE802.11 specification

5. Pin Definition

5.1 The detail pin definition information

Pin Number	Pin Name	type	Description	Alternate Function	Mapping STM32F20x LQFP176
1	GND	I/O	Ground		
2	ANT	I/O	RF transmitter output and RF receiver input		
3	GND	-	Ground		
4	RF_SW_CTRL_ANT1	I/O	Antenna diversity control signal		
5	RF_SW_CTRL_ANT0	I/O	Antenna diversity control signal		
6	GND	-	Ground		
7	VDD_3V3_Wifi_PA	PI	Wi-Fi PA power supply		
8	VDD_3V3_Wifi_PA	PI	Wi-Fi PA power supply		
9	GND	-	Ground		
10	MICRO_SPI_SSN	I/O	MCU_SPI_SSN	ADC_IN_4 / DAC1_OUT / EVENTOUT / General purpose I/O	PA4
11	MICRO_SPI_SCK	I/O	MCU_SPI_SCK form MCU	ADC_IN_5 / TIMER/DAC2_OUT / EVENTOUT / General purpose I/O	PA5
12	DCMI_PIX_CLK /MICRO_SPI_MISO	I/O	MCU_DCMI_PIX_CLK or MCU_SPI_MISO	ADC_IN_6 / TIMER/EVENTOUT / General purpose I/O	PA6
13	MICRO_SPI_MOSI	I/O	MCU_SPI_MOSI	ADC_IN_7 / TIMER/EVENTOUT / General purpose I/O	PA7
14	WIFI_VDD_EN	I/O	Enable Wi-Fi VDD		
15	GND	-	Ground		
16	VDD_3V3_3	PI	DC supply for MCU and I/O		
17	GND		Ground		
18	VDD_3V3_Wifi_IN	PI	Wi-Fi power supply		
19	VDD_3V3_Wifi_IN	IP	Wi-Fi power supply		
20	GND	-	Ground		
21	DCMI_HSYNC	I/O	MCU_DCMI_HSYNC	EVENTOUT / General purpose I/O	PH8
22	DCMI_D0	I/O	MCU_DCMI_D0	EVENTOUT / General purpose I/O	PH9
23	DCMI_D1	I/O	MCU_DCMI_D1	EVENTOUT / General purpose I/O	PH10

Pin Number	Pin Name	type	Description	Alternate Function	Mapping STM32F20x LQFP176
24	DCMI_D2	I/O	MCU_DCMI_D2	EVENTOUT / General purpose I/O	PH11
25	DCMI_D3	I/O	MCU_DCMI_D3	EVENTOUT / General purpose I/O	PH12
26	DCMI_D4	I/O	MCU_DCMI_D4	EVENTOUT / General purpose I/O	PH14
27	GND	PI	Ground		
28	MICRO_UART_TX	I/O	MCU_UART_TX	EVENTOUT/TIMER/ General purpose I/O	PA9
29	MICRO_UART_RX	I/O	MCU_UART_TX	EVENTOUT/ TIMER/ General purpose I/O	PA10
30	32K_PWM_OUT	I	WiFi 32.768KHz (Sleep Clock) input		
31	CAN_RX	I/O	MCU_CAN_RX	EVENTOUT/ General purpose I/O	PD0
32	CAN_TX	I/O	MCU_CAN_TX	EVENTOUT / General purpose I/O	PD1
33	GND	-	Ground		
34	MICRO_USART2_TX	I/O	MCU_USART2_TX	EVENTOUT / General purpose I/O	PD5
35	MICRO_USART2_RX	I/O	MCU_USART2_RX	EVENTOUT / General purpose I/O	PD6
36	MICRO_JATG_TMS	I/O	MCU_JATG_TMS	EVENTOUT / General purpose I/O	PA13
37	MICRO_JATG_TCK	I/O	MCU_JATG_TCK	EVENTOUT / General purpose I/O	PA14
38	MICRO_JATG_TDI	I/O	MCU_JATG_TDI	EVENTOUT/TIMER/ General purpose I/O	PA15
39	MICRO_JATG_TDO	I/O	MCU_JATG_TDO	EVENTOUT / General purpose I/O	PB3
40	MICRO_JATG_TRSTN	I/O	MCU_JATG_RSTN	EVENTOUT / General purpose I/O	PB4
41	VDD_3V3_2	PI	DC supply for MCU and I/O		
42	VDDIO_WIFI	PI	DC supply for WIFI and I/O		
43	GND	-	Ground		
44	WL_RST_N	I/O	WIFI Reset (If use Only WiFi Function)		
45	MICRO_ I2C1_SCL	I/O	MCU_I2C1_SCL	EVENTOUT/ General purpose I/O	PB6
46	MICRO_ I2C1_SDA	I/O	MCU_I2C1_SDA	EVENTOUT General purpose I/O	PB7
47	BOOT0	O	Normal operation if connected to ground at power up.		BOOT0
48	GND	-	Ground		

Pin Number	Pin Name	type	Description	Alternate Function	Mapping STM32F20x LQFP176
49	DCMI_D5	I/O	MCU_DCMI_D5	EVENTOUT / General purpose I/O	PI4
50	DCMI_VSYNC	I/O	MCU_DCMI_VSYNC	EVENTOUT / General purpose I/O	PI5
51	DCMI_D6	I/O	MCU_DCMI_D6	EVENTOUT / General purpose I/O	PI6
52	DCMI_D7	I/O	MCU_DCMI_D7	EVENTOUT / General purpose I/O	PI7
53	GND	-	Ground		
54	GND	-	Ground		
55	OSC_32K_IN	I/O	MCU_32KHz Crystal input		PC14
56	OSC_32K_OUT	I/O	MCU_32KHz Crystal output		PC15
57	GND	-	Ground		
58	LED0	O	LED		PI9
59	GND	-	Ground		
60	VBAT	PI	Power supply for backup circuitry when VDD is not present		
61	GND	-	Ground		
62	MICRO_GPIO_0	I/O	MCU_General purpose I/O	EVENTOUT / I2C2_SDA	PF0
63	MICRO_GPIO_1	I/O	MCU_General purpose I/O	EVENTOUT / I2C2_SCL	PF1
64	MICRO_RST_N	I/O	MCU_RST_N		RST_L
65	WL_CLK_REQ	I/O	WIFI_CLK_Request		
66	GND	-	Ground		
67	VDD_3V3_1	PI	DC supply for MCU and I/O		
68	GND		Ground		
69	MICRO_WKUP	I/O	MCU_WKUP		PA0
70	MICRO_ADC_IN1	I/O	MCU_ADC_IN_1	EVENTOUT / TIMER/ General purpose I/O	PA1
71	MICRO_ADC_IN2	I/O	MCU_ADC_IN_2	EVENTOUT / TIMER/ General purpose I/O	PA2
72	MICRO_ADC_IN3	I/O	MCU_ADC_IN_3	EVENTOUT / TIMER/ General purpose I/O	PA3
73	GND		Ground		
74	MICRO_I2S2_WS	I/O	MCU_I2S2_WS	EVENTOUT / General purpose I/O	PB12
75	SDIO_DATA_2	I/O	WIFI_SDIO_DATA2		
76	SDIO_DATA_0	I/O	WIFI_SDIO_DATA0	WIFI_SPI_MISO	
77	SDIO_DATA_1	I/O	WIFI_SDIO_DATA_1	WIFI_SPI_IRQ	
78	SDIO_DATA_3	I/O	WIFI_SDIO_DATA_3	WIFI_SPI_CSX	

Pin Number	Pin Name	type	Description	Alternate Function	Mapping STM32F20x LQFP176
79	SDIO_DATA_CLK	I/O	WIFI_SDIO_DATA_CLK	WIFI_SPI_CLK	
80	SDIO_DATA_CMD	I/O	WIFI_SDIO_DATA_CMD	WIFI_SPI_MOSI	
81	MICRO_TIM8_CH1N	I/O	MCU_TIM8_CH1N	EVENTOUT / General purpose I/O	PH13
82	MICRO_TIM8_CH3N	I/O	MCU_TIM8_CH3N	EVENTOUT / General purpose I/O	PH15
83	MICRO_SPI2_MISO	I/O	MCU_SPI2_MISO	EVENTOUT / TIMER/ General purpose I/O	PI2
84	MICRO_SPI2_SCK	I/O	MCU_SPI2_SCK	EVENTOUT / General purpose I/O	PI1
85	MICRO_SPI2_NSS	I/O	MCU_SPI2_NSS	EVENTOUT / TIMER/ General purpose I/O	PI0
86	MICRO_SPI2_MOSI	I/O	MCU_SPI2_MOSI	EVENTOUT / TIMER/ General purpose I/O	PI3
87	MICRO_I2S2_MCK	I/O	MCU_I2S2_MCK	EVENTOUT / TIMER/ General purpose I/O	PC6
88	MICRO_TIM9_CH1	I/O	MCU_TIM9_CH1	EVENTOUT / General purpose I/O	PE5
89	MICRO_TIM9_CH2	I/O	MCU_TIM9_CH2	EVENTOUT / General purpose I/O	PE6
90	Potentiometer	I/O	MCU_Potentiometer	EVENTOUT / TIMER/ADC/ General purpose I/O	PF9
91	WL_GPIO_0	I/O	WiFi_General purpose I/O		
92	WL_GPIO_1	I/O	WiFi_General purpose I/O		
93	MICRO_I2S2_SCK	I/O	MCU_I2S2_SCK	EVENTOUT / TIMER/ General purpose I/O	PB10
94	MICRO_I2S2_SD/ USB_HS_DP	I/O	MCU_2S2_SD or MCU_USB_HS_DP	EVENTOUT / TIMER/ General purpose I/O	PB15
95	USB_HS_DM	I/O	MCU_USB_HS_DM	EVENTOUT / TIMER/ General purpose I/O	PB14

* Marked yellow Pins are only using in WICED Module without MCU function.

5.2 Alternate function mapping Table

Pin NO	Mapping STM32F20x_LQFP176	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/I2C2/I2C3	SPI1/SPI2/I2S2	SPI3/I2S3	UASRT1/2/3	UART4/5/USART6	CAN1/CAN2/TIM12/13/14	OTG_FS/OTG_HS	FSMC/SDIO/OTG_HS	DCMI	ADC/DAC	EVENTOUT/GPIO
10	PA4						SPI1_NSS	SPI3_NSS, I2S3_WS	USART2_CK				OTG_HS_SOF	DCMI_HSYNC	ADC12_IN4/DAC1OUT	EVENTOUT/GPIO
11	PA5		TIM2_CH1, TIM2_ETR		TIM8_CH1N		SPI1_SCK					OTG_HS_ULPI_CK			ADC12_IN5/DAC2_OUT	EVENTOUT/GPIO
12	PA6		TIM1_BKIN	TIM3_CH1	TIM8_BKIN		SPI1_MISO				TIM13_CH1			DCMI_PIXCK	ADC12_IN6	EVENTOUT/GPIO
13	PA7		TIM1_CH1N	TIM3_CH2	TIM8_CH1N		SPI1_MOSI				TIM14_CH1				ADC12_IN7	EVENTOUT/GPIO
21	PH8					I2C3_SDA								DCMI_HSYNC		EVENTOUT/GPIO
22	PH9					I2C3_SMBA					TIM12_CH2			DCMI_D0		EVENTOUT/GPIO
23	PH10			TIM5_CH1										DCMI_D1		EVENTOUT/GPIO
24	PH11			TIM5_CH2										DCMI_D2		EVENTOUT/GPIO
25	PH12			TIM5_CH3										DCMI_D3		EVENTOUT/GPIO
26	PH14				TIM8_CH2N									DCMI_D4		EVENTOUT/GPIO
28	PA9		TIM1_CH2			I2C3_SMBA			USART1_TX					DCMI_D0		EVENTOUT/GPIO
29	PA10		TIM1_CH3						USART1_RX			OTG_FS_ID		DCMI_D1		EVENTOUT/GPIO
31	PD0										CAN1_RX		FSMC_D2			EVENTOUT/GPIO
32	PD1										CAN1_TX		FSMC_D3			EVENTOUT/GPIO
34	PD5								USART2_TX				FSMC_NWE			EVENTOUT/GPIO
35	PD6								USART2_RX				FSMC_NWAIT			EVENTOUT/GPIO
36	PA13	JTMS-														EVENTOU

		SWDIO														T/GPIO

Pin NO.	Mapping STM32F 20x_LQ FP176	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/I2C2/I2C3	SPI1/SPI2/I2S2	SPI3/I2S3	UASRT1/2/3	UART4/5/USART6	CAN1/CAN2/TIM12/13/14	OTG_FS/OTG_HS	FSMC/SDIO/OTG_HS	DCMI	ADC/DAC	GPIO
37	PA14	JTCK-SWCLK														EVENTOUT/GPIO
38	PA15	JTDI	TIM2_CH1 TIM2_ETR				SPI1_NSS	SPI3_NSS, I2S3_WS								EVENTOUT/GPIO
39	PB3	JTDO/TRACESWO	TIM2_CH2				SPI1_SCK	SPI3_SCK , I2S3_SCK								EVENTOUT/GPIO
40	PB4	JTRST		TIM3_CH1			SPI1_MISO	SPI3_MISO								EVENTOUT/GPIO
45	PB6			TIM4_CH1		I2C1_SCL			USART1_TX		CAN2_TX			DCMI_D5		EVENTOUT/GPIO
46	PB7			TIM4_CH2		I2C1_SDA			USART1_RX				FSMC_NL	DCMI_VSYNC		EVENTOUT/GPIO
49	PI4				TIM8_BKIN									DCMI_D5		EVENTOUT/GPIO
50	PI5				TIM8_CH1									DC MI_VSYNC		EVENTOUT/GPIO
51	PI6				TIM8_CH2									DCMI_D6		EVENTOUT/GPIO
52	PI7				TIM8_CH3									DCMI_D7		EVENTOUT/GPIO
62	PF0					I2C2_SDA							FSMC_A0			EVENTOUT/GPIO
63	PF1					I2C2_SCL							FSMC_A1			EVENTOUT/GPIO
69	PA0-WKUP		TIM2_CH1 TIM2_ETR	TIM5_CH1	TIM8_ETR				USART2_CTS	UART4_TX					ADC123_IN0	EVENTOUT/GPIO
70	PA1		TIM2_CH2	TIM5_CH2					USART2_RTS	UART4_RX					ADC123_IN1	EVENTOUT/GPIO
71	PA2		TIM2_CH3	TIM5_CH3	TIM9_CH1				USART2_TX						ADC123_IN2	EVENTOUT/GPIO
72	PA3		TIM2_CH4	TIM5_CH4	TIM9_CH2				USART2_RX			OTG_HS_ULPI_D0			ADC123_IN3	EVENTOUT/GPIO
74	PB12		TIM1_BKIN			I2C2_SM	SPI2_		USART3		CAN2_R	OTG_HS	OTG_H			EVENTOU

						BA	NSS, I2S2_WS		_CK		X	_ULPI_D5	S_ID			T/GPIO

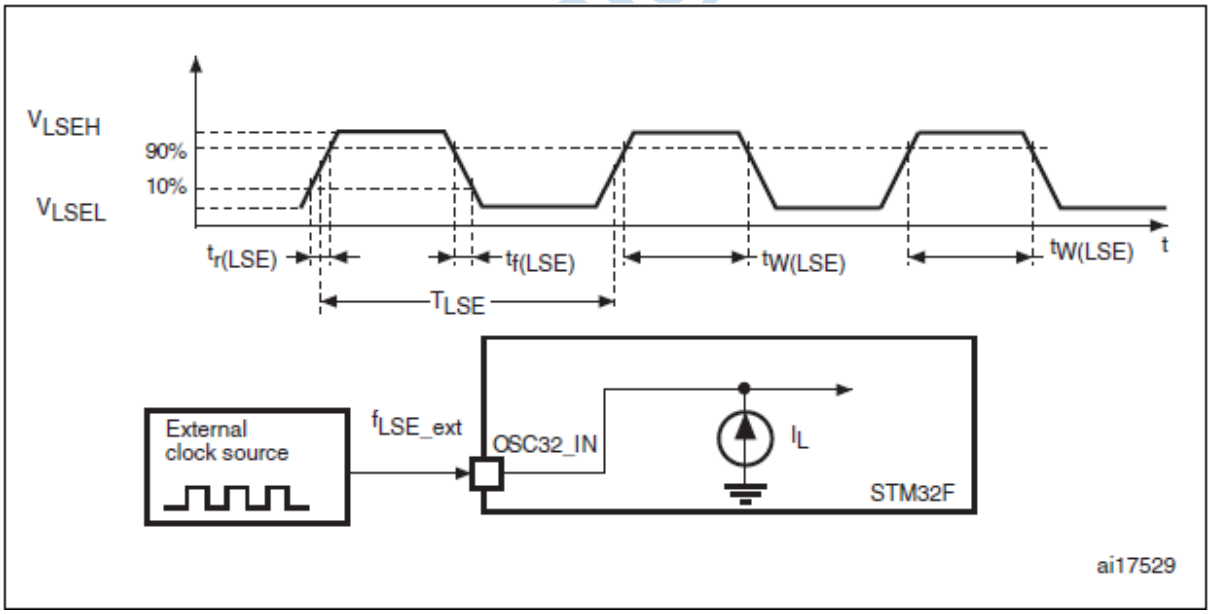
Pin NO.	Mapping STM32F 20x_LQ FP176	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7	AF8	AF9	AF10	AF12	AF13	AF14	AF15
		SYS	TIM1/2	TIM3/4/5	TIM8/9/10/11	I2C1/I2C2/I2C3	SPI1/SPI2/I2S2	SPI3/I2S3	UASRT1/2/3	UART4/5/USART6	CAN1/CAN2/TIM12/13/14	OTG_FS/OTG_HS	FSMC/SDIO/OTG_HS	DCMI	ADC/DAC	GPIO
81	PH13				TIM8_CH1N						CAN1_TX					EVENTOUT/GPIO
82	PH15				TIM8_CH3N									DCMI_D11		EVENTOUT/GPIO
83	PI2				TIM8_CH4		S PI2_MISO							DCMI_D9		EVENTOUT/GPIO
84	PI1						SPI 2_SCK, I2S2_SC K							DCMI_D8		EVENTOUT/GPIO
85	PI0			TIM5_CH4			SPI 2_NSS, I2S2_WS							DCMI_D13		EVENTOUT/GPIO
86	PI3				TIM8_ETR		S PI2_MOSI, I2S2_SD							DCMI_D10		EVENTOUT/GPIO
87	PC6			TIM3_CH1	TIM8_CH1		I2S2_MCK			USART6_TX			SDIO_D6	DCMI_D0		EVENTOUT/GPIO
88	PE5	TRACED2			TIM9_CH1								FSMC_A21	DCMI_D6		EVENTOUT/GPIO
89	PE6	TRACED3			TIM9_CH2								FSMC_A22	DCMI_D7		EVENTOUT/GPIO
90	PF9										TIM14_CH1		FSMC_CD		ADC3_IN7	EVENTOUT/GPIO
93	PB10		TIM2_CH3			I2C2_SCL	SPI2_SCK, I2S2_SCK		USART3_TX			OTG_HS_ULPI_D3				EVENTOUT/GPIO
94	PB15	RTC_50Hz	TIM1_CH3N		TIM8_CH3N		SPI2_MOSI, I2S2_SD				TIM12_CH2		OTG_HS_DP			EVENTOUT/GPIO
95	PB14		TIM1_CH2N		TIM8_CH2N		SPI2_MISO		USART3_RTS		TIM12_CH1		OTG_HS_DM			EVENTOUT/GPIO

6. Addition Information

6.1 Low Speed External Clock Source Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE_ext}	User External clock source frequency(1)		-	32.768	1000	kHz
V_{LSEH}	OSC32_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LSEL}	OSC32_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LSE)}$ $t_{f(LSE)}$	OSC32_IN high or low time(1)		450	-	-	ns
$t_{r(LSE)}$ $t_{f(LSE)}$	OSC32_IN rise or fall time(1)		-	-	50	
$C_{in(LSE)}$	OSC32_IN input capacitance(1)		-	5	-	pF
$DuCy_{(LSE)}$	Duty cycle		30	-	70	%
I_L	OSC32_IN Input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	µA

1. Guaranteed by design, not tested in production.



Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified above table. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_F	Feedback resistor		-	18.4	-	MΩ
$C^{(2)}$	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)$^{(3)}$	R_S = 30 kΩ	-	-	15	pF
I_2	LSE driving current	V_{DD} = 3.3 V, V_{IN} = V_{SS}	-	-	3.5	µA
g_m	Oscillator Transconductance		7	-	-	µA/V
$t_{SU(LSE)}^{(4)}$	startup time	V_{DD} is stabilized	-	2	-	s

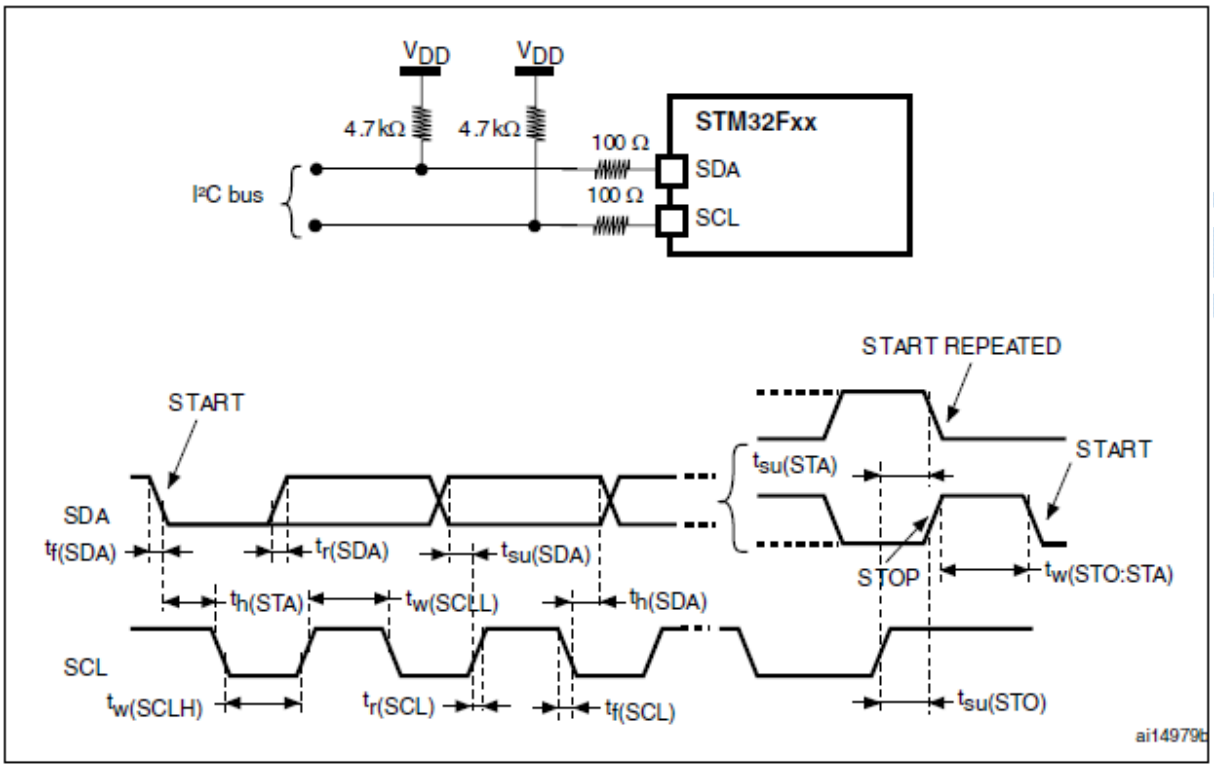
1. Based on characterization, not tested in production.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. The oscillator selection can be optimized in terms of supply current using an high quality resonator with small RS value for example MSIV-TIN32.768kHz. Refer to crystal manufacturer for more details
4. tSU(LSE) is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

6.2 Communications Interfaces

6.2.1 I2C Interface Characteristics

Symbol	Parameter	Standard mode I^2C(1)		Fast mode I^2C(1)(2)		Unit
		Min	Max	Min	Max	
$t_{w(SCLL)}$	SCL clock low time	4.7	-	1.3	-	µs
$t_{w(SCLH)}$	SCL clock high time	4.0	-	0.6	-	
$t_{su(SDA)}$	SDA setup time	250	-	100	-	ns
$t_{h(SDA)}$	SDA data hold time	0(3)	-	0(4)	900(3)	
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time	-	1000	$20 + 0.1C_b$	300	
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time	-	300	-	300	
$t_{h(STA)}$	Start condition hold time	4.0	-	0.6	-	µs
$t_{su(STA)}$	Repeated Start condition setup time	4.7	-	0.6	-	
$t_{su(STO)}$	Stop condition setup time	4.0	-	0.6	-	µs
$t_{w(STO:STA)}$	Stop to Start condition time (bus free)	4.7	-	1.3	-	µs
C_b	Capacitive load for each bus line	-	400	-	400	pF

1. Guaranteed by design, not tested in production.
2. fP CLK1 must be at least 2 MHz to achieve standard mode I2C frequencies. It must be at least 4MHz to achieve fast mode I2C frequencies, and a multiple of 10 MHz to reach the 400 kHz maximum I2C fast mode clock.
3. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.
4. The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

6.2.2 SPI Interface Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	30	MHz
		Slave mode	-	30	
$t_{r(SCL)}$ $t_{f(SCL)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	8	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$ (2)	NSS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(NSS)}$ (2)	NSS hold time	Slave mode	$2t_{PCLK}$	-	
$t_{w(SCLH)}$ (2) $t_{w(SCLL)}$ (2)	SCK high and low time	Master mode, f_{PCLK} = 30 MHz, presc = 2	t_{PCLK}-3	t_{PCLK}+3	
$t_{su(MI)}$ (2) $t_{su(SI)}$ (2)	Data input setup time	Master mode	5	-	
		Slave mode	5	-	
$t_{h(MI)}$ (2) $t_{h(SI)}$ (2)	Data input hold time	Master mode	5	-	
		Slave mode	4	-	
$t_{a(SO)}$ (2)(3)	Data output access time	Slave mode, f_{PCLK} = 20 MHz	0	$3t_{PCLK}$	
$t_{dis(SO)}$ (2)(4)	Data output disable time	Slave mode	2	10	
$t_{v(SO)}$ (2)(1)	Data output valid time	Slave mode (after enable edge)	-	25	
$t_{v(MO)}$ (2)(1)	Data output valid time	Master mode (after enable edge)	-	5	
$t_{h(SO)}$ (2)	Data output hold time	Slave mode (after enable edge)	15	-	
$t_{h(MO)}$ (2)		Master mode (after enable edge)	2	-	

1. Remapped SPI1 characteristics to be determined.
2. Based on characterization, not tested in production.
3. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
4. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

6.2.3 DCMI Interface Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
	Frequency ratio DCMI_PIXCLK/f_{HCLK}	DCMI_PIXCLK= 48 MHz		0.4	

6.2.4 TIM timer Interface Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	AHB/APB1 prescaler distinct from 1, $f_{TIMxCLK}$ = 60 MHz	1	-	$t_{TIMxCLK}$
			16.7	-	ns
		AHB/APB1 prescaler = 1, $f_{TIMxCLK}$ = 30 MHz	1	-	$t_{TIMxCLK}$
			33.3	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	$f_{TIMxCLK}$ = 60 MHz APB1= 30 MHz	0	$f_{TIMxCLK}/2$	MHz
			0	30	MHz
Res_{TIM}	Timer resolution		-	16/32	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected		1	65536	$t_{TIMxCLK}$
			0.0167	1092	µs
	32-bit counter clock period when internal clock is selected		1	-	$t_{TIMxCLK}$
			0.0167	71582788	µs
t_{MAX_COUNT}	Maximum possible count		-	65536 × 65536	$t_{TIMxCLK}$
			-	71.6	s

1. TIMx is used as a general term to refer to the TIM2, TIM3, TIM4, TIM5, TIM6, TIM7, and TIM12 timers.

6.2.5 I2S timer Interface Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{CK} $1/t_{c(CK)}$	I^2S clock frequency	Master	1.23	1.24	MHz
		Slave	0	TBD	
$t_{r(CK)}$ $t_{f(CK)}$	I^2S clock rise and fall time	capacitive load C_L = 50 pF	-	TBD	ns
$t_{v(WS)}$ (2)	WS valid time	Master	0.3	-	
$t_{h(WS)}$ (2)	WS hold time	Master	0	-	
$t_{su(WS)}$ (2)	WS setup time	Slave	3	-	
$t_{h(WS)}$ (2)	WS hold time	Slave	0	-	
$t_{w(CKH)}$ (2) $t_{w(CKL)}$ (2)	CK high and low time	Master f_{PCLK}= 120 MHz, presc = 7	396	-	
$t_{su(SD\_MR)}$ (2) $t_{su(SD\_SR)}$ (2)	Data input setup time	Master receiver Slave receiver	45 0	-	
$t_{h(SD\_MR)}$ (2)(3) $t_{h(SD\_SR)}$ (2)(3)	Data input hold time	Master receiver Slave receiver	13 0	-	
$t_{h(SD\_MR)}$ (2) $t_{h(SD\_SR)}$ (2)	Data input hold time	Master f_{PCLK} = 120 MHz, Slave f_{PCLK}=120 MHz	13 0	-	
$t_{v(SD\_ST)}$ (2)(3)	Data output valid time	Slave transmitter (after enable edge)	-	12	
		f_{PCLK} = 120 MHz	-	12	
$t_{h(SD\_ST)}$ (2)	Data output hold time	Slave transmitter (after enable edge)	10	-	
$t_{v(SD\_MT)}$ (2)(3)	Data output valid time	Master transmitter (after enable edge)	-	4	
		f_{PCLK} = 120 MHz	4	6	
$t_{h(SD\_MT)}$ (2)	Data output hold time	Master transmitter (after enable edge)	0	-	

1. TBD stands for “to be defined”.
2. Based on design simulation and/or characterization results, not tested in production.
3. Depends on f_{PCLK}. For example, if f_{PCLK}=8MHz, then TPCLK=f / f_{PCLK}=125ns.

6.2.5 USB HS characteristics

USB HS DC electrical characteristics

Symbol		Parameter	Min.(1)	Max.(1)	Unit
Input level	V_{DD}	Ethernet operating voltage	2.7	3.6	V

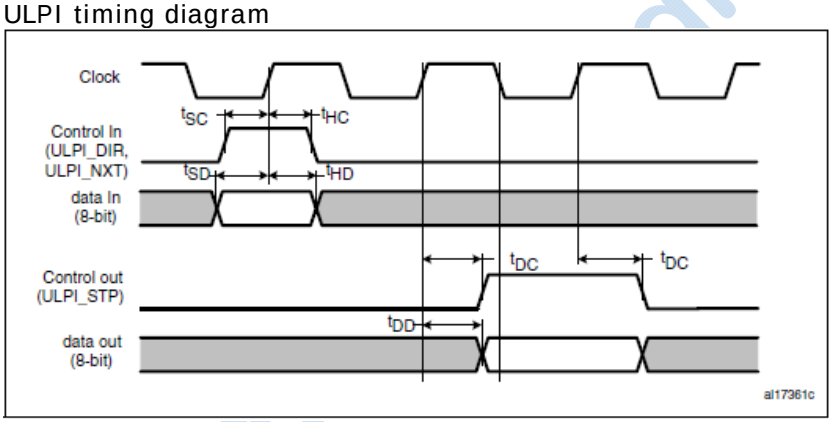
1. All the voltages are measured from the local ground potential.

Clock timing parameters

Parameter(1)		Symbol	Min	Nominal	Max	Unit
Frequency (first transition)	8-bit ±10%	F_{START_8BIT}	54	60	66	MHz
Frequency (steady state) ±500 ppm		F_{STEADY}	59.97	60	60.03	MHz
Duty cycle (first transition)	8-bit ±10%	D_{START_8BIT}	40	50	60	%
Duty cycle (steady state) ±500 ppm		D_{STEADY}	49.975	50	50.025	%
Time to reach the steady state frequency and duty cycle after the first transition		T_{STEADY}	-	-	1.4	ms
Clock startup time after the de-assertion of SuspendM	Peripheral	T_{START_DEV}	-	-	5.6	ms
	Host	T_{START_HOST}	-	-	-	
PHY preparation time after the first transition of the input clock		T_{PREP}	-	-	-	µs

1. Guaranteed by design, not tested in production.

ULPI timing diagram



ULPI timing

Parameter	Symbol	Value(1)		Unit
		Min.	Max.	
Control in (ULPI_DIR) setup time	t_{SC}	-	2.0	ns
Control in (ULPI_NXT) setup time		-	1.5	
Control in (ULPI_DIR, ULPI_NXT) hold time	t_{HC}		-	
Data in setup time	t_{SD}	-	2.0	
Data in hold time	t_{HD}	0	-	
Control out (ULPI_STP) setup time and hold time	t_{DC}	-	9.2	
Data out available from clock rising edge	t_{DD}	-	10.7	

1. V_{DD} = 2.7 V to 3.6 V and T_A = –40 to 85 °C.

7. Mechanical & Weight Specification

7.1 Size of the Module

The following paragraphs provide the requirements for the size, weight.
The size and thickness of the WiFi Network Controller module 10mm (W) x 10mm (L) x 1.1mm (H):

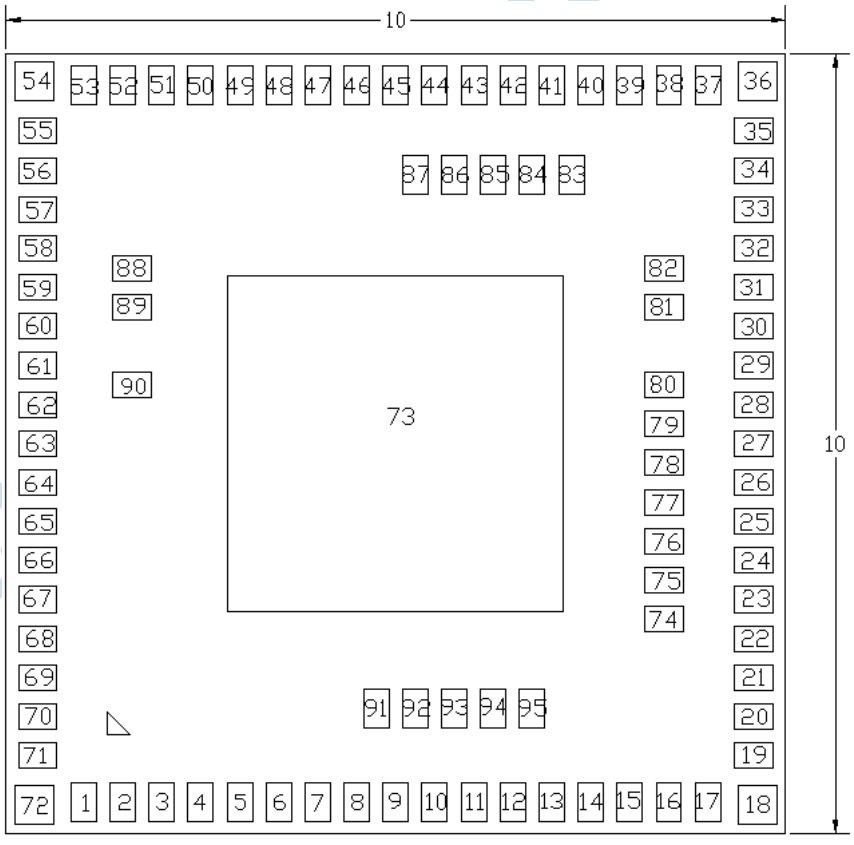
(Tolerance: +/- 0.1mm)

7.2 Weight of the Module

	Min	Typ	Max	Unit
Module's Weight		TBD		gram

7.3 Mechanical Dimension

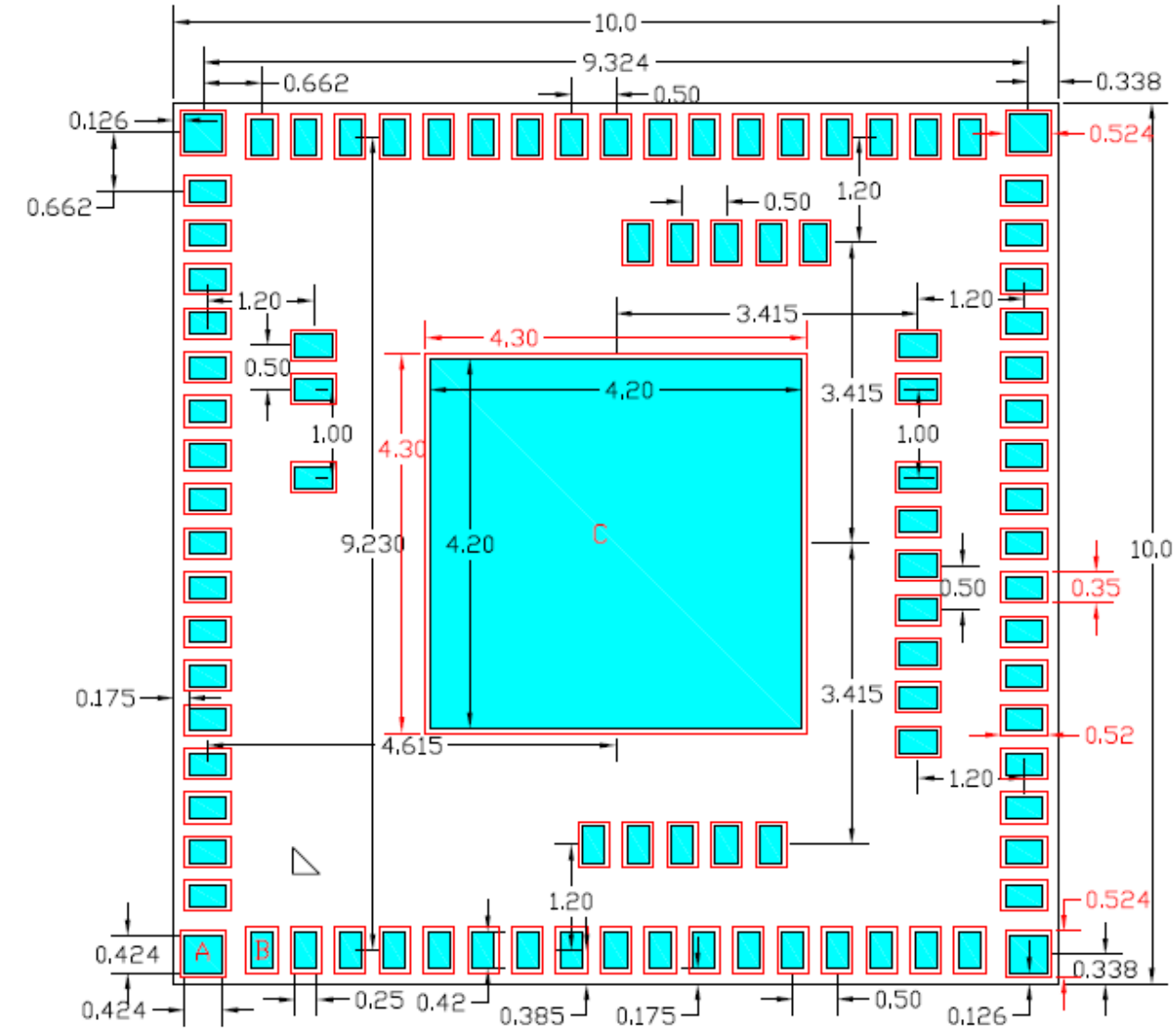
Dimension: 10 x 10 x 1.1 mm3



TOP View

8. Recommend Footprint

Unit: mm



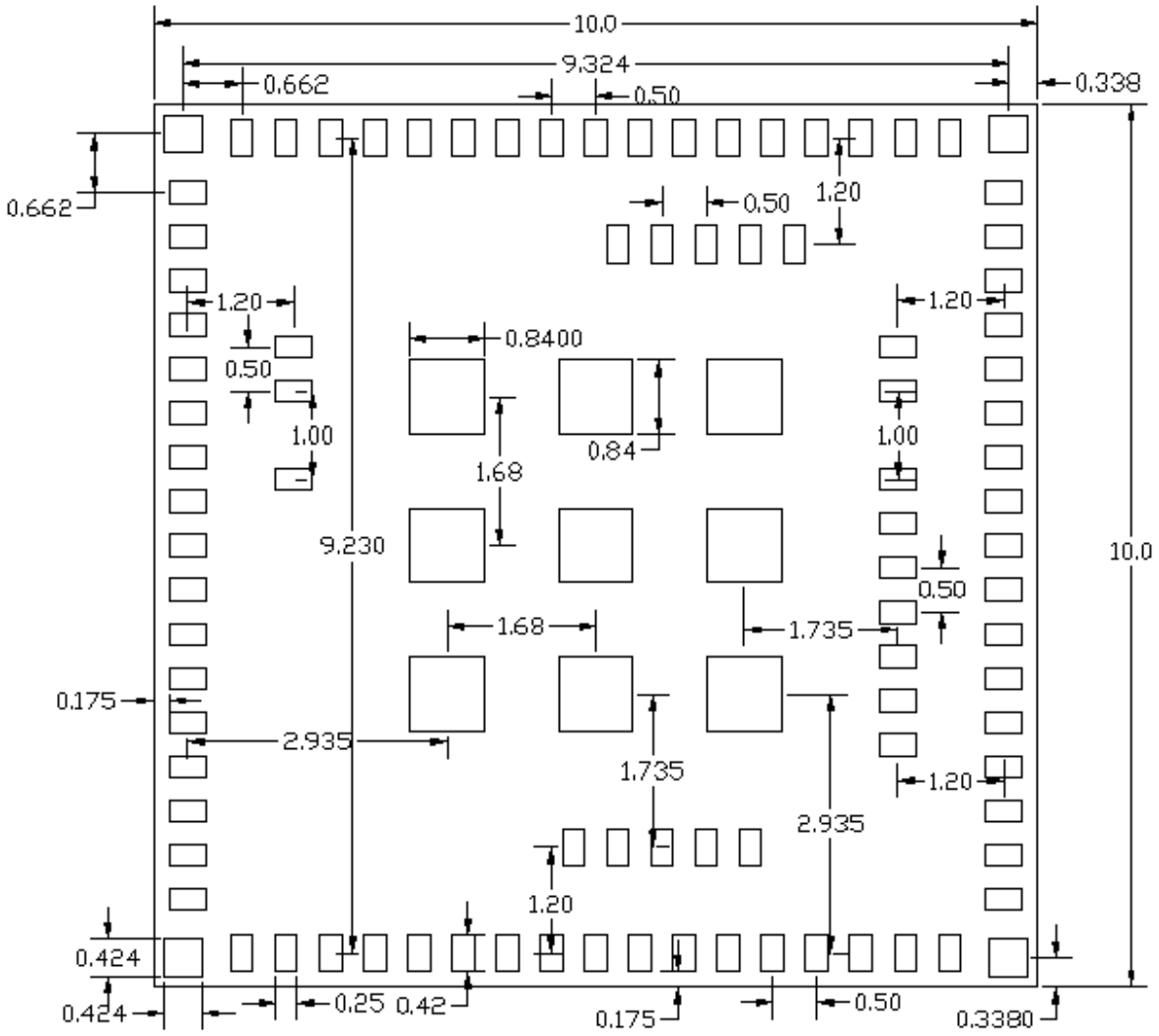
TOP View

Note:

1. Please use Un-Solder Mask to design the Module Footprint.
2. There are three types pad size in the Module.
   - Type A:
     Pad size: 0.424 x 0.424mm^2 & Solder Mask size: 0.524 x 0.524 mm^2
   - Type B
     Pad size: 0.25 x 0.42mm^2 & Solder Mask size: 0.35 x 0.52 mm^2
   - Type C
     Pad size: 4.2 x 4.2mm^2 & Solder Mask size: 4.3 x 4.3 mm^2

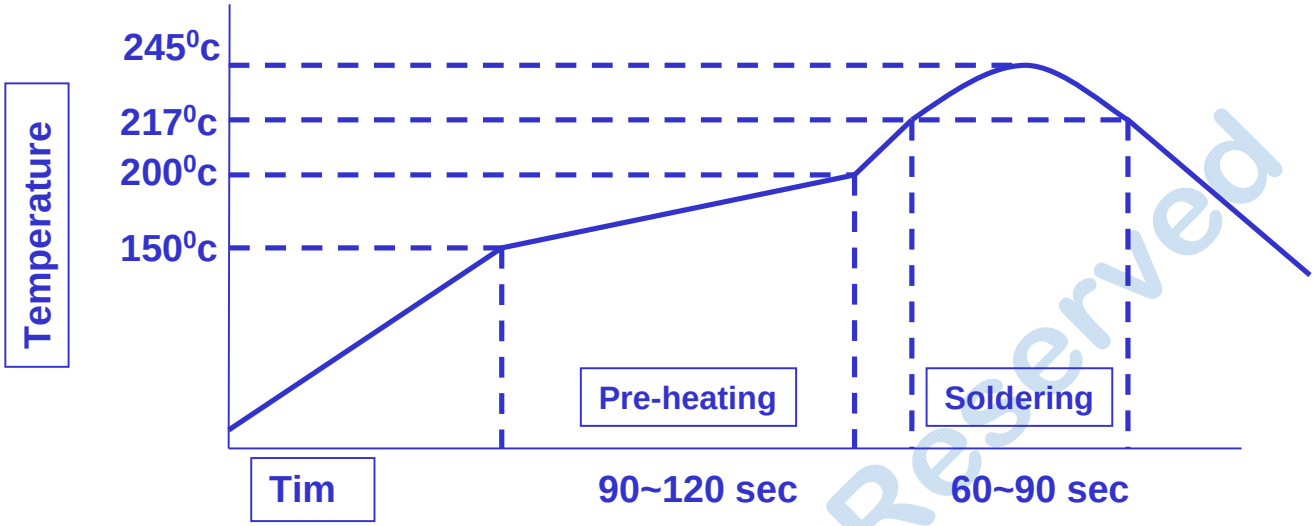
9. Recommend Stencil

Unit: mm



TOP View

10. Recommended Reflow Profile



11. Package and Storage Condition

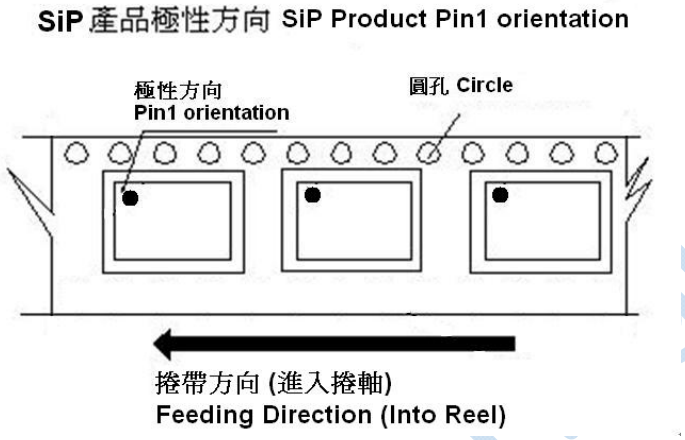
11.1 Package Dimension

Reel Size 捲軸尺寸	Vacuum Pressure 真空壓力	Vacuum Time 真空時間	Sealing Time 封口時間	Fill N2 Time 充氮時間
7” (7 英吋)	-250 +/- 50 mmHg (毫米汞柱)	2 sec (秒)	3~6 sec (秒)	0 sec (秒)
13” (13 英吋)	-450 +/- 50 mmHg (毫米汞柱)	4 sec (秒)	3~6 sec (秒)	0 sec (秒)

11.2 Laser Mark

TBD

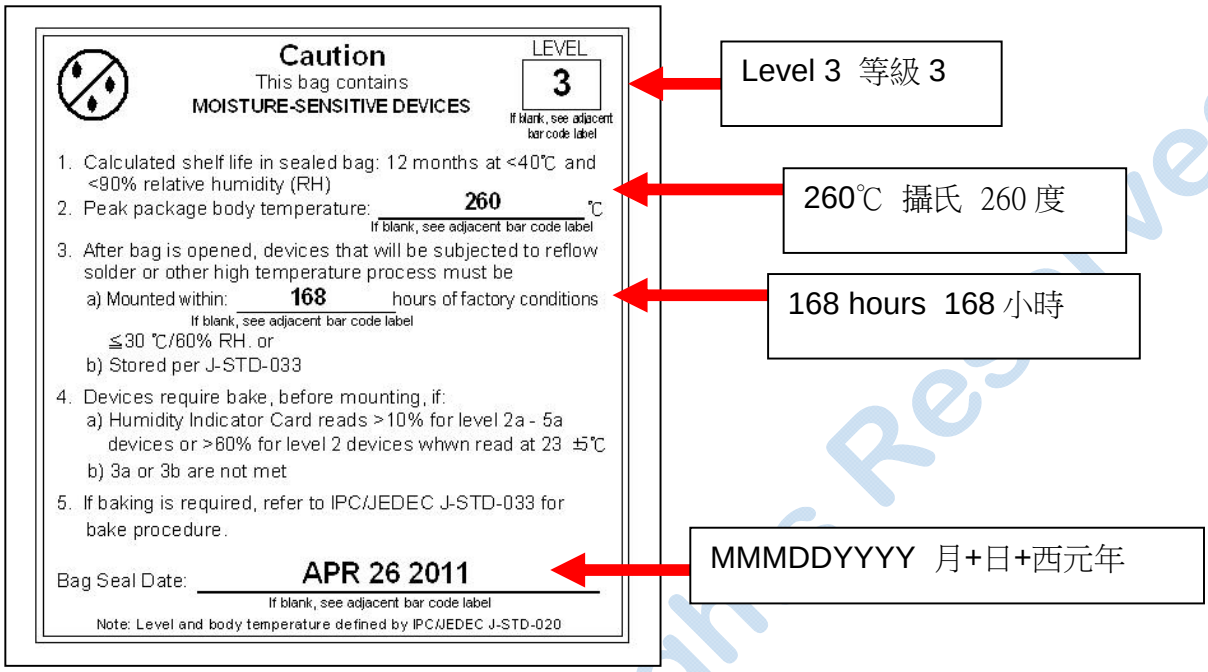
11.3 Pin 1 Location in the Tape/Reel



11.4 Ordering Information

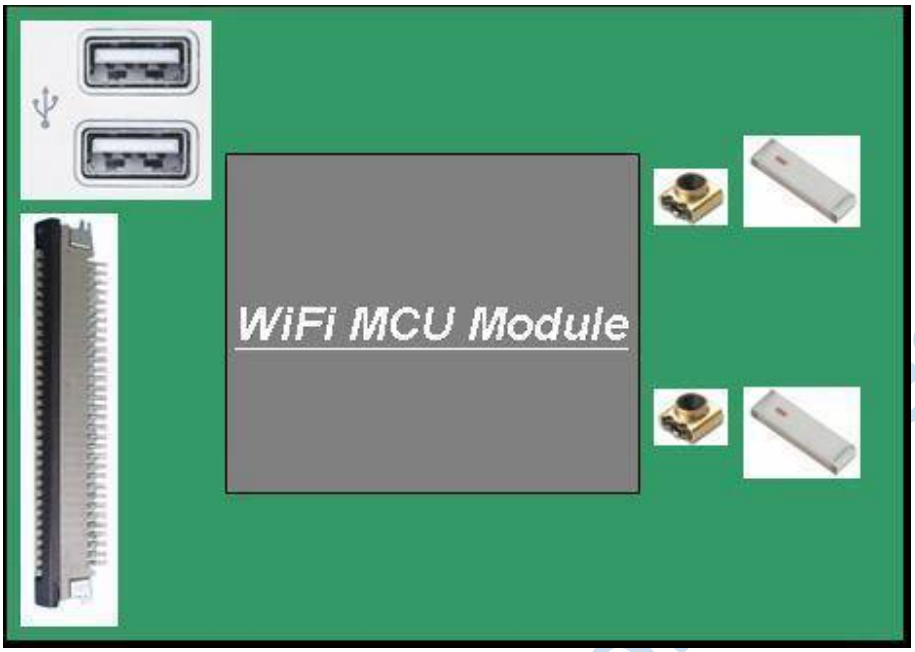
TBD

11.5 MSL & Moisture Sensitive LEVEL



12. APPLICATION REFERENCE DESIGN

TBD



- FCC and CE Certification.
- Manufactory Testing.
- Customer Promotion

13. Sales Information

If you need to buy this product, please call MXCHIP during the working hours. (Monday~Friday A.M.9:00~12:00; P.M. 1:00~6:00)

Telephone: +86-21-52655026 / 52655025
Address: Room 811, Tongpu Building, No.1220 Tongpu Road, Shanghai
Post Code: 200333
Email: sales@mxchip.com

14. Technical Support

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Development tools technical support
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