Annotated schematic diagram of an MC68HC11A8 microprocessor-based memory system. The following handwritten notes and labels appear on the diagram:

Blue handwritten annotations:

- Address/data (dual use) line
- from datasheet ← when AS asserted, AD line is "A" value
- these labels defined w.r.t. the bus
- DATA BUS
- power, clocking, int, chip reset
- bus signals
- pull up
- model #
- A0-A15
- ADDRESS BUS
- CONTROL BUS
- A15 is the sub address space allocated to the chips
- controlled by this decoder (A0 - A12) shared by all memory
- decoder: only one output asserted @ any time
- 8-bit system data lines.
- full address space available for processor
- labels (within the chip: defined for the chip)
- when asserted, data bus will be accessed (R/W), based on address values
- (pull up resistors)

Green table (bottom):

A2 A1 A0 : decoder asserted line

Red annotations:

- processor tells this latch to grab the value as "A" values (A0-A7). After the latch on is done, the AD line becomes a "D" line
- constantly enabled
- A14? processor memory space decoding
- Is there a black hole in the address space?
- A15 is
- controlled by this decoder

Orange annotations:

- control signals
- (read only) 3 memory modules
- (A12,A13 = 0), W
- R/W
- 0 0 / X X X
- 00/Xxxx

Green highlight: broadcast to all chips

Component labels:

- MC68HC11A8
- 10K TYP
- V_DD, V_SS
- PA0/IC3, PA1/IC2, PA2/IC0, PA3/OC5/OC1, PA4/OC4/OC1, PA5/OC3/OC1, PA6/OC2/OC1, PA7/PAI/OC1
- EXTAL, XTAL
- AD0, AD1, AD2, AD3, AD4, AD5, AD6, AD7
- AS, R/W, E
- RESET
- A8, A9, A10, A11, A12, A13, A14, A15
- XIRQ, IRQ
- PD0/RxD, PD1/TxD, PD2/MISO, PD3/MOSI, PD4/SCK, PD5/SS
- MODA/LIR, MODB/V_STBY
- PE0/AN0, PE1/AN1, PE2/AN2, PE3/AN3, PE4/AN4, PE5/AN5, PE6/AN6, PE7/AN7
- V_RH, V_RL
- 74HC373: D0-D7, Q0-Q7, LE, OE
- 74HC138: A0, A1, A2, A13, A14, A15, E, G1, G2, Y0-Y7, G
- 8K X 8 EPROM: A0-A12, D0-D7, CS, OE
- 8K X 8 RAM: A0-A12, D0-D7, WE, RD
- 8-bit system data lines
- 10K TYP, V_DD, D0-D7

Bottom truth table (partial):

A14	A13	R/W	asserted line
0	0	0	Y0
0	0	1	Y1
0	1	0	Y2 ← 01 write
0	1	1	Y3 01 read

XXXXXXXXXXXXX A0

A12

FIGURE 7-18 A 48K × 8 memory system using twenty-four TMS4016 SRAMS.

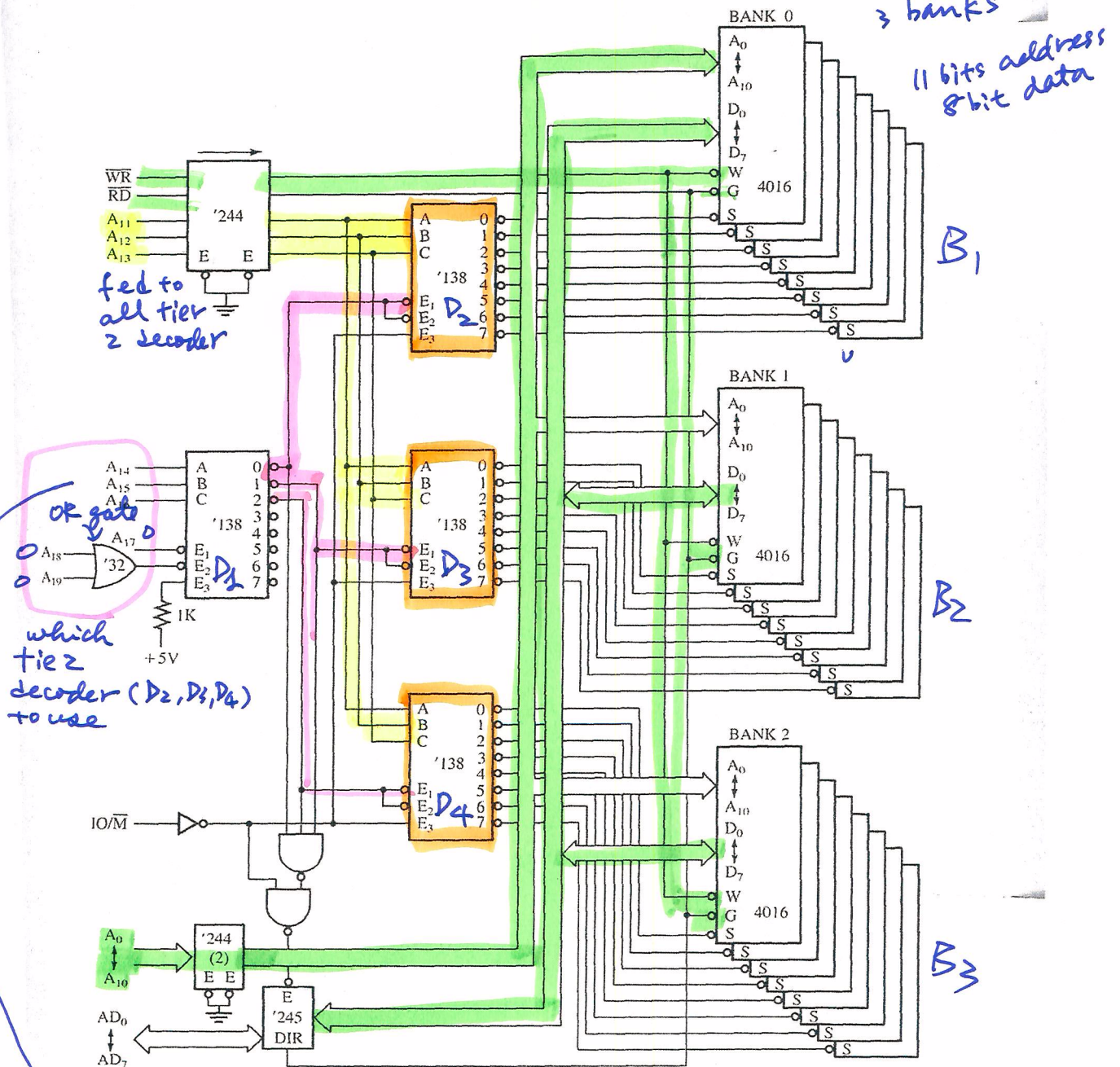*Handwritten annotations:*

what's the address map of the memory modules?

3 banks
11 bits address
8 bit data

BANK 0 — B_1

fed to all tier 2 decoder

OR gate

which tier 2 decoder (D_2, D_3, D_4) to use

B_2

B_3

19	18	17	16	15	14	A_{13}	A_{12}	A_{11}	A_{10} — A_0

0 0 0 0 0 0 (B_1)
0 0 1 (B_2)
0 1 0 (B_3) ← subject to the output of decoder 1