23.5.1 Global Configuration Register (HETGCR)

N2HET1: offset = FFF7 B800h; **N2HET2:** offset = FFF7 B900h

Figure 23-100. Global Configuration Register (HETGCR)

31	25	24	23	22	21	20	19	18	17	16
Reserved		HET PIN ENA	Rsvd.	MP		Reserved		PPF	IS	CMS
R-0		R/W-1	R-0	R/W-0		R-0		R/W-0	R/W-0	R/W-0

15	1	0
Reserved		TO
R-0		R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 23-80. Global Configuration Register (HETGCR) Field Descriptions

Bit	Field	Value	Description
31-25	Reserved	0	Read returns 0. Writes have no effect.
24	HET PIN ENA		Enables the output buffers of the pin structures depending on the value of nDIS and DIR.x when PINDIS.x is set.
			Note: This bit will automatically get cleared when nDIS pin (input port) value is "0".
		0	No affect on the pin output buffer structure.
		1	Enables the pin output buffer structure when DIR = output, PINDIS.x is set and nDIS = 1.
23	Reserved	0	Read returns 0. Writes have no effect.
22-21	MP		Master Priority
			The NHET can prioritize master accesses to N2HET RAM between the HET Transfer Unit and another arbiter, which outputs the access of one of the remaining masters. The MP bits allow the following selections:
		0	The HTU has lower priority to access the N2HET RAM than the arbiter output.
		1h	The HTU has higher priority to access the N2HET RAM than the arbiter output.
		2h	The HTU and the arbiter output use a round robin scheme to access the N2HET RAM.
		3h	Reserved
20-19	Reserved	0	Read returns 0. Writes have no effect.
18	PPF		Protect Program Fields
			The PPF bit together with the Turn On/Off bit (TO) allows to protect the program fields of all instructions in N2HET RAM.
		0 (TO = 0)	All masters can read and write the program fields.
		0 (TO = 1)	All masters can read and write the program fields.
		1 (TO = 0)	All masters can read and write the program fields.
		1 (TO = 1)	The program fields are readable but not writable for all masters, which could access the N2HET RAM. Possible masters are the CPU, HTU, DMA and a secondary CPU (if available). Writes initiated by these masters are discarded.
17	IS		Ignore Suspend
			When Ignore Suspend = 0, the timer operation is stopped on suspend (the current timer instruction is completed). Timer RAM can be freely accessed during suspend. When set to 1, the suspend is ignored and the N2HET continues operating.
		0	N2HET stops when in suspend mode.
		1	N2HET ignores suspend mode and continues operation.
16	CMS		Clk_master/slave
			This bit is used to synchronize multi-N2HETs. If set (N2HET is master), the N2HET outputs a signal to synchronize the prescalers of the slave N2HET. By default, this bit is reset, which means a slave configuration.
			Note: This bit must be set to one (1) for single-N2HET configuration.
		0	N2HET is configured as a slave.
		1	N2HET is configured as a master.
15-1	Reserved	0	Read returns 0. Writes have no effect.

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Table 23-80. Global Configuration Register (HETGCR) Field Descriptions (continued)

Bit	Field	Value	Description
0	TO		Turn On/Off When TO = 0, the timer program stops executing. Turn-off is automatically delayed until the current timer program loop is completed. Turn-off does not affect the content of the timer RAM, ALU registers, or control registers. Turn-off resets all flags. TO does not affect the state of the pins. You must set/reset the timer pins when they are turned off, or re-initialize the timer RAM and control registers before a reset. After a device reset, the timer is turned off by default. When TO = 1, timer program execution starts synchronously to the Loop clock. In case of multiple N2HETs configuration, the slave N2HETs are waiting for the loop clock to come from the master before starting execution. Then, the timer address points automatically address 00h (corresponding to program start).
		0	N2HET is OFF.
		1	N2HET is ON.

23.5.2 Prescale Factor Register (HETPFR)

N2HET1: offset = FFF7 B804h; **N2HET2:** offset = FFF7 B904h

Figure 23-101. Prescale Factor Register (HETPFR)

31	17	16
Reserved		
R-0		

15	11	10	8	7	6	5	0
Reserved		LRPFC		Reserved		HRPFC	
R-0		R/WP-0		R-0		R/WP-0	

LEGEND: R/W = Read/Write; R = Read only; WP = Write in privileged mode only; -*n* = value after reset

Table 23-81. Prescale Factor Register (HETPFR) Field Descriptions

Bit	Field	Value	Description
31-11	Reserved	0	Read returns 0. Writes have no effect.
10-8	LRPFC		Loop Resolution Pre-scale Factor Code LRPFC determines the loop resolution prescale divide rate (lr). See Table 23-5.
7-6	Reserved	0	Read returns 0. Writes have no effect.
5-0	HRPFC		High Resolution Pre-scale Factor Code HRPFC determines the high resolution prescale divide rate (hr). See Table 23-5.

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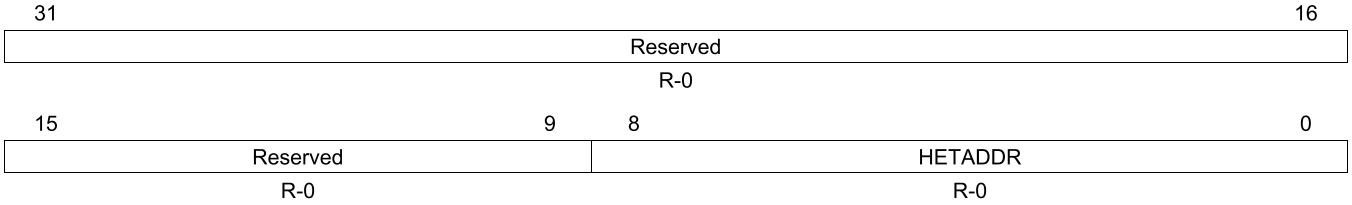
23.5.3 N2HET Current Address Register (HETADDR)

N2HET1: offset = FFF7 B808h; **N2HET2:** offset = FFF7 B908h

Figure 23-102. N2HET Current Address (HETADDR)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

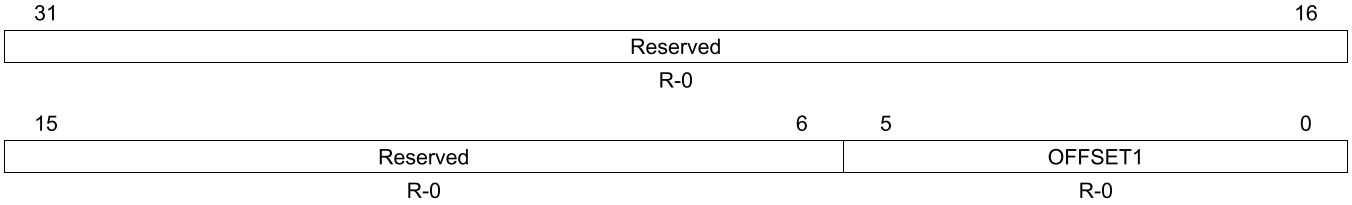
Table 23-82. N2HET Current Address (HETADDR) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Read returns 0. Writes have no effect.
8-0	HETADDR		N2HET Current Address Read: Returns the current N2HET program address. Write: Writes have no effect.

23.5.4 Offset Index Priority Level 1 Register (HETOFF1)

N2HET1: offset = FFF7 B80Ch; **N2HET2:** offset = FFF7 B90Ch

Figure 23-103. Offset Index Priority Level 1 Register (HETOFF1)



LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 23-83. Offset Index Priority Level 1 Register (HETOFF1) Field Descriptions

Bit	Field	Value	Description
31-6	Reserved	0	Read returns 0. Writes have no effect.
5-0	OFFSET1		HETOFF1[5:0] indexes the currently pending high-priority interrupt. Offset values and sources are listed below and the interrupt encoding format is presented in Table 23-84. Read: Read of these bits determines the pending N2HET interrupt. Write: Writes have no effect. **Note:** In any read operation mode, the corresponding flag (in the HETFLG) is also cleared. In Emulation mode the corresponding flag is not cleared.

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Table 23-84. Interrupt Offset Encoding Format

Source No.	Offset Value
No interrupt	0
Instruction 0, 32, 64...	1
Instruction 1, 33, 65...	2
:	:
Instruction 31, 63, 95...	32
Program Overflow	33
APCNT Underflow	34
APCNT Overflow	35

23.5.5 Offset Index Priority Level 2 Register (HETOFF2)

N2HET1: offset = FFF7 B810h; **N2HET2:** offset = FFF7 B910h

Figure 23-104. Offset Index Priority Level 2 Register (HETOFF2)

31	16
Reserved	
R-0	

15	6	5	0
Reserved		OFFSET2	
R-0		R-0	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 23-85. Offset Index Priority Level 2 Register (HETOFF2) Field Descriptions

Bit	Field	Value	Description
31-6	Reserved	0	Read returns 0. Writes have no effect.
5-0	OFFSET2		HETOFF2[5:0] indexes the currently pending low-priority interrupt. Offset values and sources are listed above and the interrupt encoding format is presented in Table 23-84. Read: Read of these bits determines the pending N2HET interrupt. Write: Writes have no effect. **Note:** In any read operation mode, the corresponding flag (in the HETFLG) is also cleared. In Emulation mode the corresponding flag is not cleared.

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23.5.6 Interrupt Enable Set Register (HETINTENAS)

N2HET1: offset = FFF7 B814h; **N2HET2:** offset = FFF7 B914h

Figure 23-105. Interrupt Enable Set Register (HETINTENAS)

31	16
HETINTENAS	
R/W-0	

15	0
HETINTENAS	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 23-86. Interrupt Enable Set Register (HETINTENAS) Field Descriptions

Bit	Field	Value	Description
31-0	HETINTENAS		Interrupt Enable Set bits. HETINTENAS is readable and writable in any operation mode. Writing a one to bit x enables the interrupts of the N2HET instructions at N2HET addresses x+0, x+32, x+64... Generating an interrupt requires to set bit x in HETINTENAS and to enable the interrupt bit in one of the instructions at addresses x+0, x+32, x+64... To avoid ambiguity only one of the instructions x+0, x+32, x+64... should have the interrupt enable bit (inside the instruction) set. Writing a zero to HETINTENAS has no effect. When reading from HETINTENAS bit x gives the information, if N2HET instructions x+0, x+32, x+64... have the interrupt enabled or disabled.
		0	Read: Interrupt is disabled. Write: Writes have no effect.
		1	Read: Interrupt is enabled. Write: Interrupt will be enabled.

23.5.7 Interrupt Enable Clear Register (HETINTENAC)

N2HET1: offset = FFF7 B818h; **N2HET2:** offset = FFF7 B918h

Figure 23-106. Interrupt Enable Clear (HETINTENAC)

31	16
HETINTENAC	
R/W-0	

15	0
HETINTENAC	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 23-87. NHET Interrupt Enable Clear (HETINTENAC) Field Descriptions

Bit	Field	Value	Description
31-0	HETINTENAC		Interrupt Enable Clear bits. HETINTENAC is readable and writable in any operation mode. Writing a one to bit x disables the interrupts of the N2HET instructions at N2HET addresses x+0, x+32, x+64... (See also description in Table 23-86). Writing a zero to HETINTENAC has no effect. When reading from HETINTENAC bit x gives the information, if N2HET instructions x+0, x+32, x+64... have the interrupt enabled or disabled.
		0	Read: Interrupt is disabled. Write: Writes have no effect.
		1	Read: Interrupt is enabled. Write: Interrupt will be enabled.

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23.5.8 Exception Control Register 1 (HETEXC1)

N2HET1: offset = FFF7 B81Ch; **N2HET2:** offset = FFF7 B91Ch

Figure 23-107. Exception Control Register (HETEXC1)

31	25	24
Reserved		APCNT OVRFL ENA
R-0		R/W-0

23	17	16
Reserved		APCNT UNRFL ENA
R-0		R/W-0

15	9	8
Reserved		PRGM OVRFL ENA
R-0		R/W-0

7	3	2	1	0
Reserved		APCNT OVRFL PRY	APCNT UNRFL PRY	PRGM OVRFL PRY
R-0		R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 23-88. Exception Control Register 1 (HETEXC1) Field Descriptions

Bit	Field	Value	Description
31-17	Reserved	0	Read returns 0. Writes have no effect.
24	APCNT OVRFL ENA		APCNT Overflow Enable
		0	APCNT overflow exception is not enabled.
		1	Enables the APCNT overflow exception.
23-17	Reserved	0	Read returns 0. Writes have no effect.
16	APCNT UNRFL ENA		APCNT Underflow Enable
		0	APCNT underflow exception is not enabled.
		1	Enables the APCNT underflow exception.
15-9	Reserved	0	Read returns 0. Writes have no effect.
8	PRGM OVRFL ENA		Program Overflow Enable
		0	The program overflow exception is not enabled.
		1	Enables the program overflow exception.
7-3	Reserved	0	Read returns 0. Writes have no effect.
2	APCNT OVRFL PRY		APCNT Overflow Exception Interrupt Priority
		0	Exception priority level 2
		1	Exception priority level 1
1	APCNT UNRFL PRY		APCNT Underflow Exception Interrupt Priority
		0	Exception priority level 2
		1	Exception priority level 1
0	PRGM OVRFL PRY		ProgramOverflow Exception Interrupt Priority
		0	Exception priority level 2
		1	Exception priority level 1

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23.5.9 Exception Control Register 2 (HETEXC2)

N2HET1: offset = FFF7 B820h; **N2HET2:** offset = FFF7 B920h

Figure 23-108. Exception Control Register 2 (HETEXC2)

31	16
Reserved	
R-0	

15	9	8
Reserved		DEBUG STATUS FLAG
R-0		R/WC-0

7	3	2	1	0
Reserved		APCNT OVRFL FLAG	APCNT UNRFL FLAG	PRGM OVRFL FLAG
R-0		R/WC-0	R/WC-0	R/WC-0

LEGEND: R/W = Read/Write; R = Read only; C = Clear; -*n* = value after reset

Table 23-89. Exception Control Register 2 (HETEXC2) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Read returns 0. Writes have no effect.
8	DEBUG STATUS FLAG		Debug Status Flag. This flag is set when N2HET has stopped at a breakpoint. Also generates a debug request to halt the ARM CPU.
		0	Read: N2HET is either running, or stopped, flag cleared but not yet restarted. Write: No effect.
		1	Read: N2HET is stopped at a breakpoint. Write: Clears the bit. To restart N2HET clear this bit and then restart the ARM CPU. The N2HET and ARM CPU will start synchronously.
7-3	Reserved	0	Read returns 0. Writes have no effect.
2	APCNT OVRFL FLAG		APCNT Overflow Flag
		0	Read: Exception has not occurred since the flag was cleared. Write: No effect.
		1	Read: Exception has occurred since the flag was cleared. Write: Clears the bit.
1	APCNT UNDFL FLAG		APCNT Underflow Flag
		0	Read: Exception has not occurred since the flag was cleared. Write: No effect.
		1	Read: Exception has occurred since the flag was cleared. Write: Clears the bit.
0	PRGM OVERFL FLAG		Program Overflow Flag
		0	Read: Exception has not occurred since the flag was cleared. Write: No effect.
		1	Read: Exception has occurred since the flag was cleared Write: Clears the bit.

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23.5.10 Interrupt Priority Register (HETPRY)

N2HET1: offset = FFF7 B824h; **N2HET2:** offset = FFF7 B924h

Figure 23-109. Interrupt Priority Register (HETPRY)

31	16
HETPRY	
R/WP-0	

15	0
HETPRY	
R/WP-0	

LEGEND: R/W = Read/Write; R = Read only; WP = Write in privileged mode only; -*n* = value after reset

Table 23-90. Interrupt Priority Register (HETPRY) Field Descriptions

Bit	Field	Value	Description
31-0	HETPRY		HET Interrupt Priority Level bits Used to select the priority of any of the 32 potential interrupt sources coming from N2HET instructions.
		0	Interrupt priority level 2.
		1	Interrupt priority level 1.

23.5.11 Interrupt Flag Register (HETFLG)

N2HET1: offset = FFF7 B828h; **N2HET2:** offset = FFF7 B928h

Figure 23-110. Interrupt Flag Register (HETFLG)

31	16
HETFLAG	
R/WC-0	

15	0
HETFLAG	
R/WC-0	

LEGEND: R/W = Read/Write; R = Read only; C = Clear; -*n* = value after reset; X = Unknown

Table 23-91. Interrupt Flag Register (HETFLG) Field Descriptions

Bit	Field	Value	Description
31-0	HETFLAG		Interrupt Flag Register Bits Bit x is set when an interrupt condition has occurred on one of the instructions x+0, x+32, x+64.... The flag position x (in the register) is decoded from the five LSBs of the instruction address that generated the interrupt. The hardware will set the flag only if the interrupt enable bit (in the corresponding instruction) is set. The flag will be set even if bit x in the Interrupt Enable Set Register (HETINTENAS) is not enabled. Enabling bit x in HETINTENAS is required if an interrupt should be generated. Clearing the flag can be done by writing a one to the flag. Alternatively reading the corresponding Offset Index Priority Level 1 Register (HETOFF1) or Offset Index Priority Level 2 Register (HETOFF2) will automatically clear the flag.
		0	Read: No N2HET instruction with an interrupt has been reached since the flag was cleared. Write: No effect.
		1	Read: A N2HET instruction with an interrupt has been reached since the flag was cleared. Write: Clears the bit.

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23.5.12 AND Share Control Register (HETAND)

N2HET1: offset = FFF7 B82Ch; **N2HET2:** offset = FFF7 B92Ch

Figure 23-111. AND Share Control Register (HETAND)

31							16
Reserved							
R-0							
15	14	13	12	11	10	9	8
ANDSHARE31/30	ANDSHARE29/28	ANDSHARE27/26	ANDSHARE25/24	ANDSHARE23/22	ANDSHARE21/20	ANDSHARE19/18	ANDSHARE17/16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
ANDSHARE15/14	ANDSHARE13/12	ANDSHARE11/10	ANDSHARE9/8	ANDSHARE7/6	ANDSHARE5/4	ANDSHARE3/2	ANDSHARE1/0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 23-92. AND Share Control Register (HETAND) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Read returns 0. Writes have no effect.
15-0	AND SHARE n+1 / n		AND Share Enable Enable the AND sharing of the same pin for two HR structures. For example, if bit AND SHARE 1/0 is set, the pin HET[0] will then be commanded by a logical AND of both HR structures 0 and 1. **Note:** If HR AND SHARE bits are used, pins not connected to HR structures (the odd number pin in each pair) can be accessed as general inputs/outputs.
		0	HR Output of HET[n+1] and HET[n] are not AND shared
		1	HR Output of HET[n+1] and HET[n] are AND shared onto pin HET[n]

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23.5.13 HR Share Control Register (HETHRSH)

N2HET1: offset = FFF7 B834h; **N2HET2:** offset = FFF7 B934h

Figure 23-112. HR Share Control Register (HETHRSH)

31							16
Reserved							
R-0							
15	14	13	12	11	10	9	8
HRSHARE31/30	HRSHARE29/28	HRSHARE27/26	HRSHARE25/24	HRSHARE23/22	HRSHARE21/20	HRSHARE19/18	HRSHARE17/16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
HRSHARE15/14	HRSHARE13/12	HRSHARE11/10	HRSHARE9/8	HRSHARE7/6	HRSHARE5/4	HRSHARE3/2	HRSHARE1/0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 23-93. HR Share Control Register (HETHRSH) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Read returns 0. Writes have no effect.
15-0	HR SHARE n+1 / n		HR Share Bits Enables the share of the same pin for two HR structures. For example, if bit HR share 1/0 is set, the pin HET[0] will then be connected to both HR input structures 0 and 1. **Note:** If HR share bits are used, pins not connected to HR structures (the odd number pin in each pair) can be accessed as general inputs/outputs.
		0	HR Input of HET[n+1] and HET[n] are not shared.
		1	HR Input of HET[n+1] and HET[n] are shared; both measure pin HET[n]

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23.5.14 XOR Share Control Register (HETXOR)

N2HET1: offset = FFF7 B838h; **N2HET2:** offset = FFF7 B938h

Figure 23-113. XOR Share Control Register (HETXOR)

31							16
Reserved							
R-0							
15	14	13	12	11	10	9	8
XORSHARE31/30	XORSHARE29/28	XORSHARE27/26	XORSHARE25/24	XORSHARE23/22	XORSHARE21/20	XORSHARE19/18	XORSHARE17/16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
XORSHARE15/14	XORSHARE13/12	XORSHARE11/10	XORSHARE9/8	XORSHARE7/6	XORSHARE5/4	XORSHARE3/2	XORSHARE1/0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 23-94. XOR Share Control Register (HETXOR) Field Descriptions

Bit	Field	Value	Description
31-16	Reserved	0	Read returns 0. Writes have no effect.
15-0	XOR SHARE n+1 / n		XOR Share Enable Enable the XOR-share of the same pin for two output HR structures. For example, if bit XOR SHARE 1/0 is set, the pin HET[0] will then be commanded by a logical XOR of both HR structures 0 and 1. **Note:** If XOR share bits are used, pins not connected to HR structures (the odd number pin in each pair) can be accessed as general inputs/outputs.
		0	HR Output of HET[n+1] and HET[n] are not XOR shared
		1	HR Output of HET[n+1] and HET[n] are XOR shared onto pin HET[n]

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23.5.15 Request Enable Set Register (HETREQENS)

N2HET1: offset = FFF7 B83Ch; **N2HET2:** offset = FFF7 B93Ch

Figure 23-114. Request Enable Set Register (HETREQENS)

31							8
Reserved							
R-0							
7	6	5	4	3	2	1	0
REQ ENA 7	REQ ENA 6	REQ ENA 5	REQ ENA 4	REQ ENA 3	REQ ENA 2	REQ ENA 1	REQ ENA 0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 23-95. Request Enable Set Register (HETREQENS) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Read returns 0. Writes have no effect.
7-0	REQ ENA n		Request Enable Bits
		0	Read: Returns the information that request line n is disabled.
			Write: Writing a 0 has no effect.
		1	Read: Returns the information that request line n is enabled.
			Write: Writing a 1 to bit n enables the N2HET request line n.
			Note: The request line can trigger a DMA control packet (DMA channel), an HTU double control packet (DCP) or both simultaneously. The HETREQDS register determines to which module(s) the N2HET request line n is assigned.
			Note: A disabled request line does not memorize old requests. So there are no pending requests to service after enabling request line n.

23.5.16 Request Enable Clear Register (HETREQENC)

N2HET1: offset = FFF7 B840h; **N2HET2:** offset = FFF7 B940h

Figure 23-115. Request Enable Clear Register (HETREQENC)

31							8
Reserved							
R-0							
7	6	5	4	3	2	1	0
REQ DIS 7	REQ DIS 6	REQ DIS 5	REQ DIS 4	REQ DIS 3	REQ DIS 2	REQ DIS 1	REQ DIS 0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 23-96. Request Enable Clear Register (HETREQENC) Field Descriptions

Bit	Field	Value	Description
31-8	Reserved	0	Read returns 0. Writes have no effect.
7-0	REQ DIS n		Request Disable Bits
		0	Read: Returns the information that request line n is disabled.
			Write: Writing a 0 has no effect.
		1	Read: Returns the information that request line n is enabled.
			Write: Writing a 1 to bit n disables the N2HET request line n.

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23.5.17 Request Destination Select Register (HETREQDS)

N2HET1: offset = FFF7 B844h; **N2HET2:** offset = FFF7 B944h

Figure 23-116. Request Destination Select Register (HETREQDS) [offset = FFF7 B844h]

31	24	23	22	21	20	19	18	17	16
Reserved		TDBS 7	TDBS 6	TDBS 5	TDBS 4	TDBS 3	TDBS 2	TDBS 1	TDBS 0
R-0		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	8	7	6	5	4	3	2	1	0
Reserved		TDS 7	TDS 6	TDS 5	TDS 4	TDS 3	TDS 2	TDS 1	TDS 0
R-0		R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 23-97. Request Destination Select Register (HETREQDS) Field Descriptions

Bit	Field	Value	Description
31-24	Reserved	0	Read returns 0. Writes have no effect.
23-16	TDBS n		HTU, DMA or Both Select Bits
		0	N2HET request line n is assigned to the module specified by TDS bit n.
		1	N2HET request line n is assigned to both DMA and HTU. TDS bit n is ignored in this case.
15-8	Reserved	0	Read returns 0. Writes have no effect.
7-0	TDS n		HTU or DMA Select Bits
			Note: It must be ensured in the N2HET program, that one request line is triggered by only one N2HET instruction.
		0	N2HET request line n is assigned to HTU (TDBS bit n is zero).
		1	N2HET request line n is assigned to DMA (TDBS bit n is zero).

NOTE: Please refer to the device data sheet how each of the 8 N2HET request lines are connected to these modules. See also Section 23.2.9.

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23.5.18 NHET Direction Register (HETDIR)

N2HET1: offset = FFF7 B84Ch; **N2HET2:** offset = FFF7 B94Ch

Figure 23-117. N2HET Direction Register (HETDIR)

31	16
HETDIR	
R/W-0	

15	0
HETDIR	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 23-98. N2HET Direction Register (HETDIR) Field Descriptions

Bit	Field	Value	Description
31-0	HETDIR n		Data direction of NHET pins
		0	Pin HET[n] is an input (and its output buffer is tristated)
		1	Pin HET[n] is an output

NOTE: Table 23-9 shows how the register bits of DIR, PULDIS and PULSEL are affecting the N2HET pins.

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23.5.19 N2HET Data Input Register (HETDIN)

N2HET1: offset = FFF7 B850h; **N2HET2:** offset = FFF7 B950h

Figure 23-118. N2HET Data Input Register (HETDIN)

31	16
HETDIN	
R-x	

15	0
HETDIN	
R-x	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset;

Table 23-99. N2HET Data Input Register (HETDIN) Field Descriptions

Bit	Field	Value	Description
31-0	HETDIN n		Data input. This bit displays the logic state of the pin.
		0	Pin HET[n] is at logic low (0)
		1	Pin HET[n] is at logic high (1)

23.5.20 N2HET Data Output Register (HETDOUT)

N2HET1: offset = FFF7 B854h; **N2HET2:** offset = FFF7 B954h

Figure 23-119. N2HET Data Output Register (HETDOUT)

31	16
HETDOUT	
R/W-0	

15	0
HETDOUT	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

Table 23-100. N2HET Data Output Register (HETDOUT) Field Descriptions

Bit	Field	Value	Description
31-0	HETDOUT n		Data out write. Writes to this bit will only take effect when the pin is configured as an output. The current logic state of the pin will be displayed by this bit even when the pin state is changed by writing to HETDSET or HETDCLR.
		0	Pin HET[n] is at logic low (0).
		1	Pin HET[n] is at logic high (1) if the HETPDR[n] bit = 0 or the output is in high impedance state if the HETPDR[n] bit = 1

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23.5.21 NHET Data Set Register (HETDSET)

N2HET1: offset = FFF7 B858h; **N2HET2:** offset = FFF7 B958h

Figure 23-120. N2HET Data Set Register (HETDSET)

31	16
HETDSET	
R/WS-0	

15	0
HETDSET	
R/WS-0	

LEGEND: R/W = Read/Write; R = Read only; S = Set; -*n* = value after reset

Table 23-101. N2HET Data Set Register (HETDSET) Field Descriptions

Bit	Field	Value	Description
31-0	HETDSET n		This register allows bits of HETDOUT to be set while avoiding the pitfalls of a readmodify- write sequence in a multitasking environment. Bits written as a logic 1 set the same bit in the HETDOUT register; while bits written as logic 0 leave the same bit in HETDOUT unchanged. Reads from this address return the value of the HETDOUT register.
		0	Write: HETDOUT[n] unchanged.
		1	Write: HETDOUT[n] is set.

23.5.22 N2HET Data Clear Register (HETDCLR)

N2HET1: offset = FFF7 B85Ch; **N2HET2:** offset = FFF7 B95Ch

Figure 23-121. N2HET Data Clear Register (HETDCLR)

31	16
HETDCLR	
R/WC-0	

15	0
HETDCLR	
R/WC-0	

LEGEND: R/W = Read/Write; R = Read only; C = Clear; -*n* = value after reset

Table 23-102. N2HET Data Clear Register (HETDCLR) Field Descriptions

Bit	Field	Value	Description
31-0	HETDCLR n		This register allows bits of HETDOUT to be cleared while avoiding the pitfalls of a read-modify-write sequence in a multitasking environment. Bits written as a logic 1 clear the same bit in the HETDOUT register; while bits written as logic 0 leave the same bit in HETDOUT unchanged. Reads from this address return the value of the HETDOUT register.
		1	Write: HETDOUT[n] unchanged.
		0	Write: HETDOUT[n] is cleared.

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23.5.23 N2HET Open Drain Register (HETPDR)

Values in this register enable or disable the open drain capability of the data pins.
N2HET1: offset = FFF7 B860h; **N2HET2:** offset = FFF7 B960h

Figure 23-122. N2HET Open Drain Register (HETPDR)

31	16
HETPDR	
R/W-0	

15	0
HETPDR	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 23-103. N2HET Open Drain Register (HETPDR) Field Descriptions

Bit	Field	Value	Description
31-0	HETPDR n		Open drain control for HET[n] pins
		0	The pin is configured in push/pull mode.
		1	The pin is configured in open drain mode. The HETDOUT register controls the state of the output buffer:
			HETDOUT[n] = 0 The output buffer of pin HET[n] is driven low.
			HETDOUT[n] = 1 The output buffer of pin HET[n] is tristated.

23.5.24 N2HET Pull Disable Register (HETPULDIS)

Values in this register enable or disable the pull-up/-down functionality of the pins.
N2HET1: offset = FFF7 B864h; **N2HET2:** offset = FFF7 B964h

Figure 23-123. N2HET Pull Disable Register (HETPULDIS)

31	16
HETPULDIS	
R/W-n	

15	0
HETPULDIS	
R/W-n	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset; n is device dependent, see device specific data sheet

Table 23-104. N2HET Pull Disable Register (HETPULDIS) Field Descriptions

Bit	Field	Value	Description
31-0	HETPULDIS n		Pull disable for N2HET pins
		0	The pull functionality is enabled on pin HET[n].
		1	The pull functionality is disabled on pin HET[n].

NOTE: See device data sheet for which pins provide programmable pullups/pulldowns.

Table 23-9 shows how the register bits of HETDIR, HETPULDIS and HETPSL are affecting the N2HET pins.

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23.5.25 N2HET Pull Select Register (HETPSL)

Values in this register select the pull-up or pull-down functionality of the pins.
N2HET1: offset = FFF7 B868h; **N2HET2:** offset = FFF7 B968h

Figure 23-124. N2HET Pull Select Register (HETPSL)

31	16
HETPSL	
R/W-0	

15	0
HETPSL	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 23-105. N2HET Pull Select Register (HETPSL) Field Descriptions

Bit	Field	Value	Description
31-0	HETPSL n		Pull select for NHET pins
		0	The pull down functionality is enabled if corresponding bit in HETPULDIS is 0.
		1	The pull up functionality is enabled if corresponding bit in HETPULDIS is 0.

NOTE: See device data sheet for which pins provide programmable pullups/pulldowns.

Table 23-9 shows how the register bits of HETDIR, HETPULDIS and HETPSL are affecting the N2HET pins.

The information of this register is also used to define the pin states after a parity error:

After a parity error all N2HET pins, which are

1. Defined as output pins in the HETDIR register
2. Not defined as open drain pins (with the HETPDR register)
3. Selected with the HETPPR register, will remain outputs, but automatically change their levels in the following way:
   - If the HETPSL register specifies 0 for the pin, it will switch to low level.
   - If the HETPSL register specifies 1 for the pin, it will switch to high level.

This behavior is independent of the value, which register HETPULDIS specifies for the corresponding pin.

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23.5.26 Parity Control Register (HETPCR)

N2HET1: offset = FFF7 B874h; **N2HET2:** offset = FFF7 B974h

Figure 23-125. Parity Control Register (HETPCR)

31															16
Reserved															
R-0															
15							9	8	7			4	3		0
Reserved								TEST	Reserved				PARITY_ENA		
R-0								R/WP-0	R-0				R/WP-5h		

LEGEND: R/W = Read/Write; R = Read only; WP = Write in privileged mode only; -*n* = value after reset

Table 23-106. Parity Control Register (HETPCR) Field Descriptions

Bit	Field	Value	Description
31-9	Reserved	0	Read returns 0. Writes have no effect.
8	TEST		Test Bit. When this bit is set, the parity bits are mapped into the peripheral RAM frame to make them accessible by the CPU.
		0	Read: Parity bits are not memory mapped.
			Write: Disable mapping.
		1	Read: Parity bits are memory mapped.
			Write: Enable mapping.
7-4	Reserved	0	Read returns 0. Writes have no effect.
3-0	PARITY_ENA		Enable/disable parity checking. This bit field enables or disables the parity check on read operations and the parity calculation on write operations. If parity checking is enabled and a parity error is detected the N2HET_UERR signal is activated.
		5h	Read: Parity check is disabled.
			Write: Disable checking.
		Others	Read: Parity check is enabled.
			Write: Enable checking.

NOTE: It is recommended to write an "Ah" to enable error detection, to guard against soft errors flipping PARITY_ENA to a disable state.

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23.5.27 Parity Address Register (HETPAR)

N2HET1: offset = FFF7 B878h; **N2HET2:** offset = FFF7 B978h

Figure 23-126. Parity Address Register (HETPAR)

31	16
Reserved	
R-0	

15	13	14	2	1	0
Reserved		PAOFF		Reserved	
R-0		R-X		R-0	

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset; X = Value unchanged after reset

Table 23-107. Parity Address Register (HETPAR) Field Descriptions

Bit	Field	Value	Description
31-13	Reserved	0	Read returns 0. Writes have no effect.
12-2	PAOFF		Parity Error Address Offset. This register holds the offset address of the first parity error, which is detected in N2HET RAM. This error address is frozen from being updated until it is read by the CPU. During emulation mode, this address is frozen even when read. In case of a N2HET RAM parity error, PAOFF will contain the offset address of the erroneous 32-bit N2HET RAM field counted from the beginning of the N2HET RAM. Examples: The 32-bit program field of instruction 0 will return 0, the 32-bit control field of instruction 0 will return 1, ..., the 32-bit control field of instruction 1 will return 5, and so on. Read: Returns the offset address of the erroneous 32-bit word in bytes from the beginning of the N2HET RAM. Write: Writes have no effect.
1-0	Reserved	0	Read returns 0. Writes have no effect.

NOTE: The Parity Error Address Register will not be reset, neither by PORRST nor by any other reset source.

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23.5.28 Parity Pin Register (HETPPR)

N2HET1: offset = FFF7 B87Ch; **N2HET2:** offset = FFF7 B97Ch

Figure 23-127. Parity Pin Register (HETPPR)

31	16
HETPPR	
R/W-0	

15	0
HETPPR	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 23-108. Parity Pin Register (HETPPR) Field Descriptions

Bit	Field	Value	Description
31-0	HETPPR n		NHET Parity Pin Select Bits - Allows HET[n] pins to be configured to drive to a known state when an N2HET parity error is detected.
		0	Pin HET[n] is not affected by the detection of an N2HET parity error.
		1	Pin HET[n] is driven to a known state when an N2HET parity error is detected. The known state is a function of bits HETDIR[n], HETPSL[n], HETPDR[n] as described in Table 23-109 (this state is also independent of HETPULDIS[n]).

Table 23-109. Known State on Parity Error

HETDIR[n]	HETPDR[n]	HETPSL[n]	Known State on Parity Error
0	x	x	High Impedance
1	0	0	Drive Logic 0
1	0	1	Drive Logic 1
1	1	x	High Impedance

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23.5.29 Suppression Filter Preload Register (HETSFPRLD)

N2HET1: offset = FFF7 B880h; **N2HET2:** offset = FFF7 B980h

Figure 23-128. Suppression Filter Preload Register (HETSFPRLD)

31	18	17	16
Reserved		CCDIV	
R-0		R/W-0	

15	10	9	0
Reserved		CPRLD	
R-0		R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 23-110. Suppression Filter Preload Register (HETSFPRLD) Field Descriptions

Bit	Field	Value	Description
31-18	Reserved	0	Read returns 0. Writes have no effect.
17-16	CCDIV		Counter Clock Divider
			CCDIV determines the ratio between the counter clock and VCLK2.
		0	CCLK = VCLK2
		1h	CCLK = VCLK2 / 2
		2h	CCLK = VCLK2 / 3
		3h	CCLK = VCLK2 / 4
15-10	Reserved	0	Read returns 0. Writes have no effect.
9-0	CPRLD		Counter Preload Value
			CPRLD contains the preload value for the counter clock.

23.5.30 Suppression Filter Enable Register (HETSFENA)

N2HET1: offset = FFF7 B884h; **N2HET2:** offset = FFF7 B984h

Figure 23-129. Suppression Filter Enable Register (HETSFENA)

31	16
HETSFENA	
R/W-0	

15	0
HETSFENA	
R/W-0	

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 23-111. Suppression Filter Enable Register (HETSFENA) Field Descriptions

Bit	Field	Value	Description
31-0	HETSFENA n		Suppression Filter Enable Bits
			Note: If the pin is configured as an output by the N2HET Direction Register (HETDIR), the filter is automatically disabled independent on the bit in HETSFENA.
		0	The input noise suppression filter for pin HET[n] is disabled.
		1	The input noise suppression filter for pin HET[n] is enabled.

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23.5.31 Loop Back Pair Select Register (HETLBPSEL)

N2HET1: offset = FFF7 B88Ch; **N2HET2:** offset = FFF7 B98Ch

Figure 23-130. Loop Back Pair Select Register (HETLBPSEL)

31	30	29	28	27	26	25	24
LBPTYPE31/30	LBPTYPE29/28	LBPTYPE27/26	LBPTYPE25/24	LBPTYPE23/22	LBPTYPE21/20	LBPTYPE19/18	LBPTYPE17/16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
23	22	21	20	19	18	17	16
LBPTYPE15/14	LBPTYPE13/12	LBPTYPE11/10	LBPTYPE9/8	LBPTYPE7/6	LBPTYPE5/4	LBPTYPE3/2	LBPTYPE1/0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
15	14	13	12	11	10	9	8
LBPSEL 31/30	LBPSEL 29/28	LBPSEL 27/26	LBPSEL 25/24	LBPSEL 23/22	LBPSEL 21/20	LBPSEL 19/18	LBPSEL 17/16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
7	6	5	4	3	2	1	0
LBPSEL 15/14	LBPSEL 13/12	LBPSEL 11/10	LBPSEL 9/8	LBPSEL 7/6	LBPSEL 5/4	LBPSEL 3/2	LBPSEL 1/0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 23-112. Loop Back Pair Select Register (HETLBPSEL) Field Descriptions

Bit	Field	Value	Description
31-16	LBPTYPE n+1 / n		Loop Back Pair Type Select Bits These bits are valid only when IODFT mode is enabled (HETLBPDIR[19:16] = "1010").
		0	Digital loopback is selected for HR structures on pins HET[n+1] and HET[n].
		1	Analog loopback is selected for HR structures on pins HET[n+1] and HET[n].
15-0	LBPSEL n+1 / n		Loop Back Pair Select Bits These bits are valid only when IODFT mode is enabled (HETLBPDIR[19:16] = "Ah"). If bit x is set, the HR structures on pins HET[n+1] and HET[n] are connected in a loop back mode. The direction is given by LBPDIR n+1/n and type is selected by LBPTYPE n+1/n. The pin which is not driven by the N2HET pin actions can still be used as normal GIO pin.

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23.5.32 Loop Back Pair Direction Register (HETLBPDIR)

N2HET1: offset = FFF7 B890h; **N2HET2:** offset = FFF7 B990h

Figure 23-131. Loop Back Pair Direction Register (HETLBPDIR)

31						20	19			16
Reserved							IODFTENA			
R-0							R/WP-5h			
15	14	13	12	11	10		9			8
LBPDIR 31/30	LBPDIR 29/28	LBPDIR 27/26	LBPDIR 25/24	LBPDIR 23/22	LBPDIR 21/20		LBPDIR 19/18			LBPDIR 17/16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		R/W-0			R/W-0
7	6	5	4	3	2		1			0
LBPDIR 15/14	LBPDIR 13/12	LBPDIR 11/10	LBPDIR 9/8	LBPDIR 7/6	LBPDIR 5/4		LBPDIR 3/2			LBPDIR 1/0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		R/W-0			R/W-0

LEGEND: R/W = Read/Write; R = Read only; WP = Write in privileged mode only; -*n* = value after reset

Table 23-113. Loop Back Pair Direction Register (HETLBPDIR) Field Descriptions

Bit	Field	Value	Description
31-20	Reserved	0	Read returns 0. Writes have no effect.
19-16	IODFTENA		Module IODFT Enable Key
			Reset Value is 5h (I/O DFT is enabled).
		5h	I/O DFT is enabled.
		Others	I/O DFT is disabled.
15-0	LBPDIR n+1 / n		Loop Back Pair Direction Bits
		0	The HR structures on pins HET[n+1] and HET[n] are internally connected with HET[n] as input and HET[n+1] as output.
		1	The HR structures on pins HET[n+1] and HET[n] connected with HET[n] as output and HET[n+1] as input.

NOTE: The loop back direction can be selected independent on the HETDIR register setting.

23.5.33 N2HET Pin Disable Register (HETPINDIS)

N2HET1: offset = FFF7 B894h; **N2HET2:** offset = FFF7 B994h

Figure 23-132. N2HET Pin Disable Register (HETPINDIS)

31																16
HETPINDIS																
R/W-0																
15																0
HETPINDIS																
R/W-0																

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

Table 23-114. NHET Pin Disable Register (HETPINDIS) Field Descriptions

Bit	Field	Value	Description
31-0	HETPINDIS n		N2HET Pin Disable Bits
		0	Logic low: No affect on the output buffer enable of the pin (is controlled by the value of the HETDIR[n] bit).
		1	Logic high: Output buffer of the pin is enabled if pin nDIS = 1, HET PIN ENA = 1 and HETDIR = 1, or else disabled if nDIS = 0 or HETDIR = 0 or HET PIN ENA = 0.

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23.6 Instruction Set

23.6.1 Instruction Summary

Table 23-115 presents a list of the instructions in the N2HET instruction set. The pages following describe each instruction in detail.

Table 23-115. Instruction Summary

Abbreviation	Instruction Name	Opcode	Sub-Opcode	Cycles [1]
ACMP	Angle Compare	Ch	-	1
ACNT	Angle Count	9h	-	2
ADCNST	Add Constant	5h	-	2
ADC	Add with Carry and Shift	4h	C[25:23]=001, C5 = 1	1 - 3
ADD	Add and Shift	4h	C[25:23]=011, C5 = 1	1 - 3
ADM32	Add Move 32	4h	C[25:23]=000, C5 = 1	1 - 2
AND	Bitwise AND and Shift	4h	C[25:23]=010, C5 = 1	1 - 3
APCNT	Angle Period Count	Eh	-	1 - 2
BR	Branch	Dh	-	1
CNT	Count	6h	-	1 - 2
DADM64	Data Add Move 64	2h	-	2
DJZ	Decrement and Jump if -zero	Ah	P[7:6] = 10	1
ECMP	Equality Compare	0h	C[6:5] = 00	1
ECNT	Event Count	Ah	P[7:6] = 01	1
MCMP	Magnitude Compare	0h	C[6] = 1	1
MOV32	Move 32	4h	C[5] = 0	1 - 2
MOV64	Move 64	1h	-	1
PCNT	Pulse/Period Count	7h	-	1
PWCNT	Pulse Width Count	Ah	P[7:6]=11	1
RADM64	Register Add Move 64	3h	-	1
RCNT	Ratio Count	Ah	P[7:6]=00, P[0]=1	3
SBB	Subtract with Borrow and Shift	4h	C[25:23] =110 C[5] =1	1 - 3
SCMP	Sequence Compare	0h	C[6:5] = 01	1
SCNT	Step Count	Ah	P[7:6] = 00, P[0] = 0	3
SHFT	Shift	Fh	C[3]=0	1
SUB	Subtract and Shift	4h	C[25:23]=101, C[5] = 1	1 - 3
WCAP	Software Capture Word	Bh	-	1
WCAPE	Software Capture Word and Event Count	8h	-	1
XOR	Bitwise Exclusive-Or and Shift	4h	C[25:23] , C[5] = 1	1 - 3

(1) Cycles refers to the clock cycle of the N2HET module; which on most devices is VCLK2. (Check the device datasheet description of clock domains to confirm). If the high resolution prescale value is set to /1, then this is also the same as the number of HR clock cycles.

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Table 23-116. FLAGS Generated by Instruction

Abbreviation	Flag Name	Set/Reset by	Used by
C	Carry Flag	ADC, ADD, AND, OR, RCNT, SBB, SUB, XOR	ADC, BR, SBB
N	Negative Flag	ADC, ADD, AND, OR, SBB, SUB, XOR	BR
V	Overflow Flag	ADC, ADD, AND, OR, SBB, SUB, XOR	BR
Z	Zero flag	ACNT, ADC, ADD, AND, APCNT, CNT, OR, PCNT, SBB, SCNT, SHFT, XOR,	ACMP, ACNT, BR, ECMP, MCMP, MOV32, RCNT, SCMP, SHFT
X	Angle Compare Match Flag	ACMP	SCMP
SWF 0-1	Step width flags	SCNT	ACNT
NAF	New Angle Flag	ACNT	NAF_global
NAF_global	New Angle flag (global)	*HWAG or NAF*	ACMP, BR, CNT, ECMP, ECNT
ACF	Acceleration flag	ACNT	,ACNT, SCNT
DCF	Deceleration flag	ACNT	,ACNT, SCNT
GPF	Gap flag	ACNT	ACNT, APCNT

The instructions capable of generating SW interrupts are listed in Table 23-117.

Table 23-117. Interrupt Capable Instructions

Interrupt Capable Instructions	Non Interrupt Capable Instructions
ACMP	ADC
ACNT	ADCNST
APCNT	ADD
BR	ADM32
CNT	AND
DJZ	DADM32
ECMP	MOV32
ECNT	MOV64
MCMP	OR
PCNT	RADM64
PWCNT	RCNT
SCMP	SBB
SHFT	SCNT
WCAP	SUB
WCAPE	XOR

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