EE477L Homework 2

Assigned Date: Tuesday September 13, 2005
Due Date: Friday September 23, 2005

Theory

1. Answer exercise 3.6 of Kang & Leblebici book.
2. Answer exercise 3.7 of Kang & Leblebici book.
3. Answer exercise 3.11 of Kang & Leblebici book.
4. Answer exercise 3.16 of Kang & Leblebici book.
Show and explain your work clearly and in detail.

Lab

5. Design an Inverter and a 2-input NOR (with CMOS complementary logic) in Magic. Use minimum size transistors for the NMOS and 2x minimum size transistors for the PMOS. Try to use close-to-minimum possible layout area.

Layout constraints:
• The height of the design should be 56 lambda for all of the layout blocks.
• VDD and GND should be routed in metal1at top and bottom of the cell.
• Width of internal VDD and GND should 8 lambda.
• Poly and metal1 can be used for the internal routing within the cell.
• Input and output pins should be brought up to Metal2 and Metal2 cannot be used otherwise internal to the cell.
• The cell should be made abuttable such that there are no DRC errors when this cell is placed right next to any other cell. The power and ground wires should align and abut. N-well and P-wells should go to the edge of the cell, such that they align and abut. Metal/poly wiring should adhere to ½ spacing rule to the boundary of the cell, such that wires in neighboring cells that follow the same guidelines will not cause DRC spacing violations.
• Make sure the width of the cell is a multiple of one metal pitch (8 lambda).

Extract the netlist from layout and simulate it using IRSIM to ensure correctness. Ensure all input cases are tested.

Extract the spice netlist and analyze in HSPICE by making this circuit a sub-circuit. Characterize all timing arcs, but assume that the load is 300fF and input slew rate is 10ps (rather than considering all 25 cases). Measure difference in each timing arc. Printout the spice decks and the mt0 files and explain any differences.
Hint: See the .include and .subckt commands in HSPICE. Outputs should have different names. And only one of the inputs can have a transition at any given time.

You should submit plot of your layout, HSPICE netlist, IRSIM and MWAVES plots. Also calculate the area of your layout.

6. Design a 3-input NAND gate cell in Magic.
Use minimum size transistors for the NMOS and 2x minimum size transistors for the PMOS. Try to use close-to-minimum possible layout area. (Layout constraints explained above are applicable)

Extract the netlist from layout and simulate it using IRSIM and HSPICE to evaluate its performance (i.e. output delay, output slew rate and power dissipation.)

You should submit plot of your layout, HSPICE netlist, IRSIM and MWAVES plots. Also calculate the area of your layout.

7. Simulate an Inverter by using HSPICE to find its I-V curve for beta ratios 1/10, 1/5, 1/1, 5/1, and 10/1 and for beta ratio measure its noise margins.
Hint: See .dc and .measure commands and derivative function in HSPICE manual.

For minimum size inverter find output delay, output slew rate, power dissipation and leakage power dissipation as function of temperature.
Temperature steps are 0, 25, 50, 75, 100, 125 and 150 degrees.
Leakage power dissipation can be measured by measuring the power dissipation while all of the inputs are stable
Hint: See .temp command in HSPICE manual.