Proposal for Report on Processor Architectures

To: Prof. Richard McGuire
From: Zhiyang Ong
Date: October 9, 2014

Contents

1 Introduction to Processor Architecture

In this section, I provide the motivation to write a report on processor architecture, and introduction to processor architecture.

Current and emerging trends in "Big Data" [1,8], Internet of Things [9], and cyber-physical systems [6] drives a need for energy-efficient computing. From mobile devices to high-performance super computing, the cost of power and cooling these computers have become so dominant that they have become a barrier to improving the performance of computers [3,4]. Without better computers, it can be harder for companies to sell computers to consumers and enterprises. Furthermore, computer architecture is a difficult subject to teach, especially at the undergraduate level [10]. Due to the demand for high-performance, energy-efficient processors [2], we need to train more highly-skilled computer engineering students to pursue a career in the field of computer architecture. In addition, before students and professionals can tackle grand challenges in computer architecture [7], they need to master the basics of modern processor design.

Processor architecture refers to the structure and organization of the computer chip (or processor), including the set of instructions that it can comprehend [4]. The study of this is critical to designing faster computers, reducing energy consumption of computers, and improving the reliability of

computers. It also defines the hardware and software interface [5], so that engineers designing computer hardware and software developers can collaborate or work independently to create compelling products for customers and end users.

2 Description of the Report

In this section, a structure for the report is described. In Subsection 2.1, we specify the audience and purpose of the report proposal and the report. Following that in Subsection 2.2, we provide a tentative outline of the report. Lastly, in Subsection 2.3, we provide a preliminary bibliography for the report.

2.1 Audience and Purpose

The sole audience of the report proposal and a primary audience for the report is Prof. Richard McGuire. Secondary audience for the report would include my peers and myself, who can use the report to help them review the basics of processor architecture for their classes on computer architecture. We (my peers and myself) can also use the report to help us prepare for the Ph.D. qualifying examination, or equivalent, and for job interviews. Tertiary audience would include undergraduates who want to learn about processor architecture design, so that they can engage in undergraduate research projects and consider going to graduate school or pursue an engineering career in computer architecture. Since processor architecture is poorly taught in many universities, this is important in the context of broadening participation of not-so-privileged students in processor architecture.

2.2 Tentative Outline

A tentative outline for the structure of the report is given as follows, with annotations to describe the importance and relevance of each section.

1. Introduction. *This section introduces processor architecture, and basic concepts in processor architecture (or microarchitecture) and some background information.*
2. Single-cycle processor. *This section describes how to design the most basic type of processor architecture*
3. Multi-cycle processor. *This section describes a faster microarchitecture, which allocates multiple clock cycles for each instruction.*
4. Pipelined processor. *This section describes an even faster microarchitecture based on the notion of pipelining.*
5. Out-of-order pipelined processor. *This section describes a microarchitecture that rearranges instructions of a computer program to improve performance.*
6. Out-of-order superscalar processor. *This section addresses contemporary microarchitectures by issuing multiple instructions per clock cycle to improve performance.*
7. Conclusion. *This section concludes the report by summarizing the basic concepts in processor architecture and providing some directions for more advanced work in processor architecture.*

2.3 Preliminary Bibliography

My preliminary bibliography is listed below with annotations. For each publication, I would indicate the publication followed by a brief explanation of why I am using that publication.

1. John L. Hennessy and David A. Patterson, "Computer Architecture: A Quantitative Approach," Fifth edition, Morgan Kaufmann, 2012.

   This is the seminal textbook on modern computer architecture, including processor architecture. It addresses the most important concept in processor architecture, and other related aspects of computer architecture. It has worked examples and exercises to help people learn contemporary concepts in computer architecture. It covers current and emerging trends in processor architecture, and analyzes some modern processors to help readers see how advance concepts of processor architecture are used in commercial products.
2. David A. Patterson and John L. Hennessy, "Computer Organization and Design: The Hardware/Software Interface," Fifth edition, Morgan Kaufmann, Waltham, MA, 2014.

   This book is a seminal textbook to the fundamentals of computer architecture, including processor architecture. It provides adequate details to enable readers to design their own processors using technologies developed in the 1980s. It has worked examples and exercises for readers to test their knowledge of processor architecture, and related topics.
3. David Money Harris and Sarah L. Harris, "Digital Design and Computer Architecture," Morgan Kaufmann,Waltham, MA, 2007.

   This book introduced the basic concepts of processor architecture, circa the 1980s, such as pipelined reduced instruction set computing (RISC) processors. It includes examples and exercises to help us learn the material. Furthermore, it includes material on logic design to help us implement the microarchitecture of simple processors, circa the 1980s.

Some ancillary publications that may help me explain various concepts of modern processor architecture design to engineering and computer science students and junior professionals are listed as follows.

1. Rajeev Balasubramonian and Norman P. Jouppi and Naveen Muralimanohar, "Multi-Core Cache Hierarchies," Synthesis Lectures on Computer Architecture series, Morgan & Claypool Publishers, San Rafael, CA, November, 2011.

   This book covers advanced material on hierarchical cache design for multi-core processors. However, it does not provide the basics for simple cache design for single-core/uni- processors. It also does not cover other topics in processor architecture design. Given its brevity on advanced topics, lack of examples, and lack of exercises (or problem sets) to help us learn concepts, I do consider it as a primary resource for architecture resource. That said, it is a helpful secondary resource for advanced topics in multi-core processors.
2. Stephen W. Keckler and Kunle Olukotun and H. Peter Hofstee, "Multicore Processors and Systems," Integrated Circuits and Systems series, Springer Science+Business Media, LCC, New York, NY, 2009. DOI: http://dx.doi.org/10.1007/978-1-4419-0263-4.

   This book covers contemporary trends in multicore processor architectures. However, it does not cover the design flow of processor architecture, which is important to help people get an overview of how to design multicore processors. In addition, it also does not have worked examples nor exercises to help students learn about multicore processor design.
3. Vojin G. Oklobdzija and Ram K. Krishnamurthy, "High-Performance Energy-Efficient Microprocessor Design," Integrated Circuits and Systems series, Springer, Dordrecht, The Netherlands, 2006.

This covers some contemporary topics in processor design, but does not contain adequate information to help readers acquire the basics and the design flow of processors. Readers of this book are expected to have a significant background in processor design.

4. Tim Harris, James Larus, Ravi Rajwar, "Transactional Memory," Synthesis Lectures on Computer Architecture series, Morgan & Claypool Publishers, San Rafael, CA, Second edition, December 2010.

   This book provides an introduction into a special topic, transactional memory, and addresses it from a parallel programming approach. Hence, it addresses the lack of coverage of transactional memory in other references from a modern perspective.

3 Project Plan

This section introduces how the project of writing my report shall be planned. In Subsection 3.1, I would discuss the tasks and subtasks that need to be completed to finish writing my report, and the methods that I would use to complete the tasks. This subsection would also include milestones that need to be completed. Subsequently, in Subsection 3.2, I would discuss the schedule for the milestones of this report writing process. Lastly, in Subsection 3.3, risk management is carried out to determine the risks involved in the report writing process.

3.1 Tasks and Methods

The tasks of writing the report would include some literature review of the books regarding computer architecture, as well as going over worked examples and solving exercises in the textbook to help me improve my knowledge of processor architecture design. It also includes designing a processor to test my concepts in processor architecture, and running processor simulators to examine how would changing the parameters of a processor affect its performance and power consumption. For the primary concepts involved in design processors, I would include a section to describe them in my report.

The aforementioned tasks and proposed methods to accomplish these tasks are listed below.

1. Literature review of some books about computer architecture
2. Single-cycle processor section
3. Multi-cycle processor section
4. Pipelined processor section
5. Out-of-order pipelined processor section
6. Out-of-order superscalar processor section
7. Report writing
8. Progress report
9. Review drafts of report

Progress reports are due according to dates set in the course syllabus, but are subject to be rescheduled upon the recommendation of the course instructor, Prof. Richard McGuire. Drafts for my report, segmented by sections can be completed and reviewed by my peers. Completing drafts on schedule, as indicated in Figure 1, would enable me to stay on track and mitigate the risk of having to complete the report in rush just before the deadline. Each section shall be completed with a write-up for that section, so that the report would be a concatenation of these sections. For the each section, I shall

comprehend worked examples from the textbooks and solve exercises in them. For the single-cycle processor and pipelined processor, I would simulate them with processor simulators and design them as integrated circuits. These activities would help me explain the basics of processor architecture better.

3.2 Schedule

In this section, I briefly describe the schedule for the report writing process. In Figure 1, the Gantt chart shows the schedule for managing my report writing process. It indicates that the time frame in which I expect to complete the main tasks of the report. Since the concepts for single-cycle processors, multi-cycle processors, and pipelined processors are easier than out-of-order pipelined processors and out-of-order superscalar processors, I would cover these material in a week each. As for out-of-order pipelined processors and out-of-order superscalar processors, I need more time to elaborate the details involved in designing these modern processor architectures. Hence, I have set aside two weeks for each of these sections.

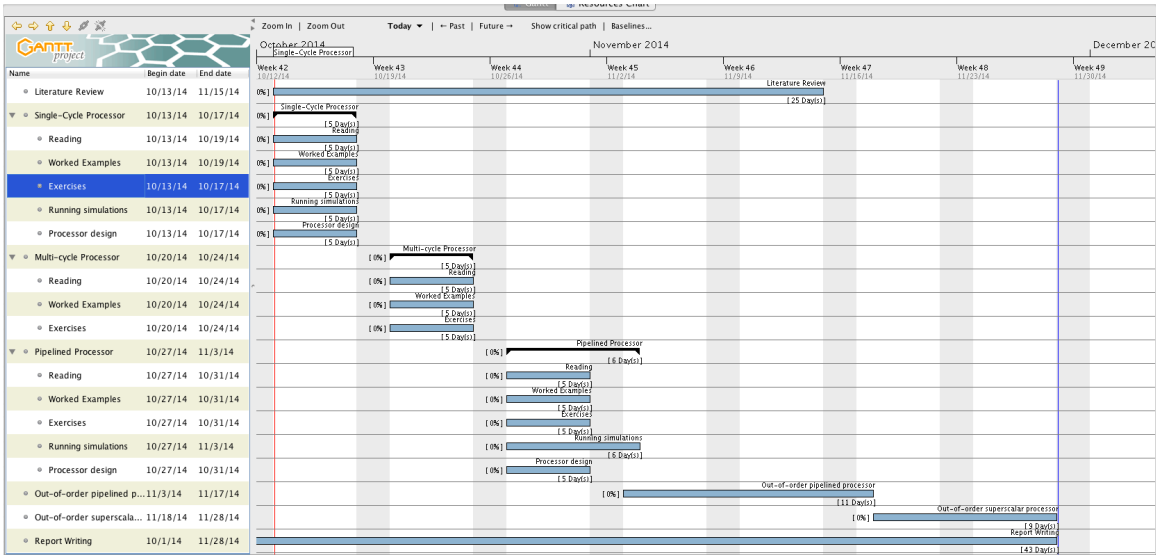

Figure 1: This Gantt chart shows the project schedule.

3.3 Risk Management

A major risk to writing a good report for the class would include not being able to obtain experimental results from the processor design projects. If I cannot adequately test the designs by simulating them, I cannot verify if my processor designs are correct. In addition, I need to be able to find good samples of simple computer programs to test my processor design(s), so that I can use them as examples to explain the intricacies of modern processors. I would mitigate this risk by using very small snippets of computer programs that are used in my computer architecture classes to test my processors and demonstrate certain concepts. In addition, a minor risk to the project would be lost of data and text that I have written till date. I am addressing this risk by using an online repository (i.e., *Bitbucket*), based on cloud computing, to store various versions and modifications of my report and relevant class material (e.g., project proposal).

4 Summary and Recommendation

This proposal summaries what report I would write, why is this report important, what I plan to do for my report writing process, and project management issues for writing this report.

I strongly recommend that Prof. Richard McGuire approve this report proposal.

References

[1] Pedro Less Andrade, Scott C. Beardsley, Beñat Bilbao-Osorio, Roberto Crotti, Bahjat El-Darwiche, Soumitra Dutta, Luís Enríquez, Peter Haynes, John Garrity, Ferry C. Grijpink, Anant Gupta, Jess Hemerly, Volkmar Koch, Bruno Lanvin, David Meer, M-H. Carolyn Nguyen, Alex "Sandy" Pentland, Robert Pepper, Matt Quinn, Gabriel Recalde, Patrick Ryan, Sergio Sandoval, Ramez T. Shehadi, Steven Spittaels, Malin Strandell-Jansson, Chris Taylor, and Walid Tohme. The global information technology report 2014: Rewards and risks of big data. Technical report, World Economic Forum Switzerland, Cologny, Geneva, Switzerland, 2014.

[2] M. Duranton, D. Black-Schaffer, K. De Bosschere, and J. Maebe. The HiPEAC vision for advanced computing in horizon 2020. Technical report, European Network of Excellence on High Performance and Embedded Architecture and Compilation, Luxembourg, Luxembourg, March 2013.

[3] Samuel H. Fuller and Lynette I. Millett. The future of computing performance: Game over or next level? Technical report, National Research Council, Washington, D.C., 2011.

[4] John L. Hennessy and David A. Patterson. Computer Architecture: A Quantitative Approach. Morgan Kaufmann, Waltham, MA, fifth edition, 2012.

[5] David A. Patterson and John L. Hennessy. Computer Organization and Design: The Hardware/Software Interface. Morgan Kaufmann, Waltham, MA, fifth edition, 2014.

[6] President's Council of Advisors on Science and Technology. Designing a digital future: Federally funded research and development in networking and information technology. Technical report, President's Council of Advisors on Science and Technology, Office of Science and Technology Policy, Executive Office of the President, Washington, D.C., January 2013.

[7] Elie K. Track, Tom Conte, Dan Allwood, David Atienza, Jonathan Candelaria, Erik DeBenedictis, Paolo Gargini, Glen Gulak, Bichlien Hoang, Subramanian (Subu) Iyer, Yung-Hsiang Lu, Scott Holmes, Alan M. Kadin, David Mountain, Oleg Mukhanov, Vojin G. Oklobdzijja, Angelos Stavrou, Bill Tonti, and Ian Young. 2^{nd} rebooting computing summit: Summary report. Technical report, Institute of Electrical and Electronics Engineers, Santa Cruz, CA, June 2014.

[8] Robin Wedewer. Rebooting computing summit – event summary. Technical report, The Wedewer Group, Washington, D.C., December 11–12 2013.

[9] Clint Witchalls. The Internet of Things business index: A quiet revolution – a report from The Economist Intelligence Unit. Available online at: http://www.arm.com/files/pdf/EIU_Internet_Business_Index_WEB.PDF; November 7, 2013 was the last accessed date, 2013.

[10] William Yurcik and Edward F. Gehringer. A survey of web resources for teaching computer architecture. In Proceedings of the 2002 Workshop on Computer Architecture Education (WCAE '02), Anchorage, AK, May 26 2002. ACM, ACM Press.