JEFFREY GOEDERS

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Department of Electrical and Computer Engineering
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EDUCATION

2016 **The University of British Columbia**, *Ph.D., Computer Engineering*
Advisor: Steve Wilton
Dissertation Title: Techniques for Enabling In-System Observation-based Debug of High-Level Synthesis Circuits on FPGAs

2012 **The University of British Columbia**, *M.A.Sc., Computer Engineering*
Advisor: Steve Wilton
Thesis Title: Power Estimation for Diverse FPGA Architectures

2012 **University of Toronto**, *B.A.Sc. w/ Honors, Computer Engineering*

PROFESSIONAL EXPERIENCE

July 2016 to Present **Brigham Young University**, *Assistant Professor*
Department of Electrical and Computer Engineering

PUBLICATIONS

Book Chapters

1. **Jeffrey Goeders**, Graham M. Holland, Lesley Shannon, and Steven J.E. Wilton, "Systems-on-Chip on FPGAs", in FPGAs for Software Programmers, Springer, 2016.
2. Andrew Canis, Jongsok Choi, Blair Fort, Bain Syrowik, Ruo Long Lian, Yu Ting Chen, Hsuan Hsiao, **Jeffrey Goeders**, Stephen Brown, and Jason Anderson, "LegUp high-level synthesis", in FPGAs for Software Programmers, Springer, 2016.

Peer-Reviewed Journal Articles

3. (*Under Review, submitted June 2021*) Hayden Cook, Jacob Arscott, Brent George, Tanner Gaskin, **Jeffrey Goeders**, and Brad Hutchings, "Inducing Non-Uniform FPGA Aging Using Configuration-Based Short Circuits", in ACM Transactions on Reconfigurable Technology and Systems (TRETS), 2021.
4. (*Under Review, submitted April 2021*) Eli Cahill, **Jeffrey Goeders**, and Brad Hutchings, "Approaches for FPGA Design Assurance", in ACM Transactions on Reconfigurable Technology and Systems (TRETS), 2021.

5. Benjamin James, Michael Wirthlin, and **Jeffrey Goeders**, “Investigating How Software Characteristics Impact the Effectiveness of Automated Software Fault Tolerance”, in IEEE Transactions on Nuclear Science (TNS), vol. 68, no. 5, pp. 1014-1022, Apr 2021.

6. Al-Shahna Jamal, Eli Cahill, **Jeffrey Goeders**, and Steven JE Wilton, “Fast Turnaround HLS Debugging using Dependency Analysis and Debug Overlays”, in ACM Transactions on Reconfigurable Technology and Systems (TRETS), vol. 13, no. 1, pp. 1-26, Feb 2020.

7. Benjamin James, Heather Quinn, Michael Wirthlin, and **Jeffrey Goeders**, “Applying Compiler-Automated Software Fault Tolerance to Multiple Processor Platforms”, in IEEE Transactions on Nuclear Science (TNS), vol. 67, no. 1, pp. 321-327, Jan 2020.

8. Matthew Bohman, Benjamin James, Michael Wirthlin, Heather Quinn, and **Jeffrey Goeders**, “Microcontroller Compiler-Assisted Software Fault Tolerance”, in IEEE Transactions on Nuclear Science (TNS), vol. 66, no. 1, pp. 223-232, Jan 2019.

9. **Jeffrey Goeders**, and Steven J.E. Wilton, “Signal-Tracing Techniques for In-System FPGA Debugging of High-Level Synthesis Circuits”, in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), vol. 36, no. 1, pp. 83-96, Jan 2017.

10. **Jeffrey Goeders** and Steven J.E. Wilton, “Power Aware Architecture Exploration for Field Programmable Gate Arrays”, in Journal of Low Power Electronics (JOLPE), vol. 10, no. 3, pp. 297-312, Sep. 2014.

11. Jason Luu, **Jeffrey Goeders**, Michael Wainberg, Andrew Somerville, Thien Yu, Konstantin Nasartschuk, Miad Nasr, Sen Wang, Tim Liu, Nooruddin Ahmed, Kenneth B Kent, Jason Anderson, Jonathan Rose, and Vaughn Betz, “VTR 7.0: Next Generation Architecture and CAD System for FPGAs”, in ACM Transactions on Reconfigurable Technology and Systems (TRETS), vol 7, no. 2, pp. 6:1–30, Jul 2014.

Peer-Reviewed International Conference Publications

Note: Conferences which were refereed by abstract, or had acceptance rates close to 100

12. Benjamin James, and **Jeffrey Goeders**, “Automated Software Compiler Techniques to Provide Fault Tolerance for Real-Time Operating Systems”, in Design, Automation and Test in Europe Conference (DATE), Feb 2021.

13. Tanner Gaskin, Hayden Cook, Wesley Stirk, Robert Lucas, **Jeffrey Goeders**, and Brad Hutchings, “Using Novel Configuration Techniques for Accelerated FPGA Aging”, in International Conference on Field-Programmable Logic and Applications (FPL), Aug 2020.

14. Matthew Ashcraft and **Jeffrey Goeders**, “Synchronizing On-Chip Software and Hardware Traces for HLS-Accelerated Programs”, in International Conference on Field Programmable Technology (FPT), Dec 2019.

15. Wesley Stirk and **Jeffrey Goeders**, “Implementation and Design Space Exploration of a Turbo Decoder in High-Level Synthesis”, in International Conference on Reconfigurable Computing and FPGAs (ReConFig), Dec 2019.

16. Daniel Holanda Noronha, Ruizhe Zhao, Zhiqiang Que, **Jeffrey Goeders**, Wayne Luk and Steve Wilton, “An Overlay for Rapid FPGA Debug of Machine Learning Applications”, in International Conference on Field Programmable Technology (FPT), Dec 2019.

17. Daniel Holanda Noronha, Ruizhe Zhao, **Jeffrey Goeders**, Wayne Luk, and Steven J.E. Wilton, “On-chip FPGA Debug Instrumentation for Machine Learning Applications”, in International Symposium on Field-Programmable Gate Arrays (FPGA), pp. 110-115, Feb 2019.

18. Matthew Ashcraft and **Jeffrey Goeders**, “Unified On-Chip Software and Hardware Debug for HLS-Accelerated Programs”, in International Conference on Field Programmable Technology (FPT), pp. 354-357, Dec 2018.

19. Al-Shahna Jamal, **Jeffrey Goeders** and Steve Wilton, “An FPGA Overlay Architecture Supporting Rapid Implementation of Functional Changes during On-Chip Debug”, in International Conference on Field Programmable Logic and Applications (FPL), Aug 2018.

20. **Jeffrey Goeders**, Tanner Gaskin, and Brad Hutchings, “Demand Driven Assembly of FPGA Configurations Using Partial Reconfiguration, Ubuntu Linux, and PYNQ”, in International Symposium on Field-Programmable Custom Computing Machines (FCCM), May 2018.

21. Al-Shahna Jamal, **Jeffrey Goeders**, and Steven J.E. Wilton, “Architecture Exploration for HLS-Oriented FPGA Debug Overlays”, in International Symposium on Field-Programmable Gate Arrays (FPGA), Feb 2018.

22. Pavan Kumar Bussa, **Jeffrey Goeders**, and Steven JE Wilton, “Accelerating in-system FPGA debug of high-level synthesis circuits using incremental compilation techniques”, in International Conference on Field Programmable Logic and Applications (FPL), Sep 2017.

23. **Jeffrey Goeders**, “Enabling Long Debug Traces of HLS Circuits Using Bandwidth-Limited Off-Chip Storage Devices”, in International Symposium on Field-Programmable Custom Computing Machines (FCCM), May 2017.

24. **Jeffrey Goeders**, and Steven J.E. Wilton, “Quantifying observability for in-system debug of high-level synthesis circuits”, in International Conference on Field Programmable Logic and Applications (FPL), pp. 1–11, Aug 2016.

25. **Jeffrey Goeders**, and Steven J.E. Wilton, “Using Round-Robin Tracepoints to Debug Multithreaded HLS Circuits on FPGAs”, in International Conference on Field Programmable Technology (FPT), Dec 2015.

26. **Jeffrey Goeders**, and Steven J.E. Wilton, “Using Dynamic Signal-Tracing to Debug Compiler-Optimized HLS Circuits on FPGAs”, in International Symposium on Field-Programmable Custom Computing Machines (FCCM), pp. 127–134, May 2015.**Best Paper Award**.

27. **Jeffrey Goeders**, and Steven J.E. Wilton, “Effective FPGA Debug for High-Level Synthesis Generated Circuits”, in International Conference on Field Programmable Logic and Applications (FPL), pp. 1–8, Sep 2014.

28. Eddie Hung, **Jeffrey Goeders**, and Steven J.E. Wilton, “Faster FPGA Debug: Efficiently Coupling Trace Instruments with User Circuitry”, in International Symposium on Applied Reconfigurable Computing (ARC), pp. 73–84, Apr 2014.

29. **Jeffrey Goeders**, and Steven J.E. Wilton, “VersaPower: Power Estimation for Diverse FPGA Architectures”, in International Conference on Field Programmable Technology (FPT), pp. 229–234, Dec 2012.

30. Jonathan Rose, Jason Luu, Chi Wai Yu, Opal Densmore, **Jeffrey Goeders**, Andrew Somerville, Kenneth B. Kent, Peter Jamieson, and Jason Anderson, “The VTR Project: Architecture and CAD for FPGAs from Verilog to Routing”, in International Symposium on Field Programmable Gate Arrays (FPGA), pp. 77 – 86, Feb 2012.

31. **Jeffrey Goeders**, Guy Lemieux, and Steven J.E. Wilton, “Deterministic Timing-Driven Parallel Placement by Simulated Annealing Using Half-Box Window Decomposition”, in International Conference on Reconfigurable Computing and FPGAs (ReConFig), pp. 41–48, Dec 2011.

Peer-Reviewed International Workshop Publications

32. Adam Hastings, Sean Jensen, **Jeffrey Goeders**, and Brad Hutchings, “Using Physical and Functional Comparisons to Assure 3rd-Party IP for Modern FPGAs”, in International Verification and Security Workshop (IVSW), Jul 2018.

Peer-Reviewed International Oral Presentations

33. Benjamin James, Michael Wirthlin, and **Jeffrey Goeders**, “Understanding How Software Properties Impact the Effectiveness of Automated Software Fault Tolerance”, in Nuclear and Space Radiation Effects Conference (NSREC), Dec 2020.
34. Benjamin James, Michael Wirthlin, Heather Quinn, and **Jeffrey Goeders**, “Applying Compiler-Automated Software Fault Tolerance to Multiple Processor Platforms”, in Nuclear and Space Radiation Effects Conference (NSREC), Jul 2019.

Peer-Reviewed International Poster Presentations

35. Matthew Bohman, Benjamin James, Michael Wirthlin, Heather Quinn, and **Jeffrey Goeders**, “Microcontroller Compiler-Assisted Software Fault Tolerance”, in Nuclear and Space Radiation Effects Conference (NSREC), Jul 2018.

TALKS

Invited Talks

1. **Jeffrey Goeders**, “Debug Techniques for Digital Circuits”, at University of Waterloo, Ontario, Canada (virtual), July 2021.
2. **Jeffrey Goeders**, Tanner Gaskin, and Brad Hutchings, “Demand Driven Assembly of FPGA Configurations Using Partial Reconfiguration, Ubuntu Linux, and PYNQ”, at Xilinx Inc., Boulder, CO, May 2018.
3. **Jeffrey Goeders**, and Steven J.E. Wilton, “In-System FPGA Debugging of High-Level Synthesis Circuits”, at Intel Programmable Solutions Group, Toronto, ON, Canada, Apr 2016.
4. **Jeffrey Goeders**, and Steven J.E. Wilton, “Techniques for In-System FPGA Debugging of High-Level Synthesis Circuits”, at University of Toronto, Toronto, ON, Canada, Apr 2016.
5. **Jeffrey Goeders**, and Steven J.E. Wilton, “Effective FPGA Debug for High-Level Synthesis Generated Circuits”, at Xilinx Inc., San Jose, CA, USA, Apr 2015.
6. **Jeffrey Goeders**, and Steven J.E. Wilton, “Effective FPGA Debug for High-Level Synthesis Generated Circuits”, at Altera Corp., Toronto, ON, Canada, Jan 2015.

Conference Talks

7. **Jeffrey Goeders**, Tanner Gaskin, and Brad Hutchings, “Demand Driven Assembly of FPGA Configurations Using Partial Reconfiguration, Ubuntu Linux, and PYNQ”, at International Symposium on Field-Programmable Custom Computing Machines (FCCM), May 2018.
8. **Jeffrey Goeders**, “Enabling Long Debug Traces of HLS Circuits Using Bandwidth-Limited Off-Chip Storage Devices”, at International Symposium on Field-Programmable Custom Computing Machines (FCCM), May 2017.
9. **Jeffrey Goeders**, and Steven J.E. Wilton, “Quantifying observability for in-system debug of high-level synthesis circuits”, at International Conference on Field Programmable Logic and Applications (FPL), Aug 2016.
10. **Jeffrey Goeders**, and Steven J.E. Wilton, “Using Round-Robin Tracepoints to Debug Multithreaded HLS Circuits on FPGAs”, at International Conference on Field Programmable Technology (FPT), Dec 2015.
11. **Jeffrey Goeders**, and Steven J.E. Wilton, “Using Dynamic Signal-Tracing to Debug Compiler-Optimized HLS Circuits on FPGAs”, at International Symposium on Field-Programmable Custom Computing Machines (FCCM), May 2015.

12. **Jeffrey Goeders**, and Steven J.E. Wilton, “Effective FPGA Debug for High-Level Synthesis Generated Circuits”, at International Conference on Field Programmable Logic and Applications (FPL), Sep 2014.
13. **Jeffrey Goeders**, Guy Lemieux, and Steven J.E. Wilton, “Deterministic Timing-Driven Parallel Placement by Simulated Annealing Using Half-Box Window Decomposition,” at International Conference on Reconfigurable Computing and FPGAs (ReConFig)”, at , Dec 2011.

Workshop Talks

14. **Jeffrey Goeders**, and Brad Hutchings, “Approaches for FPGA Design Assurance”, at Military and Aerospace Programmable Logic Devices (MAPLD) Workshop, Aug 2021.
15. **Jeffrey Goeders**, and Brad Hutchings, “Assurance of Trusted 3rd-Party IP for Modern FPGAs”, at Military and Aerospace Programmable Logic Devices (MAPLD) Workshop, May 2019.
16. Adam Hastings, Sean Jensen, **Jeffrey Goeders**, and Brad Hutchings, “Using Physical and Functional Comparisons to Assure 3rd-Party IP for Modern FPGAs”, at International Verification and Security Workshop (IVSW), Jul 2018.
17. Matthew Bohman, Benjamin James, Michael Wirthlin, Heather Quinn, and **Jeffrey Goeders**, “Automated Data Flow Protection for Software Fault Tolerance on Microcontrollers”, at Silicon Errors in Logic – System Effects (SELSE), Apr 2018.
18. **Jeffrey Goeders**, and Steven J.E. Wilton, “VersaPower: Power Estimation for Diverse FPGA Architectures”, at Cascadia: A joint workshop of UBC, SFU, and UWash on FPGA Research, SFU, Aug 2012.

Artifact Demonstrations

19. **Jeffrey Goeders**, Tanner Gaskin, and Brad Hutchings, “Demand Driven Assembly of FPGA Configurations Using Partial Reconfiguration, Ubuntu Linux, and PYNQ”, at Xilinx Developer Forum (XDF), Oct 2018.
20. **Jeffrey Goeders**, Tanner Gaskin, and Brad Hutchings, “Demand Driven Assembly of FPGA Configurations Using Partial Reconfiguration, Ubuntu Linux, and PYNQ”, at International Symposium on Field-Programmable Custom Computing Machines (FCCM), Oct 2018.
21. **Jeffrey Goeders**, and Steven J.E. Wilton, “HLS-Scope: Debug Hardware Like it’s Software. Effective Source-Level Debugging of High-Level Synthesis Generated Circuits”, at Innovation 360: Symposium and Exposition on Micro-Nano Technologies and Systems, Sep 2015.
22. **Jeffrey Goeders**, and Steven J.E. Wilton, “HLS-Scope: FPGA Debug for High-Level Synthesis”, at International Symposium on Field-Programmable Custom Computing Machines (FCCM), May 2015.
23. **Jeffrey Goeders**, and Steven J.E. Wilton, “HLS-Scope: FPGA Debug for High-Level Synthesis”, at International Symposium on Field-Programmable Custom Computing Machines (FCCM), May 2014.

TEACHING EXPERIENCE

Instructor

- **ECEN 220**: Fundamentals of Digital Systems (Spring 2019, Fall 2019)
- **ECEN 330**: Intro to Embedded Systems Programming (Fall 2016, Fall 2017, Fall 2018, Spring 2020, Fall 2020, Spring 2021, Fall 2021)
- **ECEN 427**: Embedded Systems (Fall 2021)
- **ECEN 522R**: High-Level Digital Design Automation (Winter 2017)

- **ECEN 625**: Compilation Strategies for High-Performance Programs (Winter 2019, Winter 2021)
- **ECEN 629**: Reconfigurable Computing Systems (Winter 2018, Winter 2020)

Teaching Assistant

- **EECE 381**: Computer Systems Design Studio (7 appointments)
- **EECE 465**: Microcomputer Systems Design (1 appointment)
- **EECE 353**: Digital Systems Design (3 appointments)
- **EECE 259**: Introduction to Microcomputers (2 appointments)

Course & Seminar Development

ECEN 427: Embedded System Design (BYU) - https://byu-cpe.github.io/ecen427/

- Developed major revisions to the lab content of the class in conjunction with the instructor, Brad Hutchings.
- New lab content focuses on development of user space and kernel code for Linux embedded systems.
- New labs give students a full-stack experience: creating a new digital circuit IP through both Verilog and high-level synthesis (HLS), integrating it into a Linux system, developing a Linux kernel driver, and finally integrating it into application code.

ECEN 625: High-Level Digital Design Automation (BYU) - https://byu-cpe.github.io/ecen625/

- Major revisions of existing course to introduce new assignments, lecture material, current research topics, and hands-on experience with major commercial tools.
- Developed five new assignments which give students experience with commercial designs, high-level synthesis algorithms, large open-source tools, including the LLVM compiler infrastructure.

BYU Computing Boot Camp - https://byu-cpe.github.io/ComputingBootCamp/

- In conjunction with other faculty members, we created a summer boot camp experience for undergraduate research students. This boot camp consists of faculty lectures three times per week, with followup student activities.
- Various modules focus on software development skills (Git, Github, Makefiles, etc.), as well as commercial and academic FPGA tools.
- In 2021 we had over 30 undergraduate students participate.

ECEN 330: Intro to Embedded Systems Programming (BYU) - http://ecen330-lin.groups.et.byu.net/wiki/doku.php

- Migrated all labs and development infrastructure to use Linux-based, open-source, command-line tools.
- Created automated testing, submission, and grading infrastructure to alleviate teaching assistant burden, and provide more time for one-on-one student interactions.

ECEN 220: Fundamentals of Digital Design (BYU) - http://ecen220wiki.groups.et.byu.net/

- Created several new labs (Codebreaker, Pong) designed to provide a more engaging student experience.

EECE 381: Computer Systems Design Studio (UBC)

- Co-developed with Professor Steve Wilton at The University of British Columbia.

- Project-based course designed to give students real-world technical project skills. Students work in groups to identify a real-world market, identify constraints and requirements, plan project milestones, implement hardware and software, and present and report on their accomplishments.
- Technical topics: Rapid development of configurable hardware systems using commercial tools (Quartus/Qsys), embedded software development (FPGAs, Raspberry Pi, ARM), mobile applications (Android), and the integration of such systems.

Employment Experience

2011 to 2016 **Teaching Assistant**, *The University of British Columbia*
Department of Electrical and Computer Engineering

2013, Summer **EDA Software Developer, Internship**, *Blackcomb Design Automation*
Vancouver, BC, Canada

2010, Summer **Firmware Developer, Internship**, *PMC-Sierra*
Burnaby, BC, Canada

2009, Summer **Undergraduate Researcher**, *High-Performance Computing Lab*
University of Toronto, Toronto, ON, Canada

2006 to 2009 **Software and Database Developer**, *Bombardier Aerospace*
Toronto, ON, Canada

Citations

Citations: 992
h-index: 10
i10-index: 11

Professional Activities

Member of IEEE and ACM

Contest Organizer
Design Automation Conference (DAC) System Design Contest - 2020 to 2021

Information Director
ACM Transactions on Reconfigurable Technology and Systems (TRETS) - 2018 to Present

Technical Program Committee (TPC) Member
International Symposium on Field-Programmable Gate Arrays (FPGA) - 2017 to Present
International Conference on Field-Programmable Technology (FPT) - 2016 to 2019
International Conference on Field-Programmable Custom Computing Machines (FCCM) - 2018, 2020 to Present

Reviewer
ACM Transactions on Reconfigurable Technology and Systems (TRETS) - 2016 to Present
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD) - 2016 to Present
IEEE Transactions on Nuclear Science (TNS) - 2018 to Present
IEEE Transactions on Computers (TC) - 2019 to 2020
ACM Transactions on Architecture and Code Optimization (TACO) - 2017
International Journal of Reconfigurable Computing - 2016

GRANTS

2020 to 2024 Michael Wirthlin and **Jeffrey Goeders**
"Interaction of Ionizing Radiation with Matter, University Research Alliance (IIRM–URA)"
Defense Threat Reduction Agency (DTRA), $1,095,000

2018 to 2022 Michael Wirthlin, **Jeffrey Goeders**, Brad Hutchings, and Brent Nelson
"Phase-I IUCRC Brigham Young University: Center For Space, High-Performance, and Reslient Computing (SHREC)"
National Science Foundation (NSF), $750,000

2020 to 2021 **Jeffrey Goeders**, Brad Hutchings and Mike Wirthlin
"SHREC Industry Memberships"
L3Harris, $100,000

2021 **Jeffrey Goeders** and Brad Hutchings
"Empirical Investigations of Field-Programmable Gate Arrays"
Northrup Grumman, $30,000

2021 **Jeffrey Goeders** and Brent Nelson
"Virtual Xilinx Platform in VTR"
Google, $60,000

2021 **Jeffrey Goeders** and Brad Hutchings
"Improving Bitstream Verification Tooling"
Google, $40,000

2021 Brent Nelson, **Jeffrey Goeders**, Mike Wirthlin, and Brad Hutchings
"Boot Camp for the FPGA Community"
Google, $40,000

2018 to 2020 Brad Hutchings and **Jeffrey Goeders**
"SHREC Industry Memberships: Trusted Electronics Research"
Air Force Research Laboratory (AFRL), $150,000

2020 Brad Hutchings and **Jeffrey Goeders**
"SHREC Industry Memberships: Trusted Electronics Research"
Lockheed Martin, $50,000

2018 to 2019 Mike Wirthlin and **Jeffrey Goeders**
"SHREC Industry Memberships"

Los Alamos National Lab (LANL), $100,000

2017 Brent Nelson and **Jeffrey Goeders**
"CHREC Industry Memberships"
National Instruments, $40,000